# Development of a Selftriggered High Counting Rate ASIC for Readout of 2D Gas Microstrip Neutron Detectors.

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## *Abstract*

In the frame of the DETNI project a 32-channel ASIC suitable for readout of a novel 2D thermal neutron detector based on a hybrid low-pressure Micro-Strip Gas Chamber with solid $^{157}$Gd converter has been developed. Each channel delivers position information, a fast time stamp of 2 ns resolution and the signal amplitude (called energy below). The time stamp is used for correlating the signals from X and Y strips while the amplitude is used for finding the center of gravity of a cluster of strips. The timing and energy information are stored in derandomizing buffers and read out via token ring architecture.

## I. Introduction

Neutron scattering and diffraction techniques are widely used for investigating the structure and dynamics of condensed matter at the atomic, molecular and mesoscopic levels. In the frame of the Joint Research Activity DETNI (DETectors for Neutron Instrumentation [1]) within the NMI3 Initiative three types of two-dimensional position sensitive detectors of thermal neutrons for future high intensity pulsed neutron sources (like ESS) are developed. One of these detectors is a low-pressure Micro-Strip Gas Chamber (MSGC) using solid converter technology based on $^{157}$Gd combined with CsI (see Fig. 1) suitable for imaging, quasi-Laue diffraction, very high resolution single crystal diffraction and very high resolution focusing low-Q small angel scattering. The very demanding requirements of global counting rate of $10^8$ cps and a two-dimensional position resolution of 50-100 µm FWHM over a detector area of 25×25 cm$^2$ covered with 400×400 strips can be met only provided that the readout electronics is realized as multi-channel Application Specific Integrated Circuits (ASICs).

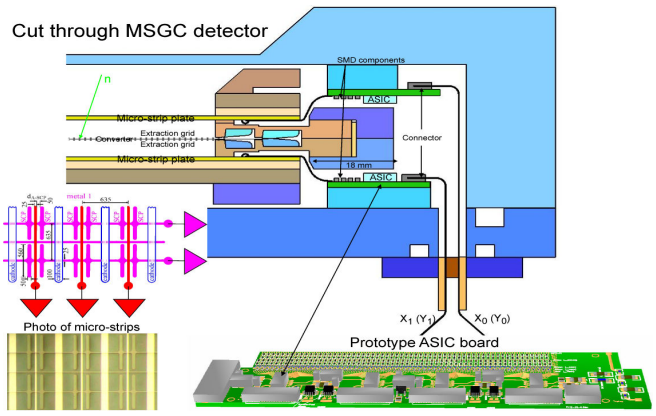



Figure 1: Cut through a prototype MSGC detector with inserts showing the orthogonal X and Y microstrip electrodes and a prototype ASIC board.

## II. MSGCROC ASIC

Reconstruction of a single neutron position in a double-sided strip detector at high count rates requires extracting timing, spatial and energy data from both (X/Y) detector planes. In order to measure time and energy, after the preamplifier each readout channel is split into a timing and an amplitude (energy) channel (see Fig. 2). The output signal from the timing channel is used to latch a 14-bit time stamp of 2 ns resolution and to enable the peak detector and hold (PDH) circuit in the energy channel. The signal amplitude from the PDH and the time stamp are stored in analogue and digital derandomizing buffers (each one four cells deep), respectively.

The readout of both buffers is performed via a token-ring based multiplexer, which ensures data sparsification and full zero suppression so that only non-zero data are transmitted to an external FPGA-based front-end board including fast ADCs for digitisation of the analogue signals. The analogue data is read out via a single differential link at a rate of 32 MHz. The digital data is readout via a parallel 8-bit LVDS bus at a rate of 128 MHz. The internal programmable bias circuits, including a number of DACs, configuration and test circuits are controlled via an I$^2$C interface.

The basic requirements concerning the ASIC parameters are the following:

- Parameters to be measured: position, time, energy
- Detector strip capacitance: 23 pF
- Strip multiplicity per event: ~ 3.5
- Hit rate per strip: ~ $9 \cdot 10^5$ /s
- Compatible with a global count rate of $10^8$ /s
- Input signal charge: $2 \cdot 10^5$ e$^-$ - $5 \cdot 10^6$ e$^-$ (depending on the gas gain chosen)

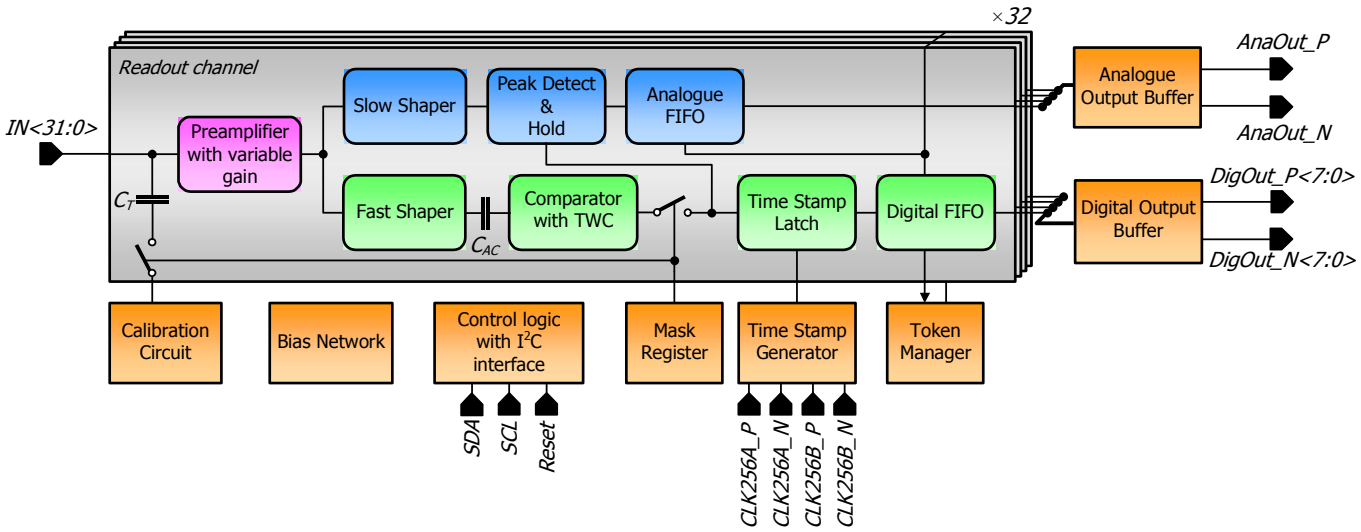



Figure 2: Architecture of the MSGCROC ASIC.

- ENC required for E (5σ threshold): ~ 2000 e⁻ rms
- X/Y coincidence window 2 ns + ($E_X$ = $E_Y$)
- Discriminator: time walk < 2 ns, jitter < 1 ns FWHM
- Variable gain to cope with different detector gas gains
- The preamp-shaper circuits must handle both polarities of the input signal and deliver signals of one polarity to the discriminator and peak detector circuit

## A. *Preamplifier*

The input stage is a transimpedance amplifier built around a folded cascode fast amplifier with a bridged-T lowpass filter in the feedback loop (Fig. 3). The preamplifier delivers fast pulses with short tails to minimize pile-up. Variable gain is implemented in the preamplifier stage by selecting one of five feedback networks. The switchable gain factors are: ×1, ×2, ×4, ×8, and ×16 and are supposed to recover possible variations of the internal multiplication gain of the detector. The preamplifier is also equipped with a switchable inverter stage so that it delivers signals of the same polarity for either polarity of the input charge.

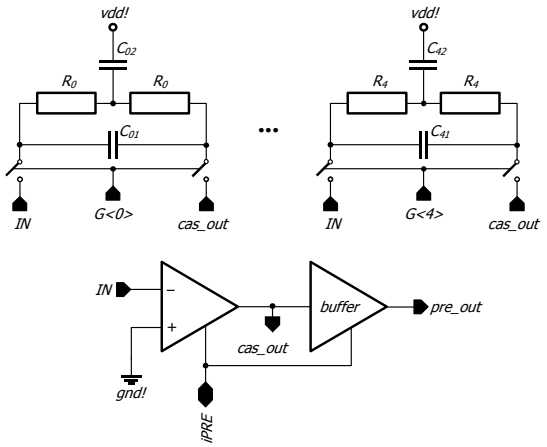



Figure 3: Schematic diagram of the preamplifier with folded cascode core and switchable bridged-T lowpass filter feedback.

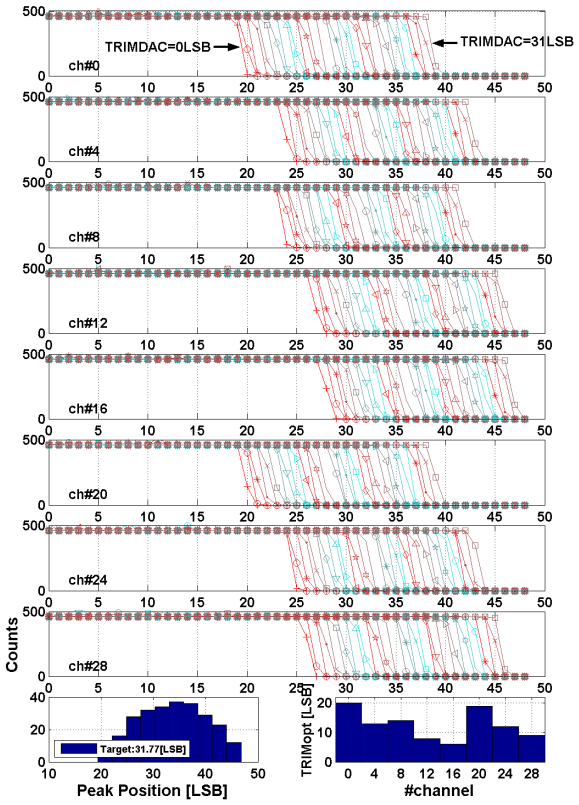
Every channel is equipped with a test capacitor $C_T$ = 1 pF, connected to the input of the preamplifier, which can be used for test and calibration purposes. Specific patterns of the channels to be pulsed simultaneously can be programmed. The test pulses of required amplitudes are generated internally. The test pulse amplitudes are controlled by an internal DAC of 8-bit resolution.

## B. *Timing channel*

The timing channel consists of a fast shaper (with a peaking time $T_p$ = 25 ns) and a comparator with a Time Walk Compensation circuit (TWC) [2]. It delivers the timing signal and the trigger signal to the PDH circuit in the energy channel. Thus, the detection efficiency and noise rate depend on the discrimination threshold.

Since a common threshold voltage is applied to all channels, the channel-to-channel offset spread is a very critical parameter. In order to compensate possible channel-to-channel threshold offsets, each comparator is equipped with a 5-bit trimming Digital-to-Analog Converter (DAC), which allows to correct the threshold offset on the channel basis with a precision better than 1 LSB in the threshold DAC common for all channels. The effectiveness of the trimming procedure for a threshold set to 116 fC is illustrated in Fig. 4.

The trimming procedure is performed in two steps. For a given value of the calibration signal, corresponding to the target value of the threshold, a threshold scan is performed for each of the 32 values of the trimming DAC. (Fig. 4 upper plot – scans for channels #0, #4, #8, #12, #16, #20, #24 and #28). On this basis trimming DACs are set to values that ensure response of all channels for chosen target value of the threshold DAC (Fig. 4 lower plot). For the eight channels shown the peak-to-peak offset spread before trimming is about 10 LSB and is reduced to 1 LSB after trimming. One can notice that best matching of the threshold is obtained for the target value. Applying the same trimming factors to other input charges results in somewhat worse matching since in addition to the offset of each channel the effective discrimination threshold is also affected by the gain of that channel, which also varies across the channels.



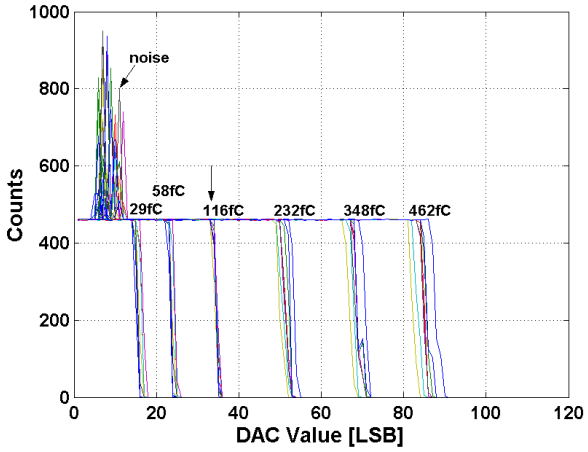




Figure 4: Illustration of the trimming procedure.

## C. Energy channel

The energy channel comprises a slow shaper (with a peaking time $T_p$ = 85 ns) and a classical peak detector and hold circuit (PDH) [3], which detects the peaks of incoming pulses and holds their values for a given time period triggered by the comparator in the fast timing channel. The shaping function of the slow channel is optimised taking into account the requirements concerning the noise (energy resolution), count rate, dynamic range and speed limitations of the peak detector.

## D. Time stamp generation

The principle and the block diagram of the time stamp generation block is shown in Fig. 5. The 14-bit time stamp signature is composed of a 12-bit Gray-encoded counter

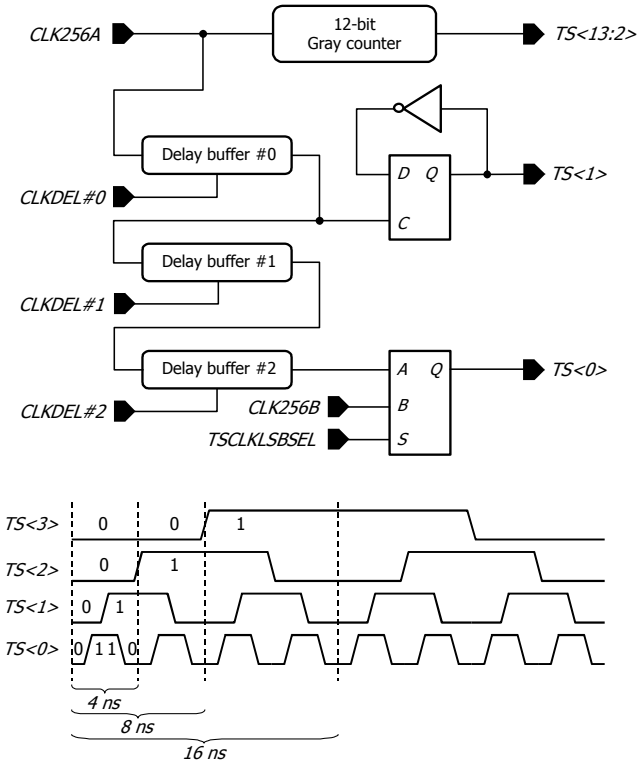



Figure 5: Principle of the time stamp generation.

(TS<13:2>), a toggle flip-flop (TS<1>) and the buffered input clock (TS<0>). The correct timing of bits TS<1> and TS<0>, to ensure that all 14 bits are Gray encoded, is achieved by adjusting the delays appropriately through the programmable delay buffers #0 ÷ #2. In this scheme we can achieve 1 ns resolution at the clock frequency 256 MHz.

## E. Physical design

The MSGCROC ASIC has been designed and manufactured in the 0.35um CMOS process from Austria Microsystems. The dimensions of the ASIC are 3.2×6.7 $mm^2$. Figure 6 shows the microphotograph of the MSGCROC.

A critical aspect of the MSGCROC design, which has been analysed carefully at the level of physical mask design, is the cross-coupling between the analogue and the digital blocks. In order to minimise the crosstalk special attention has been paid to proper isolation between the analogue and the digital parts. Separate power supply busses and bonding pads for each part have been implemented. The analogue and

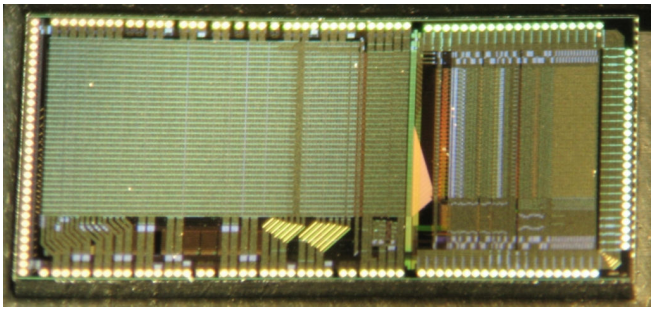


Figure 6: Microphotograph of the MSGCROC ASIC

digital blocks are enclosed in guard rings connected to separate bonding pads. It should be also noted that in the digital part we have used standard cells with the bulk connection separated from the lower (digital) power supply.

## III. Measurements

The test bench for the evaluation of the ASICs performance is based on a standard double-sided silicon microstrip detector of a 300 µm thickness and 50 µm strip pitch (Fig. 7). The detector and the ASICs are mounted on a PCB with a window allowing the connection of the ASICs to each side of the detector. One 32-channel MSGCROC per side is connected to the detector and every second strip of the detector is wire bonded to the ASIC. The ASICs are read out with a custom designed data acquisition board from the SUCIMA project [4], which has been adapted to the structure of the output data and the readout protocol of the MSGCROC. The available data acquisition board can deliver a clock signal of 128 MHz.

The basic functionality of the prototype ASIC has been investigated using electronic signals delivered by the internal calibration system. Although the MSGCROC has been designed for higher input charges from the MSGC detector, setting up the highest gain (x16) in the preamplifier allows us to measure also lower charges from a silicon strip detector.

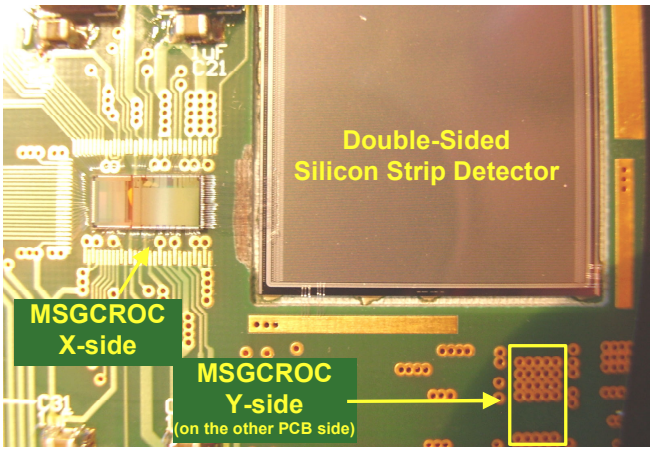



Figure 7: Prototype evaluation board based on a double-sided silicon strip detector.

### A. Timing measurements

A histogram of time coincidences between signals from two MSGCROC ASICs connected to X and Y channels is shown in Fig. 8. As expected for the clock frequency of 128 MHz, the majority of events is confined within a single bin of 2 ns. The plot confirms that the time jitter is well below 2 ns FWHM, as expected for a relatively low input capacitance represented by the silicon strip detector. We observe some tails in the distribution, which are most likely due to errors caused in the data acquisition system by the clock skew and clock jitter.

### B. Energy measurements

The response of the full energy channel, including the PDH circuit, analogue memory and analogue multiplexer, for different preamplifier gain settings is shown in Fig. 9. The measured relative gain factors are: ×1, ×1.8, ×3.7, ×7.9 and ×19.6. They differ slightly from the nominal values, however, the exact values of the gain factors are not critical as long as the different settings cover the full range of expected input signals.

The single strip amplitude distributions of electrons from a $^{90}$Sr source and of γ-rays from a $^{241}$Am source measured with the silicon strip detector are shown in Fig. 10. The measurements have been performed in the typical operation mode of the MSGCROC. The analogue signals have been read out at the end of the entire energy channel, i.e. preamplifier, slow shaper, PDH circuit triggered by the signal from the timing channel, analogue memory and analogue output multiplexer operating at the nominal clock frequency of 32 MHz.

For electrons one expects a Landau distribution and for γ-rays a Gaussian distributions. Let us note that the measured distributions are affected by two effects: (i) because of charge sharing between neighbouring strips one would expect tails extending towards lower energies, (ii) because the measured signals are just above the noise level in the timing channels the lower parts of the distributions, especially for the γ-rays are cut off by the discrimination level.

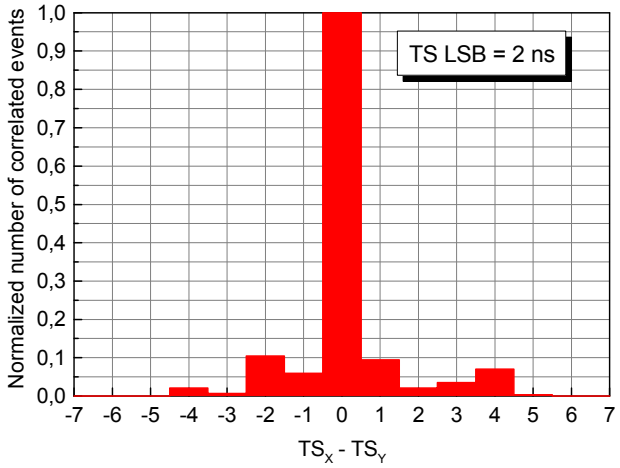



Figure 8: Distribution of coincidences between signals from two MSGCROC ASICs connected to X and Y channels.

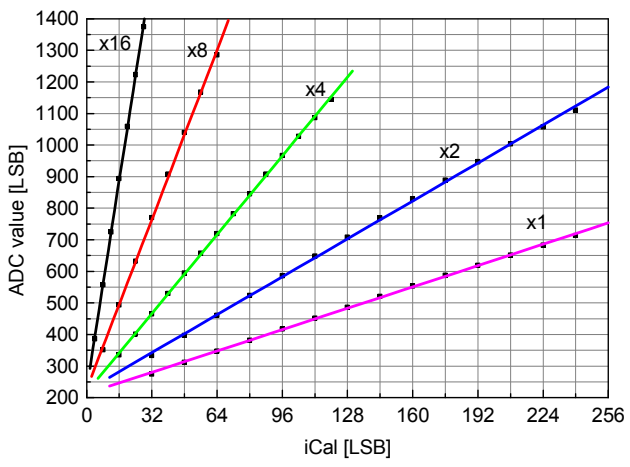



Figure 9: Response curves of the energy channel for different gain settings in the preamplifier.

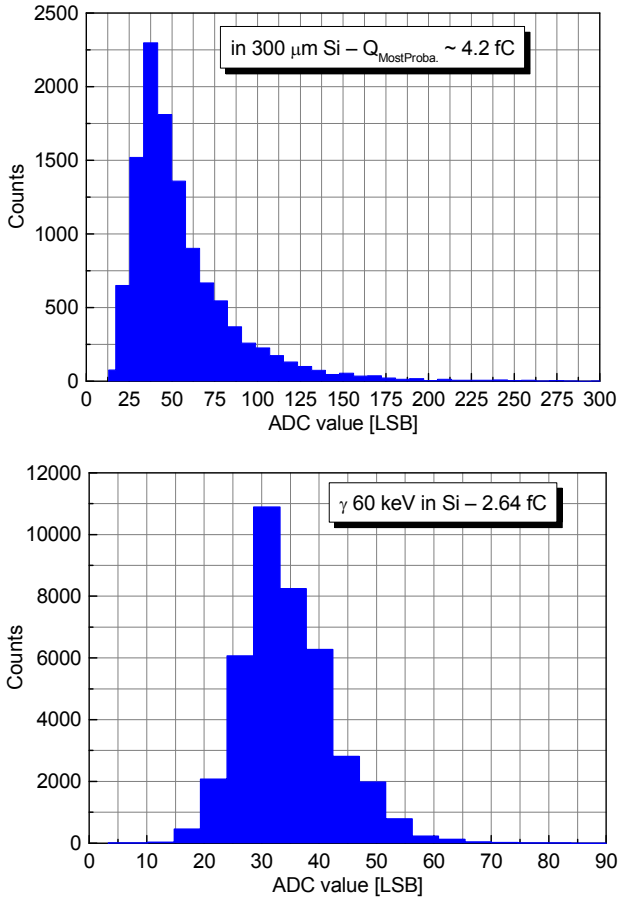



Figure 10: Amplitude distributions of electrons from a $^{90}$Sr source (upper plot) and of γ-rays from a $^{241}$Am source (lower plot) measured with the silicon strip detector.

## IV. Summary

Future high intensity pulsed neutron sources will require novel detectors with higher counting rate capability and high time and position resolution. Novel detectors and dedicated advanced readout ASICs are developed in the frame of the European DETNI project. A first 32-channel ASIC with complete functionality required for the readout of double sided MSGC detectors with composite $^{157}$Gd/CsI converter has been designed and manufactured. The performed electrical tests of the ASICs as well as the measurements performed with a test bench module based on a double sided silicon strip detector have confirmed correct functionality of all building blocks and compliance of the ASIC parameters with the design specifications. The MSGCROC ASICs will be used to build a full size MSGC detector module, which will allow us to perform further detailed evaluation of the ASIC performance.

The developed MSGCROC ASIC is a first experimental proof of the novel method of readout of double-sided strip detectors, which makes these technologies suitable for measurements with count rates of $10^8$/s per detector module and 2-D spatial resolution below 100 μm FWHM. With these parameters the double-sided strip detector technology becomes competitive with the technologies based on pixelated detectors.

## V. Acknowledgements

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## VI. References

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