Development of a small-scale prototype of the GOSSIPO-2 chip in 0.13 µm CMOS technology.

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Abstract

The GOSSIP (Gas On Slimmed Silicon Pixel) detector is a proposed alternative for silicon based pixel detectors. The Gossip Prototype (GOSSIPO) chip is being developed to serve as a prototype read-out chip for such a gas-filled detector. Thanks to the very low capacitance at the preamplifier input, the front-end of the chip demonstrates low-noise performance in combination with a fast peaking time and low analog power dissipation. Measurement of the drift time of every primary electron in the gas volume enables 3D reconstruction of the particle tracks. For this purpose a Time-to-Digital converter must be placed in each pixel. A small-scale prototype of the GOSSIP chip has been developed in the 0.13 µm CMOS technology. The prototype includes a 16 by 16 pixel array where each pixel is equipped with a front-end circuit, threshold DAC, and a 4-bit TDC. The chip is available for testing in May 2007 and after initial tests it will be post-processed to build a prototype detector. This paper describes the detector design goals, the design of the chip and the first experimental results.

I. Introduction: The Gossip Detector

Present particle detectors that reside close to the interaction point of accelerator based experiments (e.g. at the LHC) are built using silicon as detector material. In the silicon a passing particle creates free hole-electron pairs that can be detected by connected front-end electronics. A strong requirement of such a detector is that it should be made with the smallest amount of material as possible. Any material in the detector volume deteriorates the detector performance. Therefore, low power dissipation is essential for these detectors. Radiation hardness is another fundamental issue.

In order to develop a new detector for future experiments (higher track density and total dose) like for the International Linear Collider (ILC) or Super LHC (SLHC), an alternative for Silicon detectors is very interesting. By using (refreshable) gas as detector material, radiation resistance seems a good step forward. The gas can also be used for cooling, and when the drift time of individual electrons in the volume is measured, tracks can be reconstructed, even in layers of a millimetre thick.

To demonstrate this detector concept, prototypes are necessary. Therefore the use of a gas layer has been tested using available pixel front-end chips (MEDIPIX-2 [1], PSI-46).

After a preamplifier and discriminator for this type of detector have been designed in 130 nm CMOS technology and tested in 2006 [4], the next step is to build a GOSSIP detector based on this design [2]. This requires an array of pixels, with control and test functions, and readout.

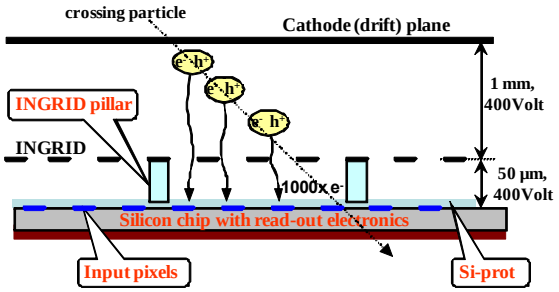

Figure 1 Principle of GOSSIP detector

The GOSSIP concept [2] is based on multiplying a single primary electron in a gas volume with an applied strong electric field, in which an avalanche generates more free electrons. The drift volume has a thickness of about 1mm, and the gas gain takes place in the gap between a mesh (INGRID) [3] placed 50 µm above the sensitive pads (see **Error! Reference source not found.**). These pads are connected to a preamplifier. The probability that at least 1 electron-hole pair is generated in the 1 mm suitable gas volume is 99%, and the gas gain can be arbitrarily high. The maximum drift time in the 1 mm region is 16 ns.

The INGRID (Figure 2) can be added to a (single) chip by means of post processing using photo lithography. In order to protect the sensitive inputs of the preamplifier against unavoidable discharges, typical for a gas filled detector, a high resistivity layer of amorphous silicon ('SiProt') is put on the chip surface first (see Figure 1).

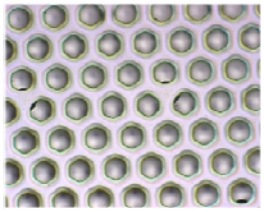

Figure 2 Example of INGRID with 55 µm pitch

A. Requirements for detector electronics

Starting with a gas gain of 1000, the average input charge is 1000 e^-, so a threshold for good single electron efficiency would be about 400 e^-. In order to minimize the number of noise hits, a 5 times lower noise level (σ) would be appropriate, resulting in about 80 e^- equivalent noise charge at the input of the input amplifier.

For proper track reconstruction an accurate drift time measurement is required and therefore the preamp and discriminator must be able to give a fast response to the input signal, in about 10 ns.

Because variations of the signal development in the gas volume, the noise (jitter) of the preamp, variations in threshold and gain, and time-walk of the discriminator all decrease

the time accuracy of the original particle hit, the value for the resolution of the time measurement is in the order of 2 ns.

Optimization of the requirements should come out of large scale simulations and calculations where optimal values will result in acceptable detector efficiency with good accuracy at reasonable costs of power dissipation and electronics (IC) design effort.

For a final design (e.g. a vertex tracker in S-LHC), the power dissipation must be low and the goal is to keep the total dissipation when active below 2 µW per 55 x 55 µm pixel cell.

II. Design of the Prototype Chip

The existing front-end design forms the basis of this pixel array. The chip will contain an array of 16 x 16 pixel cells at a pitch of 55 x 55 µm. The total sensitive area becomes 0.88 x 0.88 mm^2. To be able to process the chip later, adding an Integrated Grid (INGRID) on the array, about 0.5 mm area is required around the pixels, not covering the bond pads. The chip size is 2 x 3 mm (Figure 3), designed in standard 130 nm CMOS, using a triple well option to isolate sensitive circuit parts from the substrate, and using 8 metal layers. Layer 6 is used to create a shield between the electronic (digital) circuits and the sensitive input pads and layer seven to distribute the test signal. The power lines for the analog and digital circuits are strictly separated; there are also separate power pins. In this prototype chip, the radiation robustness requirements for the final design are not taken into account.

The chip contains the pixel cell array, and for detailed debug- and characterisation purposes, 3 individual analogue pixel cells (with different pixel pad sizes) one digital pixel cell part, and a current bandgap reference cell (not discussed in this paper).

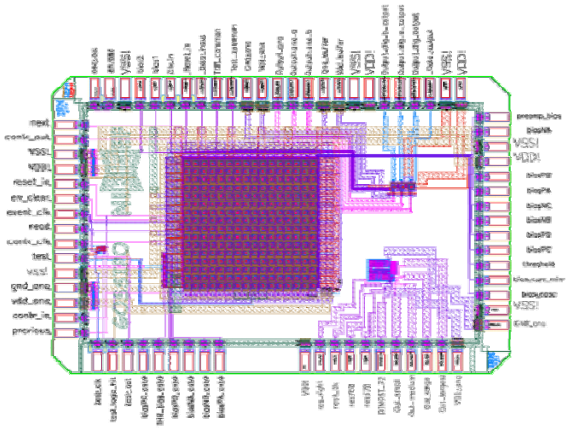

Figure 3 layout of the GOSSIPO chip

Each pixel cell (Figure 4) contains a preamp, discriminator, a 4 bit threshold DAC, control logic, oscillator, two 4 bit "counters" and a 6 bit configuration register.

A. Functionality

The chip needs just a few control signals for operation: Reset, (Event) Clock, Read and Threshold. The analogue part requires bias voltages, and for testing a test pulse can be applied to all pixel cells. The event clock is basically the bunch crossing frequency of the accelerator, in this case 40 MHz. The read signal is used to switch the chip between data taking and data readout mode.

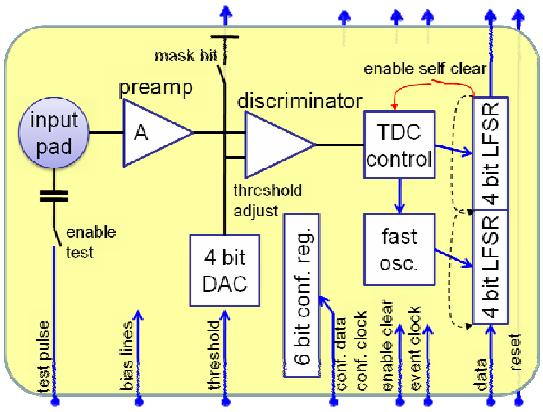

Figure 4 Pixel cell block diagram

The (inverted) drift time is measured from the moment that the pixel is hit until the end of the event (clock) cycle. In this way logic is only active shortly when there is a hit, and $t_{drift} = 25\ ns - t_{meas}$.

When a pixel receives charge that is more than the applied corresponding threshold level, the discriminator will fire and the pixel logic will start the fast (560 MHz) oscillator to measure the drift time. This will run until the first rising edge of the event clock and feeds a fast 4 bit counter. After it has stopped, the second 4 bit counter will start (40 MHz). This one counts the number of clock cycles between the hit and the readout. In this way we can readout (externally) triggered events, where the trigger has a defined latency (max. 350 ns). During readout, the value of both counters will shift out, and the pixel cells are cleared after the readout.

If the self clear function is enabled, the pixel cell will be reset after this second counter has reached its last value. If the self clear function is disabled, the second counter does never start and the pixel will hold the hit until a readout is started. In this way noise hits can be detected in a longer time window.

Because the counter is used as register, data taking is not possible during readout.

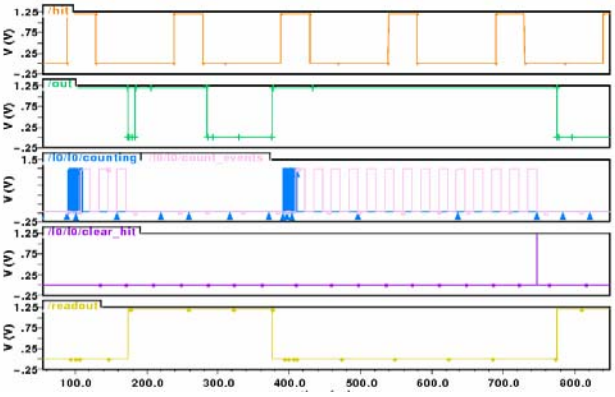

Figure 5 Simulation of pixel logic

During readout, all pixels are connected in series, which means that 256 x (4 + 4) = 2048 bits will shift out of the chip. Figure 5 shows a simulation where two hits are being detected, but only one will be readout. The upper curve simulates a discriminator output, and the bottom curve the readout signal. In the middle graph, the fast- (dense) and slow clock

can be recognized, which are a result of a hit pulse. In this simulation the enable clear function is active. The first readout pulse comes in time and the data (2nd curve) is shifted out, while the second readout comes too late and the pixel cell is already cleared by the clear_hit signal (4th curve) before the start of the readout pulse.

The configuration of the pixel data is done via a 6 bit register in each pixel: enable_test, mask and 4 DAC bits; in total a 1536 bits shift register.

B. *The Front-end*

The design of the front-end is based on a charge sensitive preamplifier [4] (Figure 6). Detector features a very low capacitance of the pixel pad, ±10 fF, and with parasitic capacitance of the routing on chip the total input capacitance becomes about 30 fF. The expected noise is ±75 e^- RMS, gain ±60 mV/1000 e^-, and the peaking time is 30 ns with the expected detector signal.

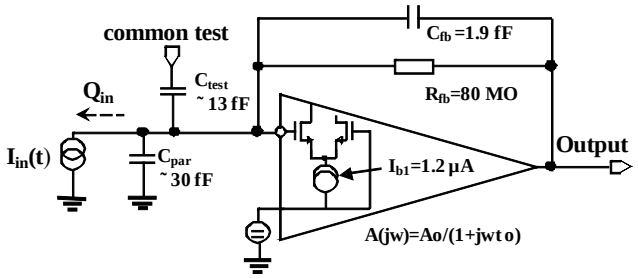

Figure 6 GOSSIPO preamp

The layers used at the input of the preamp can be seen in Figure 7. This layout has been established in deliberation with the chip foundry since it is not according to the layout design rules of the technology. The test input, C_{test} is made between Metal layer 8 (M8) and M7, the two top metal layers of the technology, so between the pad and the layer below that (horizontal plate cap.). The feedback capacitance, C_{fb} is made

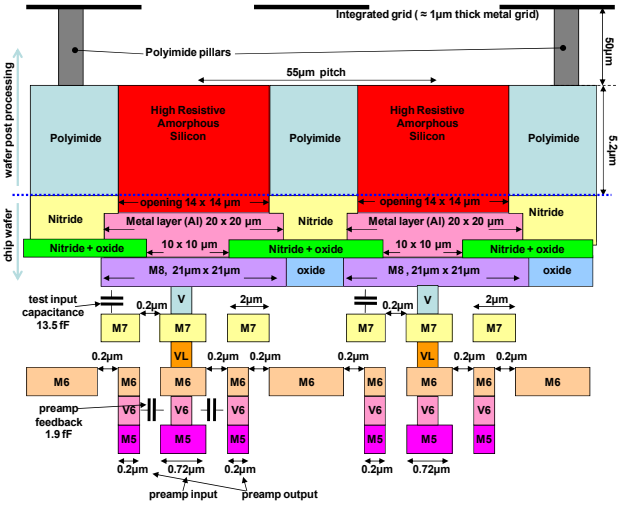

Figure 7 Layer stack of the input pad

between the edges on layers M3 to M6 (fringe cap.). The parasitic C_{par} comes from all parasitic capacitances of the pad and the via's to the input transistor to its environment (mostly substrate, gnd).

The discriminator, improved with respect to the previous version (current comparator), is now a differential pair voltage comparator with hysteresis (±70 e^-). The internal time delay is ±8 ns for large signals and ±30 ns for signals just over threshold. The threshold spread, due to comparator offset, preamp gain and baseline variation is about 26 mV (σ) which corresponds to 430 e^-.

The currents through the circuits are 1.2 µA for the preamp, 0.25 µA for the preamp output and 0.25 µA for the comparator. This results in 1.7 µA and 2 µW for the analogue front-end at 1.2 V supply voltage.

To compensate for threshold spread between pixels, a 4-bits DAC is used in each pixel. The required range (5 σ) is 130 mV, and this is implemented by controlling a current through a resistor (400 kΩ) in 15 steps, such that the local threshold voltage can be decreased. For maximum compensation with the DAC, 300 nA DC current is used. The DAC range can be controlled via an external bias input that controls the central current for the DAC.

In addition the threshold can be pulled up to Vdd to effectively mask the pixel cell (see Figure 4).

Special attention is paid to the spark protection at the input of the preamp. By using Si-Prot, the expected charge at a breakthrough of the drift voltage depends on the pixel pad area and the Si-Prot thickness. For a 5 µm thick layer and a pad of 14 x 14 µm the charge becomes ~10 pC. This charge can easily be dissipated in a small diode like the source of a NMOS transistor. This transistor and a required tie-down diode are in the circuit for DC feedback of the amplifier and are connected to the input, and therefore the circuit should be spark proof.

A passive test signal line is routed to all pixel cells, and a switch (NMOS transistor) is implemented in each pixel to control the test signal. The signal is coupled to the preamp input via a capacitor of 13.5 fF (see Figure 7).

C. *The TDC*

Because the accelerator bunch cycle time was expected to be 25 ns, a 4 bit TDC is chosen which results in 25 / 15 = 1.67 ns time resolution.

Since the pixel area, with all its electronics, is limited (55 x 55 µm), the use of chip area for the circuits is important. Therefore, Linear Feedback Shift Registers (LFSR) are used for the counters: four D-Flip-flops with a XNOR as feedback (Figure 8). A 4 bit LFSR has one "dead" state, so the time resolution becomes 25/14 = 1.78 ns. Because the LFSR is a shift register, the readout circuit does not require an additional register, and logic to control the readout can minimized.

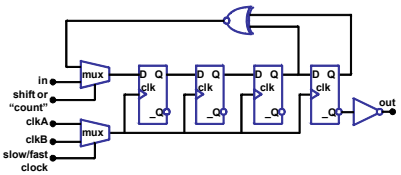

Figure 8 Fast (560 MHz) 4 bit Linear feedback shift register (LFSR)

To keep the power consumption to a minimum, a fast clock distributed to all the pixels is not an option. Instead, a local clock is generated in each pixel, only during the period that time must be measured. Therefore a fast oscillator (1 / 1.78 ns = 560 MHz) is implemented in each pixel.

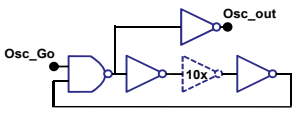

Figure 9 Local oscillator

The oscillator (Figure 9) is build with a NAND to control it, and 12 inverters to determine the proper delay. This approach results in a simulated frequency variation of -0.1 % per mV of supply voltage, and + 0.2 % per ºC of temperature. For one LSB variation (1.78 ns) this will give a range for T of ±30 ºC and a range for Vdd of ±60 mV.

An extra flip-flop is added to the circuit's control input to secure a glitch free output signal when the oscillator is stopped. An individual oscillator is placed on the test chip for detailed characterisation.

The power dissipation of the TDC is about 200 µW during the hit, but with an expected hit rate of 100 kHz / pixel, the average power becomes 250 nW / pixel.

D. *The readout*

To keep the test chip simple, no additional logic is necessary for the readout of the array. This means that only the pixel logic controls the readout. The control signals are buffered per column and the data shifts like a meander over the chip. Standard buffers send the data off chip. Since 40 MHz is used as chip clock no special features are required to drive the signals. There is the possibility to connect several chips in series, for building a larger detector area.

III. Measurements on the Chip

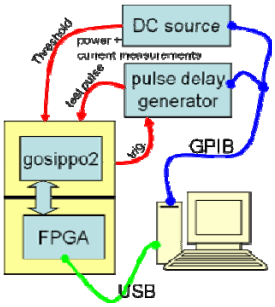

Figure 10 Test set-up

The GOSSIPO2 test set-up (Figure 10) enables us to characterize the individual circuits by accessing all pins (e.g. bias voltages). A PC controls the environment for automated tests, and makes it usable for a beam test later.

A FPGA is used to interface the GOSSIPO2 chip with a PC via a USB port, it can read and write the configuration registers, readout the pixel array and synchronize an external trigger signal (cosmic ray tests) with the local event clock. By controlling a DC-source for the threshold voltage, and a programmable delay (10 ps res.) for the test pulse, the chip can be fully characterized using this setup.

From the MOSIS MPW we received 40 chips, and 10 are packaged for tests, the others can be used for detector prototyping.

For all measurements, a positive δ pulse (~1 ns slope) is used to inject charge on the preamp inputs of all pixels on the chip. The chip supply voltage (Vdd) is 1.2 V.

A. *Front-end*

The analog part can only operate properly when its bias conditions are correct. The measured values are in correspondence with simulation although the spread is a bit more then expected. The basic front-end properties are measured on the three individual analog pixel cells of 10 chips.

The test capacitance is larger then expected; manual calculation of the capacitance based on the geometry in the layout results in better correspondence with the measurement than the extracted values that come out of the design software. The calculated value is 13.5 fF while the software gives 3 fF.

The preamp shows about 80 e^- noise (input referred), with 55 mV / 1000 e^- gain and 35 ns peaking time. This corresponds very well with simulations.

The discriminator shows a mean threshold of about 400 mV with a spread of 150mV (peak to peak). This spread corresponds to about 540 e^- (σ), and is a more then the expected 430 e^-.

The propagation delay from a test pulse (20000 e^-) to the output has a mean value of 23 ns with 29 ns spread (peak to peak). The delay and spread can be decreased by increasing the discriminator current (costs about 0.25 µA per pixel for ½ the delay). The time jitter at the output of the discriminator is between 2 and 3 ns.

B. *Oscillator and TDC*

The individual oscillator runs at 530 MHz +/- 10 MHz and varies -1.0 MHz/°C and 56 MHz/100mV supply voltage. The frequency is 30 MHz lower, but the Vdd and temperature dependency is equal to the simulation result. Further TDC results will be discussed in the array measurements.

C. *The 16 x 16 pixel array*

Three measurements can characterize the chip; a threshold scan with test pulse (two amplitudes), a threshold scan with every pixel DAC value and a time delay scan with test pulse.

Two threshold scans with different test pulse amplitudes will give information for each pixel about the baseline value (= actual threshold level), the noise level (s-curve) and gain.

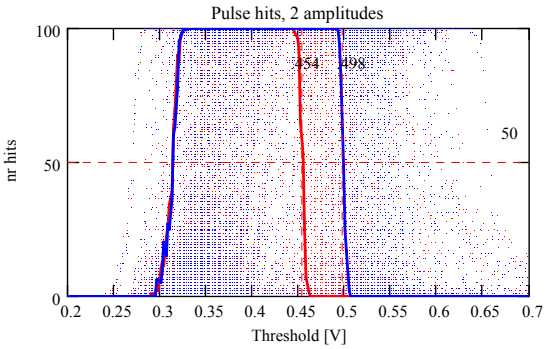

Figure 11 Hit counts of threshold scan

Figure 11 shows the result of two threshold scans, one with 1680 e^- and one with a 2530 e^- test pulse (100 measurements for each threshold value). The data of one arbitrary pixel is highlighted. The threshold value of the rising slope of the "pulse" is at the baseline (DC value of the preamp output), and the falling slope is at the peak of the output pulse of the preamp. The difference of the threshold values at the two falling slopes corresponds to the gain. From the width of the falling slope (S-curve) one can determine the noise (again about 70 electrons RMS).

The gain of all pixels in a chip is plotted in Figure 12 and the mean value of the working pixels is about 55 mV/1000 e^-.

There are many (>30) channels with a bad gain value; this is unacceptably high. Up to now this is not understood. But since the spread in bias values is more than expected, it is possible that some circuits are not operating at the correct DC operating point.

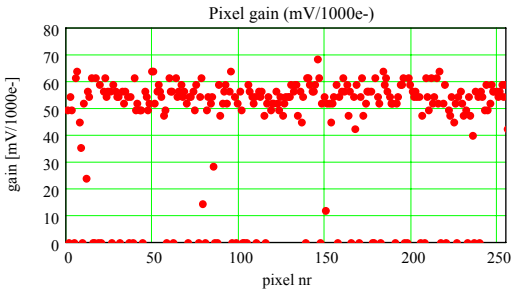

Figure 12 Gain of all pixel cells (one chip)

The test pulse delay scan in Figure 13 shows the TDC behaviour of one pixel over almost three 25 ns clock periods (average over 50 measurements). The test signal injects about 5000 electrons in each pixel at the same time. From the falling slope of the curve of the drift time counter, the jitter at the output of the discriminator can be found, 3-4 ns. The spread of the delay over the chip is about 10 ns.

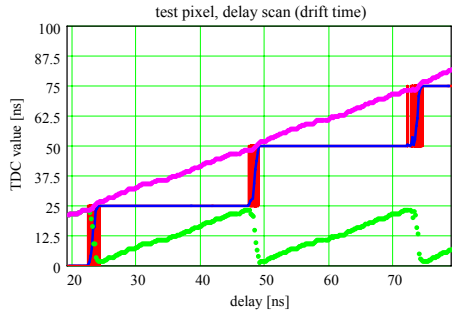

Figure 13 Test pulse delay scan; drift time counter (lower), latency counter (middle), and the sum of both (upper).

The integral non-linearity (INL) for this TDC is 2 ns, which is 1.2 times 1 LSB. A plot of an INL measurement with the data of two pixels (average over 50 values per time step) is shown in Figure 14. At Vdd = 1.2 V, the local oscillator frequency is 530 MHz, but by tuning the Vdd, the average oscillator frequency can be set at 560 MHz which results in better correspondence of the measured values for the delay.

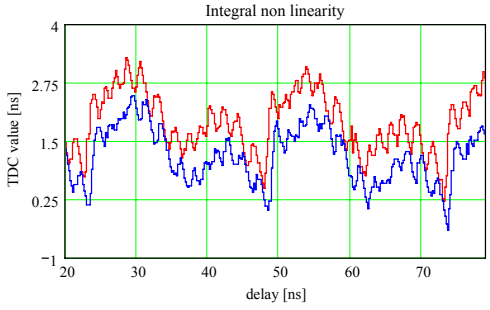

Figure 14 Integral non-linearity of two pixels: mean over 5000 measurements

Optimal values for the whole pixel array can only be obtained after a calibration run, where all pixel DAC's are set with the value for the most homogeneous threshold distribution.

IV. Future work for GOSSIP front-end

More statistics and measurements of more chips are necessary to fully characterize and understand the design.

The high voltage breakthrough protection is an ongoing issue with the first priority. The presence of diodes to ground in this chip together with a SiProt layer must be verified. This will be done with a detector built with this chip.

Masks for the post-processing for the INGRID are now being designed. After the INGRID is added an assembled detector will be placed in a beam test and should demonstrate the behaviour as particle detector.

For next generations of the GOSSIP front-end electronics, specific readout architecture needs to be designed. Features like two buffers per pixel cell, bunch identification per hit, and fast serial readout, with data taking during readout capability need to be addressed, as well as radiation hardness.

V. Conclusions

The present GOSSPO-2 chip is suitable for building a real GOSSIP detector prototype. The sensitivity for the low input signals and the noise level correspond very well to the design specifications. The TDC per pixel with local oscillator will enable us to perform drift time measurements in a 1 mm gas volume and the jitter should be acceptable for track reconstruction.

The switching noise of the pixel logic and the oscillator do not influence the sensitivity of the chip. Noise measurements with a large time window show that pixels activated by thermal noise do not activate neighbouring pixels. The triple-well isolation of sensitive circuits is a good method to achieve this.

The number of "dead" channels per chip (20-30) is unacceptable. This needs to be improved. Matching properties of the circuits are very important for next designs.

VI. References

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