Data transmission and selection for the L0 calorimeter trigger of LHCb

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Abstract

This report describes the optical transmitter boards and the Selection Crate, designed by the Bologna INFN-LHCb group, for the data transmission and the L0 calorimeter trigger of the LHCb experiment. The optical transmitters are used throughout the calorimeter system for data acquisition and the data transmission to the L0 trigger system. The optical transmitters allow transmitting 32 bit at the LHC clock of 40.08 MHz on a single fibre. The Selection Crate (SC) is used to select the most energetic deposits detected by the electromagnetic and the hadron calorimeters of LHCb, as well as to evaluate other auxiliary global trigger quantities (i.e. the total energy released and the hit multiplicity). The Selection Crate is a modular system equipped with homogeneous Selection Boards.

INTRODUCTION

The L0 trigger system of LHCb will be used to select interesting collisions, where beauty quarks production occured, while reducing the 40.08 MHz bunch crossing rate of LHC to the sustainable rate for the High Level Trigger of 1 MHz [1]. The calorimeter system of LHCb selects events on the basis of a threshold on the highest energetic energy deposits detected by the electromagnetic calorimeters (ECAL) or by the hadronic calorimeters (HCAL). The energy of the cluster is measured by the front-end boards summing up the energy over a 2x2 calorimeter cells extended area (the size varying from the 8x8 cm^2 of inner most ECAL region, to 52x52 cm^2 of the outer HCAL). ECAL is segmented in 5952 cells (each one being a possible cluster source) [2]. In order to identify the nature of the electromagnetic clusters (as electron, photon or π^0) cluster validation is performed by means of the coincidence of the electromagnetic calorimeter signals and the signals from the PS/SPD auxiliary detectors. HCAL from the other side is segmented in 1484 cells. For a correct HCAL cluster energy evaluation a mechanism is foreseen which allows for recovering the energy lost by particles traversing ECAL before hitting HCAL (it is located beyond ECAL, with respect to the interaction region). Front-end and the validation electronics boards are located in the experimental area, nearby the detector, while the Selection Crate, L0 Trigger Decision Unit and L1 Trigger Buffer electronics boards are located in a radiation protected area, at a distance of about 100 meters from the detector. The 28 foreseen Validation Cards (VC) used for cluster validation, transmit local highest ECAL clusters to the SC through ribbon fibres 100 m long. The SC sends to the L0 Decision Unit (L0DU) the highest energetic clusters, the total energy and the hit multiplicity over optical fibres 5 m long. In case a L0-Accept condition is satisfied all the input and output data used/produced by the SC are packed and transmitted to the TELL1 boards of the L1 Buffer, which is used to inject the L0 calorimeter information into the HLT trigger farm as IP datagrams. Figure 1 shows the main components of the L0 calorimeter trigger system sketched above.

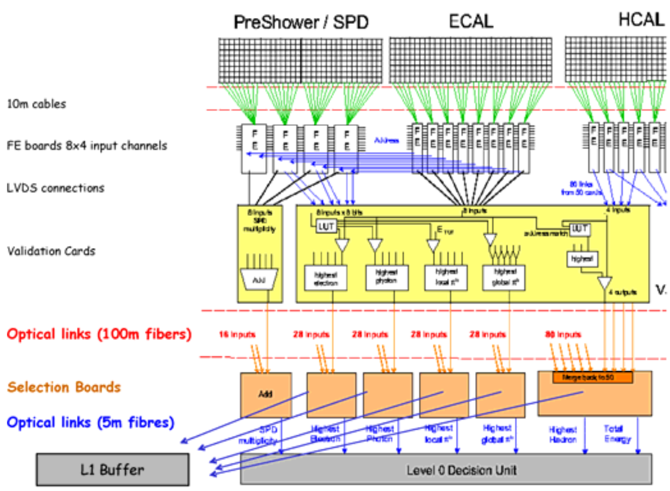

Figure 1: The LHCb L0 calorimeter trigger scheme

OPTICAL TRANSMITTERS

Two different types of optical transmitter boards have been designed to transmit data by the electronics boards from the region nearby the detector to the electronics boards located in the barrack, 100 m away: they are referred as multi-channel and single-channel optical transmitters.

A. *Multi-Channel Optical Transmitter*

The multi-channel optical transmitter modules (MCM) are built as pluggable boards. A picture of a MCM board is shown in Figure 2, the MCM logic scheme is shown in Figure 3.

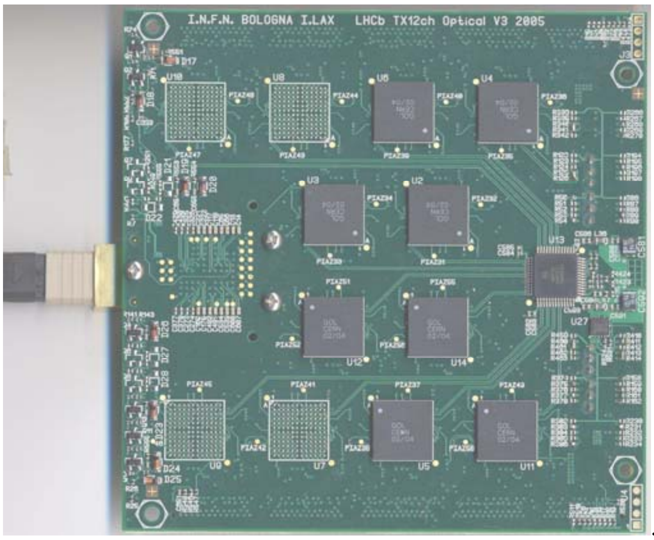

Figure 2: Picture of the multi-channel transmitter board

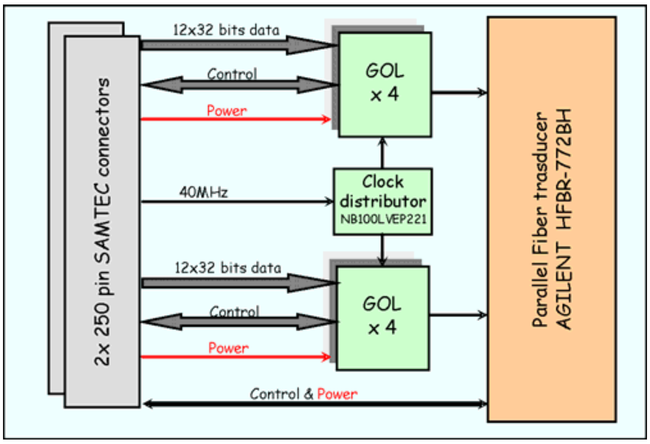

Figure 3: Multi-channel module block diagram

A MCM consists of 8 independent transmission channels. As it can be seen from Figure 2, the MCM can host up 12 transmission channels. The number of instrumented channels as requested by the end-users has been reduced to 8. Each transmission channel handles 32 bit data words at the LHC frequency of 40.08 MHz. The 32 bit data words entering a transmission channel go to a Gigabit Optical Links (GOL) [3] which performs data serialization of the incoming parallel stream using the 8B/10B encoding protocol. The encoding protocol maintains the signal DC balance, providing a good transition density for clock recovery, improving the error checking. The channel output bit rate, included the 8B/10B protocol, is of about 1.6 Gbps. As optical signal transducer to pulse the optical fibre is used the AGILENT HFBR-772BH [4]. It is plugged to the board by a 10x10 contacts array socket. It can drive up to 12 x 50/125µm 850nm multi-mode optical fibres, grouped in a ribbon of 12 fibres. It is equipped with a receptacle with guiding pins and accepts MPO-F standard optical connectors. The MCM is supposed to be driven by clock signals provided by the carrier board. The clock tree has been implemented by means of the NB100LVEP221 device, a differential clock driver manufactured by ON Semiconductor [5]. Each transmission channel is addressable both by JTAG and I^2C.

The total number of assembled and tested MCMs is 100. Each of the 28 Validation Cards hosts 1 MCM. In addition, 52 MCMs are used for data acquisition, being plugged to the Calorimeter Readout Optical Cards (CROCs). 18 MCMs have been built as spare.

B. *Single-Channel Module*

The single-channel optical transmitters (SCM) are built as pluggable board, consisting of a single channel optical transmitter, allowing the transmission of 32 bit patterns at 40.08MHz. Pictures of the SCM board are shown in Figure 4, while Figure 5 shows the SCM logical scheme.

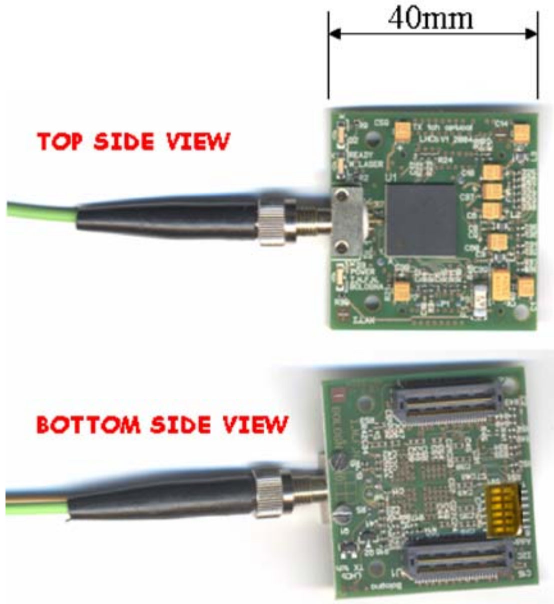

Figure 4: Pictures of the single channel board

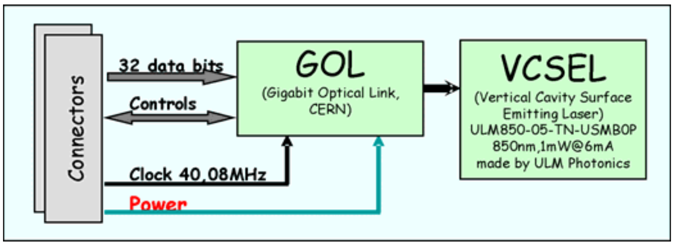

Figure 5: Single channel module block diagram

A single GOL device is directly connected to a ULM850-05-TN-USMB0P 1mW VCSEL laser diode, manufactured by ULM Photonics [6]. The VCSEL diode allows driving a 50/125µm 850nm multi-mode single fibre. Its receptacle has a SMA standard threaded optical connector. The GOL chip has to be driven by a differential clock signal to be provided by the carrier board. The SCM is both JTAG and I^2C addressable.

The total number of SCMs assembled and tested is 50. For the need of the PreShower & SPD detectors a number of 16 SCMs have been foreseen, while the 8 SBs need a total of 24 SCMs. The remaining 10 SCMs are assigned as spare.

BER MEASUREMENT

For prototypes qualification the Bit Error Rate (BER) measurement has been performed using the set-up of Figure 6 below:

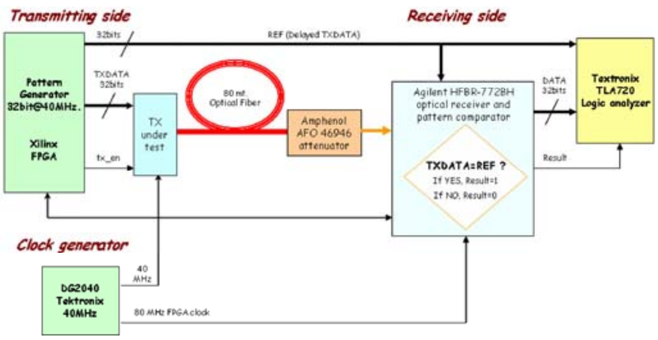

Figure 6: BER measurement set-up

The test setup consists of a 32 bit pattern generator running at 40.08MHz, used to feed up the optical transmitter board under test which is in turn connected to a receiver board through an optical fibre of 80 m length. The receiver board uses an AGILENT HFBR-782BH [7] optical receiver and hosts a dedicated decoding logic and comparators. Data transmitted through the optical link go to the receiver board also through a parallel bus to be used as reference patterns for data comparison. Input data patterns and the results of the comparison are transmitted to a logic analyzer to be easily inspected.

Duration of the BER tests lasted from 5 hours up to 1 day, depending on the level of the light attenuation being set to evaluate the performance of the link under test. For attenuation values between 0 dB and 8 dB, the measurements show that the BER level is below 10^{-13}, as expected. The optical attenuation in real working condition, due to the fibre length of about 100 m and to the presence of a couple of intermediate optical patch panels, has been measured at the level of 1 dB, well below the critical value.

THE SELECTION CRATE

The Selection Crate is hosted in a 9U VME standard crate. The power backplane however is not standard, having been customized by LHCb to drive the L1 buffer TELL1 boards. The SC consists of 8 Selection Boards that allow performing the entire data selection. 4 SBs are used to handle ECAL cluster candidates, 3 are used to handle HCAL candidates, 1 SB is used to evaluate the hit multiplicity by receiving data from the SPD, 4 more SBs have been built as spare. A picture of a SB is shown in Figure 7. The SBs are used to provide the following information to the L0DU at 40.08 MHz:

- The highest energy candidate for each foreseen particle type (electron, photon, π^0 local, π^0 global, hadron);
- The 14 bit global cluster address, by translating the 8 bit cluster local address, as it is defined by the FE boards, by means of a dedicated LUT;
- The total HCAL energy release and the SPD multiplicity, to be used as trigger quantities.

As the data coming from the Validation Cards are tagged with 8 bit local address, translation to the global 14 bit address, corresponding to the absolute coordinates of the energy deposit is needed. The address translation is performed by means of a LUT, automatically loaded at the SB board start-up. The LUT content can be set through the ECS system (see below).

In case of a L0-accepted event, all the input and output data of each SB have to be moved to the TELL1 buffer boards, at an average rate of about 1 MHz.

The hardware of the Selection Boards is identical. It can be adapted programming the SB FPGAs to serve the different needs depending on the specific task the SB has to perform.

Figure 7: The Selection Board top view

SB TECHNICAL FEATURES

The SB PCB is a 16-layers 2.6 mm thick one. Particular care has been spent in the impedance control and in the length balance while routing of the most important traces.

The SB is equipped with 30 optical inputs, grouped into 3 MPO-M connectors (28 input channels per board effectively connected to the Validation Cards). Each of the MPO-M can accept a MPO-F connector with a ribbon of 12 x 50/125µm 850nm multi-mode optical fibre. The board is equipped with 3 optical SCM boards, used to transmit data both to the L0DU and to TELL1 boards.

The required Experimental Control System (ECS) functionalities are implemented thanks to a versatile on-board diskless computer Credit Card PC (CCPC) [8] and through a PCI interface, named Glue Card (GC) [9] . The ECS is meant to allow for basic and advanced operations of configuration and monitoring such as FPGA programming, register settings, memory addressing, temperature monitoring etc.

Handling of the HCAL clusters requires the processing of 80 hadron clusters. Three SBs have to be used then to perform the selection and get the final trigger quantities. Partial results of two SBs slave boards goes then to a third master SB board via a dedicated custom backplane, inserted on the rear SB sides, as it is shown in Figure 8.

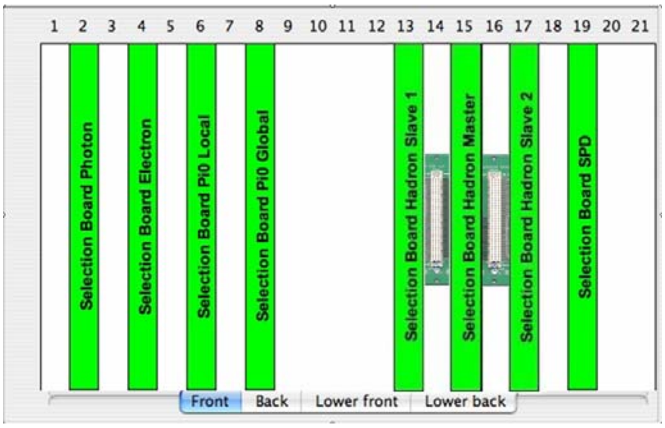

Figure 8: The Selection Crate board layout. The custom backplane used to connect the three hadron SBs is shown above.

SB INPUT LOGIC

The input logic is shown in Figure 9. Data entering the board through the optical channel are converted into electrical signals by the AGILENT HFBR-782BH. The data stream is then de-serialized by TLK2501 device [10], providing 16 bit data words at 80.156 MHz together with the related clock and control flags. A de-multiplexer is used to bring the 16 bit data words back to the 32 bit original format. The TLK2501 provides two control signals (dv and er signals) monitored to identify possible error conditions of the input channel. The 32 bit data words are written into dedicated asynchronous FIFOs (XILINX XC2VP20 FPGA). These FIFOs are used to adjust the variable latency introduced by the serialization/de-serialization devices. The writing control logic is triggered by the TLK2501 dv signal. The reading logic is triggered instead by the BCRST signal of the LHC TTC system, properly delayed. This way the input channels can be read-out synchronously. Diagnostic FIFOs, controlled via the ECS system, can be used to inspect the status of the input channels allowing recording 256 consecutive events. ECS programmable pattern generator and comparator are also foreseen, meant to allow for BER tests of the optical links on-site.

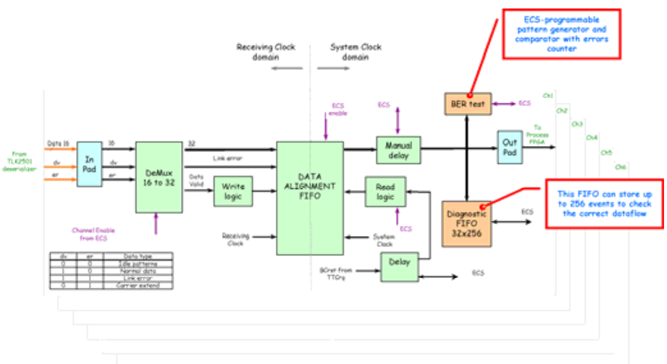

Figure 9: Input logic blocks to the active FIFO.

SB PROCESS LOGIC

A SB is equipped with 5 input buses, each connecting 6 input channels directly to the main process FPGA (XILINX XC2VP40 FPGA). The process FPGA is used to execute the whole trigger algorithm. The main blocks of the SB process logic implemented in the process FPGA are shown in Figure 10. Trigger processing implies the following actions in sequence: the 8 bit to 14 bit cluster address conversion, the selection of the highest energetic cluster and summing up clusters energy, and in the case of the HCAL clusters, evaluation of the total (transverse) energy. Processing results have to be moved to the SCMs to be transmitted to the L0DU.

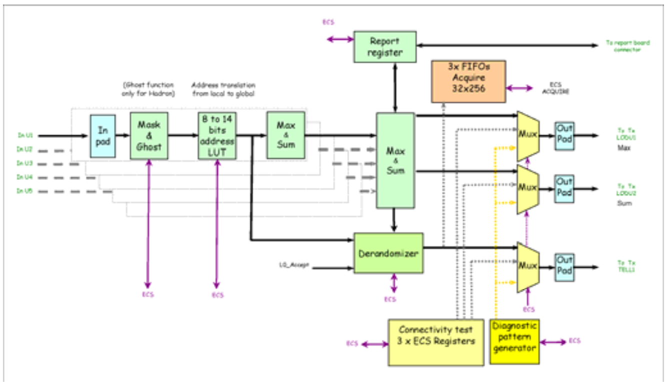

Figure 10: The SB processing logic.

The de-randomizer buffer is used to transmit 36 words of 32 bit to the TELL1 in case of L0-accept. The de-randomizer buffer contains the input and the output data of the current SB trigger processing state. The maximum allowed transmission latency for data transmission to the TELL1 is 900 ns. A maximum of 16 consecutive L0 accepted events is allowed.

As debugging feature three 32×256 bit FIFOs are foreseen to store and retrieve the output of the trigger processing. Moreover it is also possible to perform connectivity and BER tests between any SB and the destination boards L0DU and TELL1.

A first SB has been successfully installed at CERN Point 8 in April 2007. Afterwards, HCAL high energy deposits have been simulated by means of the calibration LEDs pulses. The related events have been triggered and reconstructed, as it shown in the example of Figure 11.

HCAL

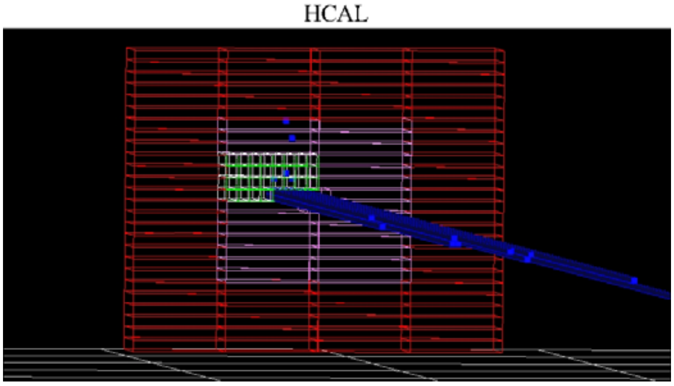

Figure 11: HCAL triggered event. The energy deposit has been produced by means of the HCAL calibration LEDs .

The Selection Crate configuration and monitoring software is under development. It relies on DIM and PVSS [11]. A preliminary version is already available and presently under test. The main control panel of the SC is shown Figure 12. The status of the SC is associated to a Finite State Machine (FSM) whose status depends in turn on the status of the FSMs associated to each the SBs.

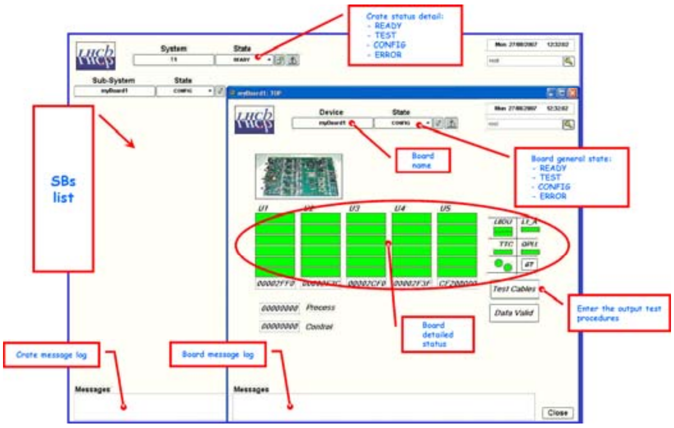

Figure 12: The main Selection Crate control panel together with a SB control panel, showing the status of the SB and the configuration parameters.

REFERENCES

[1] LHCb Trigger System
http://lhcb.web.cern.ch/lhcb/TDR/trigtdr.pdf

[2] LHCb Calorimeter System
http://lhcb.cern.ch/calorimeters/html/TDR/calo_tdr.pdf

[3] GOL
http://proj-gol.web.cern.ch/proj%2Dgol/

[4] Optical transmitter AGILENT HFBR-772BH
http://www.agilent.com

[5] Clock distributor
http://www.onsemi.com/pub/Collateral/NB100LVEP221-D.PDF

[6] VCSEL
http://www.ulm-photonics.de/

[7] Optical receiver AGILENT HFBR-782BH
http://www.agilent.com

[8] Credit Card PC
N. Neufeld, "Credit-card PC software guide", LPHE 2005-7, LHCb internal note 2004-058, July 2004
C. Gaspar et al., "The Use of Credit Card-sized PCs for interfacing electronics boards to the LHCb ECS," LHCb 2001-147

[9] GLUE CARD
F. Fontanelli et al., "Credit Card PC Implementation and Hardware Users' Guide", LHCb 2003-098

[10] TLK2501
http://focus.ti.com/docs/prod/folders/print/tlk2501.html

[11] DIM-PVSS
http://www.cern.ch/dim
http://www.cern.ch/itcobe/Services/Pvss/
http://lhcb-online.web.cern.ch/lhcb-online/ecs/PVSSIntro.htm