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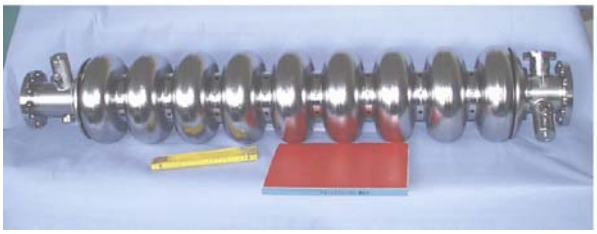

FPGA-based Neutron Radiation Tolerant Microcontroller

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Abstract

The paper presents a design of radiation-tolerant microcontroller using the COTS electronic devices. The microcontroller has been radiation-hardened by using the techniques of memory scrubbing and triple modular redundancy in the FPGA device. Using this design, a system for monitoring susceptibility of SRAM memory to neutron-induced single event upsets has been built. The results of tests of this system are also presented.

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1 ABSTRACT

The paper presents a design of radiation-tolerant microcontroller using the COTS electronic devices. The microcontroller has been radiation-hardened by using the techniques of memory scrubbing and triple modular redundancy in the FPGA device. Using this design, a system for monitoring susceptibility of SRAM memory to neutron-induced single event upsets has been built. The results of tests of this system are also presented.

Keywords: Single Event Effect, Single Event Upset, Field Programmable Logic Device, Static, Radiation Tolerance, Random Access Memory

2 MOTIVATION

Modern research in high-energy particle physics calls for new accelerator technologies. These sophisticated facilities require reliable electronic systems for its control and monitoring. New high energy linear accelerators, like X-Ray Free Electron Laser (X-FEL) and International Linear Collider (ILC), are planned to be built in single tunnels, housing both the main beam acceleration line and control electronics. Therefore, reliability of the electronic systems at elevated radiation levels becomes of exceptional concern. In in order to achieve long term reliable operation of the system used electronics must employ techniques allowing to tolerate local disturbances in the circuit. The detrimental neutron radiation is the dominating component of accelerator's radiation environment [1].

3 EFFECTS OF NEUTRON RADIATION ON ELECTRONIC CIRCUT OPERATION

Since neutrons have no electronic charge, they cannot interact with semiconductor material atoms electrically. However, they interact with semiconductor lattice atoms through collisions. This effect is significant due to high energy neutrons. Among results of the damage are resistivity changes and bipolar transistor gain degradation [2]. The displacement damage may have reversible nature. This self healing of a device is referred to as annealing. It relies on thermal motion of the defects. On the other hand, the migrating atoms may form stable associations with impurity atoms in the semiconductor structure. This will enhance the degradation, as such associations are defects in the lattice.

The second type of neutron effect on electronic systems is an indirect one. Neutrons can induce ionisation through secondary processes. The most important is the generation of alpha particles within semiconductor lattice due to the neutron capture reaction in Boron (^{10}B) atoms, present in silicon chips as dopant and used in passivation layers [3]. The product of the reaction can be either ^{7}Li ion or ^{4}He ion. The ^{4}He ion (an alpha particle) is probably the agent for triggering Single Event Effect (SEE) in silicon devices. SEEs can be subdivided into the firm and soft errors. Tolerance to firm errors, possibly resulting in permanent damage to the electronic device, can be obtained only by technological means. Soft errors are much less severe than the firm ones. There is no direct permanent damage done to silicon devices due to soft SEE. The only impairment caused, is on the functional and performance level of the subject system. Digital systems are exposed to two types of soft errors in the radiation environment. These are Single Event Upset (SEU) and Single Event Transient (SET).

Single Event Upset (SEU) concerns data storage elements. Memory cells such as Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM) and Master Slave edge triggered Flip Flops are subject to this detrimental phenomenon. The effect of SEU is distortion of data stored in the cell, simply called a bit flip. Apart from impairing the data stored by a system or system's state, the SEU can temporarily transform system's functionality. This is a severe problem of SRAM based Field Programmable Gate Array (FPGA) devices. Single Event Transient affects combinatorial circuits only. It manifests itself by transient changes of voltage levels on signal lines, either being input to combinatorial blocks, or the outputs from them. The SETs are mainly caused by ionising particles, particularly heavy ions. If an SET is latched in a storage element, it may be perceived as SEU [4], [5].

4 SINGLE EVENT UPSET MITIGATION TECHNIQUES

The techniques can be characterized in two categories [6]:

- technological, realisable in hardware only, usually through modified fabrication processes of integrated circuits
- software, which can yield a system or module, which is radiation tolerant, but not hardened

This means, that the circuits operate properly up to specified levels of radiation, possibly with some loss of performance. The software techniques can be realised in either hardware or software, depending on the platform [7].

4.1 Hardening by technology

The most effective, robust techniques allowing to harden electronic devices against radiation are those applied at the lowest, technology, level. They involve modified cells, being the building blocks of integrated circuits, altered structure of transistors and properly selected compounds for passivation of integrated circuits. The manufacturing technology can also decrease circuit's radiation sensitivity. Radiation resistance can be achieved in Silicon On Insulator (SOI) technology [6]. It enables complete elimination of latch up, due to lack of parasitic thyristor.

4.2 Modular redundancy

The technique of modular redundancy is most widely used in high reliability applications. There are various kinds of this scheme, depending on the number of single module replications. Thus, there is Double (DMR) and Triple (TMR) Modular Redundancy - the most common, there may also be Quintuple Modular Redundancy (QMR) or other of higher order (xMR) [6].

In DMR two entities function in parallel, performing the critical tasks in the same instants of time. The outcomes of the task, coming from the two entities are fed to a voter, or simply a comparator. Whenever the results are different an error is signalled. The redundant system has entered an erroneous state. It cannot recover from it, as there is sufficient information only to detect the error, no correction is possible. The two modules or systems produced different results, but it is unknown which one is correct. Therefore, the systems must be restarted, in order to initialise them with known and correct states.

TMR is more capable. In this scheme every critical entity is tripled. A voter, more sophisticated than the comparator in DMR scheme, is fed with outputs from every entity. The voter decides on the result, by performing majority voting. The limitation of TMR is that it can correct single errors only. The result is as indicated by at least two entities. If the representation of outputs from the entities is binary, the voter is always able to decide, it is never confused. Hence, the TMR scheme is not only capable of detecting an error, but also correcting it. TMR is able to sustain system's operation if an error is encountered.

4.3 Error detection and correction codes

The techniques, which can be applied to registers containing many related bits may involve using of Error Detection And Correction codes (EDAC) [8]. Frequently used are Hamming codes, relying on adding redundant bits to the stored word of information using encoder. The redundancy is used at the decoder to detect and correct errors. Hamming codes are capable of detecting and correcting bit errors within a word. Application of Hamming codes reduces the number of redundant flip-flops at the cost of the more complicated combinatorial EDAC circuit. This techniques can be used alone or with the connection with method called memory scrubbing [6].

4.4 Memory scrubbing

The general idea behind scrubbing is refreshing. It is executed periodically. The memory, its block or other data storage entity is sequentially read, word by word. The employed mitigation technique is used to assess whether data within read word is correct or not. In the latter case, the error correction follows, according to the mitigation technique. The corrected data is written back and the process continues, until whole storage space has been swept. The resource, which is being refreshed, cannot be accessed by the system. This requires the system to be halted if it claims the refreshed resource. Another solution could be executing scrubbing partially, for resources not being currently used. This, however, is not possible for a single-port memory storing program code. Therefore, the system will suffer some loss of performance if scrubbing is employed. It is important to state, that scrubbing itself is vulnerable to radiation, since an FSM handles it and should be mitigated.

5 RADIATION TOLERANT MICROCONTROLLER

5.1 Actel APA 600 family

The microcontroller has been implemented in a APA 600 FPGA. It is a Flash based-FPGA, which stores its configuration in Flash memory [9]. The configuration

is used directly from Flash during device's operation. Flash memory is immune to soft neutron induced effects, rendering the FPGA's configuration resistant to unpredictable change due to SEU. However, contents of Flash may be erased by gamma radiation, if exposed to it for extended time. The drawback of using Flash based FPGA is lower maximum frequency, as compared to SRAM-based devices.

5.2 Architecture of radiation tolerant microcontroller

The microcontroller is based on the PIC16C57. The basis for development was a description of processor core written in VHDL, published under GNU General Public License (GPL) on opencores.org. The basis core is significantly limited according to PIC16C57 specification. It is also impaired by several errors. Therefore, some corrections were necessary [10].

5.3 Methods used to mitigate SEU

The resources in the microcontroller, which are susceptible to SEUs, can be divided into the two categories [10]:

- components based on SRAM, both embedded in the FPGA and external
- Finite State Machines (FSM)

For protection of SRAMs, the scrubbing technique connected with use of the Hamming codes has been applied. This redundancy has to be embedded in the description of the design. No algorithm for automatic or semi-automatic code generation has been implemented for the purpose of this design.

The technique employed for protecting sequential components, such as FSMs or others, which rely on storing information in distributed memory elements, i.e. flip flops, is TMR. In the design, every D type flip flop is tripled. The three outputs are fed to the inputs of majority voting circuit. The majority voting circuit outputs the value indicated by at least two flip flops. The voting circuit is glitch free. The radiation tolerance or immunity of the majority voter is an important issue. The circuit is not protected against the influence of radiation. The SEU effect poses no threat on proper operation of the circuit, since the voter is purely combinatorial. The complete TMR D type flip flop is extended with error indication output. Whenever one of the sub flip flops is altered by SEU, the single error detection output is set. This may provide information on the level of vulnerability of distributed memory elements of FPGA to SEU. Once a register is mitigated with TMR, it should also be refreshed periodically, not to let errors accumulate. This, however, is done automatically. The clock is always supplied to the register's flip flops, it is never gated or disconnected. If the condition for writing a new value to the register is not met, the value from output is written back on every active clock edge. This provides sufficient rate of refreshing register's contents.

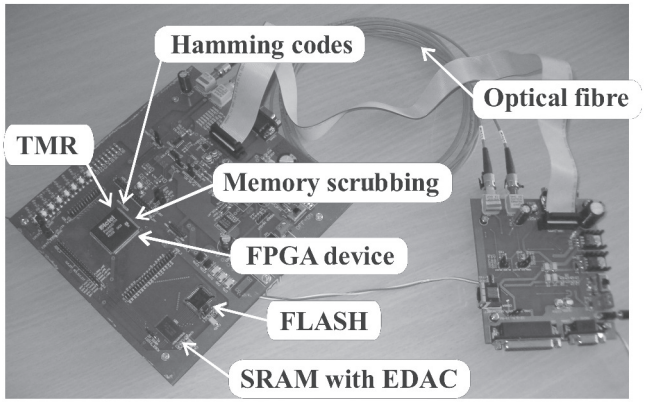

Figure 1: Radiation tolerant SRAM SEU detector

5.4 Application of TRM in Libero IDE

The starting point in applying the TMR scheme is description of a component in VHDL. The next step is to synthesize the component. The process of synthesis is handled by dedicated tools. It follows the process of compilation, which transforms every description into RTL description. The RTL description is then used as a prerequisite for the synthesis process. During synthesis the RTL is mapped to the resources available in a particular FPGA device . Therefore, the synthesis results in a netlist, which can be either an industry standard EDIF netlist or a structural VHDL description. The VHDL description is much more human readable and can be easily modified. Later, every flip-flop in a netlist has to be replaced by an instance of the component, having the same pins as a regular flip-flop, but containing three flip-flop and a voter circuit. Special software tools have been created for this purpose [10]. Then the circuit is synthesized again, followed by a standard place and route (Figure 2).

5.5 Exemplary application

Using the radiation-tolerant microcontroller the system measuring the susceptibility of various SRAM modules has been implemented (see Figure 1). The system consists of a microcontroller and UART implemented in FPGA, external FLASH and SRAM program and data memories and a SRAM memory under test [10]. The memory is periodically tested for SEU-induced errors. The results of the tests are periodically sent to a standard PC by a RS-485 or optical link.

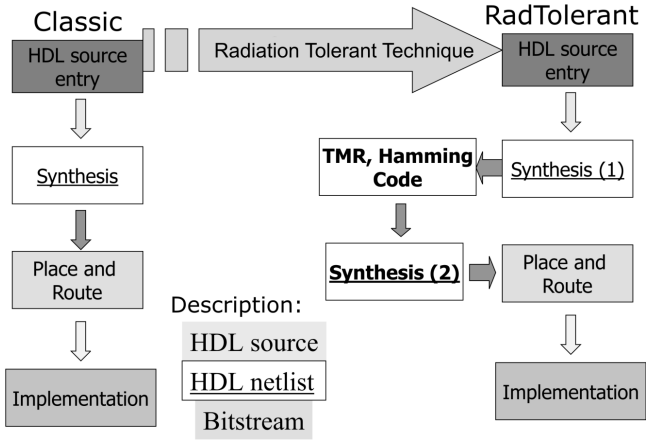

Figure 2: Classical and modified-radiation tolerant technique of designing FPGA-based digital circuits

6 RESULTS

The SRAM SEU detector was tested in DESY (Deutsches Elektronen Synchrotron). The test was run from the 30^{th} of August 2005 till the 2^{nd} of September 2005, a total of 72 hours. The purpose of the test was to verify the designed MCU's behaviour under the mixed gamma and neutron irradiation. The device was installed in the LINAC II linear lepton accelerator. The SEU detector was placed in about five meters distance from the electron-positron converter, which generates high number of neutrons. The monitoring station (PC computer running Linux operating system) together with transceiver was placed on the test bench, located in radiation free environment. The communication between PC and detector was carried over 50 meters long full duplex 62.5/125 micron multimode optical fibre. The bitrate was set to 9600 bps. No communication errors were observed. During the test period, 500 SEUs have been observed in the tested SRAM memory and five SEUs in the UART transmitter.

7 CONCLUSIONS

The hardware platform was based on COTS components only, none of the used electronic components were hardened against radiation. This renders the involved costs a fraction of a price of available radiation tolerant or hardened programmable devices. However, the designed system has been mitigated to SEUs only, which might prove to be insufficient during long term tests. On the other hand, VHDL or other HDL relies on a fixed hardware technology, which is the only level, on which the full suite of SEE mitigation and hardening mechanisms can be adopted. The mitigating capabilities of adopted techniques should be in future quantified in terms of specific radiation doses, which the mitigated circuit is able to withstand. The drawback of employed techniques is compromised performance of the system. Particularly the maximum attainable frequency is decreased when the TMR scheme or Hamming Codes are applied. The effect of Scrubbing is periodical pauses in system's operation, hence decreased computational capability. The effects caused by TMR and Hamming Codes could be potentially reduced if dedicated floorplanning of the FPGA resources was involved, but generally the speed penalty is unavoidable if these techniques are employed.

7.1 ACKNOWLEDGEMENTS

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