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The OTIS Reference Manual

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OTIS Version 1.3

Abstract

This document describes the port definitions, electrical specifications, modes of operation and programming sequences of the OTIS TDC. The chip is developed for the Outer Tracker of the LHCb experiment. OTIS1.0 is the first full-scale prototype of this 32 channel TDC and has been submitted in April 2002 in a standard 0.25µm CMOS process. Within the clock driven architecture of the chip a DLL provides the reference for the drift time measurement. The drift time data of every channel is stored in the pipeline memory until a trigger decision arrives. A control unit provides memory and trigger management and handles data transmission to the subsequent DAQ stage. The latest chip version is OTIS1.3.

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1 Document and Chip Version History

Document Version	Date	Author	Description
0.5	17.06.2002	U.S.	Document created
0.7	21.06.2002	U.S.	Typos, electrical specs
1.0	24.09.2002	U.S.	1st public version
1.1	06.02.2004	U.T.	Include `OTIS`1.1
1.2	09.08.2004	U.S.	Include `OTIS`1.2
1.3	13.03.2006	U.S.	Include `OTIS`1.3
Check `http://wwwasic.kip.uni-heidelberg.de/lhcbot/` for the latest version			

Chip Version	Submission Date	Changes relating to previous version
`OtisDLL`1.0	19.10.2000	DLL prototype
`OtisMEM`1.0	21.03.2001	DLL & Memory prototype (pipeline)
`BeetleSR`1.0[1]	18.05.2001	Memory prototype (derandomizing buffer)
`OTIS`1.0	15.05.2002	First full-scale prototype
`OTIS`1.1	10.11.2003	TDC fix & various other improvements
`OTIS`1.2	24.05.2004	Integration of `MultiHit` mode
`OTIS`1.3	08.05.2005	Fixed time bin 0 width (phase detector)

[1] We greatly appreciate that we were allowed to join this chip submission of the Beetle-Group.

2 Conventions within this Document

- This document deals with the chip version `OTIS1.3`.
- Registers are 8 bit wide.
- The numbering of registers and the indexing into single registers starts counting from zero. For example `TestReg[7:0] = 8'b00000001` represents a register called `TestReg` that is loaded with the hexadecimal value `0x01`. The rightmost bit within this register (i.e. bit number 0) is the least significant bit (LSB). In this example the LSB carries the value 1, all other bits including the most significant bit (MSB) are 0.
- Exeptions from the conventions above are noted.

3 Chip Architecture

The OTIS readout chip of the Outer Tracker of the LHCb experiment is developed at the University of Heidelberg. A first full-scale prototype of the chip has been produced in April 2002. The OTIS chip is a 32 channel TDC (Time to Digital Converter) manufactured in a standard 0.25µm CMOS process.

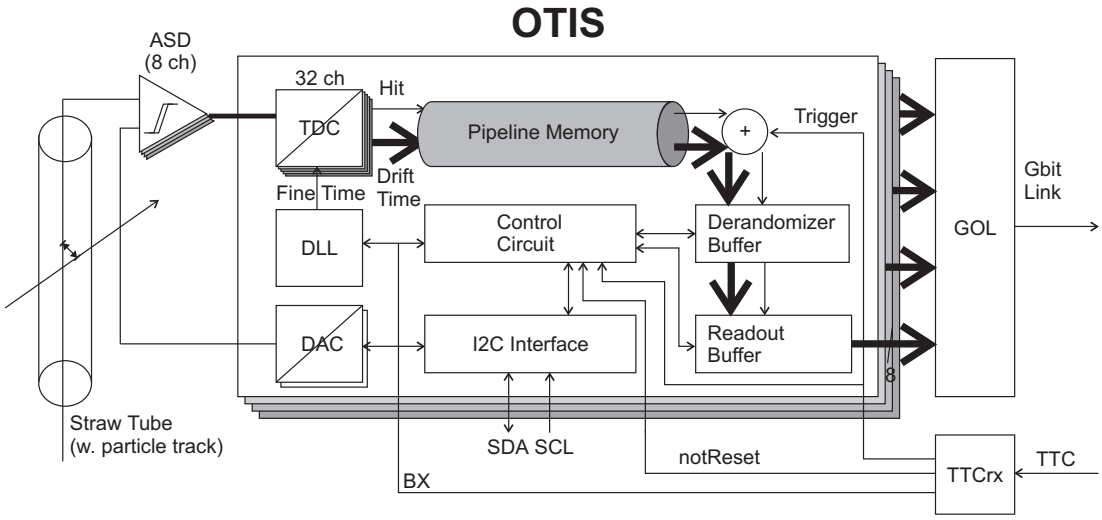

Figure 1: OTIS block diagram

In the LHCb experiment the output signals of the Outer Tracker straw tubes are digitized with discriminator chips of the ASD family [1]. The OTIS TDC measures the arrival time of the ASD signals with respect to the LHC clock. In the detector it is foreseen to combine the output data of always 4 OTIS chips (4 × 8bit) to form the input of the GOL [2] serialiser chip (1 × 32bit). The GOL chip then transmits data optically to the off detector electronics at 1.2 Gbit/s net data rate. Figure 1 depicts how the OTIS chip interfaces to the Outer Tracker front end electronics. The data processing within the OTIS TDC is clock driven: the chip operates synchronous to the 40MHz LHC clock. Main components of the OTIS chip are the TDC core, consisting of DLL, hit register and decoder and the pipeline plus derandomizing buffer. The last two are dual ported SRAM memories that cover the L0 trigger latency [3] and compensate trigger rate fluctuations. A control algorithm provides memory management and trigger handling. Additionally the chip integrates several Digital to Analog Converters (DACs) that provide the threshold voltages for the ASD discriminator chips. A standard I^2C interface [4] is used for setup and slow control.

The DLL (Delay Locked Loop) is a regulated chain of 32 delay elements consisting of two stages each. Since the output of every stage is used, the theoretical bin size is 390ps ($\frac{25ns}{2^6} \approx 0.39ns$). Furthermore, the 64 time bins require 6 bit drift time encoding per channel. The drift time data (32×6bit) plus hit mask (32bit), bunch crossing number (8bit) and status information (8bit) is stored in the 240 bit wide pipeline memory. The capacity of the memory is 164 words to allow a maximum latency of 160 clock cycles. If a trigger occurs, the corresponding data words are transferred to the derandomizing buffer which is able to store data from up to 16 consecutive trigger signals. The control unit's task is to process and read out the data of each triggered event within 900ns. The read out interface is 8 bit wide and it operates synchronous to the 40MHz LHC system clock.

The chip version `OTIS1.1` has been submitted for manufacturing in November 2003. It features a modified TDC core to overcome the problem of missing drift time codes of chip version `OTIS1.0`. Other changes visible to the user include rearranged read out header bits and a modified register map. Additionally the LVDS data output pads have been replaced by differential CMOS outputs. Further modifications provide buffers for the ASD threshold voltage outputs and a new implementation of the control algorithm as well as the possibility read out triggered event data via the I^2C interface.

The control algorithm of chip version `OTIS1.2` (submitted in May 2004) finally provides the `MultiHit` operation mode. Other changes with respect to its predecessor chip result in a smaller DNL figure and in a smaller offset voltage spread of the ASD threshold outputs. Compared to `OTIS1.1`, the chip size changed. This implicates changes in the pad positions, however the pad order did not change.

Though chip version `OTIS1.2` fulfills the specifications for LHCb front end electronics, the chip version `OTIS1.3` has been manufactured addressing further improvements in the TDC core (Phase detector was changed; As a result, the differential non-linearity has signficantly decreased - see Sect. 7.3 and 7.4).

4 Electrical Specifications

4.1 DC Characteristics

The OTIS chip needs two positive operating voltages: analog and digital supplies of nominal +2.5V with respect to Ground (`gnd`, 0V) each. The operational range of `vdda` and `vdd` is predetermined by the manufacturing process. Minimum, maximum and nominal supply voltage ratings are listed in table 1.

Name	Explanation	Min.	Typ.	Max.	Unit
`vdd, vdd_*`[2]	Positive digital supply	2.2	2.5	2.7	V
`vdda`	Positive analog supply	2.2	2.5	2.7	V
`gnd`	Detector ground	-0.2	0	0.2	V

Table 1: DC characteristics of the OTIS chip

All supply voltages should be thoroughly blocked against `gnd` (e.g. a 100nF ceramic capacitor in parallel with a 68μF tantalum capacitor between `vdd/vdda` and `gnd`). The blocking capacitors should be placed as close as possible to the chip.

After powering the chip, the OTIS chip performs a power up reset (c.f. chapter 6.1). In this state the power consumption is 225mA (or 563mW). Power consumption rises to 267mA (or 668mW) when operating the chip at the nominal LHC bunch crossing frequency of 40MHz and a trigger rate of 1MHz.

[2] any power supply net having a name starting with `vdd_`

I^2C (OTIS1.0)							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.5	3.3	2.5	V
output	—	—	0.0	—	—	2.5	V
I^2C (OTIS1.1 to OTIS1.3)							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.5	7.0	2.5	V
output	—	—	0.0	—	—	2.5	V
CMOS							
	logic 0			logic 1			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	-0.7	1.1	0.0	1.4	3.3	2.5	V
output	—	—	0.0	—	—	2.5	V
LVDS (100Ω termination)							
	offset voltage			differential voltage			Unit
	Min.	Max.	Typ.	Min.	Max.	Typ.	
input	0.0	2.5	1.2	0.1	2.5	0.2	V
output	—	—	1.02	—	—	1.38	V

Table 2: Specification of signal levels

4.2 AC Characteristics

The OTIS chip has 3 different types of I/O pads. The signal levels for these pads are given in table 2.

Note that from chip version 1.1 on the OTIS chips feature 5V tolerant I^2C-pads. This eases interfacing the OTIS chips to commercial I^2C devices that usually operate at +3.3V or +5V. To interconnect those devices to chip version OTIS1.0, a bidirectional level shifter is required. A simple solution is the use of a discrete MOS-FET for each bus line [6]. Figure 2 illustrates the level shifter circuit. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

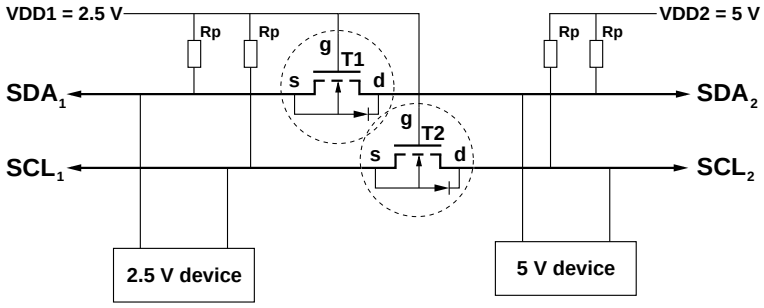

Figure 2: Bidirectional level shifter circuit (BSN20 from Philips Semiconductors)

The chips OTIS1.1 to OTIS1.3 all feature a 5V compliant I^2C interface. Thus the level shifter circuit depicted in figure 2 can be omitted. The chips directly interface with commercial I^2C controllers.

5 Slow Control

5.1 I²C Interface

The slow control interface of the OTIS chips is a standard mode I²C slave device capable to transfer data at a transfer rate of 100kbit/s. The chip address, necessary to access a single device on the I²C bus, is assigned by means of the address pads `ID<12>` (LSB) to `ID<18>` (MSB) for chip versions 1.1 to 1.3. For the chip version `OTIS`1.0 the pads are named `ID<0>` (LSB) to `ID<6>` (MSB). The ID pads (see tables 8 to 11) contain internal pull down resistors. Note that the OTIS I²C interface does not respond to reserved I²C addresses. Reserved addresses are `7'b0000XXX` and `7'b1111XXX`. In other words, the valid addresses range from 8 to 119.

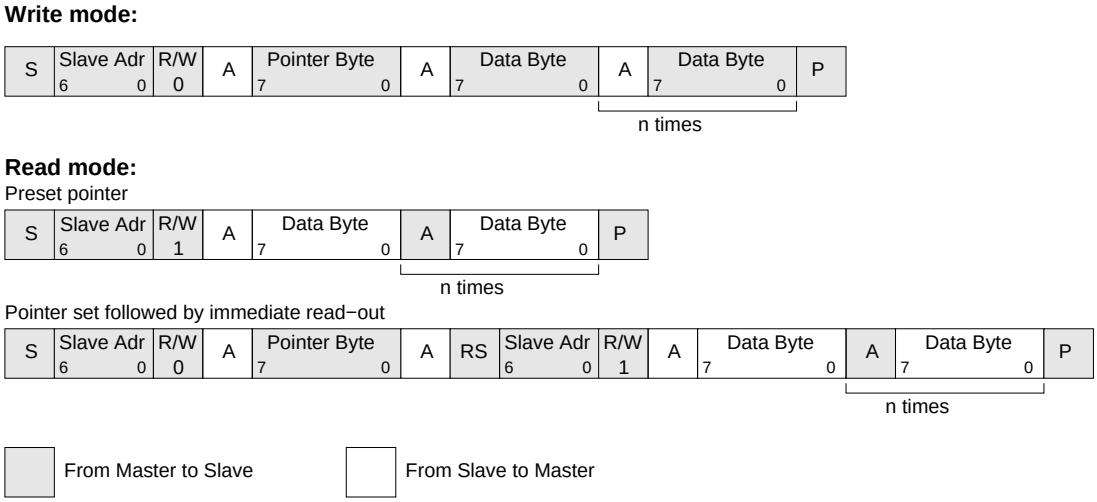

Figure 3: I²C-bus write and read sequences for accessing registers on the OTIS chip

The internal registers can be accessed via the pointer register. This register contains the address of the following register to be written to or read from. The pointer is internally incremented by 1 after each transferred data frame. Thus registers with adjacent addresses are accessed consecutively. The content of the pointer register itself remains unchanged, i.e. a new transfer will start at the previously set pointer position. Figure 3 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit first. In write mode the chip address is transmitted after initializing the transfer, followed by the pointer byte and the data byte(s). After the transmission of one data frame, the write pointer addresses the next register due to its internal auto-incrementing functionality. The transfer of the pointer register is mandatory in write mode. For the read mode two possibilities exist:

- Preset pointer: The data output immediately starts after the initialization and the transmission of the chip address. The pointer has been set in a previous I²C-data transfer.
- New pointer: After initialization and transfer of the chip address, a new pointer byte gets programmed. Then, after re-initialization and re-transmission of the chip address, the data output starts.

5.2 Configuration Registers

The register map of the TDC chip changed between chip version `OTIS`1.0 and `OTIS`1.1 following the growing functional range. Note that not only the number of registers changed but also the bit assignment of single setup or status registers.

5.2.1 Configuration Registers of OTIS1.0

OTIS1.0 provides a set of 20 status and configuration registers. Table 3 gives name, address, type and bit assignment of each register. The OTIS register set is composed of 5 read only registers and 15 writable registers. Though of type read-only, the registers `StatusReg`, `ReceivedT` and `RejectedT` allow to be re-initialized to zero by accepting and interpreting any write access as reset signal. The accompanying data byte is ignored.

Address	Name	Type	Bit Assignment/Description	
0	PosID	read only	7 - 5	0
			4 - 0	Position ID
1	I2CID	read only	7	0
			6 - 0	I2CID[6:0]
2	StatusReg	read only	7 - 4	0
			3	0
			2	Buffer overflow
			1	0
			0	Memory selftest failed
3	ReceivedT	read only	7 - 0	Number of received trigger
4	RejectedT	read only	7 - 0	Number of rejected trigger
5	ReadMode	read/write	7 - 4	X
			3	0
			2	SuppressZero / notSingleHit[3]
			1 - 0	Number of Events per trigger
6	DebugMode	read/write	7 - 6	X
			5 - 3	Signal select (see table 4)
			2	Pads on/off
			1	Playback/SFT
			0	Debug mode on/off
7	Latency	read/write	7 - 0	Latency register
8 - 11	ChannelMask	read/write	7 - 0	Channel mask register
12, 13	DLLDAC	read/write	7 - 0	DLL DAC register
14 - 17	ASDDAC	read/write	7 - 0	ASD DAC register
18, 19	PBData	read/write	7 - 0	Playback data

Table 3: OTIS1.0 status and configuration registers

The OTIS1.0 registers are:

- `POSID, I2CID:` 12 bit TDC identification number. The registers `POSID` and `I2CID` are read only. Their content is determined through the TDC ID pads 1, 138 - 141, and 2 - 8 respectively (see figure 22 and table 8). The `I2CID` register holds redundant data as the I^2C ID must be known to the user prior to any I^2C read access.

- `StatusReg:` The `StatusReg` register provides information about failed memory self tests (`StatusReg[0] = 1`) or buffer overflow (`StatusReg[2] = 1`) in case of a full derandomizing buffer. The detection of an SEU or a lost DLL lock is not implemented in OTIS1.0. The status information can be reset through I^2C write access to the `StatusReg` register.

- `ReceivedT, RejectedT:` Number of received and rejected L0-trigger signals since last L0-reset. The registers hold 8 least significant bits of the received/rejected trigger counters. The counter registers can be reset through I^2C write access.

[3] OTIS1.0 only provides the single hit mode (`ReadMode[2] = 0`).

DebugMode[5:3]	Run time information	WPWrap	RPWrap
3'b000	Zero crossing of memory write and read pointer	Write pointer	Read pointer
3'b001	Zero crossing of derandomizing buffer pointer	Write pointer	Read pointer
3'b010	Memory self test	Self test busy	Self test failure
3'b011	Read out sequence	Start of sequence	End of sequence
3'b100	Derandomizing buffer fill level	Buffer empty	Buffer full

Table 4: Status information (OTIS1.0)

- ReadMode: As OTIS1.0 only features the SingleHit operation mode, bits number 3 to 7 of the ReadMode register are ignored. Bit number 2 selects the operation mode (setting this bit to 0 is the only reasonable choice). ReadMode[1:0] represents the number of data sets that will be searched for hits upon incoming trigger signals. Note that the search depth figure starts counting from zero. Changes in the ReadMode register only take effect after a L0 reset signal.

- DebugMode: Several internal status signals can be monitored at the two service pads WPWrap and RPWrap. The signals to observe can be selected with bits number 3 - 5 of the DebugMode register. Valid bit combinations are listed in table 4. DebugMode[2]=1 switches off signal monitoring, i.e. monitoring is enabled by default. The bits DebugMode[1:0] are used to select and activate one out of two special operation modes: DebugMode[1:0]=2'b11 selects memory self test mode, DebugMode[1:0]=2'b01 selects play back mode and 2'bX0 switches off the debug mode operation.

- Latency: The content of the Latency register defines the latency, i.e. the distance between memory write and read pointer. Latency[7:0]=0x00 sets the minimum distance 1 where the read pointer immediately follows the write pointer. The maximum distance is 0xA2. Changes in the Latency register only take effect after a L0 reset.

- ChannelMask: The 32 bits of the 4 ChannelMask registers individually switch on or off single channels of the OTIS chip. To switch off a channel, the corresponding bit must be set to 1, i.e. all channels are switched on by default.

- DLLDAC, ASDDAC: Interface to the unbuffered 8bit DLL and ASD voltage DACs.

- PBData: Interface to the two shift registers that are used as storage for the play back data sets.

5.2.2 Configuration Registers of OTIS1.1, OTIS1.2 and OTIS1.3

The chips OTIS1.1, OTIS1.2 and OTIS1.3 provide a set of 66 status and configuration registers. Table 5 summarizes name, address, type and bit content of each register. The OTIS register set is composed of 5 read only and 61 writable registers. Though of type read-only, the registers StatusReg, ReceivedT and RejectedT allow to be re-initialized to zero by accepting and interpreting any write access as reset signal. The accompanying data byte is ignored.

Address	Name	Type	Bit Assignment/Description	
0	PosID0	read only	7 - 4	0
			3 - 0	TDCID[11:8]
1	PosID1	read only	7 - 0	TDCID[7:0]
2	I2CID	read only	7	0
			6 - 0	I2CID[6:0]
3	Revision	read only	7 - 6	0
			5 - 3	Chip Version (3'b001)
			2 - 0	Chip Revision (3'b001, 3'b010 or 3'b011)
4	StatusReg	read only	7 - 4	0
			3	SEU
			2	Buffer overflow
			1	DLL lock lost
			0	Memory selftest failed
5	ReceivedT	read/write	7 - 0	Number of received triggers
6	RejectedT	read/write	7 - 0	Number of rejected triggers
7	EventID	read only	7 - 0	EventID
8	SEUCntr	read/write	7 - 0	Number of detected SEUs
9	ReadMode	read/write	7	0
			6	Previous drift time
			5	DataValid (1=on, 0=off)
			4	Comma (1=on, 0=off)
			3	Truncation[4]
			2	MultiHit[4] / SingleHit
			1 - 0	Number of Events per trigger
10	DebugMode	read/write	7 - 5	Service pad signal select (see table 6)
			4	Service pads (1=on, 0=off)
			3 - 1	Debug modes:
				3'b001 ReadFIFO on
				3'b010 SFT autoBankSelect
				3'b011 SFT PadBankSelect
				3'b100 PB autoBankSelect w/o FIFO
				3'b101 PB autoBankSelect w FIFO
				3'b110 PB PadBankSelect w/o FIFO
				3'b111 PB PadBankSelect w FIFO
			0	Debug mode (1=on; 0=off, ignore bits 3-1)
11	DLLReg	read/write	7 - 1	0
			0	DLL reset (1=active, 0=off)
12	Latency	read/write	7 - 0	Latency register
13	Offset	read/write	7 - 4	BX counter wrap-around
			3 - 0	BX counter offset
14	Reserved0	read/write	7 - 0	Ignored
15 - 18	ChannelMask	read/write	7 - 0	Channel mask register
15	Reserved1	read/write	7 - 0	Ignored
20 - 23	DLLDAC	read/write	7 - 0	DLL DAC register
24 - 27	ASDDAC	read/write	7 - 0	ASD DAC register
28, 29	PBData	read/write	7 - 0	Playback data
30 - 65	ReadFIFO	read/write	7 - 0	Slow event data readout

Table 5: OTIS1.1/1.2/1.3 status and configuration registers

[4]not implemented on OTIS1.1

The registers are:

- `POSID0, POSID1:` 12 bit of TDC identification number. `POSID0` and `POSID1` are read only. The register content is determined through the TDC ID pads 5 - 15 and 22 (see tables 9, 10 and 11).

- `I2CID:` 7 bit of I^2C ID number. The register `I2CID` is read only, its content is determined through the TDC ID pads 23 - 29 (see tables 9, 10 and 11). The `I2CID` register holds redundant data as the I^2C ID must be known to the user prior to any I^2C read access.

- `Revision:` Read only register representing chip version and revision number:
  `OTIS1.1: Revision[7:0] = 8'b00001001`
  `OTIS1.2: Revision[7:0] = 8'b00001010`
  `OTIS1.3: Revision[7:0] = 8'b00001011`

- `StatusReg:` The `StatusReg` register provides information about failed memory self test (`StatusReg[0] = 1`), lost DLL lock (`StatusReg[1] = 1`), buffer overflow in case of a full derandomizing buffer (`StatusReg[2] = 1`) and detection of a SEU within the slow control (`StatusReg[3] = 1`). The status information can be reset through I^2C write access to the `StatusReg` register.

- `ReceivedT, RejectedT, EventID:` The OTIS chip counts the number of accepted and rejected L0 trigger signals as well as the number of completed data output sequences. 8 least significant bit of each counter are available through the `ReceivedT`, `RejectedT` and `EventID` registers. The first two counter registers can be reset through I^2C write access. The `EventID` register only gets reset via the L0 EventID reset signal. If there is no pending read out sequence (i.e. the derandomizing buffer is empty) and none of the counter register has been individually reset, then `ReceivedT = EventID + RejectedT` holds true (except for possible counter overflows).

- `SEUCntr:` Interface to a 8 bit counter storing the number of detected SEUs. Resettable through I^2C write access.

- `ReadMode:` Sets the operation mode of the OTIS chip. As `OTIS1.1` still lacks the `MultiHit` mode, the only reasonable choice for bit number 2 is `ReadMode[2]=0`. For chip versions `OTIS1.2` and `OTIS1.3` `ReadMode[2]=1` selects the `MultiHit` operation mode. If operating in `MultiHit` mode, `ReadMode[3]` selects the optional truncation of the data output stream to 900ns. `ReadMode[4]` selects whether or not to precede every non-consecutive data output sequence with a comma byte (`0xFF`). If bit number 5 is set, then every data output sequence gets announced through the `DataValid` pad. `ReadMode[1:0]` represents the number of data sets that will be searched for hits upon incoming trigger signals. Note that the search depth figure starts counting from zero. Changes in the `ReadMode` register only take effect after a L0 reset signal.

- `DebugMode:` Several internal status signals can be monitored at the two service pads `WPWrap` and `RPWrap`. The signals to observe can be selected with bits number 5 - 7 of the `DebugMode` register. Valid bit combinations are listed in table 6. `DebugMode[4]=1` switches off signal monitoring, i.e. monitoring is enabled by default. The bits `DebugMode[3:1]` are used to select several special operation modes. These are memory self test and play back mode (as for `OTIS1.0`). The chip versions 1.1 to 1.3 additionally offer the possibility to steer data set selection from outside the chip through the `BankSelect` pad. A third debug feature is the possibility to store a complete data output sequence in a set of FIFO registers. These registers are accessible via I^2C interface. Please refer to tables 5 and 6 on how to select and activate the different debug features.

- `DLLReg:` Setting `DLLReg[0]=1` executes a DLL reset.

DebugMode[7:5]	Run time information	WPWrap	RPWrap
3'b000	Zero crossing of memory write and read pointer	Write pointer	Read pointer
3'b001	Zero crossing of derandomizing buffer pointer	Write pointer	Read pointer
3'b010	Memory self test	Self test busy	Self test failure
3'b011	Playback info	PB mode enabled	BankSelect
3'b100	Read out sequence	Start of sequence	End of sequence
3'b101	Derandomizing buffer fill level	Buffer empty	Buffer full
3'b110	ReadFIFO information	FIFO enabled	FIFO has data
3'b111	DLL lock info	VCtrl $\leq$ DLLDAC3	VCtrl $\geq$ DLLDAC0

Table 6: Status information (OTIS1.1/1.2/1.3)

- `Latency:` The content of the `Latency` register defines the latency, i.e. the distance between memory write and read pointer. `Latency[7:0]=0x00` sets the minimum distance 1 where the read pointer immediately follows the write pointer. The maximum distance is `0xA2`. Changes in the `Latency` register only take effect after a L0 reset.

- `Offset:` The content of the `Offset` register provides the possibility to fine tune the behavior of the bunch crossing counter. Bits 4 - 7 allow the adjustment of the overflow mark (3556 - 3571) of the 12 bit wide bunch crossing counter: `Offset[7:4]=4'b0111` selects the nominal value 3563. The bits number 0 - 3 allow the adjustment of the first BX number after a BX reset: The bunch crossing counter always starts counting from zero after a L0 Reset. A BX reset (occuring latency clock cycles after the L0 reset) sets the bunch crossing counter to `Latency + Offset[3:0]`. Changes in the `Offset` register only take effect after a L0 reset.

- `ChannelMask:` The 32 bits of the 4 `ChannelMask` registers individually switch on or off single channels of the OTIS chip. To switch off a channel, the corresponding bit must be set to 1, i.e. all channels are switched on by default.

- `DLLDAC, ASDDAC:` Interface to the 8bit DLL and ASD voltage DACs.

- `PBData:` Interface to the two shift registers that are used as storage for the play back data sets.

- `ReadFIFO:` Interface to the FIFO registers that are able to store one complete data output sequence.

6 Modes of Operation

6.1 Reset

OTIS1.0: If the `PwrUpReset` pad (number 37 in table 8) is coupled capacitively (10nF - 100nF) to `gnd`, the chip performs a power up reset after power-on. Within this power up reset all status and configuration registers are set to 0 and the I^2C interface is set into the idle state, thus the chip is ready for programming. The duration of the power up reset varies with the capacity connected to the `PwrUpReset` pad.

The pads number 35 and 36 are used to execute the fast L0 reset. This is needed to synchronize the OTIS chip to the LHC bunch crossing clock or to reset the DLL if lock was lost. OTIS1.0 initiates the fast reset if the LVDS pads receive input signals representing zero. There is no timing requirement between clock and reset which must be met as long as it is guaranteed that the clock

is running while the chip receives the reset signal.

OTIS1.1 to OTIS1.3: The functionality of the PwrUpReset pad (number 130 in tables 9, 10 and 11) was slightly modified: After the expiry of the RC-delay described above, an additional delay of 32 clock cycles was introduced to assure the locking of the DLL, which is only guaranteed if the clock is running when PwrUpReset or DLLReset are released. The latter (pad number 165 in tables 9 and 10 or pad number 169 in table 11) introduces a DLL reset independent from the I^2C interface, e.g. for laboratory use. The LOReset (pad numbers 135 & 136 in tables 9 and 10 or pad numbers 139 & 140 in table 11) terminates any ongoing readout, resets the fast control to the idle state, resets all memory and derandomizer buffer pointers to zero and discards all pending triggers. However, it does not reset any on-chip counters. Thus the EVReset and BXReset signals (pad numbers 166 to 169 in tables 9 and 10 or pad numbers 170 to 173 in table 11) were introduced to perform the Event- and BX-counter reset.

6.2 Normal Operation Mode

OTIS1.0: To select normal (or SingleHit) operation mode, the content of the ReadMode register must be set to 8'bXXXXX0xx. The upper 5 bits have no functionality and the lower 2 bits determine the search depth (in BX) per trigger.

Output Data Format (SingleHit Mode)

Bit:	0..31	32..39	40..47	...	280..287
Data:	Header	Drift Time 0	Drift Time 1	...	Drift Time 31

Drift Time Encoding

Hit Position	Drift Time Encoding
1. BX	00XXXXXX
2. BX	01XXXXXX
3. BX	10XXXXXX
No Hit	11XXXXXX

Figure 4: SingleHit mode data format & drift time encoding

OTIS1.1: This chip version still lacks the MultiHit read mode. This is why the lower 4 bits of the ReadMode register show the same functionality as for chip version OTIS1.0. With bits number 4 and 5 the Comma and the DataValid option can be switched on and off. If the comma bit is set to 1, every non-consecutive data output sequence is preceded with a comma byte (0xFF). The DataValid bit determines whether or not every ongoing data output sequence gets announced through the DataValid pad. Bit number 6 of the ReadMode register determines the drift time figures for non-hit channels during data output. If set to 0, channels without hit show blank drift times: 8'b11000000. If set to 1, non-hit channels still carry the No-Hit information, but possibly show remaining drift times from previous hits: 8'b11xxxxxx. This feature is intended to possibly provide a more detailed insight into on-chip data flows.

Output Data Format (MultiHit Mode, 1BX/Trigger)

Bit:	0..31	32..63	64..71	...	64+(8n)..71+(8n)
Data:	Header	1 Hitmask	Drift Time 0	...	Drift Time n

Output Data Format (MultiHit Mode, 2BX/Trigger)

Bit:	0..31	32..95	96..103	...	96+(8n)..103+(8n)
Data:	Header	2 Hitmasks	Drift Time 0	...	Drift Time n

Output Data Format (MultiHit Mode, 3BX/Trigger)

Bit:	0..31	32..127	128..135	...	128+(8n)..135+(8n)
Data:	Header	3 Hitmasks	Drift Time 0	...	Drift Time n

Figure 5: MultiHit mode data format

OTIS1.2 & OTIS1.3: For chip versions OTIS1.2 and OTIS1.3 the bit ReadMode[2] now allows the selection between SingleHit and MultiHit operation mode. ReadMode[2] must be set to 1 to select the MultiHit mode. In this mode, ReadMode[3] = 1 turns the optional data stream truncation on. This sets the length of any data output sequence to 900ns independent from search depth or detector occupancy. Figures 4 and 5 show the output data format for the two operation modes. Note that in the MultiHit mode the 6bit drift time data is byte-aligned too: the two most significat bits are set zero. The figures 6 (OTIS1.0) and 7 (OTIS1.1 to OTIS1.3) show how the status information is organized in the header which precedes every data output sequence.

Since OTIS1.1, a newly introduced header bit indicates the optional data stream truncation for MultiHit mode. The status bits SFT, DLL lock lost and SEU are combined (disjunction) to a single error bit. The DLLLockLost bit is set if the DLL's control voltage exceeds the voltage range given by the DLLDAC registers (register 20 sets the upper voltage limit, register 23 sets the lower limit). The two other DLLDAC registers are used to set the bias of the corresponding discriminators which controls their speed and sensitivity. Register 21 sets the bias for the upper limit discriminator, register 22 sets the bias for the lower limit discriminator. Furthermore, 4 bits indicating the data frame's position in the readout stream (EventID) are added to the header data. Also the buffer overflow bit was changed to a sticky behavior, such that it can only only cleared with a LOReset signal.

6.3 Debugging Features

The OTIS chips provide several debugging features. First of all test data can be written to the pipeline via the I^2C-interface. Additionally one can start a memory self test or one can select status information such as full or empty derandomizing buffer to be observable at the two service pads. To switch on debug mode, the bit number 0 of the DebugMode register must be set to 1.

- Playback mode
  Test (or play back) data can be written to the registers number 18 and 19 (resp. 28 and 29). If data is written to these registers via the I^2C interface, the pointer does not proceed to the next register address. In combination with the fact that the two PBData registers are

Header Data Format (OTIS1.0)

Byte	1 (MSB … LSB)	2 (MSB … LSB)		3 (MSB … LSB)		4 (MSB … LSB)
Bit No.	0..11	12,13	14..17	18..21	22,23	24..31
Data	TDC ID	0	Status	RO	0	BX

Selftest failed	Buffer overflow	DLL lock lost	Single Event Upset	Number of BX	Read Mode	Playback Busy

Figure 6: Header data format of OTIS1.0

Header Data Format (OTIS1.2)

Byte	1 (MSB … LSB)	2 (MSB … LSB)		3 (MSB … LSB)		4 (MSB … LSB)
Bit No.	0..11	12	13..17	18,19	20..23	24..31
Data	TDC ID	1	RO	Err	Event-ID	BX

Read Mode	Number of BX	Truncation	Playback	Error (SFT, DLL SEU)	Buffer Overflow

Figure 7: Header Data Format of OTIS1.1/1.2/1.3

organized as shift registers, it is possible to store two independent sets of drift time and hit information which are then alternately written to the pipeline.

- Memory self test
  If started, the memory self test performs integrity checks for memory in- and output. Run time information about the memory self test can be obtained from the two debug pads `WPWrap` and `RPWrap` (see tables 4 and 6). To exit from the memory self test, the user must clear bit number 0 of the `DebugMode` register.

To make status information visible at the pads `WPWrap` and `RPWrap`, the bit number 2 of the `DebugMode` register has to be set to 0. The different combinations of status signals can be set with bits number 3 to 5 of the `DebugMode` register. The possible combinations are listed in table 4.

`OTIS1.1` to `OTIS1.3` include basically the same debug features as `OTIS1.0`, which can be selected in the same way, except for changed register addresses and bit positions (c.f. tables 5 and 6). Additionally both chips offer the possibility to store one complete data output sequence in a set of registers organized as FIFO.

7 Sample Measurements

7.1 `OTIS1.0` Sample Measurements

The first full-scale chip of the OTIS project `OTIS1.0` does not show the expected TDC output codes: an input signal scan reveals missing codes in the second half of the basic measurement range. An example measurement is shown in figure 8. This diagram prints the TDC codes from a single channel depending on the phase alignment between input signal and reference clock. In the first half of the measurement range, the measured drift times reflect the rising input signal delays, but in the second half, though detecting input signals (indicated by output codes less then `0xC0`), the TDC chip produces wrong drift times.

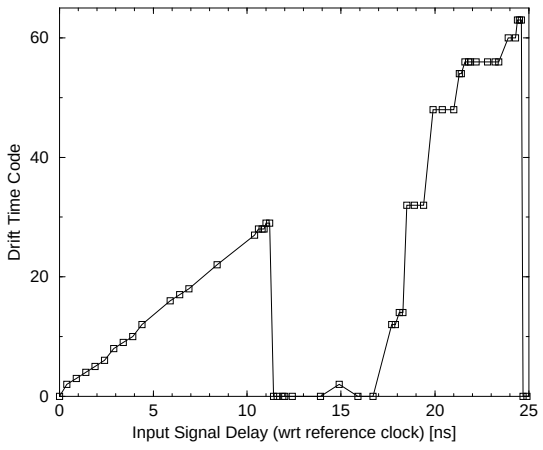

Figure 8: `OTIS1.0`: Drift time scan shows missing codes in the upper half of the basic measurement range.

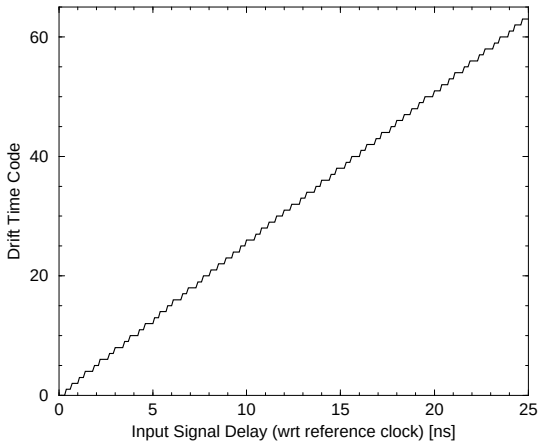

Figure 9: Drift time scan of the patched `OTIS1.0` chip. The TDC shows the expected drift time codes for the whole basic measurement range.

Weak driver strengths and underestimated parasitic capacitances have been identified as the sources of failure. The proposed corrections in the chip internal timing scheme successfully correct the problem of missing drift time codes as shown in figure 9. The patched TDC produces the expected linear dependency between input signal alignment and output codes for the whole measurement range. For this recording, the input signals for the drift time measurement originated from the pattern generator and scanned the TDCs working range in steps of 100ps.

7.2 OTIS1.1 Sample Measurements

Digital to Analog Converter:
Figure 10 shows the behavior of the 4 digital to analog converters which provide the threshold voltages for the ASD discriminator chips. The outputs of the DACs are now buffered and therefore able to drive currents up to 600μA. Figure 10 shows how the output voltages at an external load (1.2kOhm) vary with programming of the DAC registers. Extra design effort went into chip version OTIS1.2 in order to decrease the spread in between all 4 channels (which is ≈80mV for OTIS1.1).

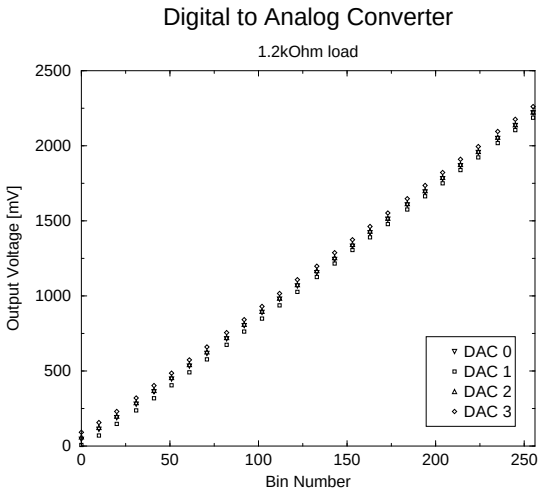

Figure 10: DAC Measurement

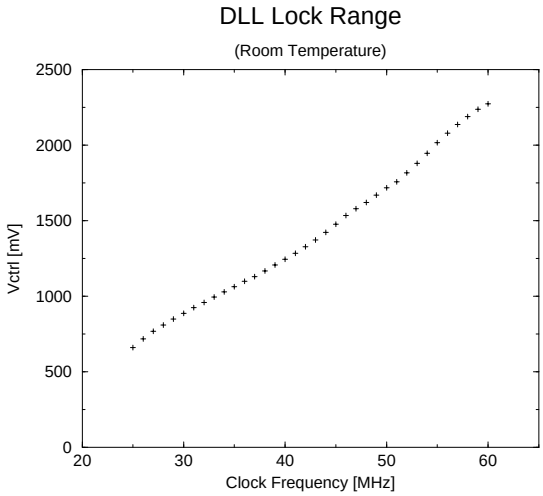

Figure 11: DLL Lock Range

DLL Lock Range:
Figure 11 combines data from 2 different measurements concerning the lock range of the DLL. The diagram shows the control voltage of the single delay elements against the LHC clock frequency. Data from 25MHz to 46MHz has been obtained with standard chip settings. The chip operated at a different supply voltage (V_{dda} = 3.3V instead of 2.5V) from 47MHz to 60Mhz. The resulting offset in V_{ctrl} has been taken into account for this summary. At room temperature and provided that reset is active before the clock is running, the DLL reaches its lock state for clock frequencies that range from 25MHz to 60MHz.

Drift Time Measurement:
Figure 12 shows the linear dependency between input signal delay (x-axis) and drift times (y-axis) derived from the input signal. The drift time data that contribe to this figure ranges from 0 to 63. Thus data only represents an overall drift time range of 25ns. In this diagram 0ns drift times belong to an input signal delay of 6ns and range to 24.9ns (resp. 30.9ns input signal delay). The drift time figures repeat below an input signal delay of 6ns and above a delay of 30.9ns .

Differential Non-Linearity:
To calculate a figure for the differential non-linearity, several million drift times derived from random input signals need to be stored and analyzed. The DLL bin sizes can be calculated from the histogram of all drift times. Now the difference in bin size of always two subsequent DLL bins can be calculated. But one needs to take into account that always two bins of different size form one delay element of the DLL. A sample diagram displaying bin size differences against the bin number is shown in figure 13. Now the sum of the biggest and (the absolute value of the) smallest bin size difference is called differential non-linearity. The data of diagram 13 results in a DNL of (1.25 ± 0.04)LSB or (489 ± 16)ps. The dominating contribution to the DNL originates from an

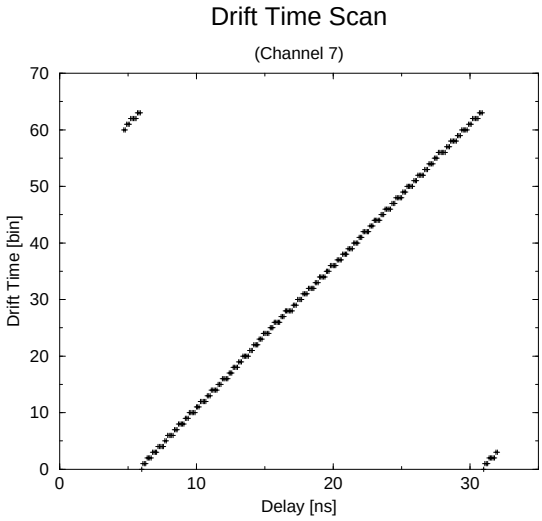

Figure 12: Drift Time Scan

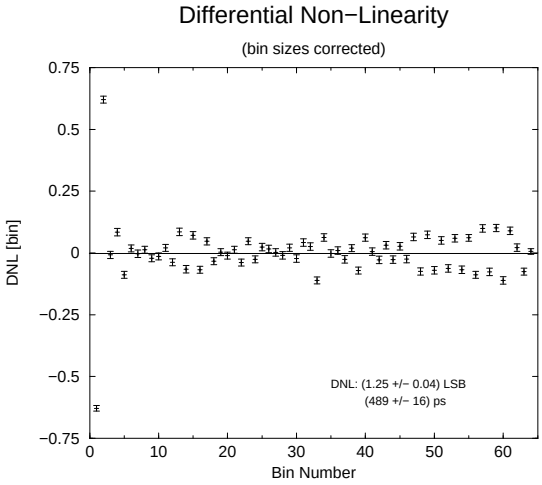

Figure 13: DNL

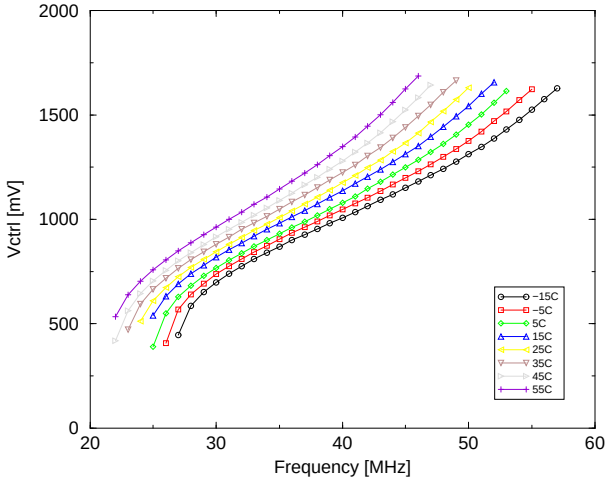

Figure 14: DLL control voltage as a function of the locking frequency for different temperatures. The DLL reliably locks from 28 to 45MHz for a temperature range from -15 to 55 centigrade.

unregulated dummy delay element at the beginning of the delay chain. As this dummy element is adjustable for the latest chip version too, the DNL figure is expected to be less than 1LSB for `OTIS`1.2.

7.3 `OTIS`1.2 Sample Measurements

DLL Lock Range:
Figure 14 presents the developing of the control voltage `V_Ctrl` of the DLL with the lock frequency for different temperatures. The stated temperatures refer to the ambient temperatures that are controlled by an oven which surrounds the test PCB. To represent the actual temperatures at the surface of the chip, 15 to 20 centigrade must be added to the surrounding temperature. The dynamic range of `V_Ctrl` of approximately 1V ranging from 600 to 1600mV combined with temperatures ranging from -15 to 55 centigrade results in a frequency range from approximately

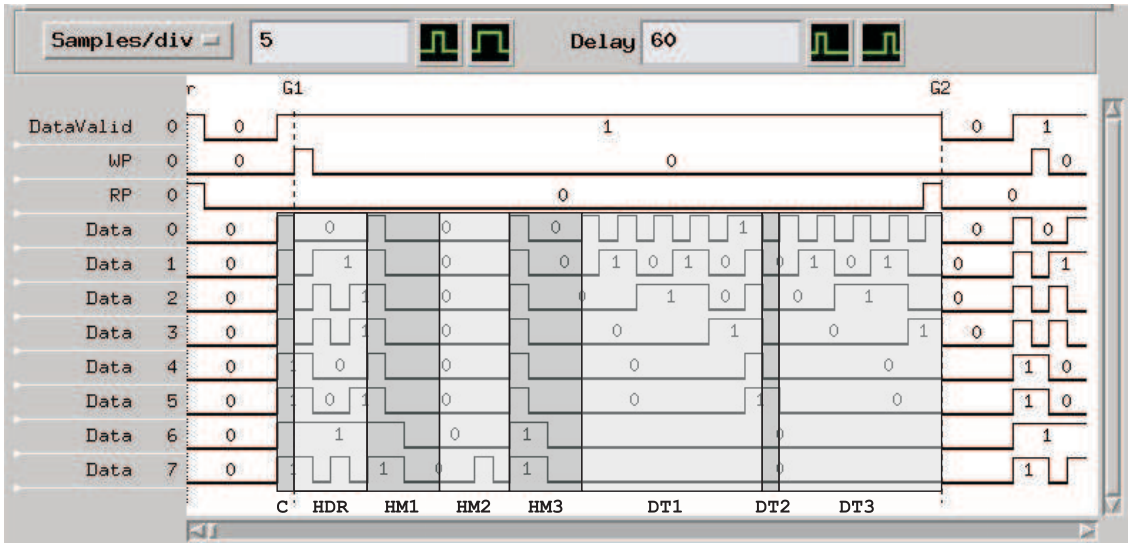

Figure 15: Recording of a data output sequence while operating in the multi hit mode. The different header, hitmask and drift time sections are alternately greyed for the ease of orientation.

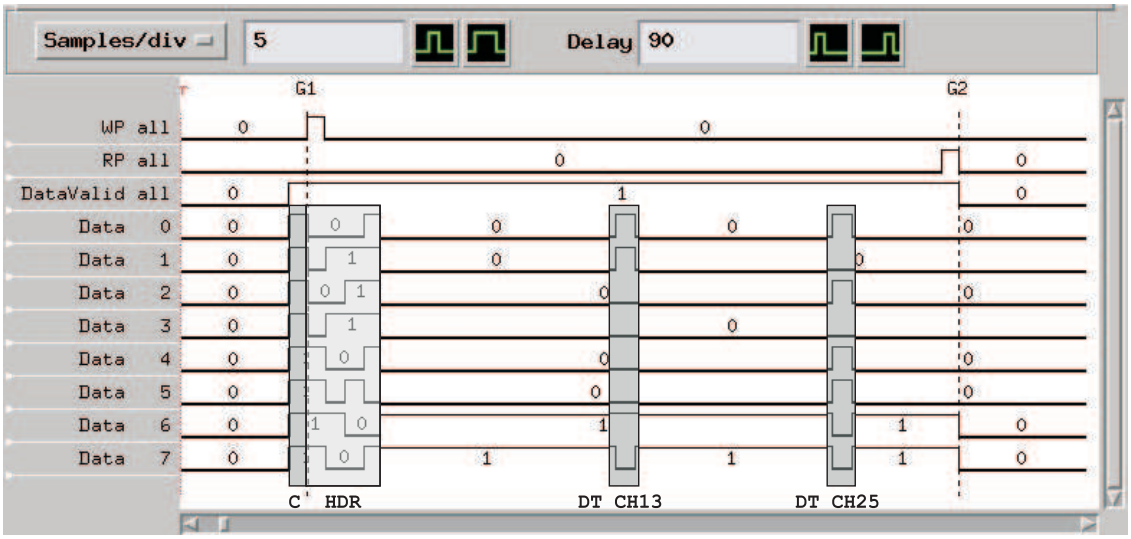

Figure 16: Recording of a data output sequence while operating in the multi hit mode. The four header bytes are followed by 32 drift time bytes. Only the channels 13 and 25 show a valid hit and drift time code.

28 to 45MHz in which the DLL reliably locks. For the chip temperature of 45 centigrade, which the design is based upon, the locking frequencies range from 24 to 50MHz.

Data Output Sequences:
Figure 15 shows an exemplary recording of a data output sequence of the OTIS chip while operating in the multi hit or plain hitmask mode. The visible section of the recording spans 50 clock cycles and between the markers `G1` and `G2` the data from 36 clock cycles is shown. Next to the eight data bits that are labeled from `Data 0` (LSB) to `Data 7` (MSB), the figure additionally presents the `DataValid` signal plus the two service pad signals that are programmed to indicate start and stop of any data transfer. While the service pads only provide signals for monitoring purposes,

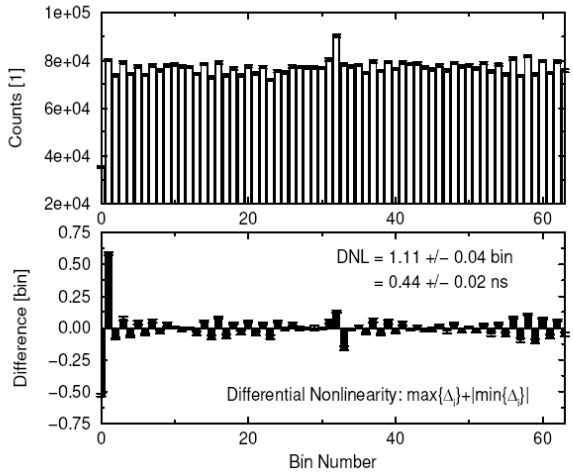

Figure 17: Width of the time bins for a single TDC channel: The width of the time bins is reflected by the occupany caused by a random signal. Bin 0 and bin 32 deviate most. Odd-even bin size differences are already corrected.

the `DataValid` output actually drives the `DataAvailable` input of the GOL chip. This is why the `DataValid` signal encloses the `Comma` byte (`0xFF` left to marker `G1`) but the start and stop signals from the service pads do not.

Figure 16 shows a sample data recording for the encoded hitmask or single hit mode. Here, 32 bytes of combined hit and drift time information follow after the four header bytes. In this example all but two channels show the out-of-range code `0xC0`. Only the bytes that represent channels number 13 and 25 carry valid drift times: `0x43` (or 26.2ns) and `0x35` (or 20.7ns).

Differential Non-Linearity:
The change from a not regulated dummy delay element (`OTIS1.1`) to a regulated one (`OTIS1.2`) didn't result in the expected improvement of the DNL figure of the DLL. The DNL is still above one LSB for `OTIS1.2` chips. As can be seen in figure 17, this is the result of a systematic bin size deviation of bin numbers 0 and 31 caused by the phase detector and charge pump and unbalanced hit signal routing. Phase detector and charge pump work as proportional controller and result in a difference between the effective regulated length of the DLL and the BX signal.

The effects of both shortcomings are visualized in figure 18 which shows the size and the position of the single time bins stacked on top of each other for all 32 channels. For the first 16 channels of the chip the size of the first time bin shrinks dramatically.
Integral Non-Linearity:

The integrated non-linearity (INL) is shown for a single channel (channel 15) in figure 19(left). The maximum deviation w/r to a straight line (INL) is about 0.3 time bins. Figure 19(right) shows the maximum integral nonlinearities (in bin sizes) of all channels as a function of the channel number for three ambient temperatures. Like for the differential nonlinearities, the chips maximum INL is determined from channel number 0.

7.4 `OTIS1.3` Sample Measurements

The DNL of the `OTIS1.3` has significantly improved with respect to earlier versions. Figure 20 shows that all odd and all even time bins have moreless the same width for all 32 channels of the TDC. Moreover, the serious size difference of time bin 0 and 32 wich was present in `OTIS1.3` has

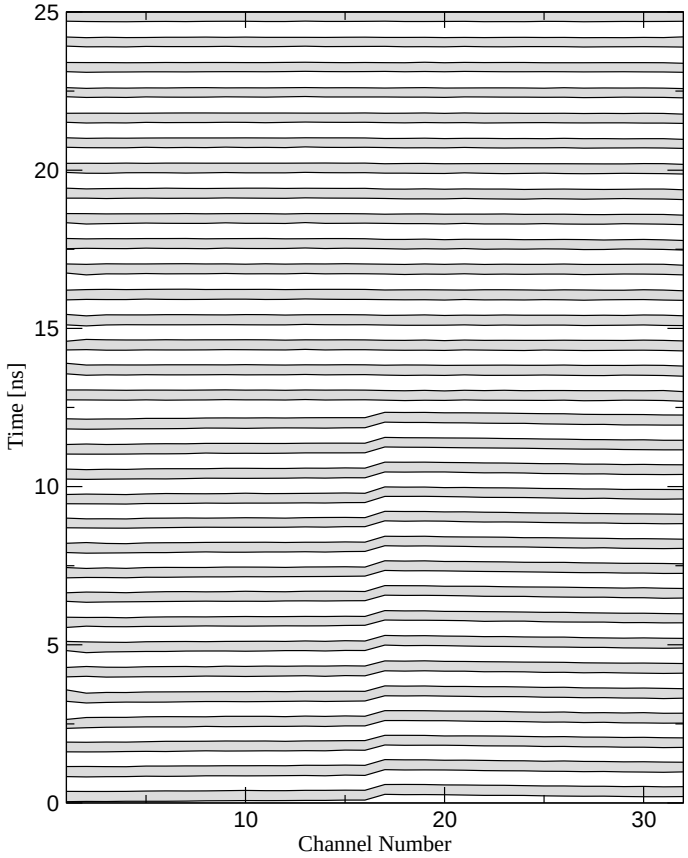

Figure 18: Time bin size and position OTIS1.2.

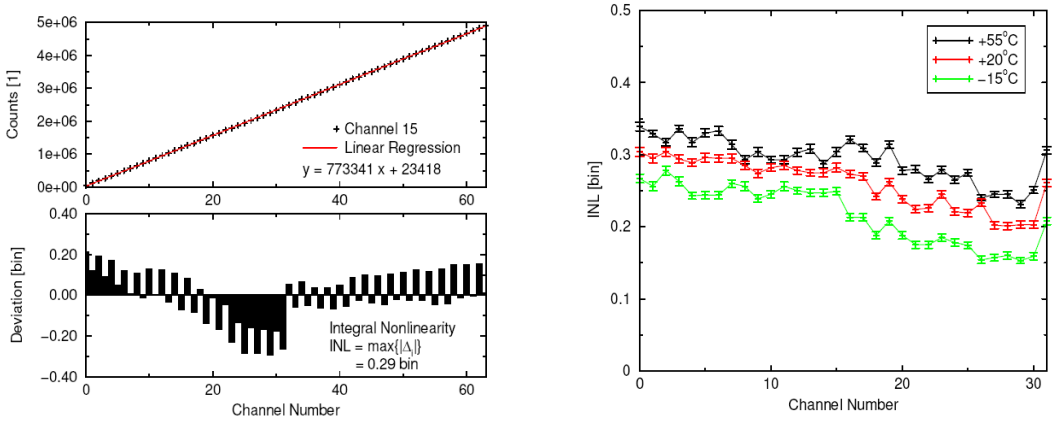

Figure 19: Integrated non-linearity (INL): for channel 15 of a single chip (left) and for all 32 channels of a single chip measured at different temperatures (right).

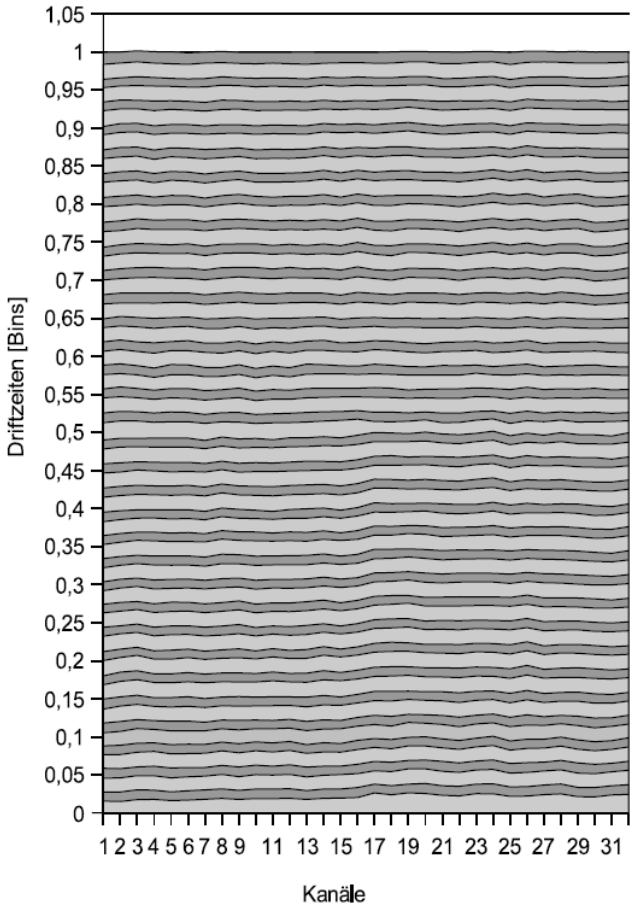

Figure 20: Time bin size and position of OTIS1.3. On the y-axis, 1 corresponds to a full BX clock cycle (25 ns).

vanished. If the different odd and even bin size is corrected the DNL is about 0.3 time bins (120 ps).

7.5 Radiation tolerance (OTIS1.3)

The OTIS TDC chip (OTIS1.2) was part of a total ionising dose irradiation campaign in February 2005 at the X-ray irradiation facility of the CERNs microelectronics group [MIC]. Two chips were subject to irradiation and accumulated a total dose of 1 Mrad(SiO2) (chip A) and 10 Mrad(SiO2) (chip B). For the operating conditions of the X-ray tube (an accelerating voltage of U_{tube} =40 kV and a X-ray tube current of I_{tube}=60 mA) the dose rate (DR) at a distance of 1 cm from the collimator is given by:

$$\mathrm{DR[rad(SiO2)/min]} = 92 + 631 : 30 \times \mathrm{I_{tube}\ [mA]}$$

A total ionising dose of 1 Mrad is accumulated within less than half an hour. No significant changes in the power consumption or in the DLLs control voltage were found after the irradiation campaign. The measured voltage and currents for the two chips before and after irradiation are given in table 7. The third column gives the results from a repeated measurement after $3\frac{1}{2}$ months of chip storage at room temperature. The small change of the values compared to the ones measured during the irradiation campaign is caused by a different ambient temperature. Figure 21

Chip	Dose	Parameter	Pre-Irradiation	Post-Irradiation	After $3\frac{1}{2}$ Months
A	1 Mrad	V_{Ctrl}	1.10 V	1.10 V	1.20 V
		I_{dig}	—	—	250 mA
		I_{ana}	—	—	6 mA
B	10 Mrad	V_{Ctrl}	1.24 V	1.25 V	1.38 V
		I_{dig}	230 mA	224 mA	242 mA
		I_{ana}	2 mA	2 mA	5 mA

Table 7: OTIS1.2 DNL measured before and after the irradiation test.

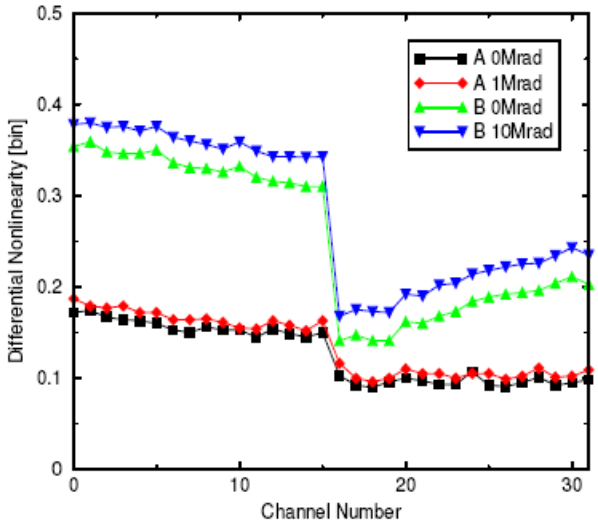

Figure 21: OTIS1.2 DNL measured before and after the irradiation test.

summarises the single channels DNL measurement for both chips before and after the irradiation test. Like above, no significant perfoermance degradation is observed. The OTIS chip thus fulls the LHCb specifications (2 Mrad).

8 List of Known Limitations

- OTIS1.0
  - The data output pads (pads number 13 to 28) are implemented as LVDS pads though the serialiser chip GOL [2] requires single ended CMOS.
  - The memory self test shows a temperature dependency.
  - The dependency between the measured drift times and the arrival time of the detector signals is non-linear.
- OTIS1.1
  - The bunch crossing counter shows erratic behavior due to underestimated driver strengths.
  - Big offset spread for ASD threshold voltages.

  - `MultiHit` mode still missing.
  - Missing inverter causes malfunction of DLL lock lost status information.

- `OTIS`1.2, `OTIS`1.3
  - N.N.

9 How to get the OTIS chip working

- Event-ID
  Problem: the EventID does not follow the number of processed triggers.
  Solution: ensure that the input pads of the EventID reset signal are not floating: an open LVDS input may reset the EventID counter.

- Output signal heights
  Problem: the data output signals (Data, DataValid) do not reach nominal values (2.5V)
  Solution: (`OTIS`1.1 test PCB V1 only) if you are using the SAMTEC connector to access data output signals, please remove the termination resistors (R5, R6, R7, R8 and R12)

- OTIS TDCID and I2CID
  Problem: changing the TDCID has side effects on the I2CID
  Solution: (`OTIS`1.1 test PCB V1 only) be aware that on the test PCB some of the I2C IDs are shorted to TDC IDs:
  ID[18] shorted to ID[5]
  ID[17] ... ID[4]
  ID[16] ... ID[3]
  ID[15] ... ID[2]
  ID[13] ... ID[1]
  ID[12] ... ID[0]

- Digital supply voltage
  Problem: Voltage drop at coil L1 is too big
  Solution: (`OTIS`1.1 test PCB V1 only) bypass (short) coil L1

- DLL Lock
  Problem: DLL lock lost bit is set quite often
  Solution: 1) There is a bug in the lock lost bit generation. Refer to Vctrl for DLL lock state. 2) There is no pull up resistor in the DLL reset pad. Therefor the pad must be tied manually to 2.5V in order to avoid unintended DLL resets (and lock lost bits).

- PowerUpReset
  Problem: A power cycle does not always trigger a PowerUpReset
  Solution: Ensure that the capacitance at the PowerUpReset pad is fully discharged. Otherwise there will be no PowerUpReset.

- `OTIS`1.1 missing drift time codes
  Problem: There are missing drift time codes around bin number 32.
  Solution: Ensure that the trigger signal is synchronized to the rising edge of the LHC bunch crossing clock.

- `OTIS`1.1 missing drift time codes
  Problem: When searching 3BX for hits, there are missing drift time codes near the end of the third BX.
  Solution: Ensure that the hit signal rate does not exceed 1/(3 x 25ns). In `SingleHit` mode only the first hit out of 3 possible hits will be reported.

A OTIS1.0 Pad Layout and Description

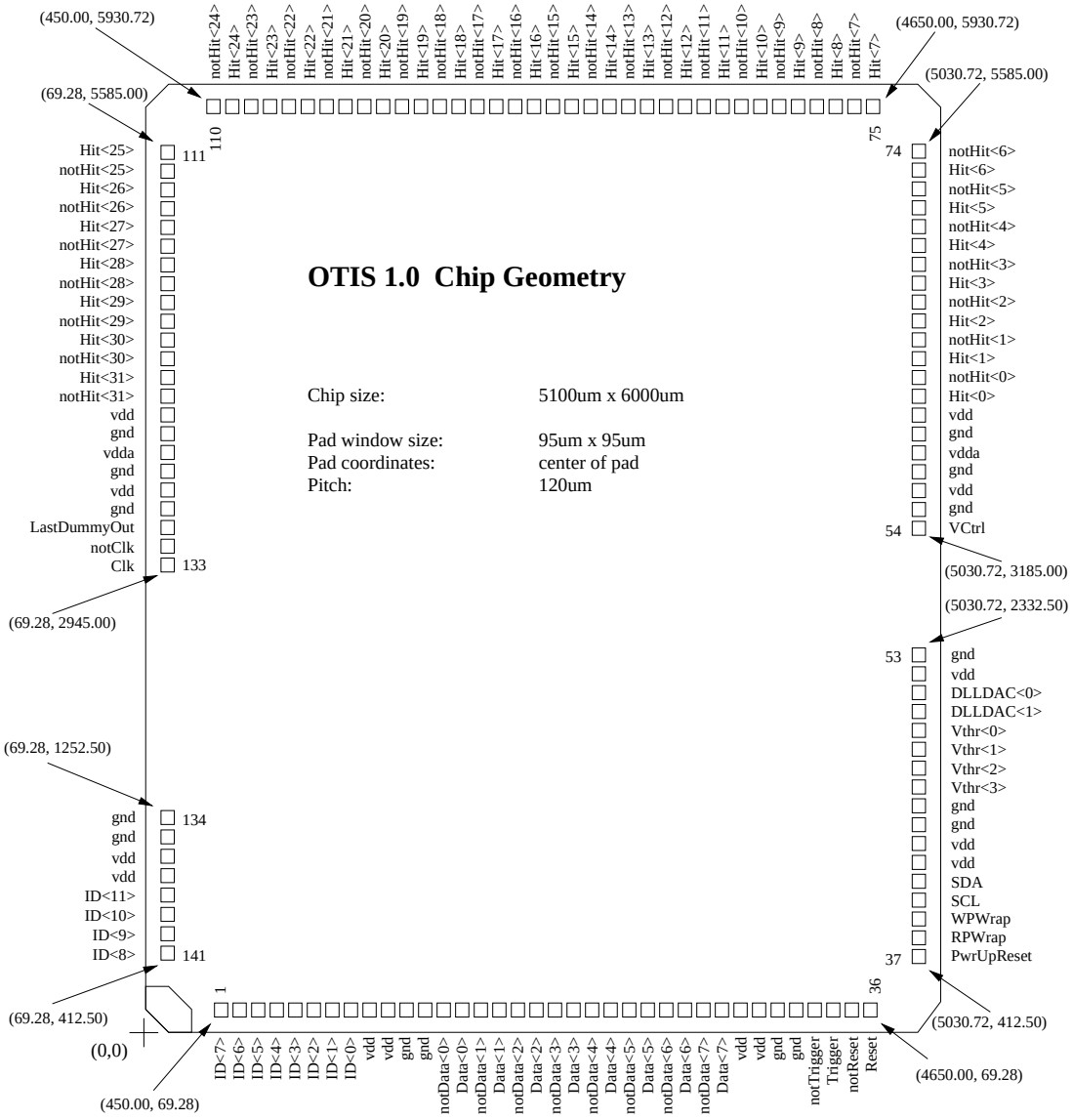

Figure 22: OTIS1.0 Pad Layout

Table 8: OTIS1.0 Pad Description

Number	Name	X [μm]	Y [μm]	Type	Description
1	ID< 7 >	450.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 7)
2	ID< 6 >	570.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 6)
3	ID< 5 >	690.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 5)
4	ID< 4 >	810.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 4)
5	ID< 3 >	930.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 3)
6	ID< 2 >	1050.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 2)
7	ID< 1 >	1170.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 1)
8	ID< 0 >	1290.00	69.28	CMOS input (pull down)	TDC-ID (Bit No 0)
9	vdd	1410.00	69.28	input	positive digital supply
10	vdd	1530.00	69.28	input	positive digital supply
11	gnd	1650.00	69.28	input	negative digital supply
12	gnd	1770.00	69.28	input	negative digital supply
13	notData< 0 >	1890.00	69.28	LVDS output (neg.)	data output (LSB)
14	Data< 0 >	2010.00	69.28	LVDS output (pos.)	
15	notData< 1 >	2130.00	69.28	LVDS output (neg.)	data output
16	Data< 1 >	2250.00	69.28	LVDS output (pos.)	
17	notData< 2 >	2370.00	69.28	LVDS output (neg.)	data output
18	Data< 2 >	2490.00	69.28	LVDS output (pos.)	
19	notData< 3 >	2610.00	69.28	LVDS output (neg.)	data output
20	Data< 3 >	2730.00	69.28	LVDS output (pos.)	
21	notData< 4 >	2850.00	69.28	LVDS output (neg.)	data output
22	Data< 4 >	2970.00	69.28	LVDS output (pos.)	
23	notData< 5 >	3090.00	69.28	LVDS output (neg.)	data output
24	Data< 5 >	3210.00	69.28	LVDS output (pos.)	
25	notData< 6 >	3330.00	69.28	LVDS output (neg.)	data output
26	Data< 6 >	3450.00	69.28	LVDS output (pos.)	
27	notData< 7 >	3570.00	69.28	LVDS output (neg.)	data output (MSB)
28	Data< 7 >	3690.00	69.28	LVDS output (pos.)	
29	vdd	3810.00	69.28	input	positive digital supply
30	vdd	3930.00	69.28	input	positive digital supply
31	gnd	4050.00	69.28	input	negative digital supply
32	gnd	4170.00	69.28	input	negative digital supply
33	notTrigger	4290.00	69.28	LVDS input (neg.)	L0 Trigger
34	Trigger	4410.00	69.28	LVDS input (pos.)	
35	notReset	4530.00	69.28	LVDS input (neg.)	Reset
36	Reset	4650.00	69.28	LVDS input (pos.)	
37	PwrUpReset	5030.72	412.50	input	Power Up Reset
38	RPWrap	5030.72	532.50	output	Read Pointer Wrap
39	WPWrap	5030.72	652.50	output	Write Pointer Wrap
40	SCL	5030.72	772.50	Input	I^2C Clock
41	SDA	5030.72	892.50	input/output	I^2C Data
42	vdd	5030.72	1012.50	input	positive digital supply
43	vdd	5030.72	1132.50	input	positive digital supply
44	gnd	5030.72	1252.50	input	negative digital supply
45	gnd	5030.72	1372.50	input	negative digital supply
46	Vthr< 3 >	5030.72	1492.50	output	Bias
47	Vthr< 2 >	5030.72	1612.50	output	Bias
48	Vthr< 1 >	5030.72	1732.50	output	Bias
49	Vthr< 0 >	5030.72	1852.50	output	Bias
50	DLLDAC< 1 >	5030.72	1972.50	output	Bias
51	DLLDAC< 0 >	5030.72	2092.50	output	Bias
52	vdd	5030.72	2212.50	input	positive digital supply
53	gnd	5030.72	2332.50	input	negative digital supply

Table 8: OTIS1.0 Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
54	VCtrl	5030.72	3185.00	output	Control Voltage
55	gnd	5030.72	3305.00	input	negative digital supply
56	vdd	5030.72	3425.00	input	positive digital supply
57	gnd	5030.72	3545.00	input	negative digital supply
58	vdda	5030.72	3665.00	input	positive analog supply
59	gnd	5030.72	3785.00	input	negative digital supply
60	vdd	5030.72	3905.00	input	positive digital supply
61	Hit< 0 >	5030.72	4025.00	LVDS input (pos.)	Hit Signal
62	notHit< 0 >	5030.72	4145.00	LVDS input (neg.)	
63	Hit< 1 >	5030.72	4265.00	LVDS input (pos.)	Hit Signal
64	notHit< 1 >	5030.72	4385.00	LVDS input (neg.)	
65	Hit< 2 >	5030.72	4505.00	LVDS input (pos.)	Hit Signal
66	notHit< 2 >	5030.72	4625.00	LVDS input (neg.)	
67	Hit< 3 >	5030.72	4745.00	LVDS input (pos.)	Hit Signal
68	notHit< 3 >	5030.72	4865.00	LVDS input (neg.)	
69	Hit< 4 >	5030.72	4985.00	LVDS input (pos.)	Hit Signal
70	notHit< 4 >	5030.72	5105.00	LVDS input (neg.)	
71	Hit< 5 >	5030.72	5225.00	LVDS input (pos.)	Hit Signal
72	notHit< 5 >	5030.72	5345.00	LVDS input (neg.)	
73	Hit< 6 >	5030.72	5465.00	LVDS input (pos.)	Hit Signal
74	notHit< 6 >	5030.72	5585.00	LVDS input (neg.)	
75	Hit< 7 >	4650.00	5930.72	LVDS input (pos.)	
76	notHit< 7 >	4530.00	5930.72	LVDS input (neg.)	Hit Signal
77	Hit< 8 >	4410.00	5930.72	LVDS input (pos.)	Hit Signal
78	notHit< 8 >	4290.00	5930.72	LVDS input (neg.)	
79	Hit< 9 >	4170.00	5930.72	LVDS input (pos.)	Hit Signal
80	notHit< 9 >	4050.00	5930.72	LVDS input (neg.)	
81	Hit< 10 >	3930.00	5930.72	LVDS input (pos.)	Hit Signal
82	notHit< 10 >	3810.00	5930.72	LVDS input (neg.)	
83	Hit< 11 >	3690.00	5930.72	LVDS input (pos.)	Hit Signal
84	notHit< 11 >	3570.00	5930.72	LVDS input (neg.)	
85	Hit< 12 >	3450.00	5930.72	LVDS input (pos.)	Hit Signal
86	notHit< 12 >	3330.00	5930.72	LVDS input (neg.)	
87	Hit< 13 >	3210.00	5930.72	LVDS input (pos.)	Hit Signal
88	notHit< 13 >	3090.00	5930.72	LVDS input (neg.)	
89	Hit< 14 >	2970.00	5930.72	LVDS input (pos.)	Hit Signal
90	notHit< 14 >	2850.00	5930.72	LVDS input (neg.)	
91	Hit< 15 >	2730.00	5930.72	LVDS input (pos.)	Hit Signal
92	notHit< 15 >	2610.00	5930.72	LVDS input (neg.)	
93	Hit< 16 >	2490.00	5930.72	LVDS input (pos.)	Hit Signal
94	notHit< 16 >	2370.00	5930.72	LVDS input (neg.)	
95	Hit< 17 >	2250.00	5930.72	LVDS input (pos.)	Hit Signal
96	notHit< 17 >	2130.00	5930.72	LVDS input (neg.)	
97	Hit< 18 >	2010.00	5930.72	LVDS input (pos.)	Hit Signal
98	notHit< 18 >	1890.00	5930.72	LVDS input (neg.)	
99	Hit< 19 >	1770.00	5930.72	LVDS input (pos.)	Hit Signal
100	notHit< 19 >	1650.00	5930.72	LVDS input (neg.)	
101	Hit< 20 >	1530.00	5930.72	LVDS input (pos.)	Hit Signal
102	notHit< 20 >	1410.00	5930.72	LVDS input (neg.)	
103	Hit< 21 >	1290.00	5930.72	LVDS input (pos.)	Hit Signal
104	notHit< 21 >	1170.00	5930.72	LVDS input (neg.)	
105	Hit< 22 >	1050.00	5930.72	LVDS input (pos.)	Hit Signal
106	notHit< 22 >	930.00	5930.72	LVDS input (neg.)	

Table 8: OTIS1.0 Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
107	Hit< 23 >	810.00	5930.72	LVDS input (pos.)	Hit Signal
108	notHit< 23 >	690.00	5930.72	LVDS input (neg.)	
109	Hit< 24 >	570.00	5930.72	LVDS input (pos.)	Hit Signal
110	notHit< 24 >	450.00	5930.72	LVDS input (neg.)	
111	Hit< 25 >	69.28	5585.00	LVDS input (pos.)	Hit Signal
112	notHit< 25 >	69.28	5465.00	LVDS input (neg.)	
113	Hit< 26 >	69.28	5345.00	LVDS input (pos.)	Hit Signal
114	notHit< 26 >	69.28	5225.00	LVDS input (neg.)	
115	Hit< 27 >	69.28	5105.00	LVDS input (pos.)	Hit Signal
116	notHit< 27 >	69.28	4985.00	LVDS input (neg.)	
117	Hit< 28 >	69.28	4865.00	LVDS input (pos.)	Hit Signal
118	notHit< 28 >	69.28	4745.00	LVDS input (neg.)	
119	Hit< 29 >	69.28	4625.00	LVDS input (pos.)	Hit Signal
120	notHit< 29 >	69.28	4505.00	LVDS input (neg.)	
121	Hit< 30 >	69.28	4385.00	LVDS input (pos.)	Hit Signal
122	notHit< 30 >	69.28	4265.00	LVDS input (neg.)	
123	Hit< 31 >	69.28	4145.00	LVDS input (pos.)	Hit Signal
124	notHit< 31 >	69.28	4025.00	LVDS input (neg.)	
125	vdd	69.28	3905.00	input	positive digital supply
126	gnd	69.28	3785.00	input	negative digital supply
127	vdda	69.28	3665.00	input	positive analog supply
128	gnd	69.28	3545.00	input	negative digital supply
129	vdd	69.28	3425.00	input	positive digital supply
130	gnd	69.28	3305.00	input	negative digital supply
131	LastDummyOut	69.28	3185.00	output	
132	notClk	69.28	3065.00	LVDS input (neg.)	LHC Clock
133	Clk	69.28	2945.00	LVDS input (pos.)	
134	gnd	69.28	1252.50	input	negative digital supply
135	gnd	69.28	1132.50	input	negative digital supply
136	vdd	69.28	1012.50	input	positive digital supply
137	vdd	69.28	892.50	input	positive digital supply
138	ID< 11 >	69.28	772.50	CMOS input (pull down)	TDC-ID (Bit No 11)
139	ID< 10 >	69.28	652.50	CMOS input (pull down)	TDC-ID (Bit No 10)
140	ID< 9 >	69.28	532.50	CMOS input (pull down)	TDC-ID (Bit No 9)
141	ID< 8 >	69.28	412.50	CMOS input (pull down)	TDC-ID (Bit No 8)

B OTIS1.1 Pad Layout and Description

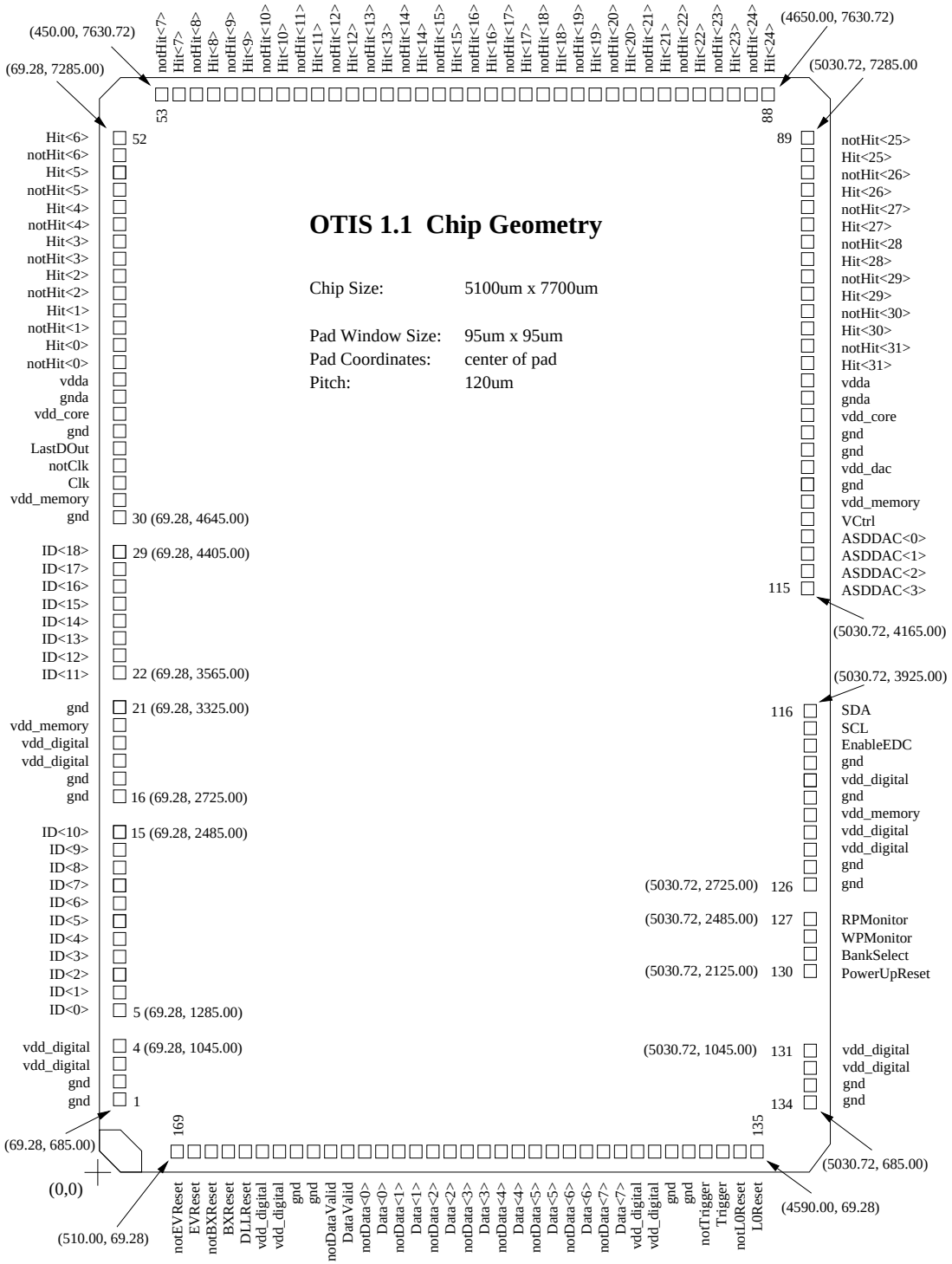

Figure 23: OTIS1.1 Pad Layout

Table 9: OTIS1.1 Pad Description

Number	Name	X [μm]	Y [μm]	Type	Description
1	gnd	69.28	685.00	input	negative digital supply
2	gnd	69.28	805.00	input	negative digital supply
3	vdd_digital	69.28	925.00	input	positive digital supply
4	vdd_digital	69.28	1045.00	input	positive digital supply
5	ID< 0 >	69.28	1285.00	CMOS input (pull down)	TDC ID (Bit no. 0)
6	ID< 1 >	69.28	1405.00	CMOS input (pull down)	TDC ID (Bit no. 1)
7	ID< 2 >	69.28	1525.00	CMOS input (pull down)	TDC ID (Bit no. 2)
8	ID< 3 >	69.28	1645.00	CMOS input (pull down)	TDC ID (Bit no. 3)
9	ID< 4 >	69.28	1765.00	CMOS input (pull down)	TDC ID (Bit no. 4)
10	ID< 5 >	69.28	1885.00	CMOS input (pull down)	TDC ID (Bit no. 5)
11	ID< 6 >	69.28	2005.00	CMOS input (pull down)	TDC ID (Bit no. 6)
12	ID< 7 >	69.28	2125.00	CMOS input (pull down)	TDC ID (Bit no. 7)
13	ID< 8 >	69.28	2245.00	CMOS input (pull down)	TDC ID (Bit no. 8)
14	ID< 9 >	69.28	2365.00	CMOS input (pull down)	TDC ID (Bit no. 9)
15	ID< 10 >	69.28	2485.00	CMOS input (pull down)	TDC ID (Bit no. 10)
16	gnd	69.28	2725.00	input	negative digital supply
17	gnd	69.28	2845.00	input	negative digital supply
18	vdd_digital	69.28	2965.00	input	negative digital supply
19	vdd_digital	69.28	3085.00	input	positive digital supply
20	vdd_memory	69.28	3205.00	input	positive memory supply
21	gnd	69.28	3325.00	input	negative digital supply
22	ID< 11 >	69.28	3565.00	CMOS input (pull down)	TDC ID (Bit no. 11)
23	ID< 12 >	69.28	3685.00	CMOS input (pull down)	TDC ID (Bit no. 12)
24	ID< 13 >	69.28	3805.00	CMOS input (pull down)	TDC ID (Bit no. 13)
25	ID< 14 >	69.28	3925.00	CMOS input (pull down)	TDC ID (Bit no. 14)
26	ID< 15 >	69.28	4045.00	CMOS input (pull down)	TDC ID (Bit no. 15)
27	ID< 16 >	69.28	4165.00	CMOS input (pull down)	TDC ID (Bit no. 16)
28	ID< 17 >	69.28	4285.00	CMOS input (pull down)	TDC ID (Bit no. 17)
29	ID< 18 >	69.28	4405.00	CMOS input (pull down)	TDC ID (Bit no. 18)
30	gnd	69.28	4645.00	input	negative digital supply
31	vdd_memory	69.28	4765.00	input	positive memory supply
32	Clk	69.28	4885.00	LVDS input (pos.)	LHC Clock
33	notClk	69.28	5005.00	LVDS input (neg.)	
34	LastDOut	69.28	5125.00		
35	gnd	69.28	5245.00	input	negative digital supply
36	vdd_core	69.28	5365.00	input	positive TDC supply
37	gnda	69.28	5485.00	input	negative DLL supply
38	vdda	69.28	5605.00	input	positive DLL supply
39	notHit< 0 >	69.28	5725.00	LVDS input (neg.)	Hit Signal
40	Hit< 0 >	69.28	5845.00	LVDS input (pos.)	
41	notHit< 1 >	69.28	5965.00	LVDS input (neg.)	Hit Signal
42	Hit< 1 >	69.28	6085.00	LVDS input (pos.)	
43	notHit< 2 >	69.28	6205.00	LVDS input (neg.)	Hit Signal
44	Hit< 2 >	69.28	6325.00	LVDS input (pos.)	
45	notHit< 3 >	69.28	6445.00	LVDS input (neg.)	Hit Signal
46	Hit< 3 >	69.28	6565.00	LVDS input (pos.)	
47	notHit< 4 >	69.28	6685.00	LVDS input (neg.)	Hit Signal
48	Hit< 4 >	69.28	6805.00	LVDS input (pos.)	
49	notHit< 5 >	69.28	6925.00	LVDS input (neg.)	Hit Signal
50	Hit< 5 >	69.28	7045.00	LVDS input (pos.)	
51	notHit< 6 >	69.28	7165.00	LVDS input (neg.)	Hit Signal
52	Hit< 6 >	69.28	7285.00	LVDS input (pos.)	

Table 9: OTIS1.1 Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
53	notHit< 7 >	450.00	7630.72	LVDS input (neg.)	Hit Signal
54	Hit< 7 >	570.00	7630.72	LVDS input (pos.)	
55	notHit< 8 >	690.00	7630.72	LVDS input (neg.)	Hit Signal
56	Hit< 8 >	810.00	7630.72	LVDS input (pos.)	
57	notHit< 9 >	930.00	7630.72	LVDS input (neg.)	Hit Signal
58	Hit< 9 >	1050.00	7630.72	LVDS input (pos.)	
59	notHit< 10 >	1170.00	7630.72	LVDS input (neg.)	Hit Signal
60	Hit< 10 >	1290.00	7630.72	LVDS input (pos.)	
61	notHit< 11 >	1410.00	7630.72	LVDS input (neg.)	Hit Signal
62	Hit< 11 >	1530.00	7630.72	LVDS input (pos.)	
63	notHit< 12 >	1650.00	7630.72	LVDS input (neg.)	Hit Signal
64	Hit< 12 >	1770.00	7630.72	LVDS input (pos.)	
65	notHit< 13 >	1890.00	7630.72	LVDS input (neg.)	Hit Signal
66	Hit< 13 >	2010.00	7630.72	LVDS input (pos.)	
67	notHit< 14 >	2130.00	7630.72	LVDS input (neg.)	Hit Signal
68	Hit< 14 >	2250.00	7630.72	LVDS input (pos.)	
69	notHit< 15 >	2370.00	7630.72	LVDS input (neg.)	Hit Signal
70	Hit< 15 >	2490.00	7630.72	LVDS input (pos.)	
71	notHit< 16 >	2610.00	7630.72	LVDS input (neg.)	Hit Signal
72	Hit< 16 >	2730.00	7630.72	LVDS input (pos.)	
73	notHit< 17 >	2850.00	7630.72	LVDS input (neg.)	Hit Signal
74	Hit< 17 >	2970.00	7630.72	LVDS input (pos.)	
75	notHit< 18 >	3090.00	7630.72	LVDS input (neg.)	Hit Signal
76	Hit< 18 >	3210.00	7630.72	LVDS input (pos.)	
77	notHit< 19 >	3330.00	7630.72	LVDS input (neg.)	Hit Signal
78	Hit< 19 >	3450.00	7630.72	LVDS input (pos.)	
79	notHit< 20 >	3570.00	7630.72	LVDS input (neg.)	Hit Signal
80	Hit< 20 >	3690.00	7630.72	LVDS input (pos.)	
81	notHit< 21 >	3810.00	7630.72	LVDS input (neg.)	Hit Signal
82	Hit< 21 >	3930.00	7630.72	LVDS input (pos.)	
83	notHit< 22 >	4050.00	7630.72	LVDS input (neg.)	Hit Signal
84	Hit< 22 >	4170.00	7630.72	LVDS input (pos.)	
85	notHit< 23 >	4290.00	7630.72	LVDS input (neg.)	Hit Signal
86	Hit< 23 >	4410.00	7630.72	LVDS input (pos.)	
87	notHit< 24 >	4530.00	7630.72	LVDS input (neg.)	Hit Signal
88	Hit< 24 >	4650.00	7630.72	LVDS input (pos.)	
89	notHit< 25 >	5030.72	7285.00	LVDS input (neg.)	Hit Signal
90	Hit< 25 >	5030.72	7165.00	LVDS input (pos.)	
91	notHit< 26 >	5030.72	7045.00	LVDS input (neg.)	Hit Signal
92	Hit< 26 >	5030.72	6925.00	LVDS input (pos.)	
93	notHit< 27 >	5030.72	6805.00	LVDS input (neg.)	Hit Signal
94	Hit< 27 >	5030.72	6685.00	LVDS input (pos.)	
95	notHit< 28 >	5030.72	6565.00	LVDS input (neg.)	Hit Signal
96	Hit< 28 >	5030.72	6445.00	LVDS input (pos.)	
97	notHit< 29 >	5030.72	6325.00	LVDS input (neg.)	Hit Signal
98	Hit< 29 >	5030.72	6205.00	LVDS input (pos.)	
99	notHit< 30 >	5030.72	6085.00	LVDS input (neg.)	Hit Signal
100	Hit< 30 >	5030.72	5965.00	LVDS input (pos.)	
101	notHit< 31 >	5030.72	5845.00	LVDS input (neg.)	Hit Signal
102	Hit< 31 >	5030.72	5725.00	LVDS input (pos.)	
103	vdda	5030.72	5605.00	input	positive DLL supply
104	gnda	5030.72	5485.00	input	negative DLL supply
105	vdd_core	5030.72	5365.00	input	positive TDC supply
106	gnd	5030.72	5245.00	input	negative digital supply

Table 9: OTIS1.1 Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
107	gnd	5030.72	5125.00	input	negative digital supply
108	vdd_DAC	5030.72	5005.00	input	positive DAC supply
109	gnd	5030.72	4885.00	input	negative digital supply
110	vdd_memory	5030.72	4765.00	input	positive memory supply
111	VCtrl	5030.72	4645.00	analogue output	DLL control voltage
112	ASDDAC< 0 >	5030.72	4525.00	analogue output	Threshold voltage 0
113	ASDDAC< 1 >	5030.72	4405.00	analogue output	Threshold voltage 1
114	ASDDAC< 2 >	5030.72	4285.00	analogue output	Threshold voltage 2
115	ASDDAC< 3 >	5030.72	4165.00	analogue output	Threshold voltage 3
116	SDA	5030.72	3925.00	input/output (5V open drain)	I^2C Data
117	SCL	5030.72	3805.00	CMOS input (5V)	I^2C Clock
118	EnableEDC	5030.72	3685.00	CMOS input (internal pull down)	enable I^2C EDC
119	gnd	5030.72	3565.00	input	negative digital supply
120	vdd_digital	5030.72	3445.00	input	positive digital supply
121	gnd	5030.72	3325.00	input	negative digital supply
122	vdd_memory	5030.72	3205.00	input	positive memory supply
123	vdd_digital	5030.72	3085.00	input	positive digital supply
124	vdd_digital	5030.72	2965.00	input	positive digital supply
125	gnd	5030.72	2845.00	input	negative digital supply
126	gnd	5030.72	2725.00	input	negative digital supply
127	RPMonitor	5030.72	2485.00	CMOS output	Read Pointer Wrap
128	WPMonitor	5030.72	2365.00	CMOS output	Write Pointer Wrap
129	BankSelect	5030.72	2245.00	CMOS input (pull down)	Bank Select
130	PowerUpReset	5030.72	2125.00	input	Power Up Reset
131	vdd_digital	5030.72	1045.00	input	positive digital supply
132	vdd_digital	5030.72	925.00	input	positive digital supply
133	gnd	5030.72	805.00	input	negative digital supply
134	gnd	5030.72	685.00	input	negative digital supply
135	L0Reset	4590.00	69.28	LVDS input (pos.)	L0Reset
136	notL0Reset	4470.00	69.28	LVDS input (neg.)	
137	Trigger	4350.00	69.28	LVDS input (pos.)	L0Trigger
138	notTrigger	4230.00	69.28	LVDS input (neg.)	
139	gnd	4110.00	69.28	input	negative digital supply
140	gnd	3990.00	69.28	input	negative digital supply
141	vdd_digital	3870.00	69.28	input	positive digital supply
142	vdd_digital	3750.00	69.28	input	positive digital supply
143	Data< 7 >	3630.00	69.28	CMOS output (pos.)	data output (MSB)
144	notData< 7 >	3510.00	69.28	CMOS output (neg.)	
145	Data< 6 >	3390.00	69.28	CMOS output (pos.)	data output
146	notData< 6 >	3270.00	69.28	CMOS output (neg.)	
147	Data< 5 >	3150.00	69.28	CMOS output (pos.)	data output
148	notData< 5 >	3030.00	69.28	CMOS output (neg.)	
149	Data< 4 >	2910.00	69.28	CMOS output (pos.)	data output
150	notData< 4 >	2790.00	69.28	CMOS output (neg.)	
151	Data< 3 >	2670.00	69.28	CMOS output (pos.)	data output
152	notData< 3 >	2550.00	69.28	CMOS output (neg.)	
153	Data< 2 >	2430.00	69.28	CMOS output (pos.)	data output
154	notData< 2 >	2310.00	69.28	CMOS output (neg.)	
155	Data< 1 >	2190.00	69.28	CMOS output (pos.)	data output
156	notData< 1 >	2070.00	69.28	CMOS output (neg.)	
157	Data< 0 >	1950.00	69.28	CMOS output (pos.)	data output (LSB)
158	notData< 0 >	1830.00	69.28	CMOS output (neg.)	

Table 9: OTIS1.1 Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
159	DataValid	1710.00	69.28	CMOS output (pos.)	Data Valid
160	notDataValid	1590.00	69.28	CMOS output (neg.)	
161	gnd	1470.00	69.28	input	negative digital supply
162	gnd	1350.00	69.28	input	negative digital supply
163	vdd_digital	1230.00	69.28	input	positive digital supply
164	vdd_digital	1110.00	69.28	input	positive digital supply
165	DLLReset	990.00	69.28	CMOS input	DLL Reset
166	BXReset	870.00	69.28	LVDS input (pos.)	BX Counter Reset
167	notBXReset	750.00	69.28	LVDS input (neg.)	
168	EVReset	630.00	69.28	LVDS input (pos.)	Event Counter Reset
169	notEVReset	510.00	69.28	LVDS input (neg.)	

C OTIS1.2 Pad Layout and Description

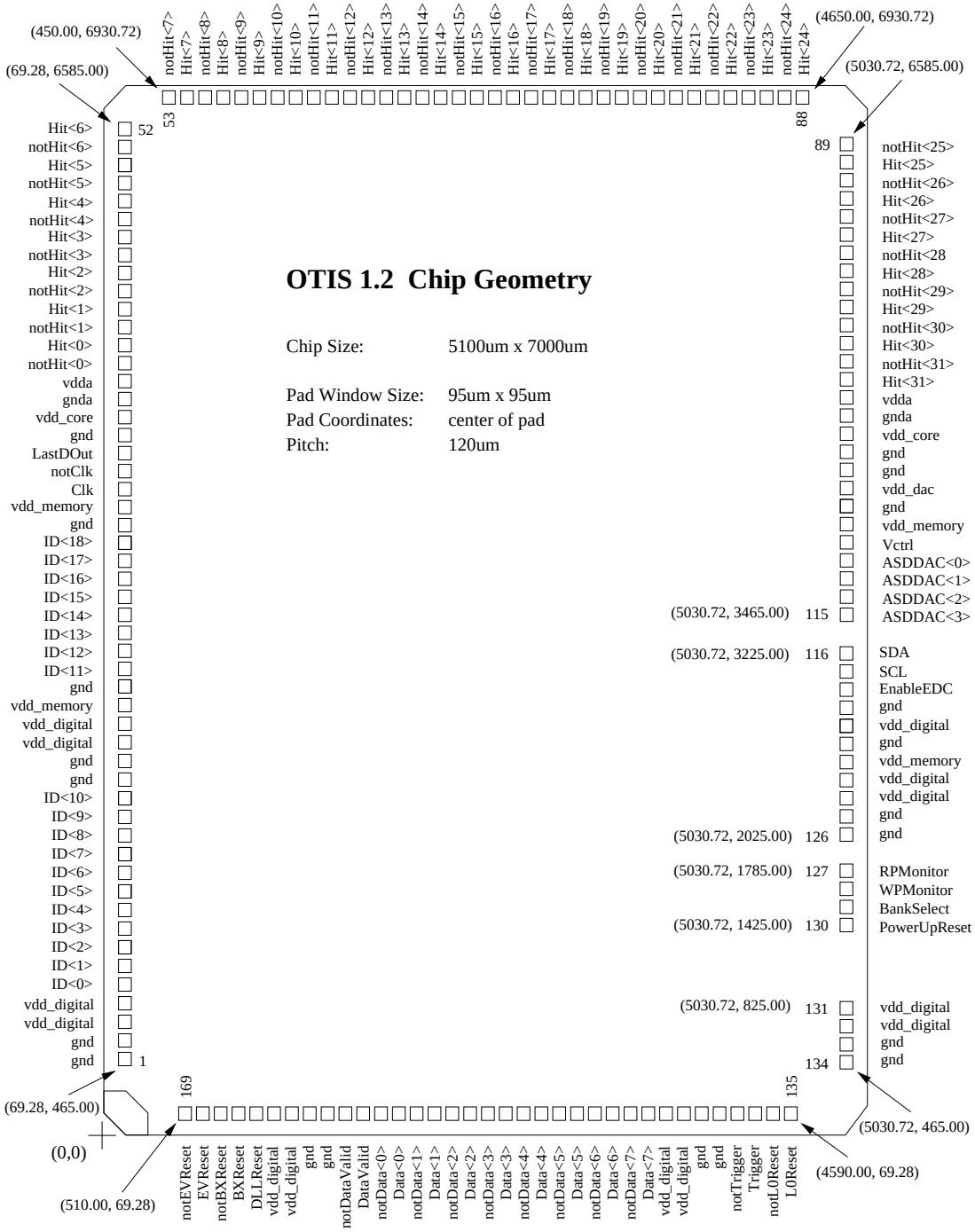

Figure 24: OTIS1.2 Pad Layout

Table 10: OTIS1.2 Pad Description

Number	Name	X [μm]	Y [μm]	Type	Description
1	gnd	69.28	465.00	input	negative digital supply
2	gnd	69.28	485.00	input	negative digital supply
3	vdd_digital	69.28	705.00	input	positive digital supply
4	vdd_digital	69.28	825.00	input	positive digital supply
5	ID< 0 >	69.28	945.00	CMOS input (pull down)	TDC ID (Bit no. 0)
6	ID< 1 >	69.28	1065.00	CMOS input (pull down)	TDC ID (Bit no. 1)
7	ID< 2 >	69.28	1185.00	CMOS input (pull down)	TDC ID (Bit no. 2)
8	ID< 3 >	69.28	1305.00	CMOS input (pull down)	TDC ID (Bit no. 3)
9	ID< 4 >	69.28	1425.00	CMOS input (pull down)	TDC ID (Bit no. 4)
10	ID< 5 >	69.28	1545.00	CMOS input (pull down)	TDC ID (Bit no. 5)
11	ID< 6 >	69.28	1665.00	CMOS input (pull down)	TDC ID (Bit no. 6)
12	ID< 7 >	69.28	1785.00	CMOS input (pull down)	TDC ID (Bit no. 7)
13	ID< 8 >	69.28	1905.00	CMOS input (pull down)	TDC ID (Bit no. 8)
14	ID< 9 >	69.28	2025.00	CMOS input (pull down)	TDC ID (Bit no. 9)
15	ID< 10 >	69.28	2145.00	CMOS input (pull down)	TDC ID (Bit no. 10)
16	gnd	69.28	2265.00	input	negative digital supply
17	gnd	69.28	2385.00	input	negative digital supply
18	vdd_digital	69.28	2505.00	input	negative digital supply
19	vdd_digital	69.28	2625.00	input	positive digital supply
20	vdd_memory	69.28	2745.00	input	positive memory supply
21	gnd	69.28	2865.00	input	negative digital supply
22	ID< 11 >	69.28	2985.00	CMOS input (pull down)	TDC ID (Bit no. 11)
23	ID< 12 >	69.28	3105.00	CMOS input (pull down)	TDC ID (Bit no. 12)
24	ID< 13 >	69.28	3225.00	CMOS input (pull down)	TDC ID (Bit no. 13)
25	ID< 14 >	69.28	3345.00	CMOS input (pull down)	TDC ID (Bit no. 14)
26	ID< 15 >	69.28	3465.00	CMOS input (pull down)	TDC ID (Bit no. 15)
27	ID< 16 >	69.28	3585.00	CMOS input (pull down)	TDC ID (Bit no. 16)
28	ID< 17 >	69.28	3705.00	CMOS input (pull down)	TDC ID (Bit no. 17)
29	ID< 18 >	69.28	3825.00	CMOS input (pull down)	TDC ID (Bit no. 18)
30	gnd	69.28	3945.00	input	negative digital supply
31	vdd_memory	69.28	4065.00	input	positive memory supply
32	Clk	69.28	4185.00	LVDS input (pos.)	LHC Clock
33	notClk	69.28	4305.00	LVDS input (neg.)	
34	LastDOut	69.28	4425.00		
35	gnd	69.28	4545.00	input	negative digital supply
36	vdd_core	69.28	4665.00	input	positive TDC supply
37	gnda	69.28	4785.00	input	negative DLL supply
38	vdda	69.28	4905.00	input	positive DLL supply
39	notHit< 0 >	69.28	5025.00	LVDS input (neg.)	Hit Signal
40	Hit< 0 >	69.28	5145.00	LVDS input (pos.)	
41	notHit< 1 >	69.28	5265.00	LVDS input (neg.)	Hit Signal
42	Hit< 1 >	69.28	5385.00	LVDS input (pos.)	
43	notHit< 2 >	69.28	5505.00	LVDS input (neg.)	Hit Signal
44	Hit< 2 >	69.28	5625.00	LVDS input (pos.)	
45	notHit< 3 >	69.28	5745.00	LVDS input (neg.)	Hit Signal
46	Hit< 3 >	69.28	5865.00	LVDS input (pos.)	
47	notHit< 4 >	69.28	5985.00	LVDS input (neg.)	Hit Signal
48	Hit< 4 >	69.28	6105.00	LVDS input (pos.)	
49	notHit< 5 >	69.28	6225.00	LVDS input (neg.)	Hit Signal
50	Hit< 5 >	69.28	6345.00	LVDS input (pos.)	
51	notHit< 6 >	69.28	6465.00	LVDS input (neg.)	Hit Signal
52	Hit< 6 >	69.28	6585.00	LVDS input (pos.)	

Table 10: OTIS1.2Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
53	notHit< 7 >	450.00	6930.72	LVDS input (neg.)	Hit Signal
54	Hit< 7 >	570.00	6930.72	LVDS input (pos.)	
55	notHit< 8 >	690.00	6930.72	LVDS input (neg.)	Hit Signal
56	Hit< 8 >	810.00	6930.72	LVDS input (pos.)	
57	notHit< 9 >	930.00	6930.72	LVDS input (neg.)	Hit Signal
58	Hit< 9 >	1050.00	6930.72	LVDS input (pos.)	
59	notHit< 10 >	1170.00	6930.72	LVDS input (neg.)	Hit Signal
60	Hit< 10 >	1290.00	6930.72	LVDS input (pos.)	
61	notHit< 11 >	1410.00	6930.72	LVDS input (neg.)	Hit Signal
62	Hit< 11 >	1530.00	6930.72	LVDS input (pos.)	
63	notHit< 12 >	1650.00	6930.72	LVDS input (neg.)	Hit Signal
64	Hit< 12 >	1770.00	6930.72	LVDS input (pos.)	
65	notHit< 13 >	1890.00	6930.72	LVDS input (neg.)	Hit Signal
66	Hit< 13 >	2010.00	6930.72	LVDS input (pos.)	
67	notHit< 14 >	2130.00	6930.72	LVDS input (neg.)	Hit Signal
68	Hit< 14 >	2250.00	6930.72	LVDS input (pos.)	
69	notHit< 15 >	2370.00	6930.72	LVDS input (neg.)	Hit Signal
70	Hit< 15 >	2490.00	6930.72	LVDS input (pos.)	
71	notHit< 16 >	2610.00	6930.72	LVDS input (neg.)	Hit Signal
72	Hit< 16 >	2730.00	6930.72	LVDS input (pos.)	
73	notHit< 17 >	2850.00	6930.72	LVDS input (neg.)	Hit Signal
74	Hit< 17 >	2970.00	6930.72	LVDS input (pos.)	
75	notHit< 18 >	3090.00	6930.72	LVDS input (neg.)	Hit Signal
76	Hit< 18 >	3210.00	6930.72	LVDS input (pos.)	
77	notHit< 19 >	3330.00	6930.72	LVDS input (neg.)	Hit Signal
78	Hit< 19 >	3450.00	6930.72	LVDS input (pos.)	
79	notHit< 20 >	3570.00	6930.72	LVDS input (neg.)	Hit Signal
80	Hit< 20 >	3690.00	6930.72	LVDS input (pos.)	
81	notHit< 21 >	3810.00	6930.72	LVDS input (neg.)	Hit Signal
82	Hit< 21 >	3930.00	6930.72	LVDS input (pos.)	
83	notHit< 22 >	4050.00	6930.72	LVDS input (neg.)	Hit Signal
84	Hit< 22 >	4170.00	6930.72	LVDS input (pos.)	
85	notHit< 23 >	4290.00	6930.72	LVDS input (neg.)	Hit Signal
86	Hit< 23 >	4410.00	6930.72	LVDS input (pos.)	
87	notHit< 24 >	4530.00	6930.72	LVDS input (neg.)	Hit Signal
88	Hit< 24 >	4650.00	6930.72	LVDS input (pos.)	
89	notHit< 25 >	5030.72	6585.00	LVDS input (neg.)	Hit Signal
90	Hit< 25 >	5030.72	6465.00	LVDS input (pos.)	
91	notHit< 26 >	5030.72	6345.00	LVDS input (neg.)	Hit Signal
92	Hit< 26 >	5030.72	6225.00	LVDS input (pos.)	
93	notHit< 27 >	5030.72	6105.00	LVDS input (neg.)	Hit Signal
94	Hit< 27 >	5030.72	5985.00	LVDS input (pos.)	
95	notHit< 28 >	5030.72	5865.00	LVDS input (neg.)	Hit Signal
96	Hit< 28 >	5030.72	5745.00	LVDS input (pos.)	
97	notHit< 29 >	5030.72	5625.00	LVDS input (neg.)	Hit Signal
98	Hit< 29 >	5030.72	5505.00	LVDS input (pos.)	
99	notHit< 30 >	5030.72	5385.00	LVDS input (neg.)	Hit Signal
100	Hit< 30 >	5030.72	5265.00	LVDS input (pos.)	
101	notHit< 31 >	5030.72	5145.00	LVDS input (neg.)	Hit Signal
102	Hit< 31 >	5030.72	5025.00	LVDS input (pos.)	
103	vdda	5030.72	4905.00	input	positive DLL supply
104	gnda	5030.72	4785.00	input	negative DLL supply
105	vdd_core	5030.72	4665.00	input	positive TDC supply
106	gnd	5030.72	4545.00	input	negative digital supply

Table 10: OTIS1.2Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
107	gnd	5030.72	4425.00	input	negative digital supply
108	vdd_DAC	5030.72	4305.00	input	positive DAC supply
109	gnd	5030.72	4185.00	input	negative digital supply
110	vdd_memory	5030.72	4065.00	input	positive memory supply
111	VCtrl	5030.72	3945.00	analogue output	DLL control voltage
112	ASDDAC< 0 >	5030.72	3825.00	analogue output	Threshold voltage 0
113	ASDDAC< 1 >	5030.72	3705.00	analogue output	Threshold voltage 1
114	ASDDAC< 2 >	5030.72	3585.00	analogue output	Threshold voltage 2
115	ASDDAC< 3 >	5030.72	3465.00	analogue output	Threshold voltage 3
116	SDA	5030.72	3225.00	input/output (5V open drain)	I^2C Data
117	SCL	5030.72	3105.00	CMOS input (5V)	I^2C Clock
118	EnableEDC	5030.72	2985.00	CMOS input (pull down)	Enable I^2C EDC
119	gnd	5030.72	2865.00	input	negative digital supply
120	vdd_digital	5030.72	2745.00	input	positive digital supply
121	gnd	5030.72	2625.00	input	negative digital supply
122	vdd_memory	5030.72	2505.00	input	positive memory supply
123	vdd_digital	5030.72	2385.00	input	positive digital supply
124	vdd_digital	5030.72	2265.00	input	positive digital supply
125	gnd	5030.72	2145.00	input	negative digital supply
126	gnd	5030.72	2025.00	input	negative digital supply
127	RPMonitor	5030.72	1785.00	CMOS output	Read Pointer Wrap
128	WPMonitor	5030.72	1665.00	CMOS output	Write Pointer Wrap
129	BankSelect	5030.72	1545.00	CMOS input (pull down)	Bank Select
130	PowerUpReset	5030.72	1425.00	input	Power Up Reset
131	vdd_digital	5030.72	825.00	input	positive digital supply
132	vdd_digital	5030.72	705.00	input	positive digital supply
133	gnd	5030.72	585.00	input	negative digital supply
134	gnd	5030.72	465.00	input	negative digital supply
135	L0Reset	4590.00	69.28	LVDS input (pos.)	L0Reset
136	notL0Reset	4470.00	69.28	LVDS input (neg.)	
137	Trigger	4350.00	69.28	LVDS input (pos.)	L0Trigger
138	notTrigger	4230.00	69.28	LVDS input (neg.)	
139	gnd	4110.00	69.28	input	negative digital supply
140	gnd	3990.00	69.28	input	negative digital supply
141	vdd_digital	3870.00	69.28	input	positive digital supply
142	vdd_digital	3750.00	69.28	input	positive digital supply
143	Data< 7 >	3630.00	69.28	CMOS output (pos.)	data output (MSB)
144	notData< 7 >	3510.00	69.28	CMOS output (neg.)	
145	Data< 6 >	3390.00	69.28	CMOS output (pos.)	data output
146	notData< 6 >	3270.00	69.28	CMOS output (neg.)	
147	Data< 5 >	3150.00	69.28	CMOS output (pos.)	data output
148	notData< 5 >	3030.00	69.28	CMOS output (neg.)	
149	Data< 4 >	2910.00	69.28	CMOS output (pos.)	data output
150	notData< 4 >	2790.00	69.28	CMOS output (neg.)	
151	Data< 3 >	2670.00	69.28	CMOS output (pos.)	data output
152	notData< 3 >	2550.00	69.28	CMOS output (neg.)	
153	Data< 2 >	2430.00	69.28	CMOS output (pos.)	data output
154	notData< 2 >	2310.00	69.28	CMOS output (neg.)	
155	Data< 1 >	2190.00	69.28	CMOS output (pos.)	data output
156	notData< 1 >	2070.00	69.28	CMOS output (neg.)	
157	Data< 0 >	1950.00	69.28	CMOS output (pos.)	data output (LSB)
158	notData< 0 >	1830.00	69.28	CMOS output (neg.)	

Table 10: OTIS1.2Pad Description — contd.

Number	Name	X [μm]	Y [μm]	Type	Description
159	DataValid	1710.00	69.28	CMOS output (pos.)	Data Valid
160	notDataValid	1590.00	69.28	CMOS output (neg.)	
161	gnd	1470.00	69.28	input	negative digital supply
162	gnd	1350.00	69.28	input	negative digital supply
163	vdd_digital	1230.00	69.28	input	positive digital supply
164	vdd_digital	1110.00	69.28	input	positive digital supply
165	DLLReset	990.00	69.28	CMOS input (pull up)	DLL Reset
166	BXReset	870.00	69.28	LVDS input (pos.)	BX Counter Reset
167	notBXReset	750.00	69.28	LVDS input (neg.)	
168	EVReset	630.00	69.28	LVDS input (pos.)	Event Counter Reset
169	notEVReset	510.00	69.28	LVDS input (neg.)	

D OTIS1.3 Pad Layout and Description

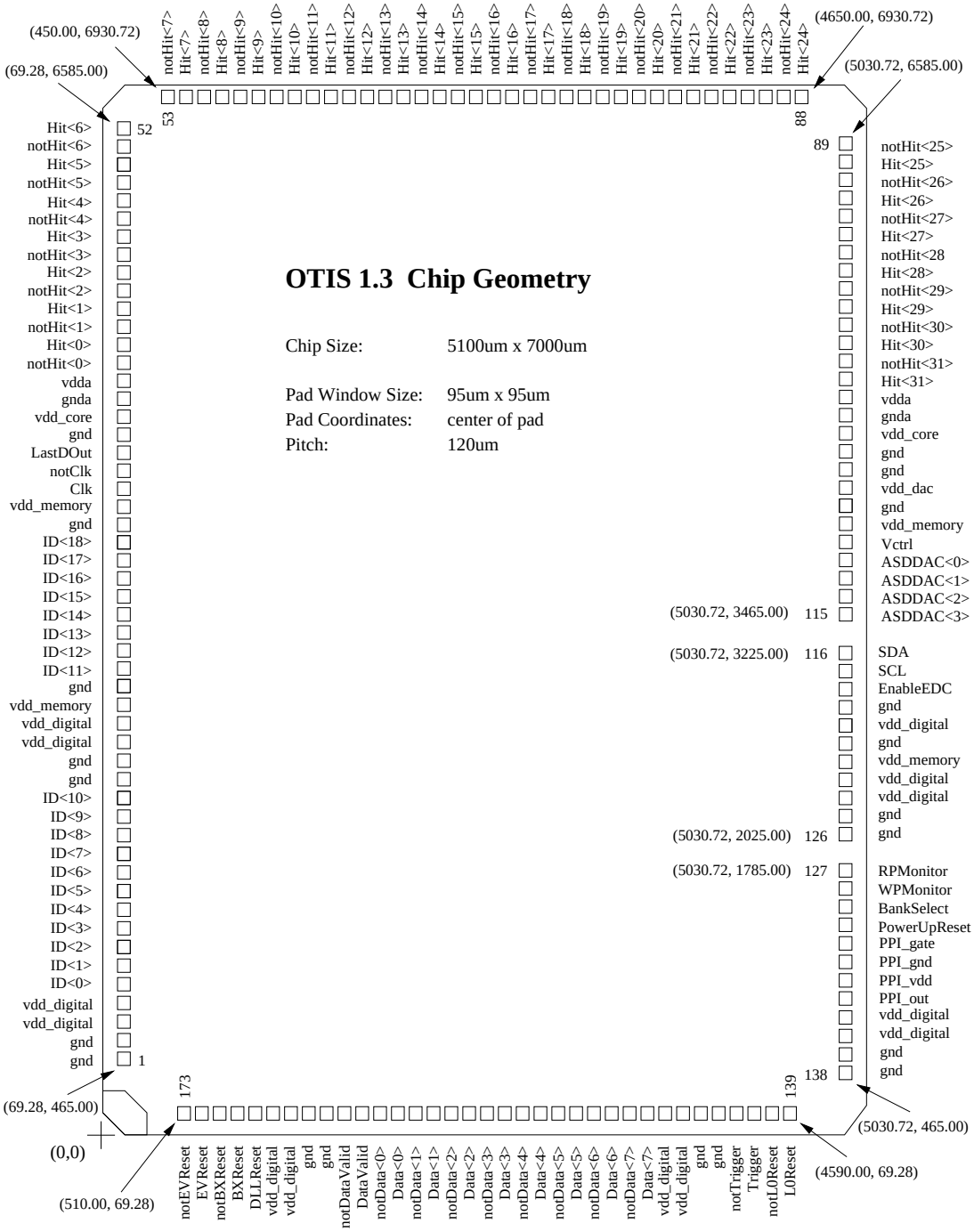

Figure 25: OTIS1.3 Pad Layout

Table 11: OTIS1.3 Pad Description

No.	Name	X [μm]	Y [μm]	Type	Description
1	gnd	69.28	465.00	input	neg. digital supply
2	gnd	69.28	485.00	input	neg. digital supply
3	vdd_digital	69.28	705.00	input	pos. digital supply
4	vdd_digital	69.28	825.00	input	pos. digital supply
5	ID< 0 >	69.28	945.00	CMOS input (pull down)	TDC ID (Bit no. 0)
6	ID< 1 >	69.28	1065.00	CMOS input (pull down)	TDC ID (Bit no. 1)
7	ID< 2 >	69.28	1185.00	CMOS input (pull down)	TDC ID (Bit no. 2)
8	ID< 3 >	69.28	1305.00	CMOS input (pull down)	TDC ID (Bit no. 3)
9	ID< 4 >	69.28	1425.00	CMOS input (pull down)	TDC ID (Bit no. 4)
10	ID< 5 >	69.28	1545.00	CMOS input (pull down)	TDC ID (Bit no. 5)
11	ID< 6 >	69.28	1665.00	CMOS input (pull down)	TDC ID (Bit no. 6)
12	ID< 7 >	69.28	1785.00	CMOS input (pull down)	TDC ID (Bit no. 7)
13	ID< 8 >	69.28	1905.00	CMOS input (pull down)	TDC ID (Bit no. 8)
14	ID< 9 >	69.28	2025.00	CMOS input (pull down)	TDC ID (Bit no. 9)
15	ID< 10 >	69.28	2145.00	CMOS input (pull down)	TDC ID (Bit no. 10)
16	gnd	69.28	2265.00	input	neg. digital supply
17	gnd	69.28	2385.00	input	neg. digital supply
18	vdd_digital	69.28	2505.00	input	neg. digital supply
19	vdd_digital	69.28	2625.00	input	pos. digital supply
20	vdd_memory	69.28	2745.00	input	pos. memory supply
21	gnd	69.28	2865.00	input	neg. digital supply
22	ID< 11 >	69.28	2985.00	CMOS input (pull down)	TDC ID (Bit no. 11)
23	ID< 12 >	69.28	3105.00	CMOS input (pull down)	TDC ID (Bit no. 12)
24	ID< 13 >	69.28	3225.00	CMOS input (pull down)	TDC ID (Bit no. 13)
25	ID< 14 >	69.28	3345.00	CMOS input (pull down)	TDC ID (Bit no. 14)
26	ID< 15 >	69.28	3465.00	CMOS input (pull down)	TDC ID (Bit no. 15)
27	ID< 16 >	69.28	3585.00	CMOS input (pull down)	TDC ID (Bit no. 16)
28	ID< 17 >	69.28	3705.00	CMOS input (pull down)	TDC ID (Bit no. 17)
29	ID< 18 >	69.28	3825.00	CMOS input (pull down)	TDC ID (Bit no. 18)
30	gnd	69.28	3945.00	input	neg. digital supply
31	vdd_memory	69.28	4065.00	input	pos. memory supply
32	Clk	69.28	4185.00	LVDS input (pos.)	LHC Clock
33	notClk	69.28	4305.00	LVDS input (neg.)	
34	LastDOut	69.28	4425.00		
35	gnd	69.28	4545.00	input	neg. digital supply
36	vdd_core	69.28	4665.00	input	pos. TDC supply
37	gnda	69.28	4785.00	input	neg. DLL supply
38	vdda	69.28	4905.00	input	pos. DLL supply
39	notHit< 0 >	69.28	5025.00	LVDS input (neg.)	Hit Signal
40	Hit< 0 >	69.28	5145.00	LVDS input (pos.)	
41	notHit< 1 >	69.28	5265.00	LVDS input (neg.)	Hit Signal
42	Hit< 1 >	69.28	5385.00	LVDS input (pos.)	
43	notHit< 2 >	69.28	5505.00	LVDS input (neg.)	Hit Signal
44	Hit< 2 >	69.28	5625.00	LVDS input (pos.)	
45	notHit< 3 >	69.28	5745.00	LVDS input (neg.)	Hit Signal
46	Hit< 3 >	69.28	5865.00	LVDS input (pos.)	
47	notHit< 4 >	69.28	5985.00	LVDS input (neg.)	Hit Signal
48	Hit< 4 >	69.28	6105.00	LVDS input (pos.)	
49	notHit< 5 >	69.28	6225.00	LVDS input (neg.)	Hit Signal
50	Hit< 5 >	69.28	6345.00	LVDS input (pos.)	
51	notHit< 6 >	69.28	6465.00	LVDS input (neg.)	Hit Signal
52	Hit< 6 >	69.28	6585.00	LVDS input (pos.)	

Table 11: OTIS1.3 Pad Description — contd.

No.	Name	X [μm]	Y [μm]	Type	Description
53	notHit< 7 >	450.00	6930.72	LVDS input (neg.)	Hit Signal
54	Hit< 7 >	570.00	6930.72	LVDS input (pos.)	
55	notHit< 8 >	690.00	6930.72	LVDS input (neg.)	Hit Signal
56	Hit< 8 >	810.00	6930.72	LVDS input (pos.)	
57	notHit< 9 >	930.00	6930.72	LVDS input (neg.)	Hit Signal
58	Hit< 9 >	1050.00	6930.72	LVDS input (pos.)	
59	notHit< 10 >	1170.00	6930.72	LVDS input (neg.)	Hit Signal
60	Hit< 10 >	1290.00	6930.72	LVDS input (pos.)	
61	notHit< 11 >	1410.00	6930.72	LVDS input (neg.)	Hit Signal
62	Hit< 11 >	1530.00	6930.72	LVDS input (pos.)	
63	notHit< 12 >	1650.00	6930.72	LVDS input (neg.)	Hit Signal
64	Hit< 12 >	1770.00	6930.72	LVDS input (pos.)	
65	notHit< 13 >	1890.00	6930.72	LVDS input (neg.)	Hit Signal
66	Hit< 13 >	2010.00	6930.72	LVDS input (pos.)	
67	notHit< 14 >	2130.00	6930.72	LVDS input (neg.)	Hit Signal
68	Hit< 14 >	2250.00	6930.72	LVDS input (pos.)	
69	notHit< 15 >	2370.00	6930.72	LVDS input (neg.)	Hit Signal
70	Hit< 15 >	2490.00	6930.72	LVDS input (pos.)	
71	notHit< 16 >	2610.00	6930.72	LVDS input (neg.)	Hit Signal
72	Hit< 16 >	2730.00	6930.72	LVDS input (pos.)	
73	notHit< 17 >	2850.00	6930.72	LVDS input (neg.)	Hit Signal
74	Hit< 17 >	2970.00	6930.72	LVDS input (pos.)	
75	notHit< 18 >	3090.00	6930.72	LVDS input (neg.)	Hit Signal
76	Hit< 18 >	3210.00	6930.72	LVDS input (pos.)	
77	notHit< 19 >	3330.00	6930.72	LVDS input (neg.)	Hit Signal
78	Hit< 19 >	3450.00	6930.72	LVDS input (pos.)	
79	notHit< 20 >	3570.00	6930.72	LVDS input (neg.)	Hit Signal
80	Hit< 20 >	3690.00	6930.72	LVDS input (pos.)	
81	notHit< 21 >	3810.00	6930.72	LVDS input (neg.)	Hit Signal
82	Hit< 21 >	3930.00	6930.72	LVDS input (pos.)	
83	notHit< 22 >	4050.00	6930.72	LVDS input (neg.)	Hit Signal
84	Hit< 22 >	4170.00	6930.72	LVDS input (pos.)	
85	notHit< 23 >	4290.00	6930.72	LVDS input (neg.)	Hit Signal
86	Hit< 23 >	4410.00	6930.72	LVDS input (pos.)	
87	notHit< 24 >	4530.00	6930.72	LVDS input (neg.)	Hit Signal
88	Hit< 24 >	4650.00	6930.72	LVDS input (pos.)	
89	notHit< 25 >	5030.72	6585.00	LVDS input (neg.)	Hit Signal
90	Hit< 25 >	5030.72	6465.00	LVDS input (pos.)	
91	notHit< 26 >	5030.72	6345.00	LVDS input (neg.)	Hit Signal
92	Hit< 26 >	5030.72	6225.00	LVDS input (pos.)	
93	notHit< 27 >	5030.72	6105.00	LVDS input (neg.)	Hit Signal
94	Hit< 27 >	5030.72	5985.00	LVDS input (pos.)	
95	notHit< 28 >	5030.72	5865.00	LVDS input (neg.)	Hit Signal
96	Hit< 28 >	5030.72	5745.00	LVDS input (pos.)	
97	notHit< 29 >	5030.72	5625.00	LVDS input (neg.)	Hit Signal
98	Hit< 29 >	5030.72	5505.00	LVDS input (pos.)	
99	notHit< 30 >	5030.72	5385.00	LVDS input (neg.)	Hit Signal
100	Hit< 30 >	5030.72	5265.00	LVDS input (pos.)	
101	notHit< 31 >	5030.72	5145.00	LVDS input (neg.)	Hit Signal
102	Hit< 31 >	5030.72	5025.00	LVDS input (pos.)	
103	vdda	5030.72	4905.00	input	pos. DLL supply
104	gnda	5030.72	4785.00	input	neg. DLL supply
105	vdd_core	5030.72	4665.00	input	pos. TDC supply

Table 11: OTIS1.3 Pad Description — contd.

No.	Name	X [μm]	Y [μm]	Type	Description
106	gnd	5030.72	4545.00	input	neg. digital supply
107	gnd	5030.72	4425.00	input	neg. digital supply
108	vdd_DAC	5030.72	4305.00	input	pos. DAC supply
109	gnd	5030.72	4185.00	input	neg. digital supply
110	vdd_memory	5030.72	4065.00	input	pos. memory supply
111	VCtrl	5030.72	3945.00	analogue output	DLL control voltage
112	ASDDAC< 0 >	5030.72	3825.00	analogue output	Threshold voltage 0
113	ASDDAC< 1 >	5030.72	3705.00	analogue output	Threshold voltage 1
114	ASDDAC< 2 >	5030.72	3585.00	analogue output	Threshold voltage 2
115	ASDDAC< 3 >	5030.72	3465.00	analogue output	Threshold voltage 3
116	SDA	5030.72	3225.00	input/output (5V open drain)	I^2C Data
117	SCL	5030.72	3105.00	CMOS input (5V)	I^2C Clock
118	EnableEDC	5030.72	2985.00	CMOS input (pull down)	Enable I^2C EDC
119	gnd	5030.72	2865.00	input	neg. digital supply
120	vdd_digital	5030.72	2745.00	input	pos. digital supply
121	gnd	5030.72	2625.00	input	neg. digital supply
122	vdd_memory	5030.72	2505.00	input	pos. memory supply
123	vdd_digital	5030.72	2385.00	input	pos. digital supply
124	vdd_digital	5030.72	2265.00	input	pos. digital supply
125	gnd	5030.72	2145.00	input	neg. digital supply
126	gnd	5030.72	2025.00	input	neg. digital supply
127	RPMonitor	5030.72	1785.00	CMOS output	Read Pointer Wrap
128	WPMonitor	5030.72	1665.00	CMOS output	Write Pointer Wrap
129	BankSelect	5030.72	1545.00	CMOS input (pull down)	Bank Select
130	PowerUpReset	5030.72	1425.00	input	Power Up Reset
131	PPI_gate	5030.72	1305.00	CMOS input (pull down)	PPI Gate
132	PPI_gnd	5030.72	1185.00	input	neg. supply
133	PPI_vdd	5030.72	1064.00	input	pos. supply
134	PPI_out	5030.72	945.00	CMOS output	PPI Out
135	vdd_digital	5030.72	825.00	input	pos. digital supply
136	vdd_digital	5030.72	705.00	input	pos. digital supply
137	gnd	5030.72	585.00	input	neg. digital supply
138	gnd	5030.72	465.00	input	neg. digital supply
139	L0Reset	4590.00	69.28	LVDS input (pos.)	L0Reset
140	notL0Reset	4470.00	69.28	LVDS input (neg.)	
141	Trigger	4350.00	69.28	LVDS input (pos.)	L0Trigger
142	notTrigger	4230.00	69.28	LVDS input (neg.)	
143	gnd	4110.00	69.28	input	neg. digital supply
144	gnd	3990.00	69.28	input	neg. digital supply
145	vdd_digital	3870.00	69.28	input	pos. digital supply
146	vdd_digital	3750.00	69.28	input	pos. digital supply
147	Data< 7 >	3630.00	69.28	CMOS output (pos.)	data output (MSB)
148	notData< 7 >	3510.00	69.28	CMOS output (neg.)	
149	Data< 6 >	3390.00	69.28	CMOS output (pos.)	data output
150	notData< 6 >	3270.00	69.28	CMOS output (neg.)	
151	Data< 5 >	3150.00	69.28	CMOS output (pos.)	data output
152	notData< 5 >	3030.00	69.28	CMOS output (neg.)	
153	Data< 4 >	2910.00	69.28	CMOS output (pos.)	data output
154	notData< 4 >	2790.00	69.28	CMOS output (neg.)	
155	Data< 3 >	2670.00	69.28	CMOS output (pos.)	data output
156	notData< 3 >	2550.00	69.28	CMOS output (neg.)	

Table 11: OTIS1.3 Pad Description — contd.

No.	Name	X [μm]	Y [μm]	Type	Description
157	Data< 2 >	2430.00	69.28	CMOS output (pos.)	data output
158	notData< 2 >	2310.00	69.28	CMOS output (neg.)	
159	Data< 1 >	2190.00	69.28	CMOS output (pos.)	data output
160	notData< 1 >	2070.00	69.28	CMOS output (neg.)	
161	Data< 0 >	1950.00	69.28	CMOS output (pos.)	data output (LSB)
162	notData< 0 >	1830.00	69.28	CMOS output (neg.)	
163	DataValid	1710.00	69.28	CMOS output (pos.)	Data Valid
164	notDataValid	1590.00	69.28	CMOS output (neg.)	
165	gnd	1470.00	69.28	input	neg. digital supply
166	gnd	1350.00	69.28	input	neg. digital supply
167	vdd_digital	1230.00	69.28	input	pos. digital supply
168	vdd_digital	1110.00	69.28	input	pos. digital supply
169	DLLReset	990.00	69.28	CMOS input (pull up)	DLL Reset
170	BXReset	870.00	69.28	LVDS input (pos.)	BX Counter Reset
171	notBXReset	750.00	69.28	LVDS input (neg.)	
172	EVReset	630.00	69.28	LVDS input (pos.)	Event Counter Reset
173	notEVReset	510.00	69.28	LVDS input (neg.)	

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