Time Calibration of the LHCb muon System

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Abstract

The LHCb muon System consists of about 122,000 front-end channels. It plays a basic role in the first trigger level. The trigger requires 95% efficiency in muon tracks detection. It is then necessary to reach a system time alignment at the level of about 2 ns. This alignment must be monitored against possible fluctuations due to changes in the detector operating conditions. We describe the custom instrumentation implemented at system level for time calibration, the strategy adopted, the procedure to be followed both for system alignment and monitoring, the control program realized for this purpose. We also illustrate first results obtained during the detector commissioning in the LHCb pit.

I. Introduction

LHCb is currently under commissioning at the LHC. It is designed to study CP violation and rare decays of the B meson and it will run with a bunch crossing frequency of 40 MHz [1] [2].

The LHCb muon System has a crucial role in the first trigger level, named Level zero (L0), which works with an accept rate of 40 MHz and an average output rate of 1 MHz. The muon System has to provide a hight p_T muon trigger with the 95% of efficiency already at the L0 trigger.

The muon System is organized in 5 stations, with a total of 1380 detectors, which are realized by means of Multi-Wire-Proportional-Chambers and Gas-Electron- Multipliers and consists of about 122,000 front-end channels. Each front-end channel gives a space-point binary information correlated to the bunch crossing time. There are 20 different types of detectors and the time distributions are relatively wide, with an rms of about 4 ns.

High efficiency is necessary both at detector and front-end level to satisfy the trigger requirement of 5 hits (one per station) with an overall efficiency of 95%. This corresponds to a single front-end channel detection efficiency of 99% within a time window of 20 ns and poses the problem of an accurate time calibration of the whole detector.

II. The Muon System

The 122,000 front-end channels are grouped in about 8,000 front-end boards, named CARDIAC. Each CARDIAC has in input 16 front-end channels and contains two ASICs:

- the CARIOCA (Cern And RIO Current Amplifier), which is an Amplifier Shaper Discriminator (ASD);
- the DIALOG (DIagnostic time Adjustment and LOGics), which has tools for time alignment and monitoring. The DIALOG layout and internal scheme are shown in Figure 1 and 2 respectively.

The DIALOG has to be configured and can be read-back through the Service Board (SB) using a control program developed in the PVSS environment. In the whole system there are 156 Service Boards.

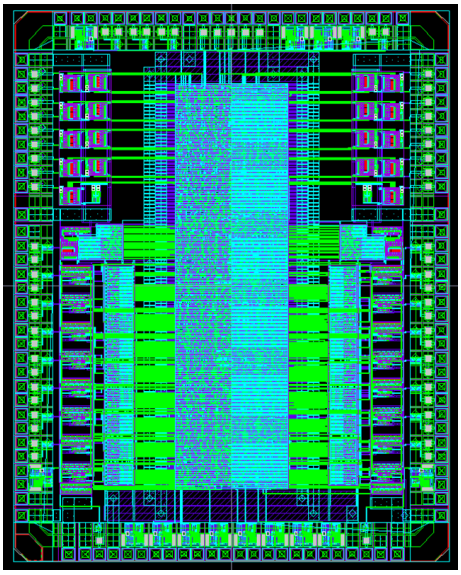

Figure 1: DIALOG layout.

The signals coming out the CARDIAC boards are to be readout from the Off Detector Electronics (ODE) boards (see Figure 3). The ODE board is synchronous with the LHC master clock and has the role of:

- collect data from front-end;
- send data to the Level zero μ-trigger;
- wait the Level zero μ-trigger response;
- send data to the Data Acquisition System (DAQ) in case of trigger affirmative answer.

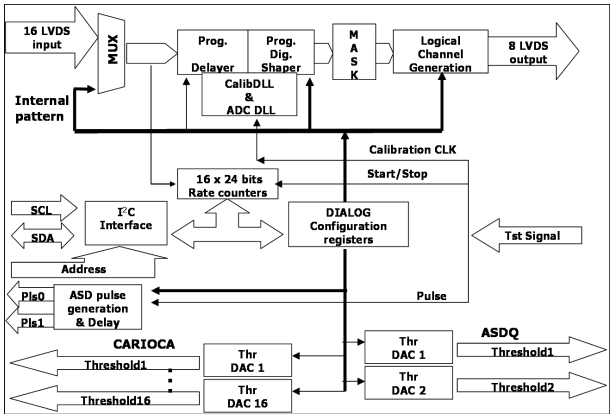

Figure 2: DIALOG internal scheme.

The muon trigger processes the binary information coming from the muon detectors according to a pipelined architecture, starting to process a new event every 25 ns (bunch-crossing period). The muon trigger expects data being tagged with an identifier of the specific bunch-crossing they originate from. However, considering the width of time distributions due to the intrinsic detector resolution, in order to reach the requested trigger efficiency, it is necessary to calibrate the internal system delays at the level of about $2 \div 3$ ns. In each ODE board there are 24 SYNCs ASIC, which measure the arrival time of front-end signals with 1.6 ns of resolution, and give them the correct bunch-crossing number. In the muon System there are 152 ODE bards.

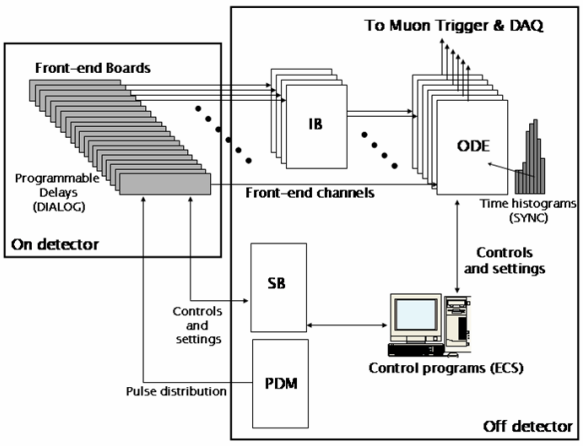

Figure 3: Muon System electronics block scheme.

The Level zero μ-trigger algorithm uses a granularity that is coarser than needed for the functionality of the chambers. Therefore the 122,000 front-end channels are logically combined to give 26,000 readout channels used by the trigger. The logical combination starts on the CARDIAC front-end board, on the DIALOG chip which has 16 input channels and can have from 2 to 8 output channels. The logical combination of channels coming from DIALOG is completed on the Intermediate Board (IB) wherever the readout channels are composed of fronted-channels coming from different CARDIAC boards. In the whole system there are 168 IB boards. The length of the LVDS cables in the electronic chains (from CARDIAC to ODE) can vary from about 10 m to 20 m, and there are about 8,000 cables of different lengths. As a consequence, the muon system is characterized by a complex connectivity. Indeed, there are 12 different types of electronic chain connections, which differ both for the number of front-end channels involved and for their logical combination to produce the readout channels. Each type of logical combination is composed of 1 ODE board, can have from 0 to 3 IBs, from 24 to 72 CARDIAC boards and can involve up to 1152 front-end channels.

An useful system feature is the Pulse System. It is possible to pulse the front-end boards sending a synchronous pulse in a bunch crossing of the LHCb orbit and with a specific phase with respect to the LHC master clock. Both the bunch crossing number and the pulse phase are programmable by the user. The pulse is given to the front-end at the input of the amplifiers. Therefore the generated signal is not affected by the chamber time response. The pulse is generated by the Pulse Distribution Module (PDM) board [3], and is controlled by the same PVSS control program used to configure DIALOGs [4] and SYNCs [5].

III. The Time Calibration

Starting from the above requirements, the muon System has been conceived and realized containing specific tools for time calibration at the channel level. Several reasons cause the system channels to be naturally misaligned in time: time of flight of particles through detectors, different cable lengths, different number of electronics stages to be crossed. Therefore, before any synchronization, signals generated in the same bunch crossing but coming from different front-end channels have different absolute delay, which can be more than one bunch crossing.

The basic strategy for system time calibration is to measure the hit time of arrival at the ODE board level, just before the hits are dispatched to the muon trigger. The delay is considered as a sum of two contributions:

- the Fine Delay, which gives the fraction of the total time delay in terms of the phase within a bunch crossing period;
- the Coarse Delay, which gives the fraction of the total time delay in terms of an integer number of bunch crossing periods.

Measuring and compensating the Fine Delay is needed because the chamber time distribution must be centered inside the bunch-crossing period to reach the requested detector efficiency. On the other hand, the Coarse Delay compensation ensure that signals sent to the level zero μ-trigger

have been tagged with the number of the bunch-crossing which they belong to.

IV. The Instruments

Inside the SYNC chip, placed on the ODE board, time spectra can be built on each input channel. SYNC is a custom chip, containing eight Time-to-Digital-Converters (TDC), one per channel, with a time resolution of 1.5 ns in a 25 ns period.

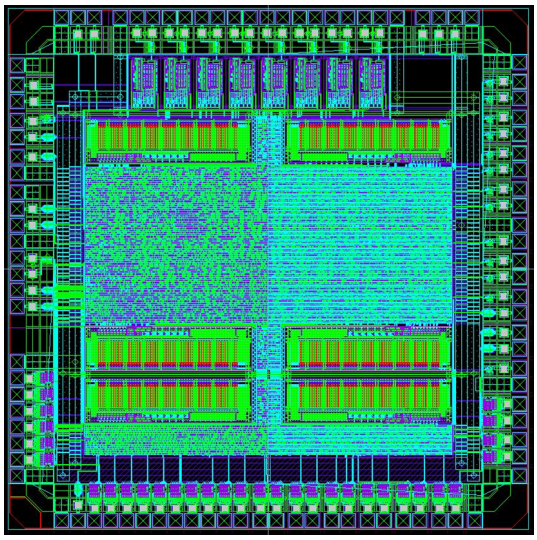

Figure 4: SYNC layout.

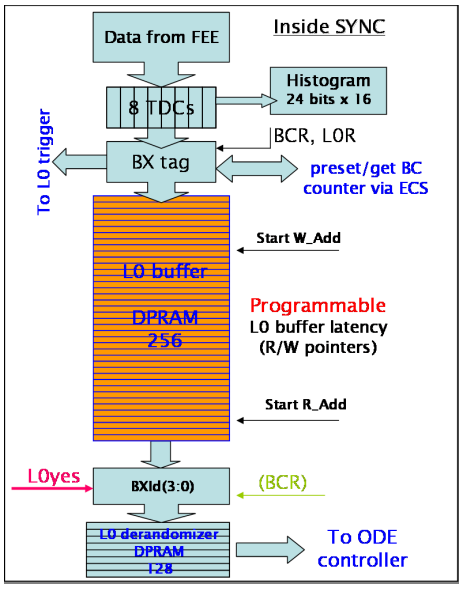

Figure 5: SYNC internal scheme.

The SYNC layout and internal scheme are shown in Figure 4 and 5 respectively. Two kinds of time spectra can be built: a fine-time histogram to measure the Fine Delay, and a coarse-time histogram to measure the Coarse Delay. The first histogram type has a range of 25 ns and bins of 1.5 ns, while the second ones has a range of 16 bunch-crossings and bins of 25 ns.

The measured Fine Delay is compensated at the beginning of the electronic chain, for each front-end channel individually, with programmable delays, placed on the DIALOG chip, which allow moving time in 32 steps of 1.6 ns each. The delay to be applied is codified into a word to be written on DIALOG by a PVSS control program, for each input channel. Therefore 16 codes have to been calculated and configured for each DIALOG chip.

The measured Coarse Delay is compensated on SYNC. Different input readout channels of the same SYNC can be time aligned acting on 3 pipelined steps, of 25 ns each, which are programmable on a channel by channel basis. The time alignment of different SYNCs is done using the SYNC chip bunch crossing counter, which allow moving time in steps of 25 ns in a range of 7 clock cycles.

V. The Procedure

There are basically two strategies for the muon System synchronization. The first one is based on the Nominal Beam Conditions. Using DIALOG and SYNC facilities it is possible to measure and compensate the total time delay in a single step, without using any triggered data [6]. However, this method is effective only at nominal beam luminosity, especially considering the low occupancies on the external regions of the muon detector. During the low luminosity phase of the LHC startup, another strategy has been developed, exploiting the Pulse System. This strategy is organized in two steps described in the following subsections.

A. Relative Alignment

In the first part of the procedure a "relative" alignment is reached. The term "relative" is in the sense that all readout channels of one ODE board can be time-aligned to the "same" bunch crossing number, which is related to the bunch crossing generating the signals detected by the TDCs on the SYNC chips. In case of pulsing, the chambers time response and the particle time of flight are not included in the total delay calculation. Therefore for a given front-end channel, the total delay that can be calculated and compensated using the pulse system is different from the total delay with respect to the chamber time distribution given by particles generated in the LHCb interaction point. Indeed there is a time offset between the two alignment, and the "right" bunch crossing has still to be measured and compensated.

As seen before, the readout channels are given by a logical combination of front-end channels, according with one of the 12 types of electronics chain connection. A single readout channel is formed from 2 to 48 front-end channels.

To align the readout channels with respect to the

"same" bunch crossing, both the fine and the coarse histograms must be acquired and analyzed for each of the 122,000 front-end channels. To do that, it is necessary to mask all front-end channels, which compose a single readout channel, and to enable them once at a time. Indeed it is not possible to make the time measurements directly on the readout channel, because the corresponding front-end channels are not yet aligned at this moment.

Once the fine and the coarse time measurements of all the front-end channels connected to one ODE board are done, the code to be set in the corresponding DIALOGs and SYNCs registers are calculated and the devices configured. At this point all the readout channels are aligned to the "same" bunch-crossing. What is still to do is to find the offset between the "same" and the "right" bunch crossing.

This first step of the procedure does not use any triggered data and all is done at the PVSS control program level.

One of the advantages to reach a relative alignment is to time-equalize the different front-end channels which compose a single readout channel. The next step can thus act directly on readout channels without masking the single front-end channels which compose it.

B. Absolute Alignment

The second part of the procedure allows reaching an "absolute" time alignment. This second part is based on the analysis of data acquired by means of calibration triggers. The time offset between the "same" and "right" bunch crossing number is found. A beam is finally required to include the chamber responses and the particle time of flights. The fine and coarse time histograms are filled with triggered data and acquired for all the read-out channels in parallel, following all the nominal acquisition chain till the DAQ. The DIALOG and SYNC devices are configured by means of the PVSS control program, while both the histograms acquisition and the offset parameter calculation are done by an analysis package to be included in the LHCb software framework. The muon System electronics is currently under commissioning. Before starting the first synchronization phase a test of system connectivity from Chambers to ODE was done. Due to complexity of connections, it cannot be pursued manually and a dedicated software has being developed in the PVSS environment.

The test is performed on one ODE board and its associated connectivity tree: the IB boards and all the front-end channels connected to them. Each ODE board is independent of the others and has one of the 12 types of electronic chain connection maps, which are being integrated in the PVSS control program.

First of all, all front-end channels are masked. Low thresholds for the CARIOCA discriminators are set on DIALOGs configuration registers, because the connectivity verification is done checking the flat distribution of the noise signals. Than, to test every single connection, only one front-end channel at a time is enabled on DIALOGs and the fine time histogram is analyzed for each readout channel of all the 24 SYNCs of the ODE board under test. The histogram analysis checks that the only one front-end channel enabled is seen from the right SYNC (chip and readout channel), while all the other SYNCs do not see anything. Half of system connectivity has been already successfully tested.

VI. Conclusions

The muon system is characterized by a large number or front-end channels, which are logically combined before readout, with complex connectivity maps, varying from region to region. Dedicated full custom ASICs, named DIALOG and SYNC, were developed as instruments for time calibration and monitoring.

The muon System electronics is currently under commissioning and half of the system connectivity has been successfully tested by means of an automatic control program developed in the PVSS environment.

The Time Alignment Procedure of the muon System can be started even without the beam using the Pulse System. The system commissioning will proceed the relative and absolute time alignment of the system.

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