Status of the ATLAS Pixel Detector

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Abstract

The pixel detector is a high precision silicon tracking detector located closest to the ATLAS interaction point. It provides crucial pattern recognition information and largely determines the ability for ATLAS to precisely track particle trajectories and find secondary vertices. This paper describes the design requirements, the components and the readout architecture of the pixel detector. It also describes the integration, testing and recent installation of the pixel detector inside the ATLAS detector.

I. Introduction

The *A Toroidal LHC ApparatuS* (ATLAS) is one of the four detector located around the Large Hadron Collider (LHC) ring. The LHC provides proton-proton collisions with a center-of-mass of 14 TeV and a bunch-crossing rate of 25 ns. ATLAS is a multi-purpose experiment that aims to explore the energy frontier of particle physics. It is made of successive detector layers, starting from the interaction points, of inner tracking detectors immersed in a 2T solenoidal magnetic field, liquid argon electromagnetic calorimetry, hadronic calorimetry and muon detectors immersed in a 4T toroidal magnetic field.

The inner detector is successively composed of a silicon pixel detector, a silicon strip detector (the Semi-Conductor Tracker (SCT)) and the Transition Radiation Tracker (TRT). The design requirements for the innermost layer of the inner detector are largely driven by the hostile LHC environment. We expect a total irradiation of 10^{15} neq/cm^2 by the end of the lifetime of the pixel detector. The pixel detector technology is well-suited for that purpose since it is naturally radiation hard. Indeed it results in lower leakage current per channel and has a reduced capacitance with respect to silicon strips.

A second constraint is the rapid LHC bunch crossing rate of 25 ns. It motivates the use of sensor made of n^+ pixels on a n-bulk that produces a large and fast electron pulse to can be detected in a timescale of less than a bunch crossing. Furthermore, this requirement forced the design of a fast on-detector electronics with buffering capacity.

Finally, the proton-proton collisions result in a very large amount of charged particles. We expect 500-1000 tracks per event inside the pixel detector acceptance at the LHC design luminosity of 10^{34}cm^{-2}s^{-1}. Figure 1 iluustrates the challenge by showing an event containing a Higgs boson decaying to a pair of b-quarks without pile-up events (left) and with pile-up events at design luminosity (right). Only tracks with a pseudorapidity[1] $|\eta| < 0.7$ are illustrated. The pixel detector, with a pitch size of 50$\times$ 400 μm, achieves an occupancy per pixel of 10^{-4} in this environment and is thus crucial for pattern recognition. For instance, pixel hits are used as seeds to the default ATLAS tracking algorithm.

The pixel detector is crucial to an other aspect of the ATLAS physics program. Since it is located close to the beamline (the first layer is at a radius of 5 cm) and possesses a very good impact parameter resolution (12 μm in r-ϕ and 70 μm in the z directions), it determines the capability of ATLAS to detect secondary vertices resulting from long-lived particles like B-hadrons contained inside b-jets.

In this document we first present an overview of the pixel detector layout. We then describe the basic building blocks of the detector: the modules, which include the sensor, the front-end chip and a controller chip. The pixel package and off-detector electronics are introducted in Sec. IV.. We then discuss recent achievements of the pixel project, i.e. the system test and the pixel package integration and installation in the ATLAS cavern. We finally present the future plans of the project.

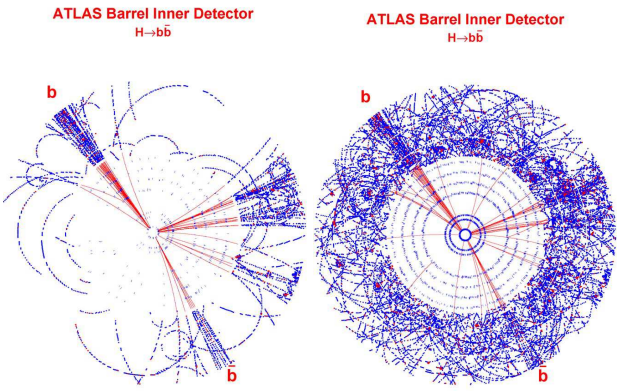

Figure 1: An event containing a Higgs boson decaying to $b\bar{b}$ without pile-up (left) and with pile-up at design luminosity (right). Only tracks with a pseudorapidity $\eta < 0.7$ are illustrated.

II. Pixel Detector Overview

The general layout of the pixel detector is illustrated in Fig. 2. The detector is made of three cylincrical layers in the barrel region (covering $|\eta| < 1.9$) and three disks on each side of the end-cap region (covering $1.9 < |\eta| < 2.5$). The three barrel layers, the B-layer, L1 and L2, are located at radii of 5, 9 and 12 cm, respectively, from the interaction point. The detector volume is 1.6m in length and 0.2m in radius and the required

[1] Pseudorapidity is defi ned as $\eta = -\ln\tan(\theta/2)$.

total surface of silicon is 1.8m^2. The total amount of material is about 10% X_0 in the transverse direction ($\eta = 0$).

The basic building blocks of the pixel detector are the modules that are described in Sec. III.. There are 1744 in total in the detector: 1456 and 288 in the barrel and end-cap regions, respectively. The total amount of power dissipated by the module electonics is 10 kW. An evaporative cooling system (with coolant C_3F_8) is employed to operate the detector at a temperature $T \approx 0°$. The modules are cooled through their support structure that is thermally conductive.

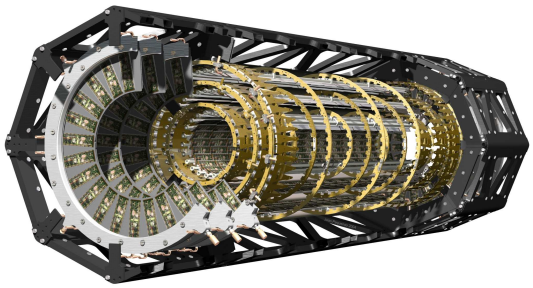

Figure 2: A simulated picture of the ATLAS pixel detector. Only shown on the picture are the modules and support structure.

III. Module Description

The pixel module covers a surface of 2.2 cm $\times$ 6 cm. The main components are the silicon sensor, 16 front-end chips, the controller chip and the flex printed circuit board as illustrated in Fig. 3.

The silicon sensors are made of n^+ pixels on n substrate and have a thickness of approximately 280 μm. A cross-section of the sensor can be found in Fig. 4. A bump-bonding technique is used to connect the sensors to the 16 front-end chips of the module with a pixel size of 50 μm $\times$ 400 μm in the $R - \phi \times z$ directions. The pixels are arranged in column pairs: there are 18 columns and 160 rows of pixels per front-end, for a total of 2880 pixels. In order to improve the radiation-hardness of the detector, the silicon sensors have been oxygenated [1].

The front-end chips [2] are connected through aluminium wire bonds to a flex hybrid that is glued on the underside of the modules. A module controller chip [3] is connected to the front-end chips through the flex printed circuit board connections. A Negative Temperature Coefficient (NTC) resistor is located on each module. A micro-cable brings the low voltage (LV), high voltage (HV), NTC information and data-in and -out of the module to the outside world. The front-end and controller chips are described in more details in the next section.

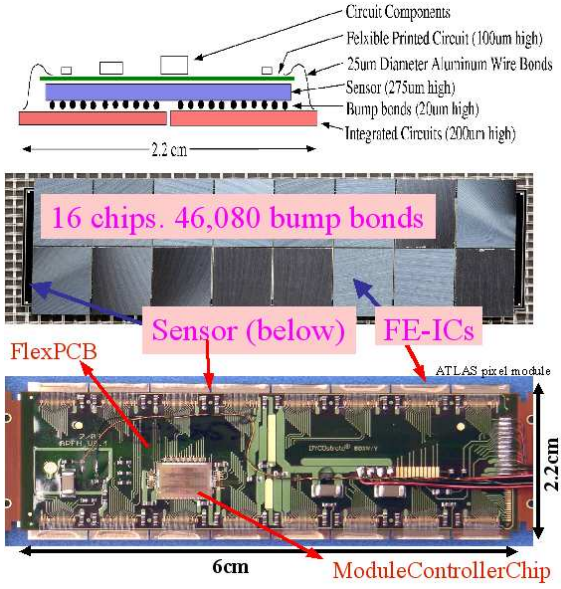

Figure 3: A sketch of the pixel detector hybrid module. The top illustration shows a cross-section of the module. The middle and bottom illustration shows the "back", i.e. where the front-end chips are visible, and the "top" of a module, i.e. the side where the flex printed circuit board and controller chip are visible.

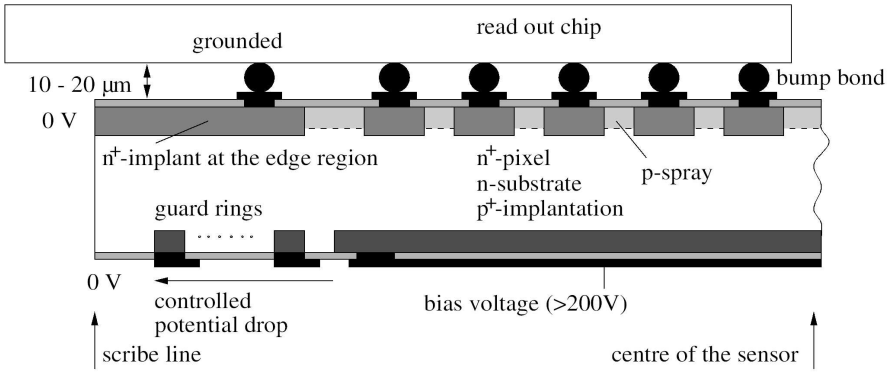

Figure 4: A sketch of the cross-section of the ATLAS pixel detector sensor. The pixels are n^+ and the bulk forms a n-p diode with a p^+ backside. Guard rings are located at the edge of the sensor to allow the HV to drop to 0V in that region.

A. Readout Architecture

Each pixel is connected to a charge sensitive feedback preamplifier that provides leakage current tolerance up to ≈100 nA, which is expected after end-of-lifetime sensor irradiation. The next step of the analog circuitry is a discriminator with an adjustable threshold usually operated at ≈4 ke. The charge is collected at this threshold in less than 25 ns to allow unique bunch crossing identification of the hit. The signal is digitized by calculating the Time over Threshold (ToT), which is proportional to the amplitude of the signal, using a 40 MHz timestamp (i.e. corresponding to the ATLAS clock speed). A typical signal remains over threshold for about 30 bunch crossings. A 14-bits pixel-level control logic can be used to tune the threshold and ToT of a given pixel. Each pixel circuitry is equipped with a charge injection mechanism to tune and measure those parameters. There also exists a front-end-level control logic to tune more globally the threshold and ToT and the charge injection circuit parameters.

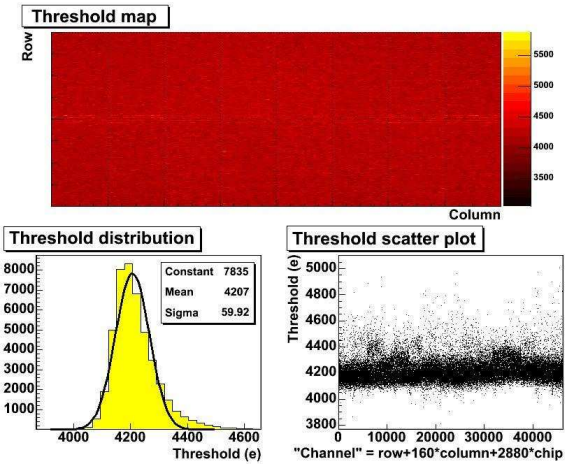

Figure 5: Results of a threshold scan after threshold tuning: the maps of tuned threshold of one module (top), the threshold distribution (bottom left) and the threshold as a function of the pixel number.

Figure 5 shows the results of a threshold scan after tuning the discriminators threshold for one module. A threshold scan is performed by sending several strobes of injected charge of different values. Such a technique can be used to determine the threshold (defined as the charge value at which a hit is registered 50% of the time) and the noise level. The bottom left plot, which shows the threshold distribution, demonstrates that a low threshold dispersion of about 60 e is achievable. The noise level (not shown) is about 200 e. These measured parameters are in good agreement with the design requirements of the pixel detector.

Figure 6 shows the map of ToT after tuning for a given injected charge (top) and the relationship between injected charge and ToT (bottom). An approximate linear dependence is observed between the injected charge and ToT after proper tuning.

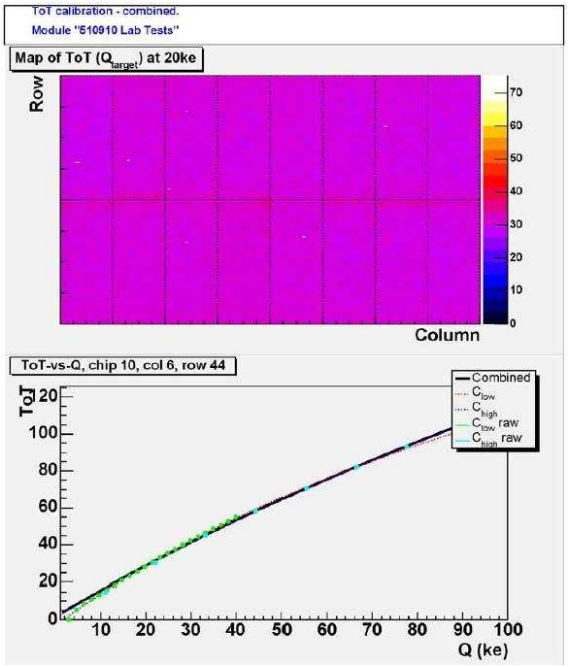

Figure 6: A map of the ToT for an injected charge of 20 ke (top) and the ToT as a function of injected charge (bottom).

The pixel hit, defined as the pixel address and the timing of the leading and trailing edges, is then transferred as soon as the trailing edge occurs through a shared bus structure in a pixel column pairs. This bus operates at a transfer rate of 20 MHz. The End-of-Column (EoC) region of the front-end chip receives the hits and stores them in a 64-hits buffer for each column pair (one buffer for each five pixel). The length of this buffer as been shown to be sufficient to operate at full luminosity with the ATLAS level 1 trigger latency of 3.2 μs.

The coincidence of the leading edge timing and the level 1 trigger, which is transferred from the off-detector electronics to the front-end chips, is performed in this buffer. The rejected hits are erased immediately. The accepted hits corresponding to the same bunch crossing are transferred to the controller chip through an output serial link. The controller chip collects the data from the 16 front-end chips, performs some initial event building and sends the data off-detector for further processing. We note that the required voltage to operate the analog and digital circuitry of a module is 1.6 V and 2.0 V, respectively.

IV. Pixel Package and Off-Detector Electronics

The pixel package is composed of the pixel detector, eight service panels, the ATLAS beampipe and the Beam Pipe and Support Structure (BPSS). The pixel package, illustrated in Fig. 7, is installed as a single entity in the ATLAS cavern as discussed in Sec.VII. The purpose of the service panels is to reduce the amount of material inside the inner detector tracking volume by bringing the pixel electrical, optical and cooling services out of the inner detector region (which is about 7m long).

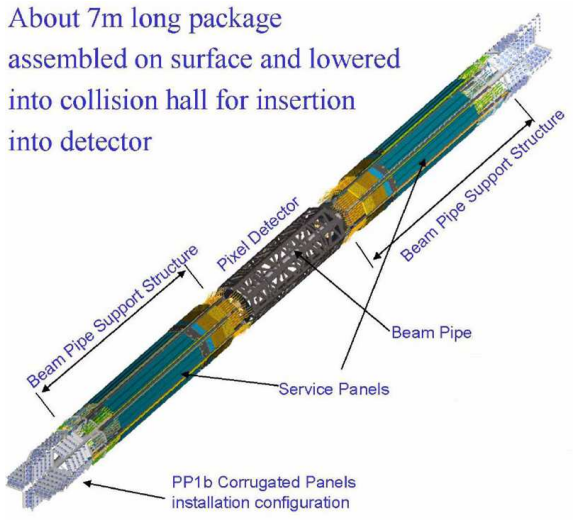

Figure 7: A sketch of the pixel package.

The module micro-cables connect to the service panels patch panel (PP0). The module electrical signal is then transferred to the only active part of the service panel, the optoboards. The optoboards are composed of a receiver, i.e. an 8-way Si PiN diode array, that converts the optical data coming from the off-detector electronics (module configuration and commands, clock and Level 1 trigger) into an electrical (LVDS) signal. They also include a transmitter, i.e. an 8-way VCSEL array, that performs the electrical to optical signal conversion. The transmitter operates at rates of 40, 80 and 160 Mbit/s for the L2, disks and L1, and B-layer modules, respectively. These readout speed are driven by the hit occupancy in each part of the pixel detector. Each optoboard serves six or seven modules. The optoboards are described in more details elsewhere [4].

The optical signal is transferred via optical fibers to off-detector electronics located in VME crates. A Back-of-Crate card, described in details in [5], performs the off-detector optical interface. The data is then transferred to Read-Out Drivers (ROD) performs further event building and data formatting and have a calibration capability. The ROD's are connected to the ATLAS data acquisition system through a 1.6 Gbit/s optical link.

The pixel detector system also include off-detector services and associated slow control software that are described in details elsewhere [6].

V. System Test

During the Fall of 2006, one of the pixel end-cap was used in a commissioning test of the pixel detector and services referred to as the "10% system test". It was performed in parallel to the final integration of the remaining parts of the pixel detector. The setup was located on the surface. The end-cap was positioned between scintillators, that provided a trigger for cosmics rays, and was attached to a prototype service panel. The service panel was itself attached to a cooling system and electrical and optical services very close to the final version. On top of commissioning the pixel services, the system test successfully tested the performance of the detector using random and cosmic triggers. A more complete summary of the system test can be found in [7].

VI. Pixel Package Integration and Connectivity Test

After the completion of the pixel detector assembly in February of 2007, the integration of the detector with the service panels, the beampipe and BPSS was performed. The service panels were installed one at a time on the BPSS. This was followed by the cooling connections between the detector and the service panel. Leak and pressurization checks were performed to verify the cooling connections. The next step was the connection of the module micro-cables to the service panels. A picture of the completed pixel package is shown in Fig. 8

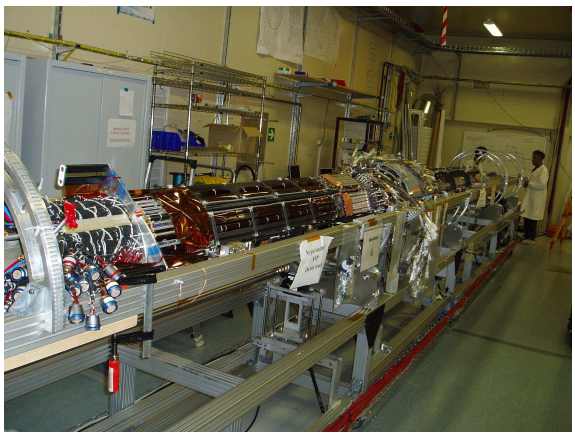

Figure 8: A picture of the completed pixel package.

The integration of a single service panel was followed by a connectivity test. This was performed using the full readout chain and employed the same services as the system test. Its general goal was to make sure that the full pixel package was ready for the installation in the pit scheduled for June of 2007. More specifically the module micro-cable mapping was checked, the environmental and electrical connections were exercised and the optical connections were tuned. Note that this test was performed without cooling to facilitate the pixel package integration. An iteration on the active part of the detector was thus required.

Only three module failures were observed during the connectivity test and were due to different sources (HV micro-cable failure, optoboard PiN diode failure, LV short on one module). Note also that this was the first time the full pixel detector was operated using the full readout chain. The connectivity test thus consisted partly in a commissioning activity for the optolink communication system. This aspect of the connectivity test was a success since we demonstrated the capability to operate every

module through the full optical readout chain[2].

VII. Installation in the ATLAS Detector

The pixel package was then inserted in a "Dummy" Support Tube (DST) to be transported and lowered inside the ATLAS cavern. The diameter of the DST is intentionnally the same as the Pixel Support Tube (PST) in which the pixel package in inserted inside the ATLAS detector. The insertion in the DST thus provided an important test for the insertion of the pixel detector inside ATLAS.

The pixel package was then lowered inside the DST through a shaft inside the ATLAS cavern and was laid down on a support structure located at the inner detector height. The pixel package was then gradually pulled inside the PST using a winch. Figure 9 shows a picture of this process.

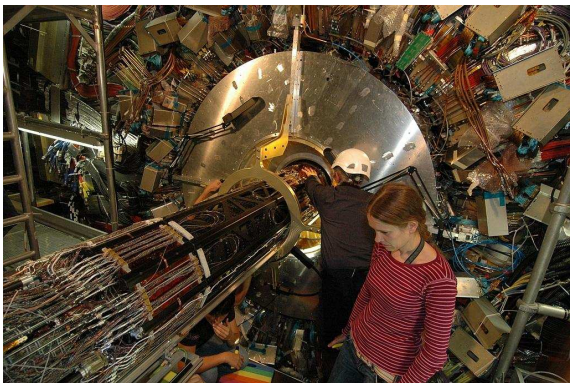

Figure 9: A picture of the installation of the pixel package inside ATLAS.

After the installation was completed on June 28, a quick test of the HV, LV and NTC connections was performed to check the status of the pixel detector and service panels. One open module NTC connection and 11 open module HV connections have been found in the whole detector. The open NTC connection is not serious since one module is thermally coupled through the support structure to at least 5 modules in the pixel detector. The 11 HV open connections are all repairable. In conclusion, it appears the installation did not damage seriously the pixel package.

VIII. Summary and Future Plans

On June 28, 2007, the pixel detector has been the last full detector to be installed in the ATLAS detector. The data from the connectivity test combined with the detailed production data suggests that 99.6% of the detector is currently operational (0.2% due to module/optoboard-level failures, 0.2% due to pixel-level failures). The next step in the project is the connection of the pixel package with the electrical and optical services. This is expected to start only about mid-November of 2007. Indeed the pixel services interfere with the access to the SCT, thus requiring the sign-off of the SCT connections and cooling to be performed first. The connection of the pixel detector is expected to continue until around January 2008. This should be followed by a period of commissioning of the cooling system as well as an incremental operation of the pixel detector. This activity should be followed during the spring by a full-scale commissioning of the pixel detector using cosmic rays data followed by LHC collisions data.

References

[1] ROSE Collaboration, Nucl. Intr. and Meth., **A466**, 308 (2001).

[2] I. Peric *et. al.*, Nucl. Intr. and Meth., **A565**, 178 (2006).

[3] R. Beccherle *et. al.*, Nucl. Intr. and Meth., **A492**, 117 (2002).

[4] K.K. Gan, Proceedings of the 32nd International Conference on High-Energy Physics, Nucl. Instr. and Meth., **A554**, 458 (2005).

[5] M.L. Chu *et. al.*, Nucl. Instr. and Meth. **A530**, 293 (2004).

[6] T. Henss *et. al.*, JINST **2**, P05006 (2007); M. Imhauser *et. al.*, Trans. Nucl. Sci. **51**, 502 (2004).

[7] M. Donega *et. al.*, Proceedings of the 11th Vienna Conference on Instrumentation, `http://indico.cern.ch/getFile.py/access?contribId=29&sessionId=13&resId=0&materialId=paper&confId=3062` (2007).

[2] Note that the optoboards will be operated in a different thermal environment in the ATLAS cavern, and their performace is known to be temperature-dependent.