A MAPS – based readout for Tera – Pixel electromagnetic calorimeter at the ILC

E. G. Villani[a] , M. Weber[a], M.Tyndel[a], R. Apsimon[a]

[a]STFC, Rutherford Appleton Laboratory

g.villani@rl.ac.uk

Abstract

A Monolithic Active Pixel Sensors (MAPS) based - option for the ILC ECAL will be presented. This novel design provides extremely fine granularity with integrated binary readout. This leads to a Tera-Pixel electromagnetic calorimeter system. An overview of the MAPS proposed solution will be given along with the advantages of this approach. A novel CMOS process used for the fabrication of the first MAPS prototype will be introduced and described. Device simulation results showing the expected detector performance will be shown. Initial preliminary reports from basic tests of the prototype will be given.

I. INTRODUCTION

Owing to the stringent physics requirements, the complexity of the design of the ILC detectors will require huge engineering efforts. Several technical aspects are expected to pose significant challenges.

The pulsed power mode of the detectors is related to the beam operation. In the ILC machine there is a short period of activity followed by a longer one of inactivity. A nominal timing can be assumed to be as in figure 1. After a quick burst of 300ns separated pulses for a total length of 1ms, a period of inactivity of 200ms follows. All the current ILC detectors designs seek to exploit this low operational duty cycle by storing the data locally on sensors during the activity period and read them out in the quiet period. An advantage of this approach is the possibility of pulse powering the system, that would reduce the average power consumption to around 1% of the peak power. However, it requires careful studies of the effects that such pulsed powering scheme might have on the overall performances of the system.

The ILC physics program will also require detectors with an unprecedented energy and spatial resolution. For the electromagnetic calorimeter of ILC (ECAL), the use of a highly granular silicon-tungsten calorimeter has been proposed [1]

In this paper, after an introduction to the existing baseline ECAL design, the proposed MAPS based solution will be presented and the potential benefits arising from such option will be described. A novel CMOS process used for the fabrication of the first MAPS prototype will be introduced and described. Device simulations results and schematic of the pixel architectures will be shown, along with expected performances. Planned tests for the first sensor prototype will be discussed. Preliminary experimental results obtained using a calibrated laser will be shown. Finally, conclusions and plans for the next submission will be discussed.

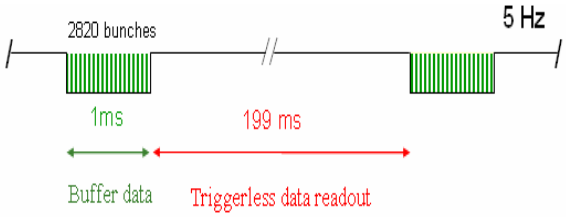

Figure 1: Nominal ILC timing operation.

II. BASELINE ECAL DESIGN

The baseline ECAL design consists of a sampling calorimeter, alternating up to 30 tungsten conversion layers with silicon measurement layers. Half of the tungsten sheets are embedded in the carbon fiber structure, figure 2, the other half sandwiched in between PCB each holding one layer of silicon detector wafers.

The silicon detectors in the baseline design are diode pads of size 1x1cm^2. Their analogue output signal is digitized, with 16bits resolution, by the Very Front End amplifier (VFE), placed inside the thin PCB to reduce the overall size, as in figure 3. Each stave PCB holding the sensors is approximately 1.5m long and 30cm wide and will consist of several smaller PCBs glued together.

Taking into account the total number of layers of the ECAL and the contribution from the end-caps, the total surface of Silicon sensitive layers turns out to be around 2000m^2.

The baseline design consists then of approximately 80million channels. The average current consumption is expected to be around 600A and the average power dissipation approximately 4μW/mm^2.

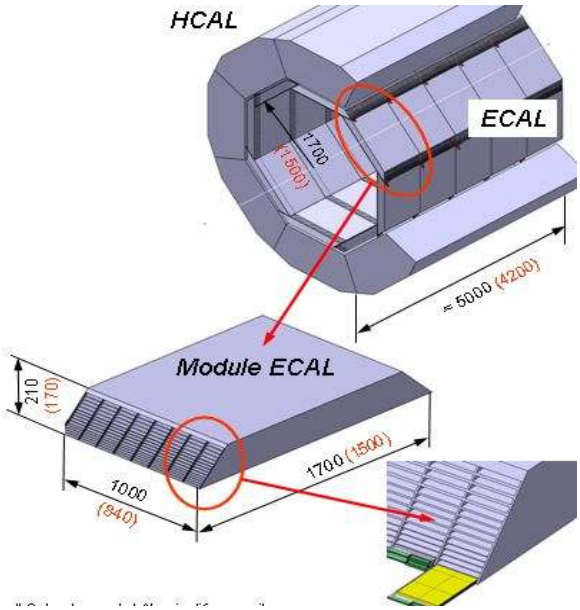

Figure 2: ECAL baseline design.

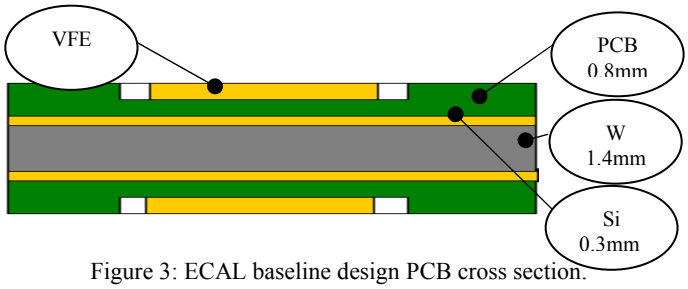

Figure 3: ECAL baseline design PCB cross section.

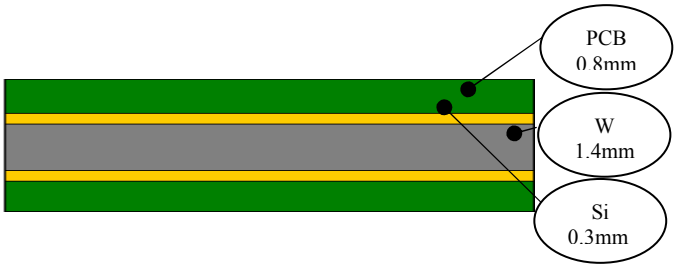

Figure 4: ECAL MAPS design PCB cross section.

A proposed alternative [2] is to use CMOS Monolithic Active Pixel Sensors (MAPS), in which the readout and the sensors are integrated onto the same substrate, figure 4. The baseline design would not be structurally affected by this option, thus allowing an easy swap in. Also, there is significant benefit in terms of overall cost, as a standard CMOS based solution is inherently cheaper than a solution based on high resistivity silicon sensors.

Furthermore, a monolithic solution would make it possible to conceive of a pixel size reduced so much as to have a small probability of double hit per bunch crossing per pixel. The resulting high-resolution tracking calorimeter would than allow measurement of deposited energy by counting the number of hits, thus only a binary readout would be required. Additional advantages arising from such MAPS based solution would be less sensitivity to single event upset because of spread logic and more uniform thermal dissipation.

III. MAPS BASED OPTION

From physics studies the pixel size to guarantee less than 1% probability of double hit is around 50x50μm^2. Therefore, this was the pixel size chosen for the first MAPS prototype designed.

Such a pixel size implies a total number of channels for the whole ECAL of approximately 8x10^{11}. The MAPS based option is then a Terapixel system that presents significant challenges in terms of electronics and overall system design but that would guarantee unprecedented energy resolution.

In order to study the performances achievable from such MAPS based solution, detailed device physics and circuits simulations have been carried out.

In MAPS devices the charge collection takes place mostly by diffusion. As a result they are prone to crosstalk, i.e. to charge sharing among neighboring pixels. Furthermore, the fraction of generated charge available for collection as useful signal is normally little, which implies that low noise readout design is of paramount importance to achieve a high signal to noise ratio.

Also, the complexity of the readout required for the ECAL MAPS option implied an amount of sophisticated electronics integrated in the pixel.

As a result, it was found that a solution based on standard CMOS processes could not guarantee satisfactory performances in terms of charge collection and signal to noise ratio. This is because some of the N-Wells housing the readout electronics in the pixel act also as collecting wells for the generated charge, thus reducing the useful signal, figure 5 and 6.

To overcome these limitations, an alternative CMOS fabrication process has been identified that should guarantee improved performances through better charge collection efficiency. It has been named INMAPS (Insulated Maps) and relies on a Deep P-Well implant that isolates the N-Wells in the pixel but not the collecting ones, see figure 7. The resulting potential barrier (≈ 150mV) around the N-Wells helps reflecting back the generated charge into the epitaxial layer and this reduces the charge loss, figure 8.

A number of device simulations using Sentaurus TCAD [3] have been carried out in order to determine the optimal location of collecting diodes and their size, to maximize the signal to noise ratio, figure 9.

The final layout of one of the implemented pixel architectures in the first MAPS prototype is shown in figure 10. It has been designed in 0.18μm CIS process and features the INMAPS process.

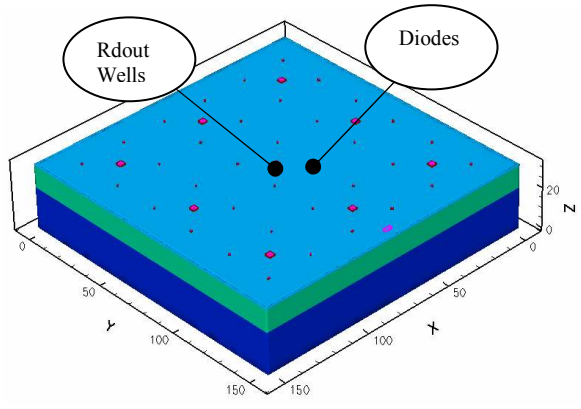

Figure 5: Example of simulated 3x3 cells array of standard CMOS process MAPS with 4 collecting diodes per pixel. In the central N-Well is integrated part of the readout electronics.

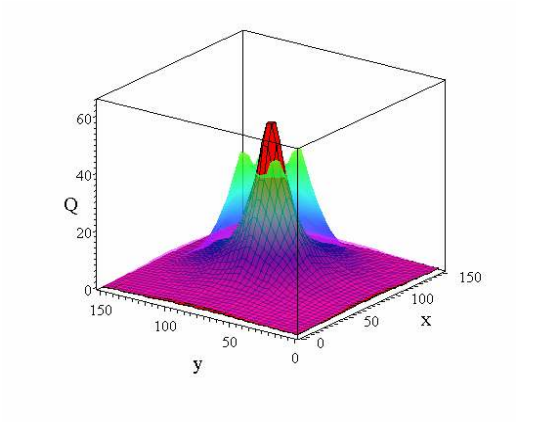

Figure 6: Plot of collected charge in e^- (x 0.1) by diodes (green) and readout N-Wells (red) vs. hit location for the structure of figure 5.Nearly 50% of generated charge is lost in the central N-Well.

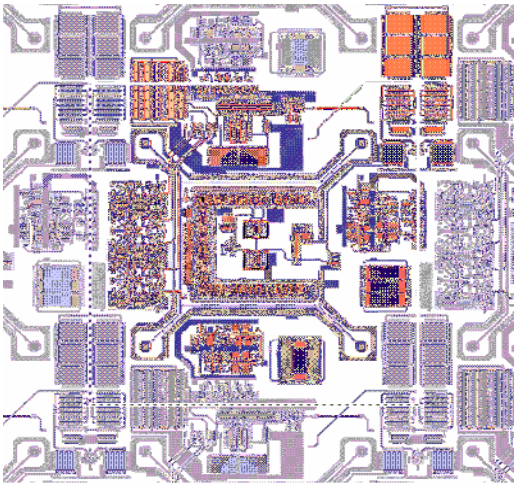

Figure 10: Pixel layout of the implemented Pre-sample architecture featuring INMAPS process.

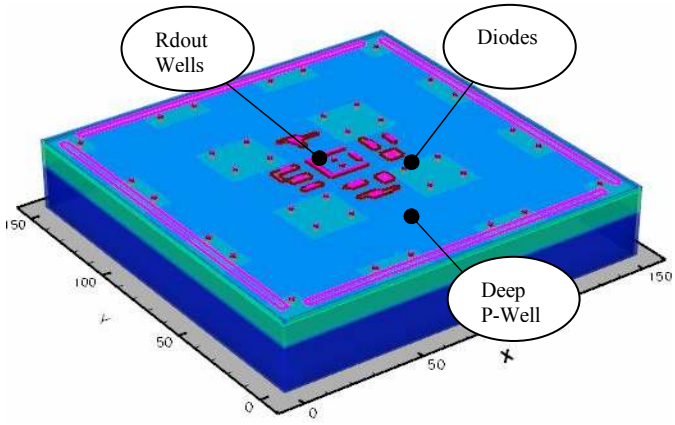

Figure 7: Simulated 3D MAPS pixel 50x50µm^2 featuring INMAPS process. For quicker simulations only the central pixel includes all the N-Well plus the four diodes. The darker blue region is where the Deep P-Well implant extends, beneath the readout N-Wells.

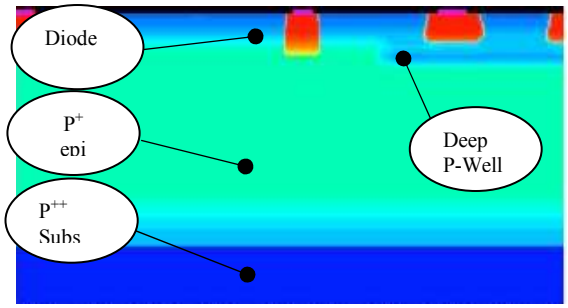

Figure 8: Cross section of an INMAPS based MAPS detector. The Deep P-Well implant isolates all the N-Wells but not the collecting ones.

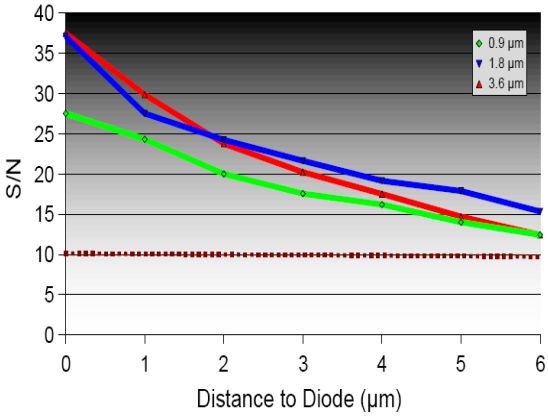

Figure 9: Example of Signal to Noise ratio vs. distance from the pixel corner to the nearest collecting diode of same pixel for an INMAPS solution. The effect of different diode size is also shown.

IV. PIXEL DESCRIPTION AND ARCHITECTURE

In the first prototype, consisting of 8 units of 42x84 pixels, two different pixel architectures have been implemented, pre-shaper and pre-sample, see figure 11. Both pixel topologies include four collecting diodes, charge amplifier, shaper,

variable threshold comparator and hit logic. The pre-logic output of some of the Pre-sample pixels is directly accessible in the prototype for general analogue testing.

The power consumption is estimated to be around 10µW/pixel when operating continuously. However, the pixels can be quickly (≈ µs) enabled/disabled and this would allow a much reduced power consumption during the period of beam inactivity.

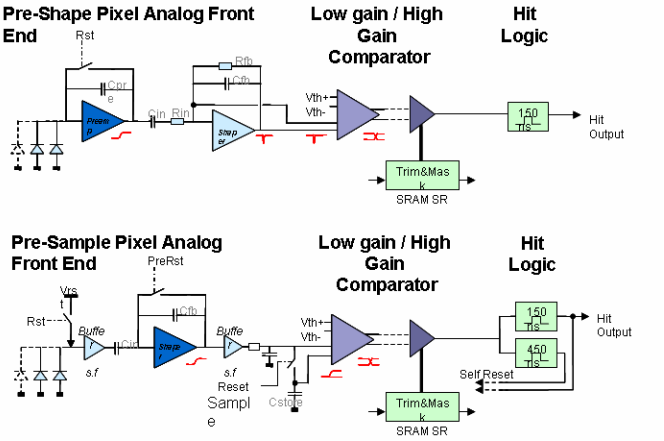

Figure 11: Block diagram of the two pixel architectures implemented in the first CALICE MAPS prototype device.

The digital block serves up to 42 pixels from one row, each row being split into 7 groups of 6 pixels. Following a hit, for each row the logic section stores in SRAM the time stamp (13 bits), pattern number (3 bits) and bit pattern (6 bits). Additional 9 bits are required for row encoding, giving then 31 bits per hit, figure 12.

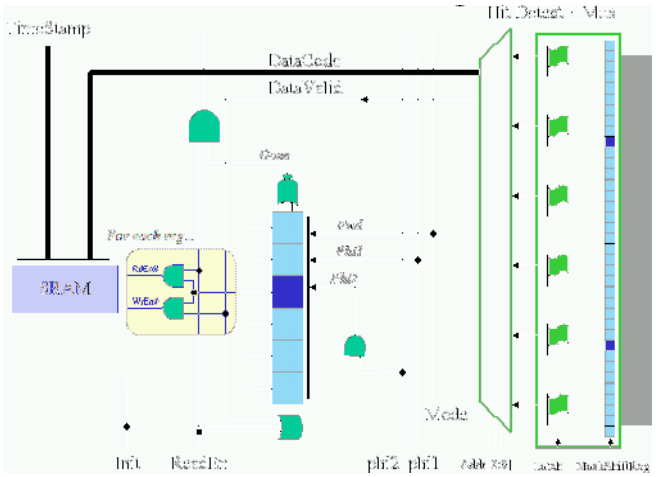

Figure 12: Digital block section.

The floor plan of the first prototype is shown in figure 13, superimposed onto a microphotograph of the actual chip.

Two different capacitor arrangements have been implemented in both pixel architectures, to investigate their effect on noise performances. The dead area needed for the digital block amounts to 250µm every 2mm. Detector size is 1x1cm^2, for a total number of 6million transistors.

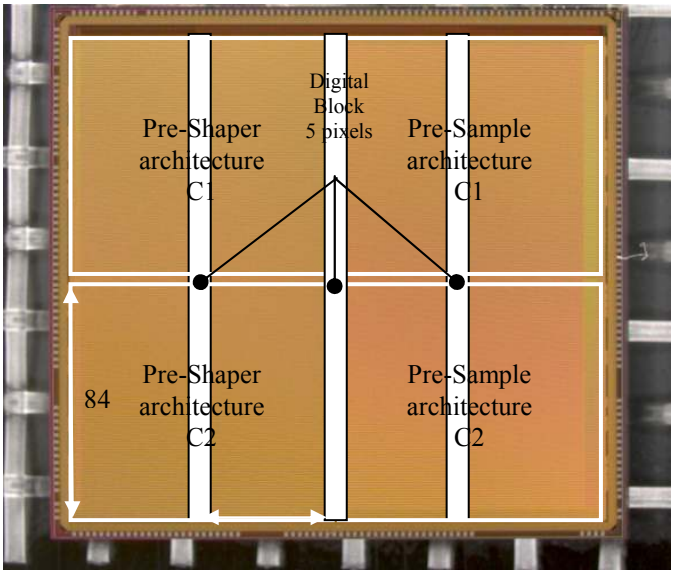

Figure 13: Microphotograph of the CALICE MAPS prototype with floor plan.

V. TEST SETUP

An extensive series of tests have been planned for the first CALICE MAPS prototype in the coming months. They include: basic functionalities tests, to assess, among other things, the general working of the digital section, source test, beam test and characterization using a calibrated Laser beam. The latter should allow detailed analysis of the effective usefulness to charge collection for the Deep P-Well process. Calibration and validation of device simulation results will also benefit from this test.

For this purpose, a laser source capable of producing pulses 4ns long at 1064nm wavelength with a focusing of 2µm has been calibrated to release a MIP charge equivalent in Silicon, see figure 14.

This has been achieved by employing a very low noise charge amplifier coupled to a silicon sensor of known characteristics. The transfer function of the charge amplifier (i.e. voltage vs. charge) has been determined by injecting charge of known value into the amplifier's test input. Next, the relationship between voltage output of amplifier vs. laser intensity has been obtained and the noise contribution (sensor plus amplifier noise, EMI interference noise, offsets) subtracted. Finally, from the two transfer functions, the relationship between released charge vs. laser intensity has been obtained. The MPV of injected charge/µm in Silicon has been estimated by dividing the MPV of the total generated charge by the average value of sensor thickness. The residual noise in charge injection using the laser pulse amounts to around 15% of MIP, see figure 15.

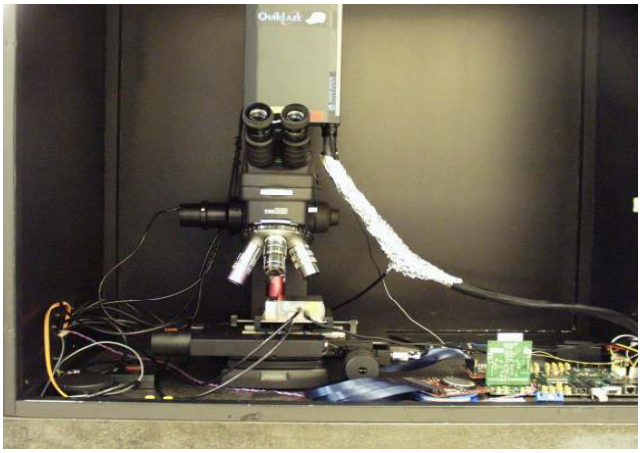

Figure 14: Laser Test system at RAL. Three wavelengths (1064, 535, 355) nm available, pulse length of 4ns and variable beam size of x1 up to 25x25μm^2 at maximum magnification. The energy available ranges from 10fJ to 500μJ.

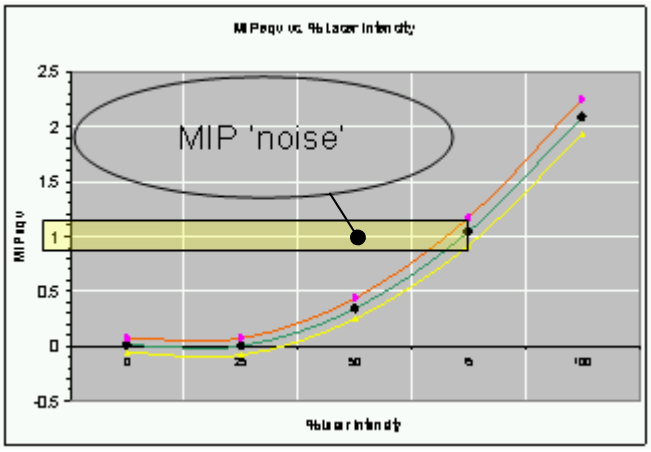

Figure 15: MIP-normalized released charge in Si vs. Laser intensity for the test setup of figure 14.

VI. Preliminary Test Results

Some very preliminary tests have been carried out to check the basic functionalities of the chip and the pixel response to light and laser pulse. The analogue output of the pre-sample architecture shows clear sign of activity when illuminated with uniform light, figure 16 and with infrared laser pulse, figure 17.

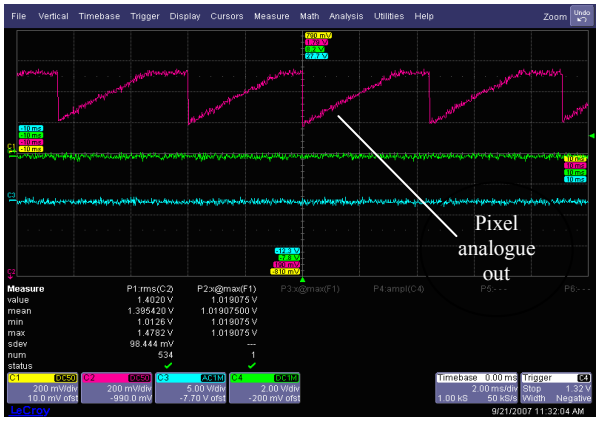

Figure 16, 17: Analogue output of the pre-sample pixel after uniform light illumination, top, and laser pulse, bottom.

VII. Conclusions

We proposed a MAPS based ECAL solution that could potentially offer a number of advantages in terms of energy resolution and overall cost.

Following this concept we designed a MAPS prototype based on a novel CMOS process (INMAPS) that might significantly improve the performances of these types of detectors in terms of charge collection efficiency. The pixel design and readout electronics have been optimized to achieve a signal to noise ratio exceeding 10 over the whole surface of the pixel.

The first MAPS prototype aims at demonstrating the feasibility of the approach, the actual usefulness and reliability of this novel fabrication process.

A series of extensive tests, to be carried out in the next months, will include basic functionalities, source, beam and Laser MIP test. Preliminary tests show that the analogue output of the pre-sample pixel architecture responds properly to uniform illumination and laser pulse.

Power consumption optimization will be addressed in the next design.

VIII. References

[1] The CALICE collaboration: calorimeter studies for a future linear collider,2002. http://www.ppd.clrc.ac.uk/AnnReps/2004/exp/Calice-317.pdf.

[2] P.D. Dauncey, Concept for a Si-W ECAL for the ILC based on MAPS. http://www.hep.ph.ic.ac.uk/calice/maps/mapscd/mapscd.pdf

[3] Synopsys Sentaurus TCAD, rel. 10.0