3D System Integration for high density Interconnects

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Abstract

3D-Integration is a promising technology towards higher interconnect densities and shorter wiring lengths between multiple chip stacks, thus achieving a very high performance level combined with low power consumption. This technology also offers the possibility to build up systems with high complexity by combining devices of different technologies. The fundamental processing steps will be described, as well as appropriate handling concepts and first electrical results of realized 3D-integrated stacks.

I. INTRODUCTION

Ultra thin silicon is the base of this integration technology, which requires appropriate handling concepts, sophisticated process integration and careful processing of thinned substrates to form the required chip stack.

Three main concepts for 3D integration have been developed at Fraunhofer IZM. The approach with the greatest flexibility, called **I**nter **C**hip **V**ia - **S**olid **L**iquid **I**nter-**D**iffusion (ICV-SLID), has been described elsewhere in detail [1, 2]. It is a chip-to-wafer stacking technology which combines the advantages of the Inter Chip Via (ICV) process and the solid-liquid-inter-diffusion technique (SLID) of copper and tin. The fully modular wafer-level 3D integration concept has the potential to build multi-layer high-performance chip stacks and is well suited as a replacement for embedded technologies based on monolithic integration. To address yield issues, a wafer-level chip-scale handling is used, to select known-good dies and work on them with wafer-level process sequences before joining them to integrated stacks.

In respect to the requirements for high density pixel detector devices, the ICV-technology has the main advantage of freely selectable locations for the electrical interconnects. The comparably small lateral dimensions in the range from 2 µm – 5 µm in diameter allow theoretically for a very high interconnect density in the range of > 50.000 ICVs /mm^2 within the Si-substrate.

The SLID technology with its galvanically grown Cu/Sn structures has a lateral size limitation to a pitch of > 15 µm due to the natural roughness of the Sn film, thus achieving a maximum number of solder pads in the range of ~ 2.500 pads/mm^2 chip area. The total metallic volume consumed for electrical interconnects through a thinned Si-substrate can be held relatively small if, for example, pixel detector devices have to be 3D integrated. Natural limitations are the achievable aspect ratios of the ICVs, especially the necessary CVD processes for isolation and metallization of the ICVs.

II. HANDLING CONCEPTS AND BASIC TECHNOLOGIES

A. *Wafer-level Chip-scale processing*

In order to integrate only known-good dies, the separated and preprocessed chips are placed on a temporary handling substrate which contains etched-in alignment marks, according to the positions of the target wafer. The handling substrate is covered with a thermoplastic polymer in which the donor chips are placed. This technique allows thorough cleaning of the chip surfaces prior to the soldering or bonding step. Even thinning and backside metallization processes are possible to a certain degree, depending on the glass point of the used thermoplastic adhesive.

The transfer to the target substrate occurs by optically adjusted soldering under vacuum and pressure. Finally, the handling wafer can be removed using a chemical solvent, thus removing the adhesive between handling substrate and the top surface of the soldered chip stacks.

Using the above described processing sequence, figure 1 shows the result of a defect free chip-to-wafer transfer by soldering (SLID), after removal of the handling substrate.

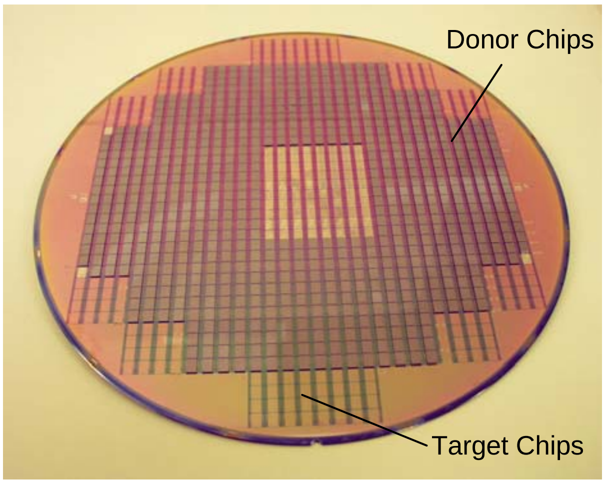

Figure 1: Wafer level chip scale processing; 100% yield transfer of chips after soldering and removal of handling substrate

B. *Thin Substrate Handling*

There are currently two main technologies used to handle thin substrates at Fraunhofer IZM. One is the use of temporary adhesives between a handling substrate and the device wafer to be thinned. Several types of adhesives were investigated in respect to the maximum allowed process temperature, to defect-free gluing results after thinning and to the ease of release after soldering.

Basically, many thermoplastic adhesives show good results in terms of bubbles and can be removed relatively easy, but are temperature-limited to a range of ~ 120 – 150°C. A second type of material, silicone-based elastomers, are currently under development. Early results show temperature stability up to 180°C and defect free gluing after thinning. However, removal of the handling substrate was so far not possible using solvents. Additionally, the maximum non-planarity of a completed device wafer has to be taken under consideration for the thinning sequence. Thermoplastic materials as temporary glues are limited to < 1.5 µm step height on the surface of a device wafer in most cases. Preliminary results with elastomer-type glues showed step height coverage in the range of 5µm and above, depending on the thickness of the glue layer. The achievable thinning accuracy, i.e. the total thickness variation (TTV) of a thinned Si-substrate, can be as low as < 2 µm TTV for a 20 µm thin Si layer, temporarily glued with an elastomer-type adhesive.

The second handling approach is the use of electrostatic force. The wafer to be thinned is held in place with a so-called mobile electrostatic carrier ("mobile eChuck"). The holding principle is based on electrostatic forces between the mobile eChuck wafer, functioning as the mobile handling substrate, and the thin Si wafer or the Si chips to be held. A DV- voltage is applied to the backside of the eChuck carrier wafer, which is then routed to 2 electrodes at the front side of the eChuck wafer, enabling an electrical field between the top dielectric layer of the eChuck wafer and the thin Si wafer or chip [3, 4]. The schematic in figure 2 shows the principle function of such a carrier wafer.

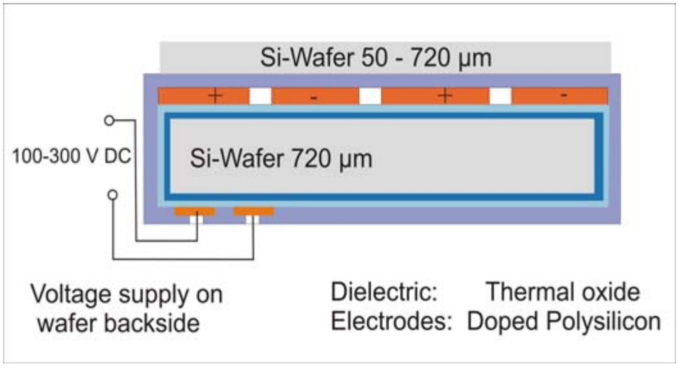
Si-Wafer 50 - 720 µm
+
-
+
-
100-300 V DC
Si-Wafer 720 µm
Voltage supply on wafer backside
Dielectric: Thermal oxide
Electrodes: Doped Polysilicon

Figure 2: Bipolar eChuck wafer – principle of operation

C. *Substrate Thinning and Dicing*

In order to thin to remaining Si-thicknesses < 50 µm, a temporarily glued handle wafer (carrier substrate) is used to support the thin Si-film. The precision thinning sequence starts with a grinding step, removing most of the material. The next step is a wet chemical spin etch process, which serves also the purpose of a stress relief etching step after the grinder. Finally, a short Si-CMP process step results in a smooth and clean backside surface. In order to open the previously formed ICVs, a Si-RIE etch process is used afterwards. If the thinned substrate needs to be separated into single chips in a later state, using a spray etch backside lithography and a fast Si-etch (Bosch process), the thin substrate can be dry etched until all chips are singulated. Thinning by etching has some advantages against conventional sawing. Firstly, there is no chipping or mechanical damage to the thinned chips, and secondly, for small chip sizes < 5x5 mm^2, the process time can be decreased compared to sawing. Thirdly, there are no limits to the desired chip geometry. Fig. 3 shows a 70 µm deep shallow trench grove next to 8 µm thick Cu/Sn metal structures after oxide etching, Si-etching and removal of spray coated photo resist. The Sn surface of the SLID structures are clean and ready to solder.

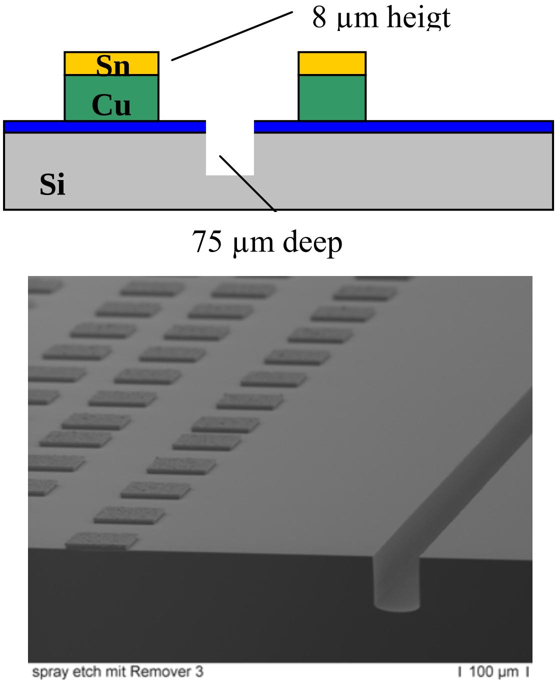

Figure 3: Schematic (top) and SEM-graph (bottom) of a chip separation etch after spray resist removal

D. *HAR Si Etching for ICV Formation*

Fraunhofer IZM concentrates on the formation of small diameter inter-chip via holes, which is mandatory if high density interconnects are desired. There are to main etching approaches to achieve high aspect ratio (HAR) trenches in silicon. Using a so-called "HBr-process", trenches with aspect ratios in the 10:1 range, with smooth sidewalls and a positive taper angle of ~ 86°-89° can be achieved. These trenches have good, void-free filling capabilities for the subsequent CVD deposition steps. However, there are limitations in the amount of open area (< 15 %), an oxide hard mask is required and the

HBr process requires a diluted HF-dip after etching for removal of unwished etch byproducts at the sidewall of the trench. Figure 4 shows an 8:1 aspect ratio trench etch result.

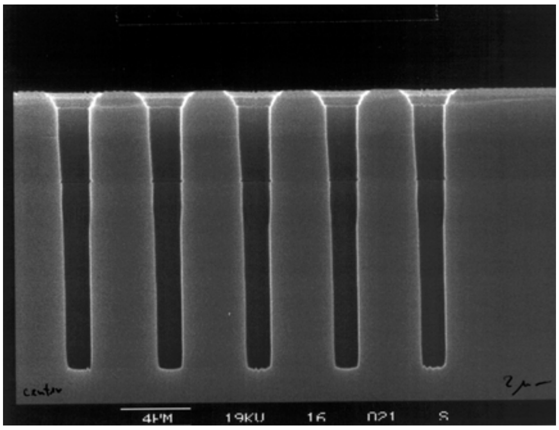

Figure 4: HBr-process; AR 8:1, 17 µm depth

Since industry requirements also ask for HAR trenches of values > 12:1, we began to work on the so-called “Bosch process”, which uses a SF6/C4F8 etching chemistry. HAR trenches up to 20:1 are achievable with this process, and there are almost no limitations regarding open area. Also, no HF-dip is required and the structures can also be etched using photoresist. However, the scallop formation and the taper angle of $\geq$ 89° make the subsequent CVD deposition steps more difficult. Figure 5 shows a 40 µm deep Si-trench with an aspect ratio of 16:1.

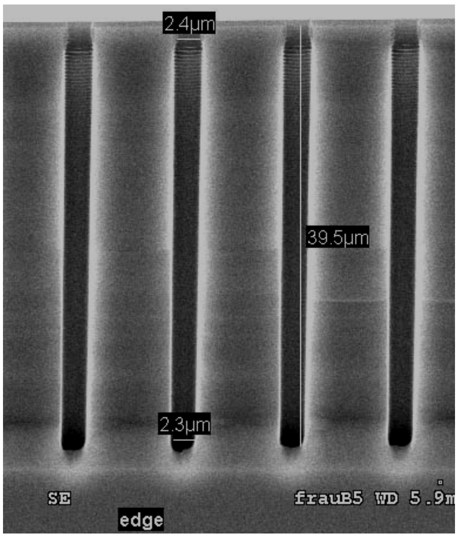

Figure 5: Bosch-process; AR 16:1, 40 µm depth

E. Isolation and Metal Filling of HAR ICVs

One of the most critical steps in the formation of ICVs are the deposition of dielectrics and metals, which in term form the electrical isolation and the electrical connection between the stacked devices.

For most high density interconnects and for ICVs with an AR > 6:1, CVD processes are currently the only processes of choice. The isolation to the bulk-Si is achieved by depositing a highly conformal O_3/TEOS based SiO_2 using SACVD (sub-atmospheric chemical vapor deposition). Depending on the taper angle, depth/aspect ratio, amount of open area and cleanliness of the trench sidewalls, conformalities in the range of 40-80% can be achieved.

Metal-filling of HAR ICVs is achieved by depositing a thin TiN film by MOCVD (metal-organic CVD) which acts as a seed layer and diffusion barrier for the subsequent W film, which is also done using a CVD process. The W-film is then partially etched back in order to release most of the film stress. A following structured W-etch step completes the formation of the ICVs. All deposition processes are run at temperatures in the 400°C range. Figure 6 shows a W-filled ICV with 50 µm depth and an AR of $\geq$ 16:1, lateral dimensions are 3x10 µm. The rectangular form of the ICV was chosen to somewhat open the CVD process window and to ease the SEM preparation technique.

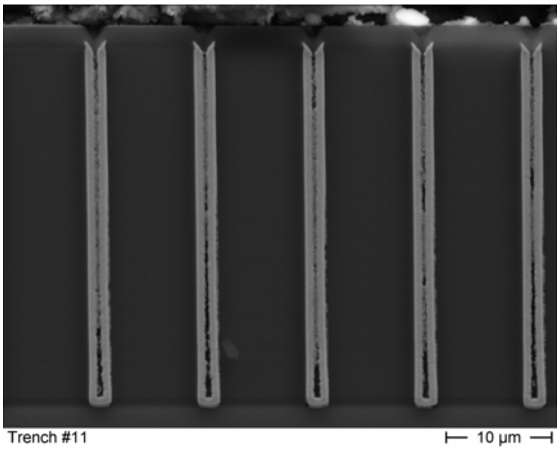

Figure 6: W-fill of HAR trench (AR 16:1, depth 50 µm)

F. SLID Metallization

The metal system name “SLID” comes from the fact, that copper and tin are inter-diffusing at elevated temperatures: **S**olid **L**iquid **I**nter-**D**iffusion. One side of the chips is covered with through mask electroplated copper. The opposite side has a double layer from copper and tin. After contacting both sides the temperature is increased to about 300 °C. The tin melts and a fast inter-diffusion of copper into the molten tin takes place. The alloy copper-6-tin-5 is formed. This alloy has a melting point of about 400 °C. That means already a short time after melting the tin, the alloy hardens again and the stack is fixed. The inter-diffusion is not completed yet, because the stable phase is copper-3-tin. This process takes more time, can be performed in principal outside the adjustment tool and is uncritical concerning the adjustment loss between the stacked layers. Copper-3-tin has a melting point above 600 °C, so this is perfectly suitable to build multilayer stacks. Figure 7 shows a FIB cross section of a three layer stack, connected using the SLID technology.

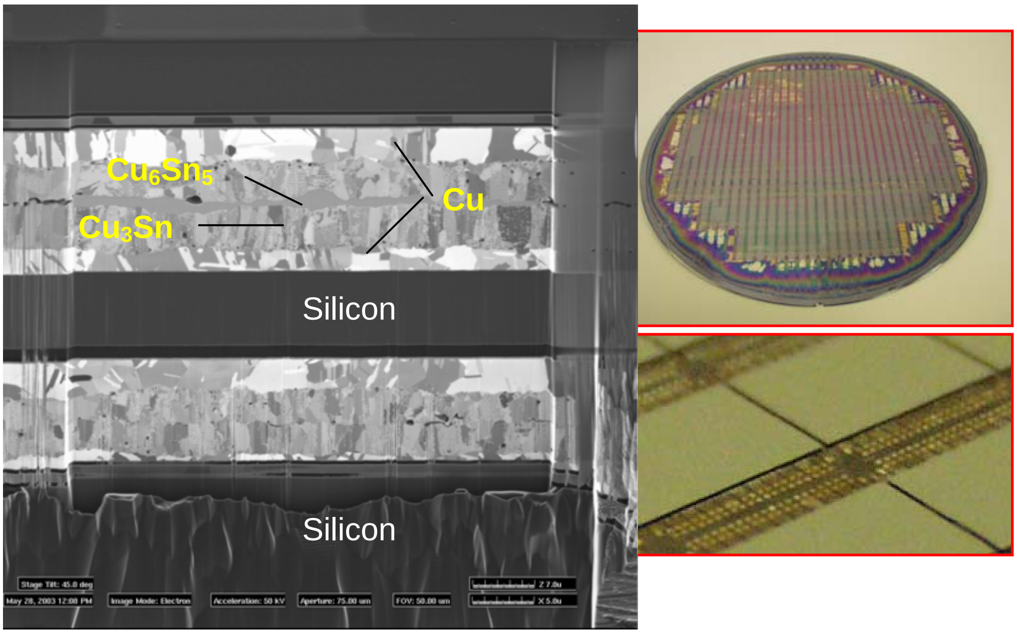
Cu$_6$Sn$_5$
Cu$_3$Sn
Cu
Silicon
Silicon
Stage Tilt: 45.0 deg
May 28, 2003 12:00 PM
Image Mode: Electron
Acceleration: 50 kV
Aperture: 75.00 um
FOV: 50.00 um

Figure 7: SLID-connection of a 3-layer chip stack

The upper metal junction still shows the first copper-6-tin-5 composition. This cannot be found in the lower part, because the processing time from the upper layer is added and the inter-diffusion is completed. In all cases copper remains at the interfaces, so no chip delaminated as can be seen in the small picture insertions. All thinning procedures and electro plating sequences were performed on wafer level.

III. INTEGRATION CONCEPTS AND REALIZATION

A. *ICV-SLID Technology*

This technology is based on two major processing blocks. ICVs (**I**nter-**C**hip-**V**ias) enable the necessary vertical electrical interconnects through thinned Si substrates. The ICVs are electrically isolated and metallized either with W or with Cu. They vary in their vertical depth between 10 and 50 µm at aspect ratios of 8:1 up to 15:1.

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SLID layers provide the required mechanical and electrical interconnects between stacked chips or stacked wafers

Figure 8 shows a cross section of a processed device stack with W-filled ICVs and a $Cu/Cu_3Sn/Cu$ SLID connection.

One of the major advantages of this technology is the possibility to work on a wafer scale processing level as long as possible, typically up to the point where the backside Cu/Sn metallization is finished. Singulation into dies, optical adjustment/chip placement and the actual soldering are the last processing blocks during the formation of a chip- or wafer stack.

Any excessive work on already separated chips can affect yield and functionality of the later to be formed chip stack and should be avoided.

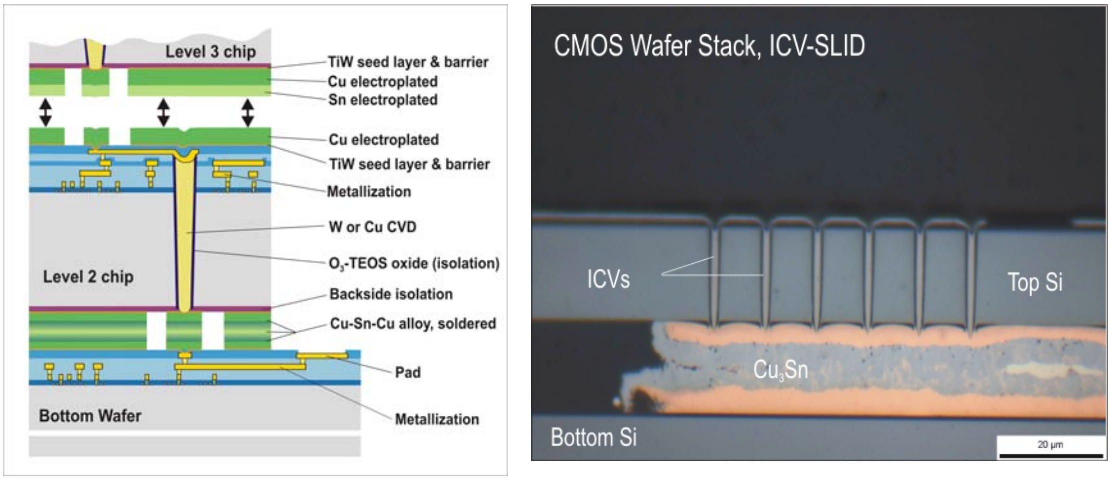
Level 3 chip
TiW seed layer & barrier
Cu electroplated
Sn electroplated
Cu electroplated
TiW seed layer & barrier
Metallization
W or Cu CVD
O$_3$-TEOS oxide (isolation)
Level 2 chip
Backside isolation
Cu-Sn-Cu alloy, soldered
Pad
Bottom Wafer
Metallization
CMOS Wafer Stack, ICV-SLID
ICVs
Top Si
Cu$_3$Sn
Bottom Si
20 µm

Figure 8: Schematic (left) and Micrograph (right) of a 3D-integrated CMOS device stack

B. 3D-Integrated Test Stacks

In order to investigate the resistance of ICVs at different length, wafer stacks with ICV-chain structures, either filled by CVD of W and following W etch back or by MOCVD of Cu with following Cu-CMP step, have been realized. After completing the ICVs and a metal layer from the front side, the substrates were temporarily glued to a handling substrate and then thinned until the ICVs were opened from the backside. A low temperature oxide was deposited onto the thinned backside and opened by oxide-CMP. Finally an AlSiCu-backside metallization was done to enable electrical measurements of the chains. Figure 9a-c shows the schematic, the completed test wafer and a FIB cut through a chauin section.

For the W-filled ICVs, area yield values in the range of > 97 % for single ICV Kelvin structures and > 80 % for ICV chain structures with more than 900 ICVs/chain could be achieved. Figure 9 shows a schematic cross section of the fabricated test structure.

The average resistance for single ICVs (2,4 µm x 9,4 µm area) with a depth of 20 µm was 0,19 Ω and for single ICVs with a depth of 45 µm was 0,32 Ω, respectively.

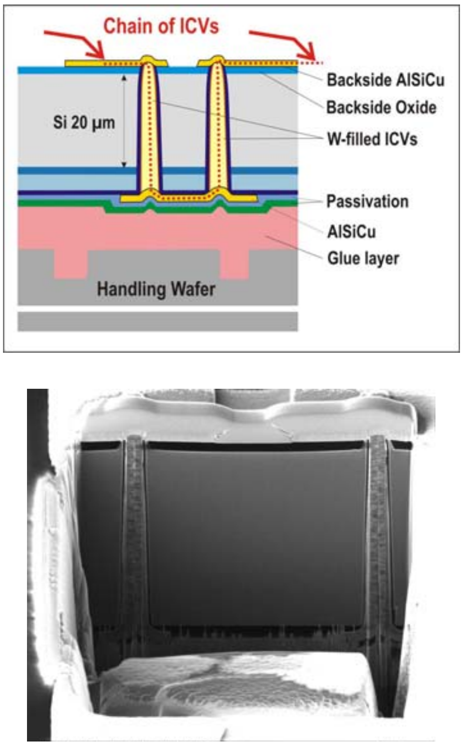

Figure 9a-c: Schematic (top) and FIB-graph (bottom) of a 3D-integrated test stack with daisy chains

C. 3D-Integrated CMOS Transistors

CMOS transistors, built on Si as well as on strained Si/SiGe substrates were integrated on 200 mm Si wafers. These wafers were then further processed according to the ICV-SLID technology: Figure 10 shows the finished wafer stack during removal of the handling wafer.

Electrical characterization of Si- and SiGe transistors of thinned top chips has been compared to reference device chips of standard thickness. The measured values of the typical output characteristics Id (Vd, Vg) and threshold voltage were within the specifications of a reference device wafer. Negligible impact of the ICV-SLID processing sequence on transistor performance has been reported elsewhere [2].

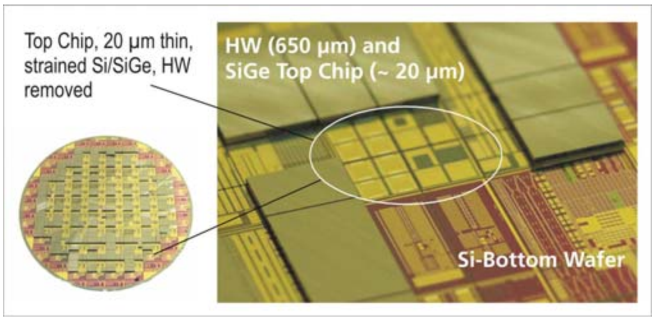
Top Chip, 20 µm thin, strained Si/SiGe, HW removed
HW (650 µm) and SiGe Top Chip (~ 20 µm)
Si-Bottom Wafer

Figure 10: Chip-to-wafer stack (SiGe-CMOS dice on Si-CMOS wafer)

IV. SUMMARY AND CONCLUSION

The wafer-level Chip-scale concept with silicon handling substrate enables the formation of high density interconnects through tinned silicon for a variety of applications. Simplified handling of thinned substrates as well as thinned chips by an mobile electrostatic carrier is under development. Feasability of 3D-integrated wafer stacks using ICV-SLID technology have been shown. Electrical resistance values of the fabricated ICV chains were in the expected range at comparably high area yield; the electrical impact of the ICV_SLID process flow on CMOS transistor behaviour was negligible.

The applicability of the presented 3D integration concepts depends strongly on the target products, their electrical and mechanical specifications, i.e. maximum allowed processing temperatures, topography, wafer size, die sizes and the provided areas to place the ICVs at their desired locations during the 3D integration process.

IV. REFERENCES

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