Distributed Power Architectures for Computing Systems
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Distributed Power Architectures in Computing Systems

P. Mattavelli, P. Tenti, L. Rossetto, S. Buso, S. Saggini

Speaker: G. Spiazzi

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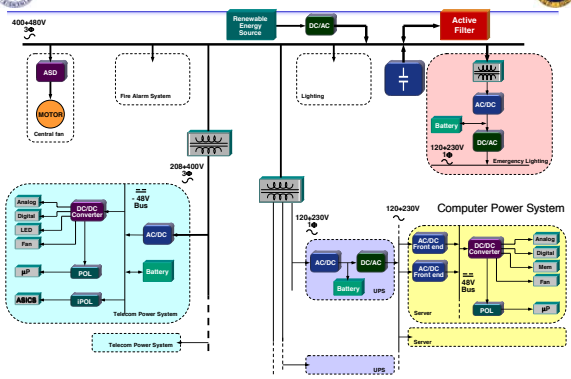
University of Padova, ITALY

Outline

- Conversion system architectures for DPS
  - Unregulated Intermediate Bus Converters (IBC)
  - Regulated Intermediate Bus Converters
- Isolated Point of Load converters (POLs)
- Non isolated POL: buck interleaved
- Digital control for high-frequency power conversion in Distributed Power Systems: current research activity at the University of Padova

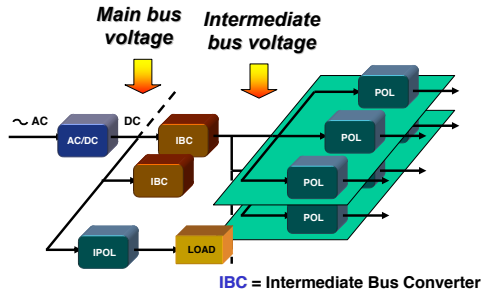
Power Distribution Problem



Power Distribution Problem

- Very complex Power Management Architectures in Computing & Networking Systems
  - Many low voltage, high current and tightly regulated voltage sources
  - Accurate management for sequencing, tracking and fault management
  - High Power density needed for real estate saving and Thermal management issues
  - Low cost always mandatory in high volume applications

Distributed Power Architectures

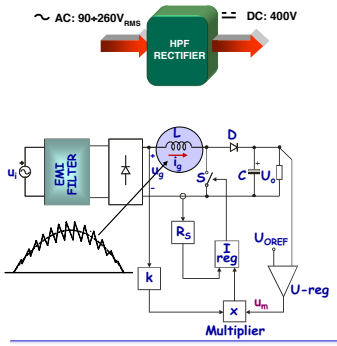


IBC = Intermediate Bus Converter
POL = Point Of Load converter

AC-DC Front End

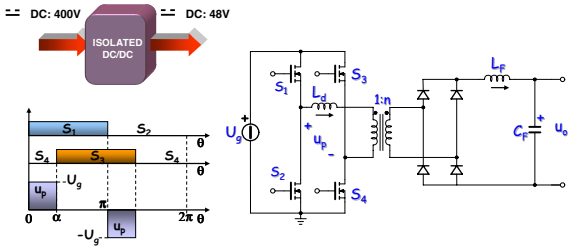
- EMI filter for attenuate high-frequency noise (both conducted and radiated) produced by the switching converters
- High-Power-Factor (HPF) rectifier for low-frequency harmonic standard compliance
- Isolated DC/DC converter for electrical isolation with the main and voltage scaling

HPF Rectifier



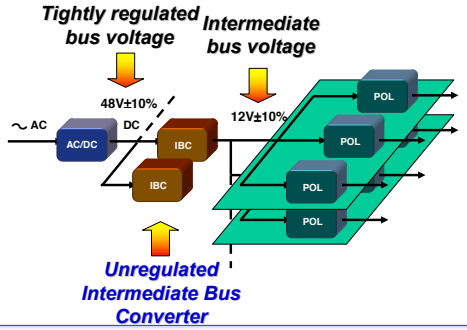
- Boost converter in CCM
- Average current mode
- High power factor
- Output voltage higher than peak input voltage
- Dedicated control IC available

Isolated DC/DC

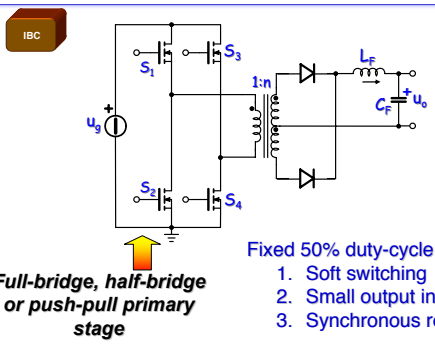


- Phase-shift modulated Full-bridge converter
- Soft switching operation exploiting the transformer leakage inductance

Narrow Input IBCs



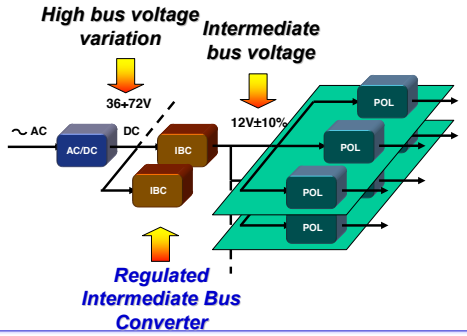
Example of Unregulated IBC



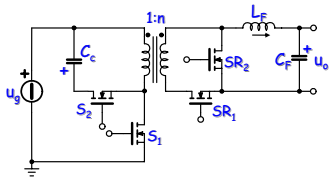
Fixed 50% duty-cycle:
1. Soft switching
2. Small output inductor
3. Synchronous rectification

Open-loop operation

Wide Input IBCs



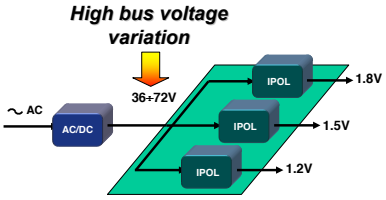
Example of Regulated IBC



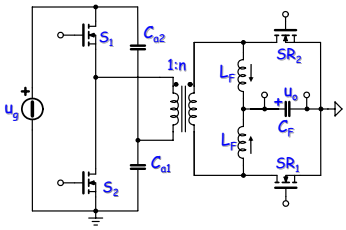
- **Active-clamped for soft switching**
- **Synchronous rectification**
- **Large output inductor**
- **High voltage rating device (60V) for SR**
- ***Switching frequency of the state-of-art: ~300KHz***

Isolated POLs

No intermediate bus voltage

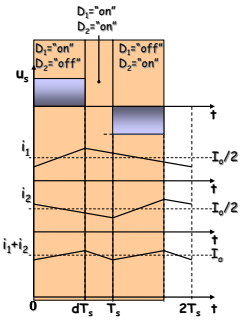


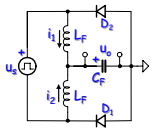
Example of Isolated POL



- Half bridge with current doubler
- Synchronous rectification

Current Doubler





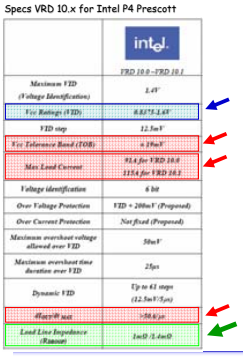
- No center-tapped windings
- Current ripple cancellation
- Splitted load current between the two inductors

Non Isolated Point Of Load Converters

- Voltage Regulator Modules (VRMs)
  - Power trend
  - Interleaved buck converters
  - Current sharing
  - Adaptive voltage positioning
  - Digital control for high-frequency power conversion in Distributed Power Systems: current research activity at the University of Padova

VRM Intel Specifications

Specs VRD 10.x for Intel P4 Prescott



- Low supply voltage
- Small tolerance band
- High load current
- High current slew rate
- Resistive output impedance

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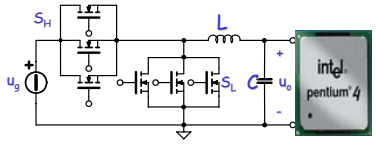
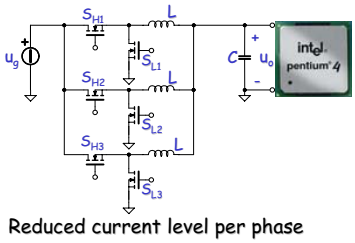
Single-Phase Synchronous Buck Converter

- High load current requires the use of parallel power MOSFETs or parallel power converters



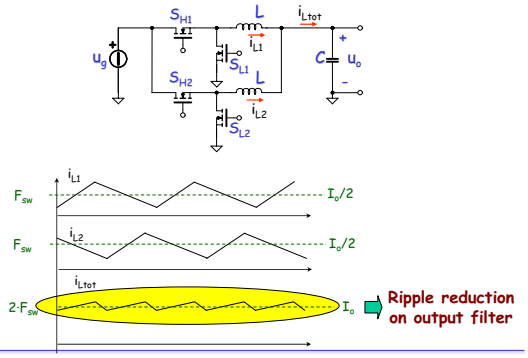
Parallel device approach is not convenient
since interleaved operation reduces output and input ripple

Multiphase Interleaved Buck Converters

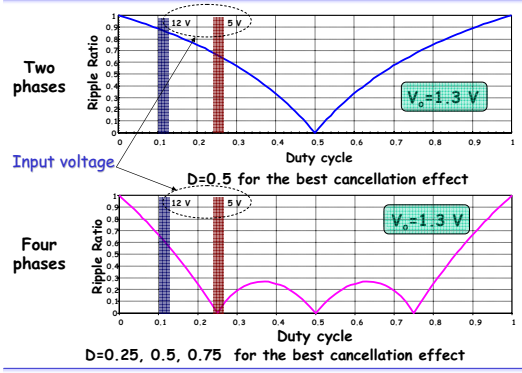


- Reduced current level per phase
- Reduced output current ripple
- Reduced input current ripple
- Increased bandwidth (F_{eq}=N F_{sw})

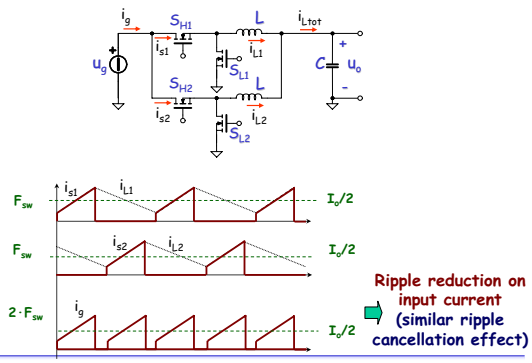
Multi-Phase Interleaved Converters



Output Current Ripple Cancellation



Multi-Phase Interleaved Converters



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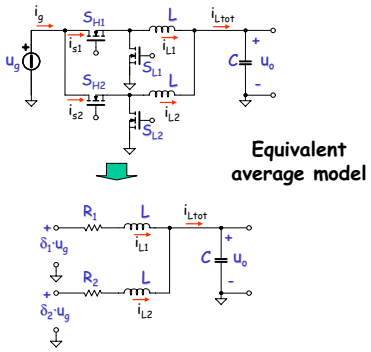
Current Sharing in Parallel Channels



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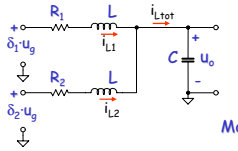


k-channel resistance

$$R_k = R_{dsonk} + R_{Lk} + R_{PCBk}$$

Mosfet R_{dson} — inductor resistance — trace resistance (PCB layout)

Dc inductor current mismatch:

$$\Delta i_L = i_{L1} - i_{L2} = 2u_g \frac{\delta_1 - \delta_2}{R_1 + R_2} \left(\frac{1 + \frac{R_2\delta_1 - R_1\delta_2}{2(\delta_1 - \delta_2)} \cdot \frac{1}{R_L}}{1 + \frac{R_1 R_2}{R_1 + R_2} \cdot \frac{1}{R_L}} \right)$$

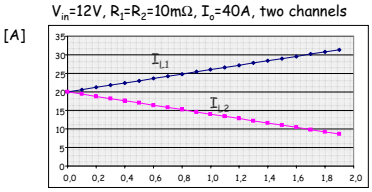
R_L = load resistance

- Unmatched duty cycle
- Unmatched channel resistance

Current Sharing in Parallel Channels

- Even small mismatches of duty-cycle or of channel resistance generate serious current sharing issues
- Example with unmatched duty-cycles:

V_{in}=12V, R_1=R_2=10mΩ, I_o=40A, two channels



- Similar results for small unmatched channel resistances (spread of MOSFET R_{dson}, difference on PCB layout, etc..)

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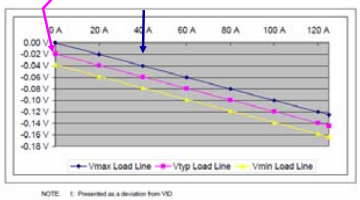
VRM Intel Specifications

Specs VRD 10.x for Intel P4 Prescott

	intel VRD 10.0 -VRD 10.1
Maximum VID (Voltage Identification)	1.4V
Vcc Ratings (VID)	0.8375-1.45V
VID step	12.5mV
Vcc Tolerance Band (TOB)	± 19mV
Max Load Current	91A for VRD 10.0 115A for VRD 10.1
Voltage identification	6 bit
Over Voltage Protection	VID + 200mV (Proposed)
Over Current Protection	Not fixed (Proposed)
Maximum overshoot voltage allowed over VID	50mV
Maximum overshoot time duration over VID	25µs
Dynamic VID	Up to 61 steps (12.5mV/5µs)
Slew Rate	>50.6/µs
Load Line Impedance (Rmotor)	1mΩ /1.4mΩ

Resistive output impedance

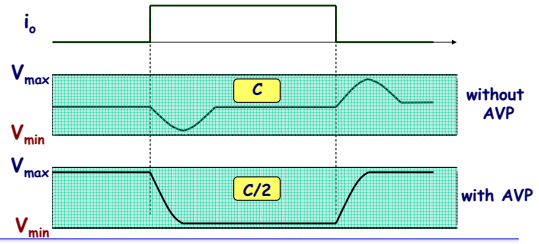
$$V_{TYP,out} = VID - |TOB| - R_{DROOP} \cdot I_{load}$$



"Droop Function" or "Adaptive Voltage Positioning"

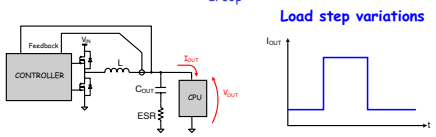
Adaptive Voltage Positioning

- Adaptive voltage positioning (AVP) is required by VRM specs
- AVP is very effective on reducing VRM output caps:
  - For given output caps, output voltage variation is halved
  - For a given output voltage tolerance, output caps are halved



Adaptive Voltage Positioning

- AVP is realized by VRM resistive output impedance
- Number of parallel electrolytic caps is determined by condition: ESR = R_{droop}



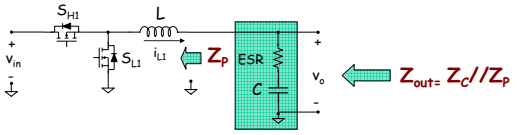
Load step variations

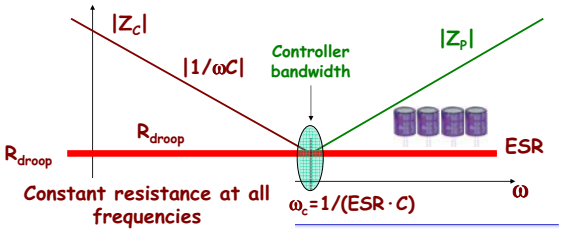
Output voltage

without Droop Function

with Droop Function

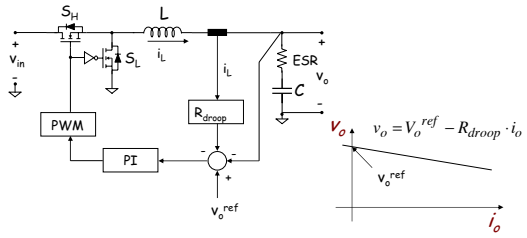
Constant Resistive Output Impedance





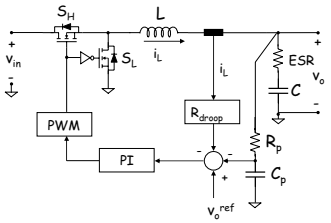
Constant resistance at all frequencies

AVP: Control Block Diagram



- Closed-loop control on $v_T = v_o + R_{droop} \cdot i_L$
- PI design so as to impose controller bandwidth $\omega_c = 1/(ESR \cdot C)$ (theoretically no need for high-performance controller)

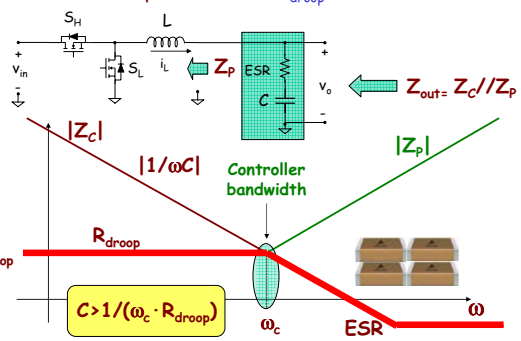
AVP: Control Block Diagram



- Closed-loop control on $v_T = v_o + R_{droop} \cdot i_L$
- PI design so as to impose controller bandwidth $\omega_c = 1/(ESR \cdot C)$
- Use of an additional R_p-C_p to limit precisely controller bandwidth

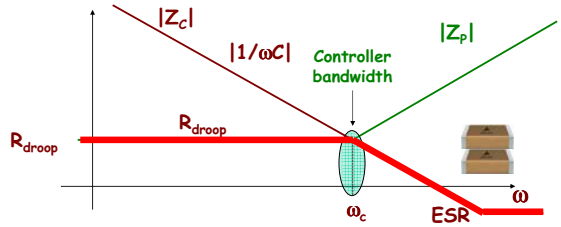
AVP with Ceramic Capacitors

- In ceramic capacitor ESR < R_{droop}



AVP with Ceramic Capacitors

- The higher the control bandwidth, the lower the output capacitor requirement: $C > 1/(\omega_c \cdot R_{droop})$
- Need for high-performance controller



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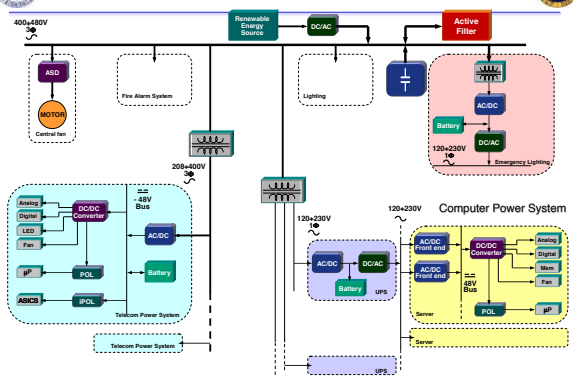

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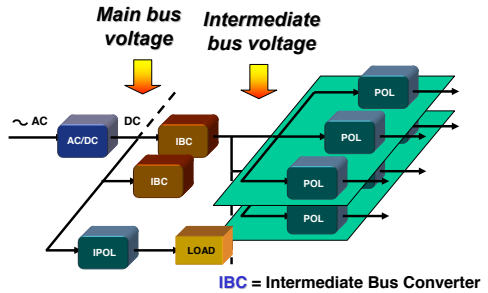
Distributed Power Architectures



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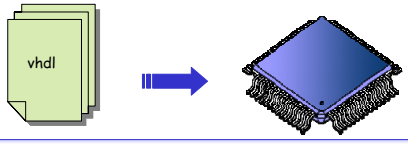
Digital Control

- Technology independent design

(Hardware Description Language - HDL)

Better resources employment

- Lower Time to market (faster design process)
- Intellectual Property - IP
- Easy scaling with advances in fabrication technologies



Critical Issues of Digital Control

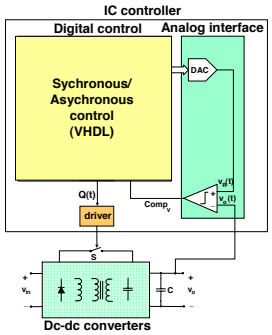
- *Lack of experienced people* in digital design and power electronics
- *Lack of understanding* and research on how to realize simple digital IC which comply with the cost/complexity constraints of computing/telecom applications
  - Specific dedicated digital or mixed-signal ICs are needed (no discrete uC or DSP)
- Quantization effects (limit cycles) and control delays (bandwidth limitation) has to be considered
- Conversion solutions and digital complexity
  - High resolution DPWM
  - High resolution AD and DA converters

Need of simple-mixed signal control architectures

Research Activities in Digital Control

- Investigating the digital advantage
  - Auto-tuning systems
  - Complex power management
- Solving the digital trouble
  - Mixed signal control architectures

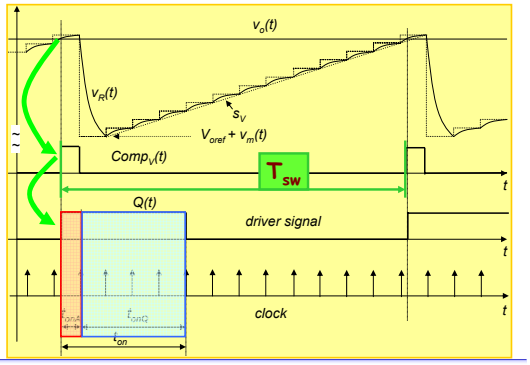
Mixed-Signal Voltage-Mode Control



Features:

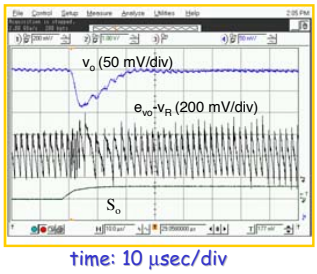
- ✓ Simple analog interface (low-resolution DAC + comparator)
- ✓ No need for ADC and DPWM
- ✓ No quantization effects
- ✓ High dynamic performance

DAC operation



Experimental Results

Load step variation



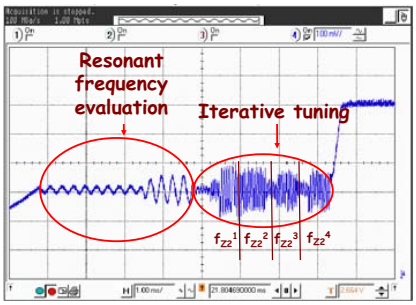
time: 10 µsec/div

Auto-Tuning System

Objective:

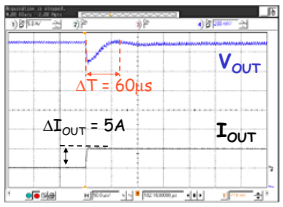
- Investigation of PID autotuning techniques for digitally controlled voltage-mode synchronous buck converters
- Features:
  - ✓Closed-loop operation during autotuning
  - ✓Direct autotuning based on specified dynamic requirement without transfer function identification
  - ✓Simple algorithm

Experimental Results



Experimental Results

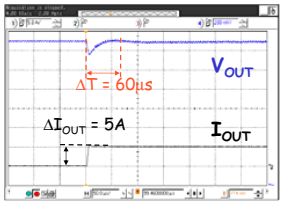
Load step variation after autotuning (f_c=13kHz, m_ϕ=60°)



C_O = 660µF

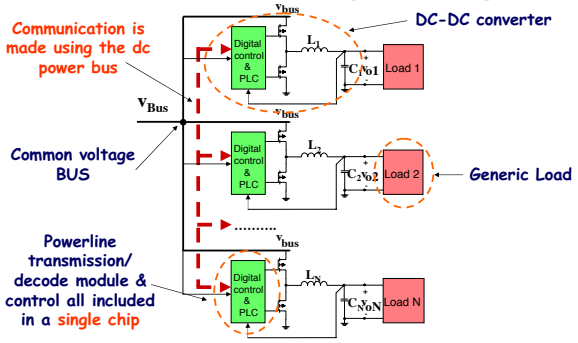
Tantalum caps

C_O = 1320µF



Power Line Communication

Distributed dc-dc converters sharing the same voltage bus



16-Phases Interleaved Buck Converter

- High number of phases enables higher switching frequencies and lower L
- The requirement for precise timing and automatic current sharing call for digital control
- Prototype
  - 16 Phases Buck converter
  - 1.56 MHz Switching Frequency (each channel)
  - ≈25 MHz Sampling Frequency
  - V_{in} = 3 V
  - V_{out} = 1 V, I_{out}=8A
  - q_{ADC} = 16 mV
  - L = 300 nH
  - C_{out} = 30 µF

Project in which our Ph.D student (Daniele Trevisan) was involved during his visit at COPEC (Colorado Power Electronics Center) - Boulder

Digital Control for 16-Phases Buck Converter