Design and development of the Control Board for the LHCb Silicon Tracker

LHCB Technical Note

Issue: 1
Revision: 1

Reference: LHCB 2007-153
Created: 15th Dec 2006
Last modified: 15th Jan 2008

Prepared By: Daniel Esperante
Achim Vollhardt

Abstract

This note is intended to give a detailed definition of the Silicon Tracker Control Board (CB) design and use. This electronic card is composed of several elements and it is the hardware part of the Silicon Tracker (ST) that will fulfil both the ST ECS (Experiment Control System) and TFC (Timing and Fast Control) tasks next to the detector. A description of the CB functionalities will be shown as well as a detailed description of its design and development.

Document Status Sheet

Table 1.1 Document Status Sheet

1. Document Title: Design and development of the Control Board for the LHCb Silicon Tracker			
2. Document Reference Number: 2007-153			
3. Issue	**4. Revision**	**5. Date**	**6. Reason for change**
Draft	1	15 Jan 08	First version

Table of Contents

1. Introduction

The Silicon Tracker Control Board has been designed and developed for controlling the ST hardware in the cavern. The hardware located in the cavern is hosted in the service boxes and detector boxes. The detector boxes host the silicon sensors and the readout electronics, whereas the service boxes contain the digitizing and control electronics. As the structure of the Inner Tracker detector and the Trigger Tracker is very similar but with a different partitioning scheme, a common control board has been designed for both detectors. Figure 1.2 shows the basic layout of the ST electronics.

This card provides the necessary functionalities to carry out several control and monitoring tasks, namely: the slow and fast control of the Silicon Tracker readout and digitizing electronics; control and monitor the LV power regulators; and the monitoring of the detector box temperatures and humidity.

A requirement that the Control Board has to meet is that the devices and components on it need to tolerate the radiation levels present in the cavern where the service boxes are located. For this reason some specific radiation hard devices developed at CERN are used. Several devices tested by our group have been chosen, and also other ones tested by other LHCb and CERN groups are used as well.

In the following sections a detailed description of the Control Board functionalities, construction and tests is shown. First we define the several functionalities that the CB has to fulfil, then comes a detailed description of all its functional blocks together with its implementation and then the tests performed on it. The layout and some other technical specifications for the construction and installation of the CBs are also shown in the final appendix.

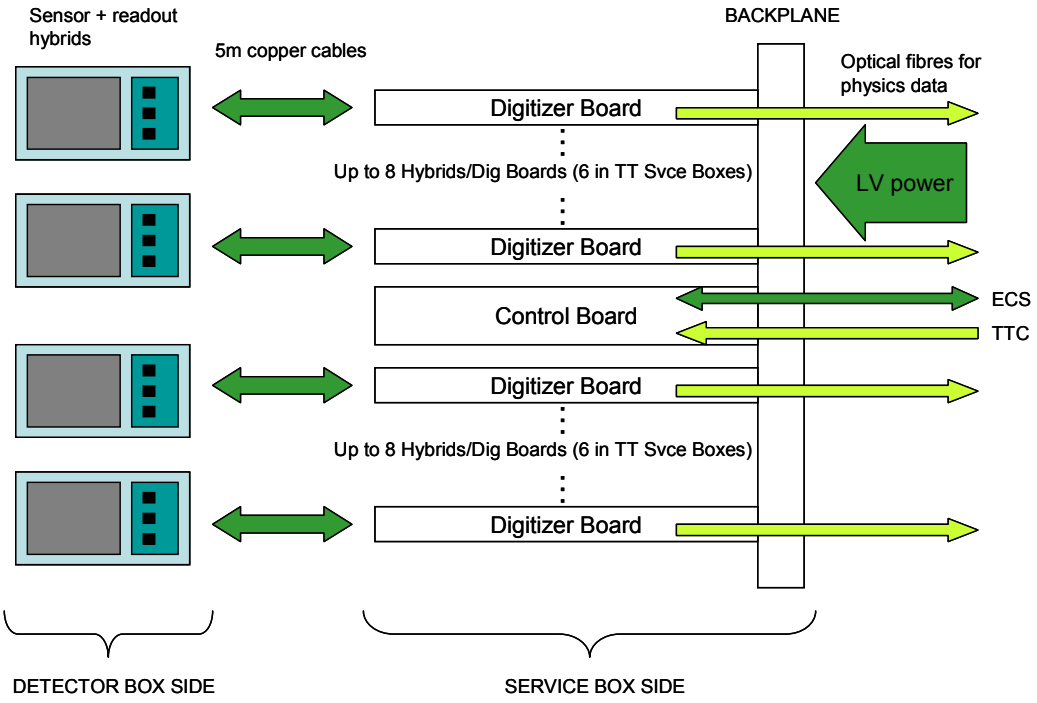


Figure 1.1: Schematic overview of the components and their connections

2. Control Board functional description

The figure 2.1 depicts the functional block diagram of the CB, and the figure 2.2 shows a prototype CB and the blocks physical distribution on it:

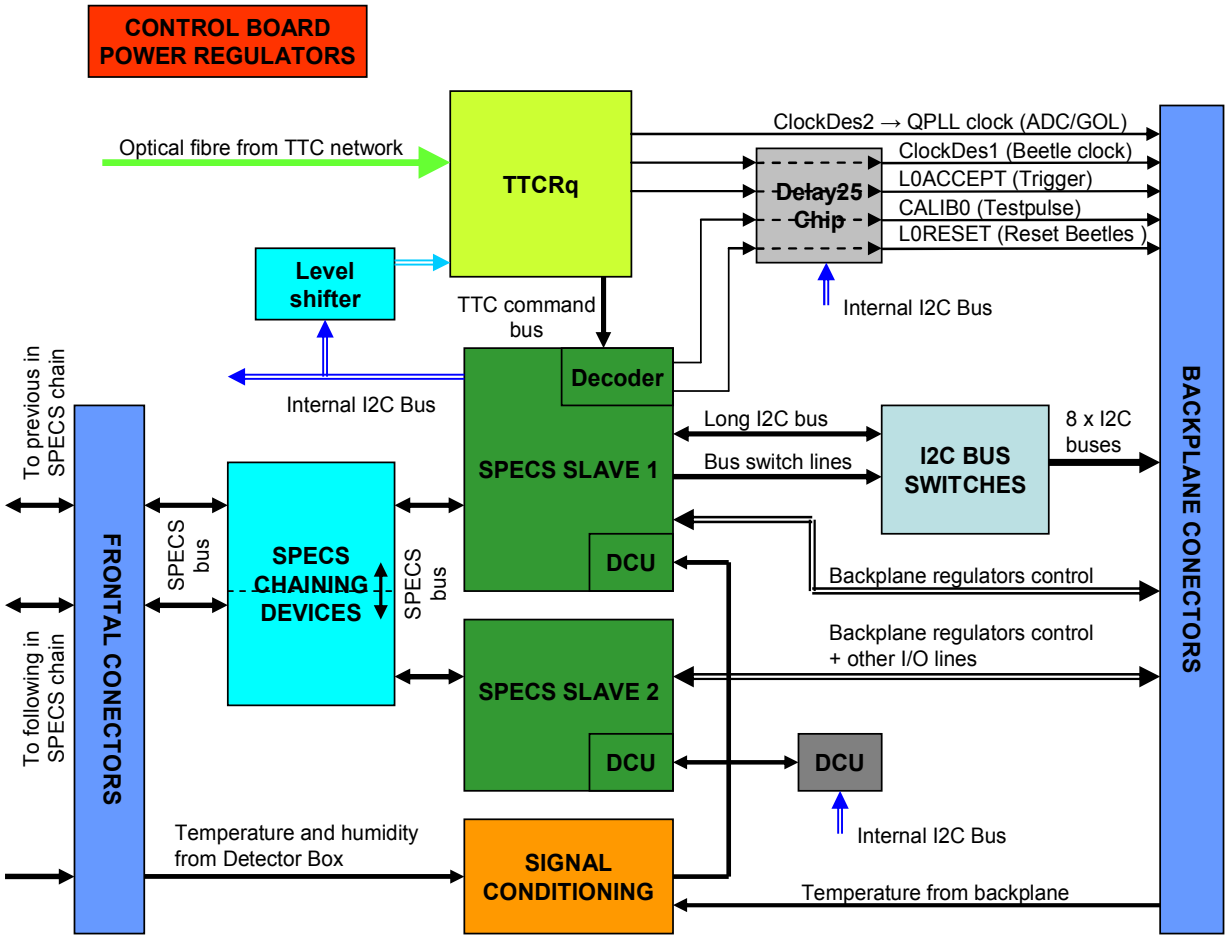


Figure 2.1:Control Board block diagram

1. **Power Regulators:** 3 LHC4913[3] power regulators for supplying the 2.5V, 3.3V and 5V needed by the CB devices.

2. **Frontal and backplane connectors:**

    a. The frontal connectors consist of:

        i. 1 SubD high density connector for the detector box environmental monitoring.

        ii. 2 RJ45 connectors for the SPECS[1] chain connection.

        iii. An AMP/Tyco 6 pin row connector for monitoring the IT half station position switches.

    b. The backplane connectors are 2 half size DIN 41612.

3. **TTCrq:** the TTCrq[2] is mezzanine card developed by the CERN microelectronics group containing the TTCrx and other associated components such as a pin-preamplifier and a QPLL.

    a. TTCrx: An ASIC receiver developed for the LHC Timing, Trigger and Control (TTC) distribution system. The ASIC implements an interface between the front–end electronics and the TTC system making the TTC coding and multiplexing schemes transparent. The receiver delivers the LHC timing reference signal, the first level trigger decisions and its associated bunch and event numbers. It can be programmed to compensate for the propagation delays associated with the detectors and their electronics. The IC supports the transmission of data and of synchronised broadcast commands.

    b. A connectorized PIN photodiode with a trans-impedance amplifier for the reception of the TFC signals from the optical TTC network. Radiation tested.

    c. QPLL: Phase-Locked Loop based on a Voltage Controlled Quartz Crystal Oscillator (VCXO). Its function is to act as a jitter-filter and clock multiplier for clock signals operating at the LHC bunch-crossing frequency (40.08 MHz). The device is implemented in a 0.25 μm CMOS technology using radiation tolerant layout practices.

4. **Delay25 chip:** it is a 5 channel CMOS programmable delay line featuring 4 channels that allow phase delaying of periodic or non-periodic digital signals and a master channel that can be used to phase delay a clock signal. The master channel serves as a calibration reference. The phase of each channel can be independently programmed with a resolution of 0.5 ns through an I2C interface. The reference clock frequency can be any of the following: 32, 40, 64 or 80 MHz.

5. **SPECS slaves:** These are two mezzanine cards hosted in the CB developed for interfacing electronic devices to the Experiment Control System. The SPECS System is composed of a PCI master card (typically located in the control room faraway form the nasty radiation environment) which can address several SPECS slave mezzanines. The heart of the mezzanines is a radiation tolerant FPGA, but it also contains a radiation hard ADC (the DCU) and some radiation tolerant LVDS drivers and receivers for driving the SPECS communication to the master. Three standard interfaces are provided by the SPECS Slave to control the components on the board or at distances of up to 10 meters: I^2C, JTAG and a (simple) parallel bus (only directly on the board), from which we only use the I^2C.

6. **SPECS chaining devices:** it is a compendium of LVDS drivers and receivers implemented in the CB for chaining many SPECS slaves in the same SPECS master link. This chaining mechanism is both used for interconnecting the 2 SPECS slaves in the CB and also for interconnecting with other CBs.

7. **Signal conditioning devices:** wheatstone bridges and instrumentation amplifiers used for temperature and humidity signal condititioning.

8. **DCU:** a radiation hard ADC used for sampling the humidity signal and some others.

9. **I2C bus switches:** a mezzanine card whose purpose is demultiplexing the "SPECS fashion"[1] long I^2C bus into 8 individual open collector compatible I^2C buses. These I^2C buses are necessary for controlling all the Beetles in the Detector Boxes and the GOLs and DCUs in the digitizer boards. A detailed description of the partitioning and I^2C address assignment is show later.

10. **Level shifter:** it consists of 2 bipolar transistors working in saturation mode which allow for translating the 2.5V I^2C generated by the SPECS slave into 3.3V necessary for TTCrq voltage compatibility.

[1] The standard I^2C protocol consists of 2 bi-directional open drain/collector communication lines. However, the "SPECS slave fashion" I^2C consists of 3 uni-directional lines (2 outputs and 1 input) and some circuitry is needed in order to interface it with standard I^2C.

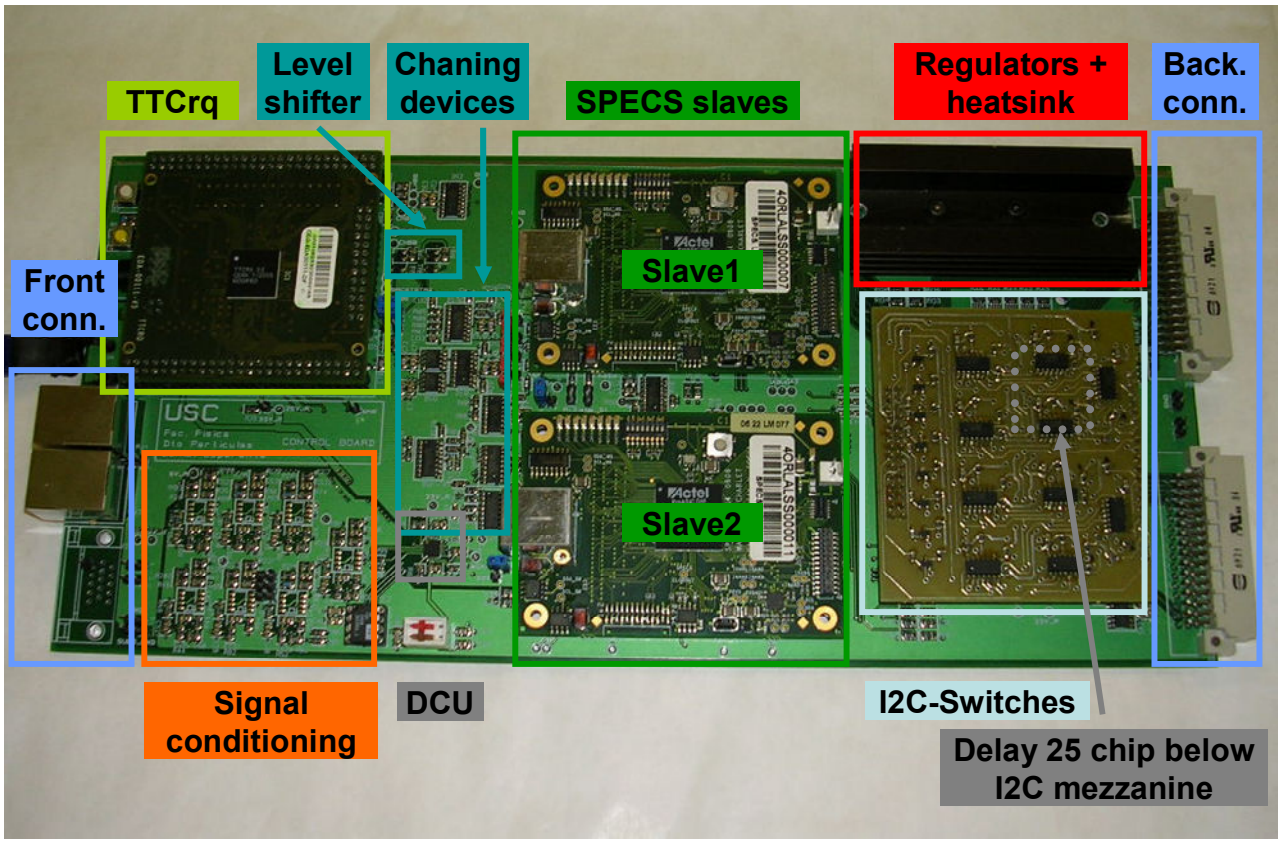


Figure 2.2 : Control Board image showing the blocks distribution

It is also of special interest the **clock and TTC signal distribution** (figure 2.15, as we'll see later. The TTCrq delivers the two clocks needed for the Beetles and the sampling electronics (clockDes1 and clockDes2), the trigger signal (L0ACCEPT) and the TTC command bus from which the L0RESET and the calibration signal (CALIB0) are decoded. The L0RESET and the TESTPULSE signal (CALIB0) are decoded in the SPECS FPGA and the decoding of the latter can be delayed by the SPECS from 0 to 16 cycles of 25ns. All these signals but the clockDes2 pass through the Delay25 chip so they can be phase delayed within a range of 32ns in steps of 0.5ns permitting a fine tuning of the signals timing.

2.1. Control Board Power regulators

The three necessary voltages (2.5V, 3.3V and 5V) for the Control Board devices are delivered by 3 rad-hard ST positive voltage regulators L4913. Two different voltages of 4V and 6.5V are supplied by the low voltage Wiener MARATON power supplies. The 4V line coming for the LV power supply will supply the 2.5V power regulator and the 6.5V will supply the 3.3V and 5V regulators.

The figure below (Figure 2.3) shows the schematic for one of the regulators. The INH line is left open since the CB must be always supplied, and the OCM line is connected to one of the SPECS I/O lines.

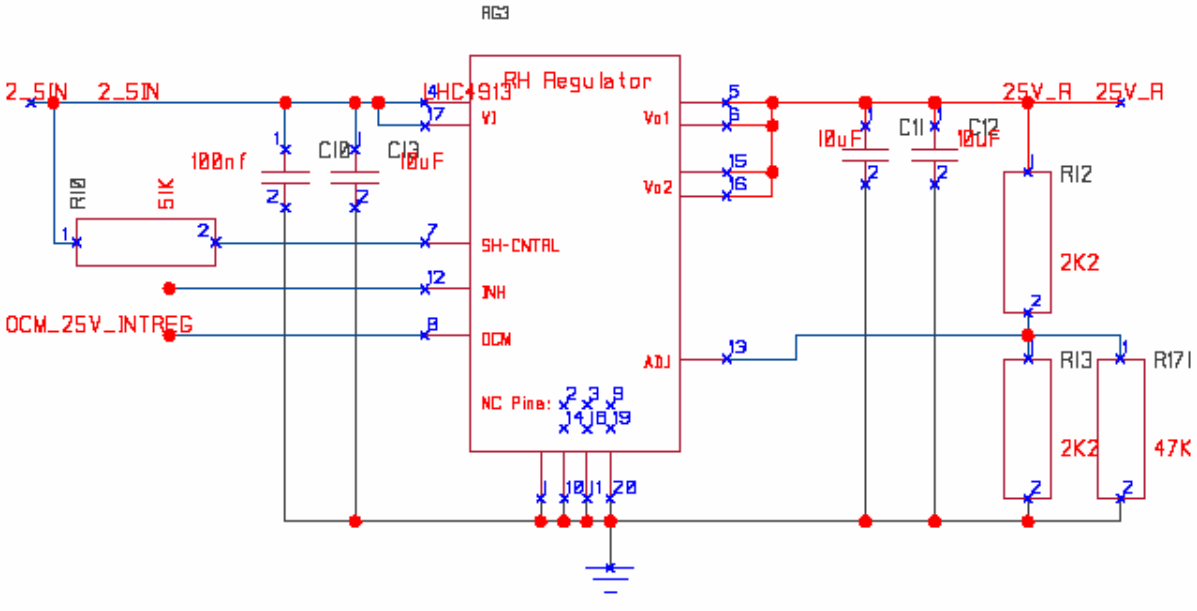


Figure 2.3: schematic design for the 2.5V voltage regulator

The 3 voltages are monitored, so there are 3 lines which go to the 3 DCU channels through a voltage divider since the maximum allowed input voltage for the DCU is 2.5V. The figure 2.4 shows the voltage divider.

2.1.1. Heat dissipation study

An important issue that becomes important when using power regulators is the thermal dissipation management. After some few calculations it is clear that heat-sinks or heat disspaters attached to the regulators are mandatory. Due to space reasons is not possible to attach a heat-sink to each regulator, but two for the group of three or building a custom cooling block.

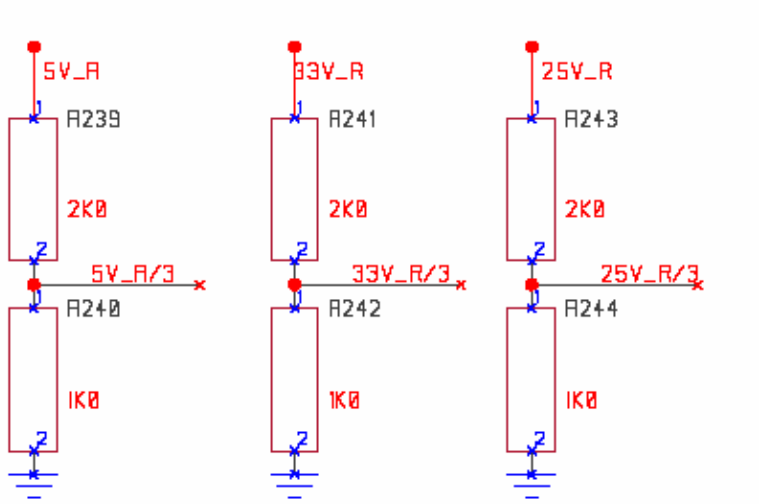


Figure 2.4: voltage dividers for power supply monitoring

Table 2.1 shows the thermal resistance for various packages taken from a ST Microelectronics note[4]. Our regulators are packaged with the PowerSO20 type and the yellow shaded cells show the values of interest for us.

Symbol	Description	PowerDIP20	SO20	PowerSO20	Unit
$R_{th\text{-}j\text{-}pins}$	Maximum Thermal Resistance Junction-Pins	12	14	-	ºC/W
$R_{th\text{-}j\text{-}case}$	Maximum Thermal Resistance Junction-Case	-	-	2	ºC/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [1]	40	51	-	ºC/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [2]	-	-	35	ºC/W
$R_{th\text{-}j\text{-}amb1}$	Maximum Thermal Resistance Junction-Ambient [3]	-	-	15	ºC/W
$R_{th\text{-}j\text{-}amb2}$	Maximum Thermal Resistance Junction-Ambient [4]	56	77	62	ºC/W

Table 2.1: Thermal resistances for the PowerSO20 package

(1) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the bottom side of 6cm2 (with a thickness of 35µm).
(2) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm2 (with a thickness of 35µm).
(3) Mounted on a multi-layer FR4 PCB with a dissipating copper surface on the top side of 6cm2 (with a thickness of 35µm), 16 via holes and a ground layer.
(4) Mounted on a multi-layer FR4 PCB without any heat sinking surface on the board.

The maximum junction temperature that the regulator can withstand is 125ºC, and the maximum power consumption will take place in the 3.3V volts regulator which will be delivering 1.5A in the TT service box.

⇒ P_j=(7-3.3)*1.5 = 5.55W.

If we don't use any kind of heatsink and we get the $R_{th\text{-}j\text{-}amb2}$ value for the SO20 we obtain a temperature difference of:

⇒ Tj –Ta = Pj * Rth-j-amb2(SO20) = 394 ºC,

which means that the junction temperature will be 394ºC higher than the ambient, so the regulator will clearly die at room temperature. Even applying reasonable layout techniques an average area of 4.7cm^2 of dissipating copper connected through many vias to the ground layer has been created for each regulator. This leads us to a $R_{th\text{-}j\text{-}amb2}$ of 52, according to the pictures2.5:

Figure 20. SO20 Junction-Ambient thermal resistance versus on-board copper area.

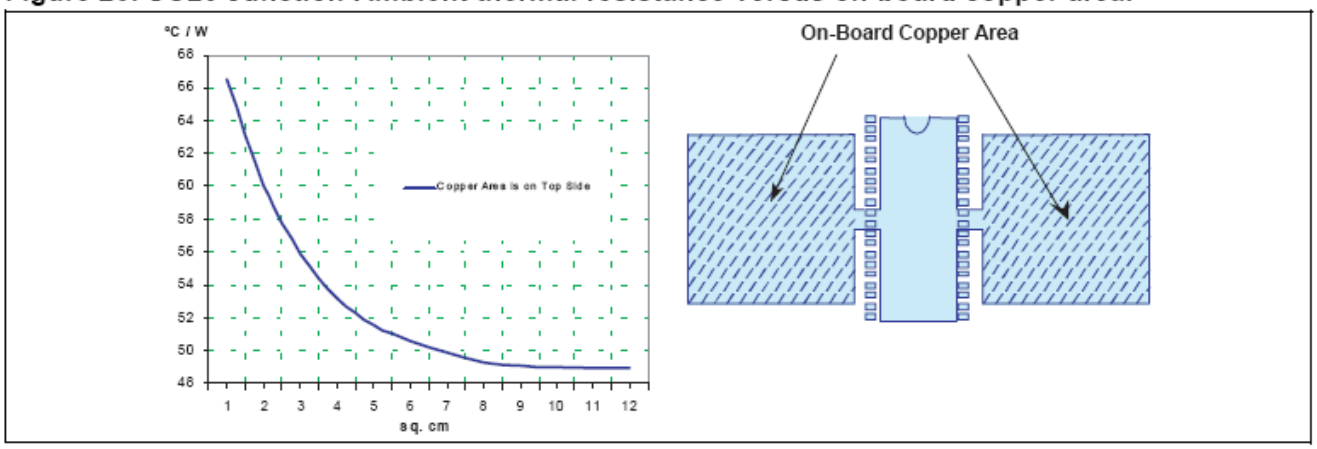


Figure 2.5: So20 mounting and Junction-Ambient thermal resistance versus on-board copper area.

This value doesn't still fit our thermal requirements:

⇒ Tj –Ta = Pj * Rth-j-amb2 (SO20 4cm2) = 288,6 ºC,

We've been making pessimistic assumptions using the SO20 thermal resistance data and supposing 4.7 cm^2, but the reliability and longevity of any semiconductor device is (roughly) inversely proportional to the square of the junction temperature change. Thus halving the junction temperature will result in approximately 4 times the expected life of the component. A worthwhile increase in reliability and component lifetime can be achieved by a relatively small reduction in operating temperature, since these parameters increase exponentially as temperature is reduced.

So it is clear that the installation of a heatsink of heat dissipater is mandatory.

The kind of package that the regulator uses is slug-up PowerSO20, so they are prepared to dissipate the power through the upper side. The junction-case thermal resistance of this package is around 2 ºC/W.

The junction to ambient thermal resistance using good layout techniques is around 53 for the SO20 package, as shown previously. This value is quite pessimistic, as the experimental data will show up.

⇒ Rth-j-case = 2 ºC/W → Thermal resistance between junction and case.

⇒ Rth-c-dis = 1 ºC/W → Thermal contact resistance between case and heatsink.

⇒ Rth-d-amb = 14 ºC/W → Thermal resistance between the chosen heatsink and ambient.

⇒ Rth-j-amb = 53 ºC/W → Thermal resistance between pin and ambient through the PCB copper.

The copper area around the regulators is ~14cm^2, so the effective area for one of them is ~4,7cm^2. We will share 2 heatsinks between the 3 regulators, so the effective thermal resistance for 1 regulator can be considered to be 3*14/2 = 21 ºC/W.

So the total thermal resistance for one regulator is:

⇒ $R_{j\text{-}amb} = (R_{th\text{-}j\text{-}case} + R_{th\text{-}c\text{-}dis} + R_{th\text{-}d\text{-}amb}*3/2) \,||\, (R_{th\text{-}j\text{-}amb}) = 16.5$ ºC/W

The regulator that dissipates most of the power is the 3.3V one, with a current of ~1.5A and a voltage drop of 3.7V in case we apply 7V to its input. So the power dissipated and the temperature difference between silicon and ambient is:

⇒ Preg33= 5.55W

⇒ Tj –Tamb = Preg33 * Rj-amb = 91.7 ºC,

Adding a parallel heatsink of 17 ºC/W to the previous one, we improve the resistance to:

⇒ Rj-amb = 11.38 ºC/W and a

⇒ Tj –Tamb = Preg33 * Rth-j-amb = 63.18 ºC.

Which is a considerable improvement.

In order to certify that the previous are realistic and even pessimistic the value of the thermal resistance has been obtained empirically: precise measurement of the current delivered by each regulator and the voltage drop on it are necessary; some temperature measurements with the electronics switched on need to be performed.

The current values for the different regulator in the CB are under the test conditions:

⇒ I3_3VReg = 0.64 A

⇒ I5VReg = 0.38 A

⇒ I2_5VReg = 0.02 A

The test has been performed with and without the 14ºC/W heatsinks plugged for three different input voltages. The temperature measurements have been performed by directly touching the regulator case with conductive glue for the T_{reg} measurement and at a distance 10cm from the regulators for the T_{amb}.

Regulators with heatsinks plugged			
V_{in}	T_{amb}	T_{reg}	$R_{j\text{-}amb}=[\ T_{reg}\text{-}T_{amb}]/[\ I_{3\_3VReg}*(V_{in}\text{-}V_{out})]$
6.5	27	51.2	$R_{j\text{-}amb}=24.2/2.048 \approx 11.8$
7	25.3	53.0	$R_{j\text{-}amb}=27.7/2.368 \approx 11.7$
7.5	25.5	56.5	$R_{j\text{-}amb}=31/2.688 \approx 11.5$
Regulators without heatsinks			
V_{in}	T_{amb}	T_{reg}	$R_{j\text{-}amb}=[\ T_{reg}\text{-}T_{amb}]/[\ I_{3\_3VReg}*(V_{in}\text{-}V_{out})]$
6.5	27	76	$R_{j\text{-}amb}=49/2.048 \approx 23.9$
7	24.6	78.1	$R_{j\text{-}amb}=53.5/2.368 \approx 22.6$
7.5	24.6	88	$R_{j\text{-}amb}=63.4/2.688 \approx 23.6$

Table 2.2: Thermal resistance empirical results

As we can see, the theoretical values have been a little bit pessimistic. We supposed the PCB copper thermal resistance to be 52 ºC/W ($R_{th\text{-}j\text{-}amb}$), when from the previous measurements we get a value around ~23. From this follows that with heatsinks plugged we obtain an experimental value ~11.7, whereas the theoretical one should be 16.5.

From the experimental results we can conclude that adding the 2 heatsinks in parallel we can obtain a thermal resistance around:

⇒ Rth-j-amb = (Rth-j-case +Rth-c-dis + [Rth-d-amb1 ||Rth-d-amb2]*3/2) || (Rth-j-amb) = (14.5 || 23.5) = **8.96 ºC/W**

And a

⇒ Tj –Tamb = Preg33 * Rth-j-amb = **49.76 ºC**.

Which is a reasonable value. This value could also be improved by setting a lower voltage at the regulators input. According to the regulator datasheet, the regulator drop-out voltage is 0.5V@I_0=1A and 1.5V@I_0=3A so an input voltage of 6.5V is high enough and implies a valuable improvement:

⇒ Pj=(6.5-3.3)*1.5 = **4.8W**.

⇒ Tj –Tamb = Preg33 * Rth-j-amb = **43 ºC**

2.1.2. Heat dissipation in the service box

Despite the careful heat dissipation study performed showing quite promising results that could lead us to think about a solution based upon air heatsinks, after installing the first CBs in the final svce boxes, the results showed up that this option is not reasonable anymore.

When having all the electronics powered working under nominal conditions, the temperature measured in the power regulators heatsink show up a value of **~70ºC** at ambient temperature of **~25ºC**. This implies a roughly estimated temperature of about **~90ºC** in the regulator silicon junction. This value has been considered to be significantly high for operating the regulator in the long term so the decision of building water cooled cooling block (Figure 2.6).

This discrepancy in the measured value when running the CB once installed in the final svce box with respect to what has been shown previously comes from 3 main points:

1. The previous calculations are performed assuming an input voltage value of 6.5V, while in the experiment up to 7.3V are foreseen.

2. In the previous tests, the heat dissipation coming from other neighbouring boards was not taken into consideration.

3. The values for the heat dissipation resistances of the heatsinks are given taking into account a "good" convection, that is, they are foreseen for being used in horizontal position. In the service box all the boards are installed vertically so the effectiveness of the heatsink fins gets considerably worse and hence the effectiveness of the heatsinks.

Apart from the previous reasons, we could add 2 more for the TT svce boxes:

1. The 3.3V regulators has to deliver ~0.6A of extra current since the power for the backplane clock LVDS drivers is taken from the CB itself.

2. The TT svce boxes are installed in the columns of 6, so the CB in the top would always be running at higher environment temperature than the other ones.

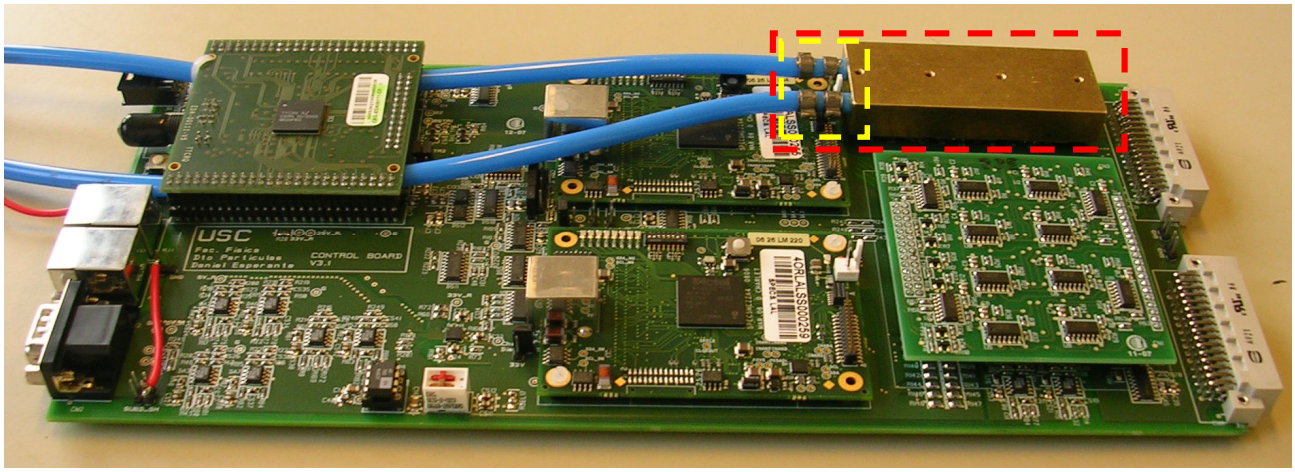


Figure 2.6: Final Ctrl Board with water cooled cooling block

The cooling block has already been tested in the lab and has been found to be effective for dissipating the power under nominal working conditions. The only weak point of this solution has been to found to be potential leaks on the hose to cooling block connection.

When running in the final experiment a water pressure in the outlet circuit of ~3-4 bar is foreseen so the pressure in the inlet must at least range from 4 to 5 bar so that we guarantee a minimal water flow. Pressure tests up to 10 bar have been carried out in the lab and after some research and several trials we've decided to adopt the following solution: clamp the hoses to the cooling block with 2 rings (see yellow box in the picture) and use some *Araldite* glue. Like this a leak tight connection can be achieved.

For more safety each cooling block has been individually temperature cycled and tested at 10 bar before it was mounted on the Control Board.

2.2. Frontal and backplane connectors

The CB features two connectors for linking to the backplane in the rear side and 4 in the front side for connecting the "outside world". The backplane connectors are two half size DIN 41612, whereas the frontal

ones are 2 RJ45 for SPECS communication, 1 SubD high density 15 pin for environmental signals and one additional one for monitoring the box position switches.

2.2.1. Backplane connectors

The Figure 2.7 shows the backplane connectors and the signal/pinout assignment.

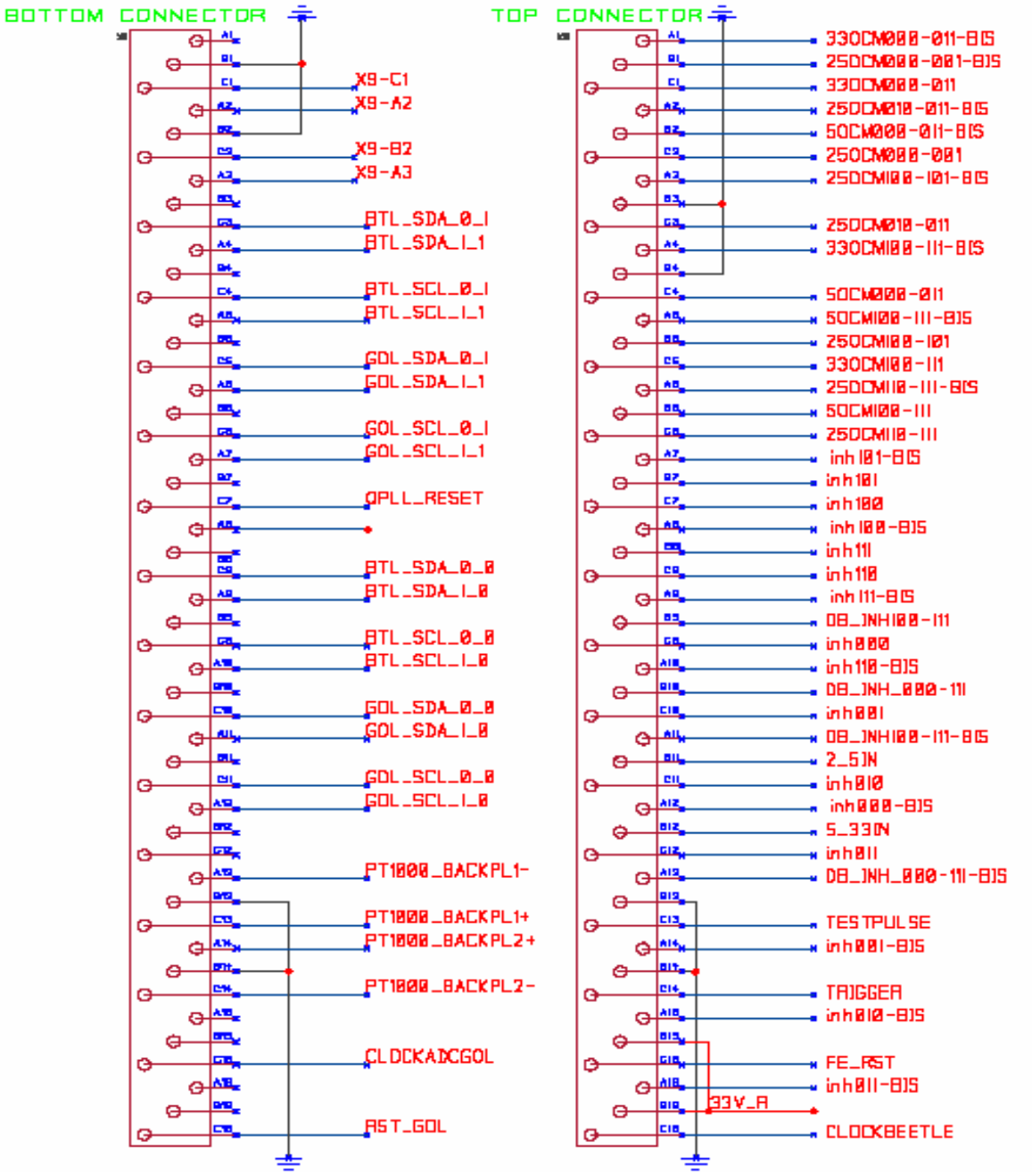


Figure 2.7: Backplane connectors

Regulators control and monitoring signals are located in the top connector and the I2C and backplane temperature monitoring in the bottom one. The power lines are in the top connector and there are ground connections in both of them. The TFC signals (TESTPULSE, TRIGGER; FE_RST, CLOCKBEETLE, CLOCKADCGOL, RST_GOL) are also distributed in both.

2.2.2. Frontal connectors

There are 4 connectors in the frontal side:

1. The ECS connector (Figure 2.8), for the detector box environmental measurements. It provides 8 lines for the 4 PT1000 sensors (2 lines per sensor), 4 lines for the HMX2000 humidity sensor (2 for sensor biasing and 2 for the sensor signal output) and 3 lines for a non rad-hard HIH-3600 humidity sensor which could be used for calibration and testing purposes. A more detailed explanation on how the biasing and readout of the sensors is done is explained in section 2.7.

   - Connector type: 15 pin high density male SUB-D connector.
   - Signals:
     1) *PT1000_2-* : 2nd PT1000 sensor inverting pin.
     2) *RH_HIH_SIG* : HIH-3600 humidity sensor voltage output.
     3) *RH_VEXC-* : HMX2000 sensor negative bias pin.
     4) *RH_VEXC+* : HMX2000 sensor negative bias pin.
     5) *RH_VSIG+* : HMX2000 sensor non inverting signal output pin.
     6) *PT1000_4-* : 4th PT1000 sensor inverting pin.
     7) *PT1000_2+* : 2nd PT1000 sensor non inverting pin.
     8) 5V_R: 5V from regulator. This connection is left open unless the jumper is plugged (figure 2.8). It was foreseen for the HIH-3600 supply.
     9) GND: Ctrl Board ground. This connection is left open unless the jumper is plugged (figure 2.8). It was foreseen for the HIH-3600 ground.
     10) *RH_VSIG-* : HMX2000 sensor inverting signal output pin.
     11) *PT1000_4+* : 4th PT1000 sensor non inverting pin.
     12) *PT1000_3-* : 3rd PT1000 sensor inverting pin.
     13) *PT1000_3+* : 3rd PT1000 sensor non inverting pin.
     14) *PT1000_1+* : 1st PT1000 sensor non inverting pin.
     15) *PT1000_1-* : 1st PT1000 sensor inverting pin.

2. The two RJ45 connectors for the SPECS bus (Figure 2.9). The upper connector carries the signals coming from the previous SPECS slave or from the master, and the lower one is for connecting to the next CB in the chain. The used cables must be shielded CAT6 Ethernet cables with 100Ω differential impedance.

   - Connector type: 8 pin RJ45.
   - Signals for connector RJ1(the upper one):
     1) *SDA_MS1_IN-* : SDA master to slave -.
     2) *SDA_MS1_IN+* : SDA master to slave +.
     3) *SCL_MS1_IN-* : SCL master to slave -.
     4) *SCL_SM1_OUT+* : SCL slave to master +.
     5) *SCL_SM1_OUT-* : SCL slave to master -.
     6) *SCL_MS1_IN+* : SCL master to slave +.
     7) *SDA_SM1_OUT-* : SDA slave to master -.
     8) *SDA_SM1_OUT+* : SDA slave to master +.

- Signals for connector RJ2 are equal to the RJ1 but instead of connecting to the slave1 (the upper one), they connect to the slave2.

3. The station position monitoring connector. This extra connector (Figure 2.10) has been added for monitoring the voltage value of the position monitoring switches. This monitoring capability can be used provided that a shielded cable is used and the input signals are protected against over and under-voltages that could damage the electronics.

   - Connector type: double row header, 2x4 way right angle, 2.54mm, from TYCO electronics.
   - Signals:

     1) *AMP_SH* : This is the pin where the cable shield must be connected.
     2) *AMP_CON1*: beam pipe distance monitoring digital output 1.
     3) *AMP_CON2*: beam pipe distance monitoring digital output 2.
     4) *AMP_CON3*: beam pipe distance monitoring digital output 3.
     5) *AMP_CON4*: beam pipe distance monitoring digital output 4.
     6) *33V_R* : 3.3V from Ctrl Board regulator.
     7) *GND* : Ctrl Board ground.
     8) *GND* : Ctrl Board ground.

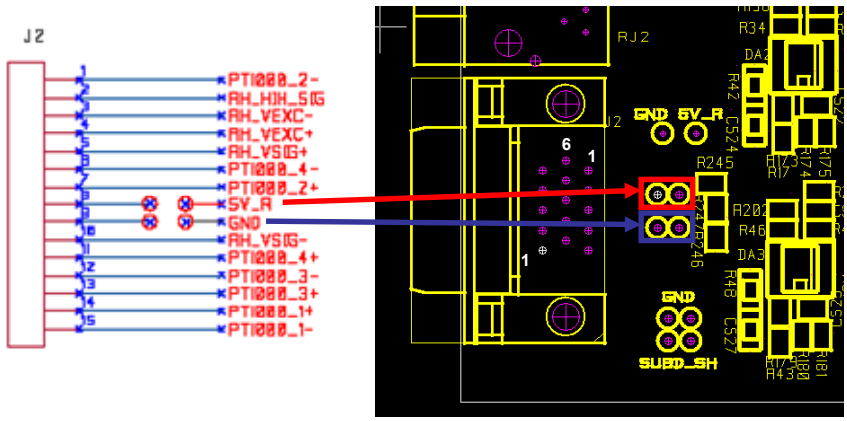


Figure 2.8: ECS connector pinout

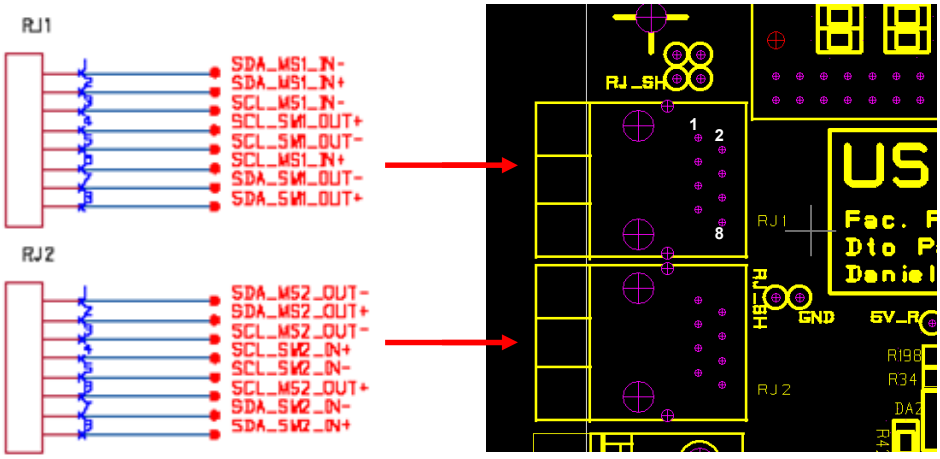


Figure 2.9:RJ45 SPECS connectors

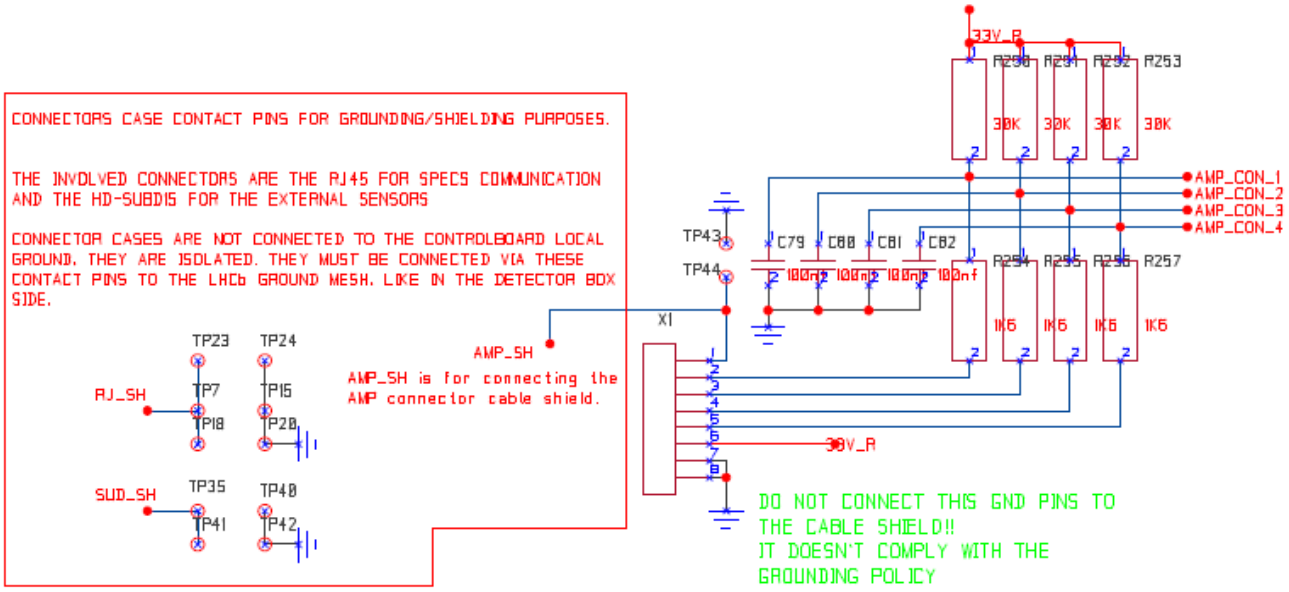


Figure 2.10 : Beam pipe approach monitoring connector and cable shield connections

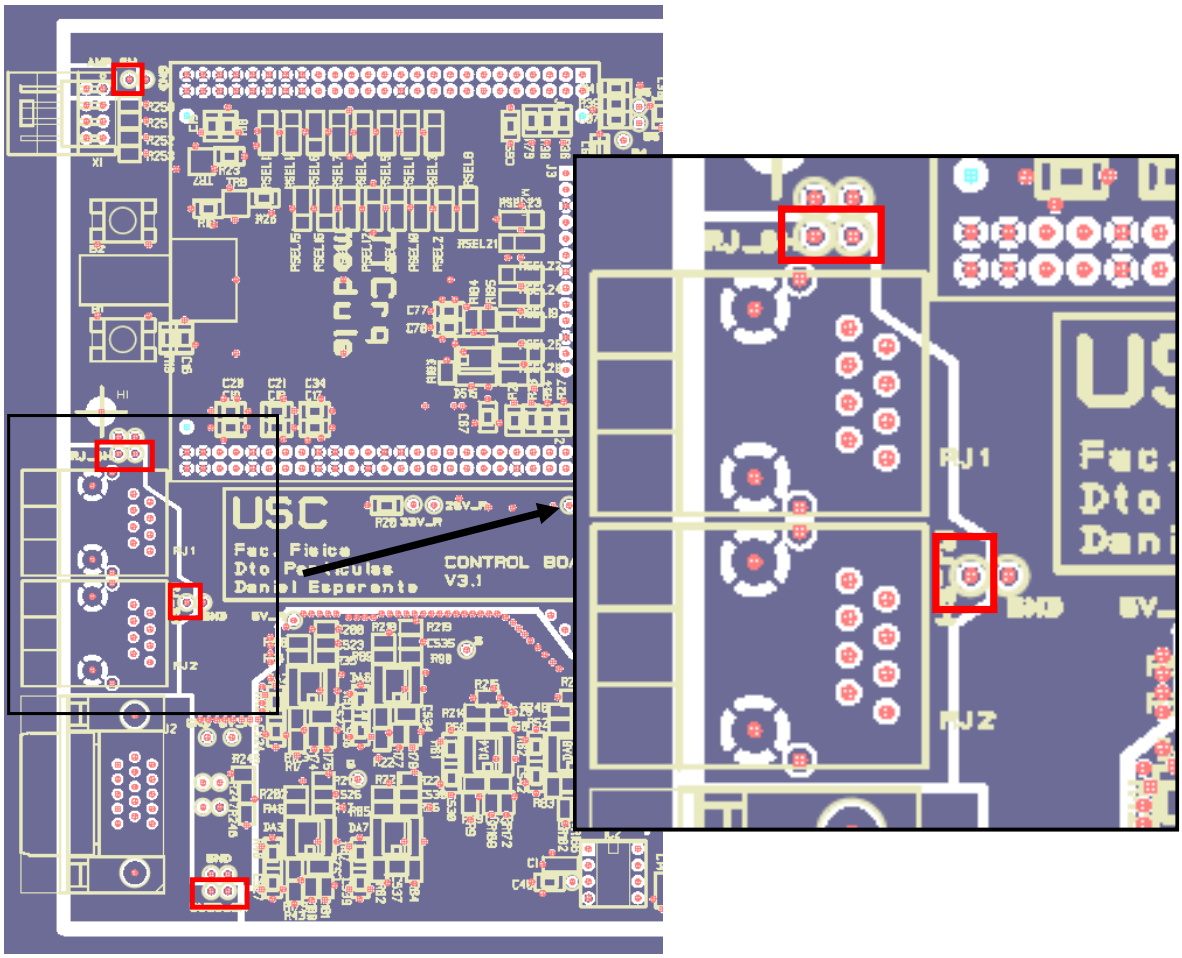


Figure 2.11: Ctrl Board ground layer view showing the connectors metal case connection pins. For each connector a copper island has been implemented in the Control Board ground layer. The red boxes enclose the pins that permit connecting the cable shields to the ground mesh for complying with the grounding and shielding policy. The zoomed view shows the SPECS RJ45 metal enclosure connections.

The shields from the cables connecting to the frontal part of the Control Board must be connected to the LHCb ground mesh in order to comply with the Silicon Tracker grounding policy [6]. For this reason, isolated copper areas have been created in the Ctrl Board ground layer for interconnecting the connector cases to some pins implemented next to the connectors (see Figure 2.11).

2.3. TTCrq

As already mentioned, the TTCrq is a mezzanine card developed by the CERN microelectronics group containing the TTCrx ASIC and other associated components such as a pin-preamplifier and a QPLL (more info in [7]). This card is located in the CB frontal side edge because this mezzanine is the interface to the TTC optical network. The TTCrq features a connectorized PIN photodiode with a trans-impedance amplifier which connects to the TTC network.

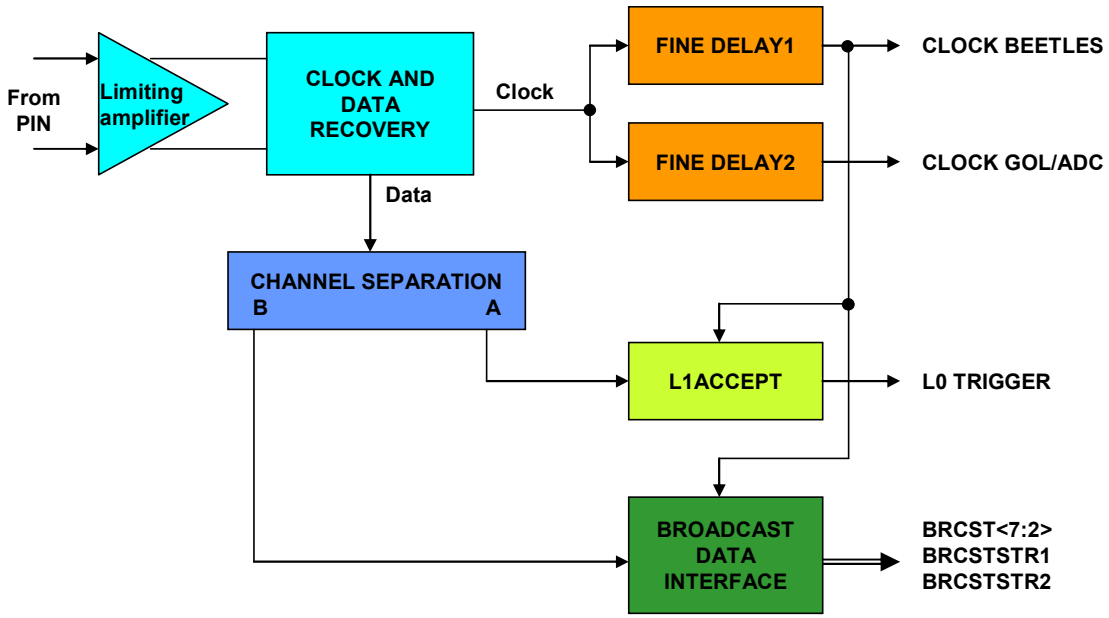


Figure 2.12: TTCrx simplified block diagram

The TTCrx ASIC implements an interface between the front–end electronics and the TTC system making the TTC coding and multiplexing schemes transparent for us. Among the TTC signals that the TTCrx delivers, the following ones (using the TTCrx signal naming convention) need to be handled in the CB, as depicted in the TTCrx simplified block diagram (figure 2.13):

- **Clock40Des1:** this is the 40.08 MHz deskewed reference clock 1. The fine phase delay factor is controlled by writing into the "fine delay register 1". Both the L1Accept signal and the channel B broadcast command signals are synchronized to the Clock40Des1 signal. This signal also provides the clock for the Beetle chips, so that the reset signal will arrive at the Beetle with a fixed phase relation. The same applies for the calibration signal. However, its phase relation has to be adjustable with respect to the Beetle clock to perform timing scans of the front-end electronics. This is accomplished by using the delay25 clock delay chip together with the SPECS chanB decoder.

- **Clock40Des2:** this is the 40.08 MHz deskewed reference clock 2 controlled by the "fine delay register 2". This output is used to provide the ADCs and the GOL serializers with a clock. As the Clock40Des2 output can be independently shifted with respect to the Clock40Des1 output, the timing relation between the Beetle and the ADCs can be adjusted to optimize the sampling point of the ADCs on the Beetle data. After this optimization has taken place, Clock40Des1 and Clock40Des2 can be shifted together to optimize the timing of the readout with respect to the particle passage through the detector.

- **L1Accept:** First level trigger-accept signal. Although in the TTCrx manual it is named L1Accept, in LHCb this signal corresponds to L0 trigger signal.

- **Brcst<7:2>:** Bits from 2 to 7 of the broadcast command. Among other commands, it distributes the L0RESET and CALIBRATION signals. An additional decoder implemented in the SPECS slave is used to generate the L0RESET and TESTPULSE signals.

- **BrcstStr1:** Broadcast command strobe for validating newly received broadcast data. It is synchronized to the clock40Des1.

- **BrcstStr2:** Broadcast command strobe for validating newly received broadcast data. Not used.

The TTCrq needs 3 different supply voltages: 2.5V for the QPLL, 5V for the PIN preamplifier and either 3.3V or 5V for the TTCrx. We've decided to supply the TTCrx with 3.3V since TTCrx timing characteristics are better (jitter is lower) although it is a little less immune to SEUs. Using 3.3V also eases the design since it is voltage compatible with the SPECS fpga (broadcast command decoder is implemented in the SPECS FPGA). The figure 2.13 shows the schematic for the TTCrq.

The TTCrx is controlled using the internal I2C line from the SPECS slave1 and a level shifter to 3.3V as will be explained in section 2.5.1. The I2C address for the TTCrq has been set to "b'101111X" by external resistors in the CB.

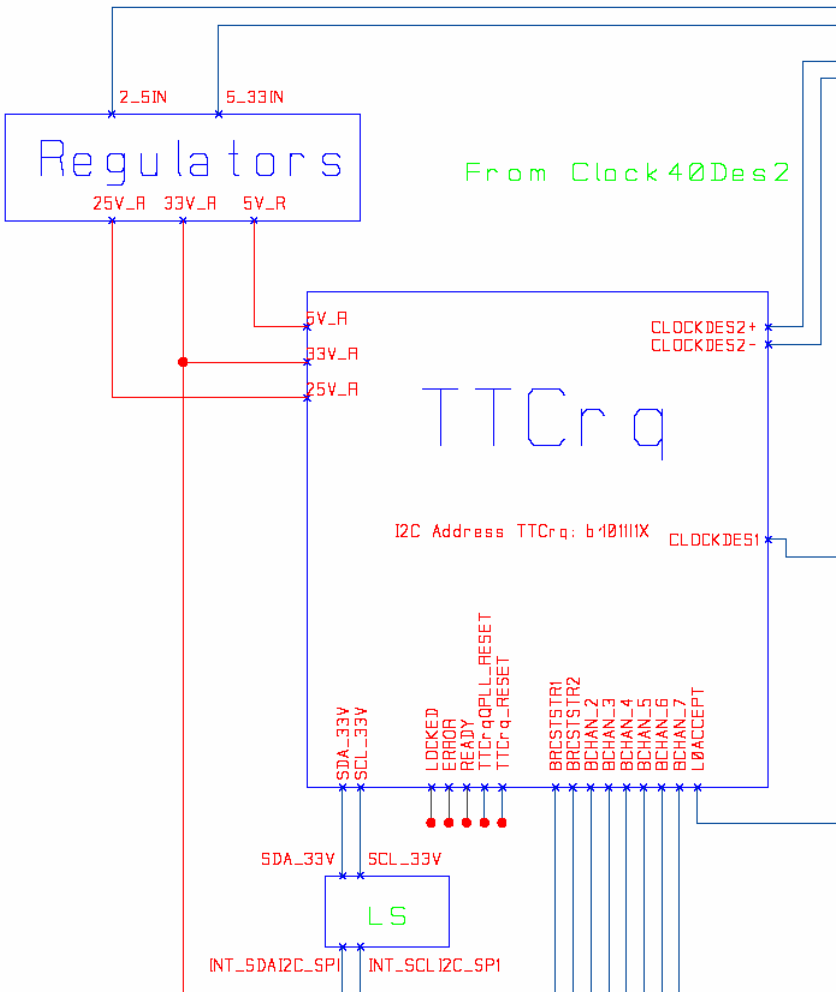


Figure 2.13: TTCrq schematic block diagram

The following lines of the TTCrq are also connected to the SPECS I/O register lines:

- QPLL reset line → TTCrqQPLL_RESET (input).

- TTCrx reset → TTCrq_RESET (input).
- QPLL locked flag → LOCKED (output).
- QPLL error flag → ERROR (output).
- TTCrx ready → READY (output).

In order to use the TTCrq in the way described above (Clock40Des1 for the Beetles, Clock40Des2 for the GOL's and source the QPLL with the Clock40Des2), some few modifications had to be performed on it. According to the TTCrq schematic shown in the TTCrq manual [7], the modifications are the following (see in figure 2.14 the bottom layout of the TTCrq and the modifications):

- Move R40 to R41: this way we source the QPLL with the Clock40Des2.
- Change ST19: so we hardwire the Clock40Des1 to the pin 2 of the J1 connector.
- Remove R55: the QPLL LVDS output clock (Clock40Des2) must be terminated in the Control Board, so this termination resistor in the TTCrq must be removed.
- Remove the 2.5V regulator and solder R59 (0Ω). As the TTCrq internal regulator is not radiation tolerant, doing this we can supply 2.5V to the TTCrq through the pin 39 of connector J2.

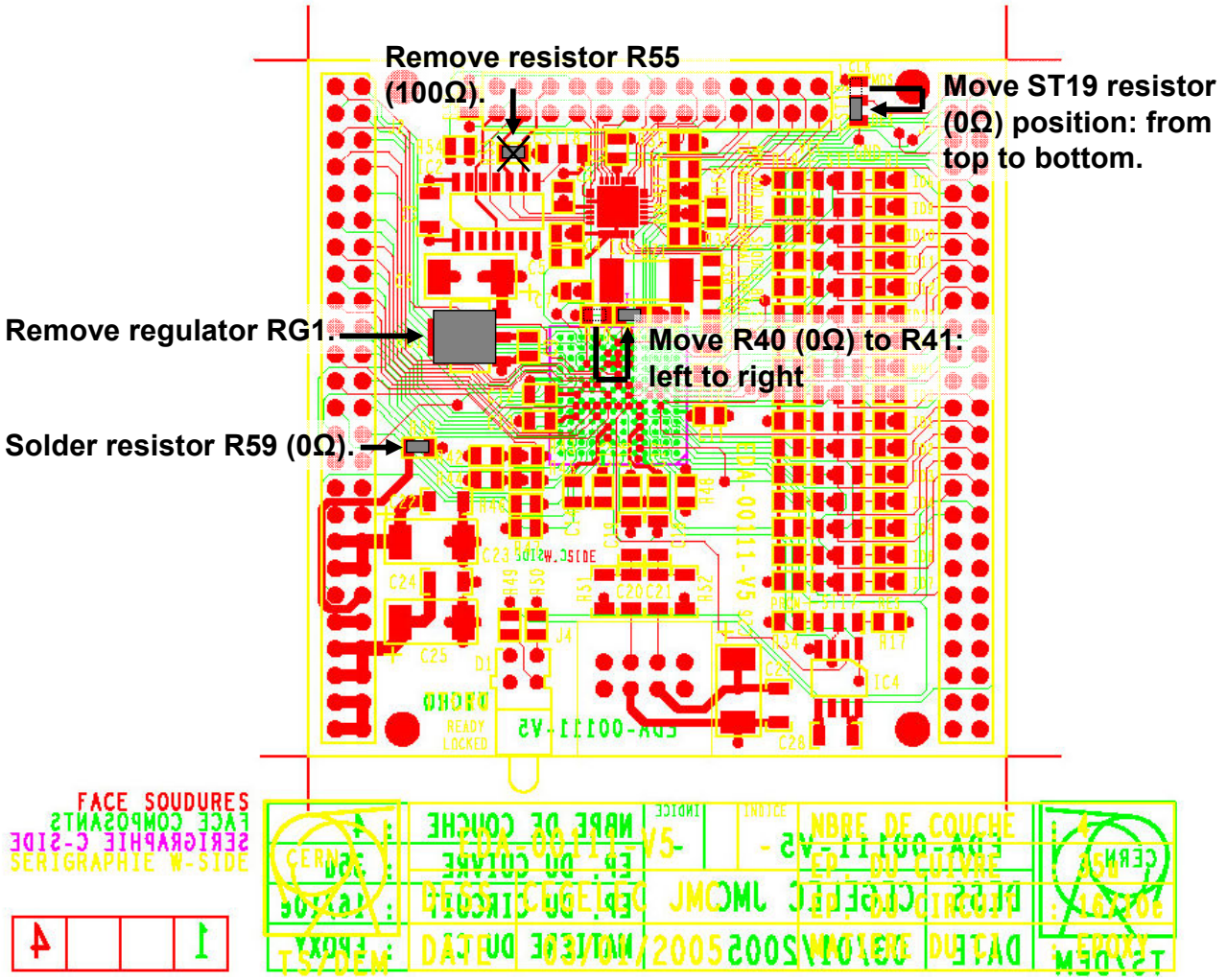


Figure 2.14: TTCrq modifications

2.3.1. The TTC and clock signal distribution

The figure 2.15 shows the clock and TTC signal distribution diagram implemented in the CB.

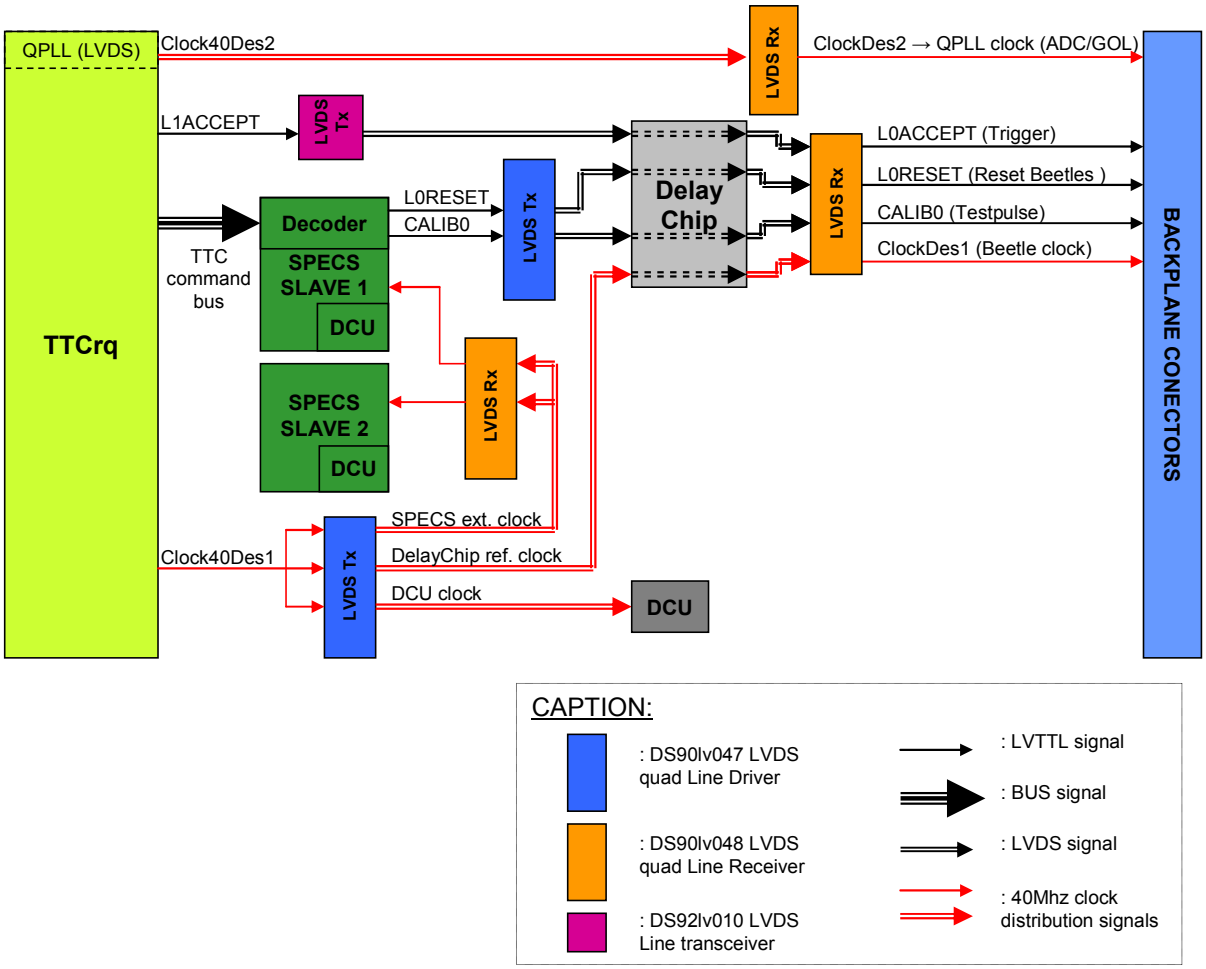


Figure 2.15: 40Mhz clock and TTC signals distribution diagram

The TTCrq delivers two different clocks (clockDes1 and clockDes2), the trigger signal (L0ACCEPT) and the TTC command bus from which the L0Reset and the calibration signal are decoded. The L0RESET and the TESTPULSE signal (CALIB0) are decoded in the SPECS FPGA and the decoding of the latter can be delayed within the SPECS in steps of 25ns. All these signals but the clockDes2 pass through the Delay25 chip so they can be phase delayed within a range of 32ns in steps of 0.5ns.

The TTC command bus and the L0TRIGGER signals are synchronized to the clockDes1, so this is the clock which must drive the SPECS slaves. The Delay25 chip needs a reference clock for the signals that it must time delay, so the clockDes1 can be used. As the DCU also needs a 40MHz differential clock, this clock signal is used as well.

For distributing these signals, LVDS radiation tested transmitters and receivers situated close to driving or receiving device have been used. The signals delivered by the TTCrq, the ones arriving at the SPECS decoder and the signals that go to the backplane connectors need to be 3.3V CMOS/TTL[2] compatible, but a translation in between to LVDS is done. There are many reasons for this translation to LVDS and then back to single ended:

- The difficulty of finding reliable radiation tolerant devices for redistributing the clock signal to many devices. These LVDS transmitters and receivers have been qualified for radiation beyond the levels present in the Silicon Tracker svce. boxes.

[2] Except the Clock40Des2 from the TTCrq QPLL which is LVDS.

- The track lengths of most of these signals is more than 25cm, so using LVDS signalling avoids signal integrity and EMC/EMI problems that can easily appear in single ended mode, such as undesirable reflections that can cause EMI or increase clock jitter.

- The voltage compatibility. The TTCrx and the SPECS work at 3.3Vand are LVTTL compatible, but the Delay25 chip is only 2.5V and LVDS compatible. So translating all of them to LVDS makes the interconnection feasible.

- The DCU needs a differential 40MHz clock.

- The Clock40Des2 from the TTCrq is LVDS.

- These LVDS drivers have an enable/disabled line, so the interruption of the signals transmission can be controlled by the SPECS.

2.4. Delay25 Chip

The Delay25 is a 5 channel CMOS programmable delay line featuring 4 channels that allow phase delaying of periodic or non-periodic digital signals and a master channel that can be used to phase delay a clock signal. The phase of each channel can be independently programmed with a resolution of 0.5 ns in a range from 0 to 32 ns. The chip can be controlled and configured via I2C.

The master channel, which serves as a calibration reference, is the “clock40Des1”. We use the delay chip to phase delay the L0RESET the L0ACCPET and the CALIB0 signal, so all of the TTC signals can be time aligned. The signal/channel assignment is the following:

- Channel 0 → empty
- Channel 1 → L0RESET.
- Channel 2 → L0ACCEPT.
- Channel 3 → CALIB0.
- Clock channel → Clock40Des1.

The delay25 reset line, active at low level, is connected to a specific reset output of the SPECS slave1, as will be shown in the SPECS blocks diagram in section 2.5.5.

The input and output buffers of the channels can either work in single ended CMOS or in LVDS mode. We use it in LVDS mode as mentioned earlier. This is done by setting the IOMODE pin to “1”.

The chip is connected to SPECS internal I2C bus. The chip address is set to “b’0100XXX” as can be seen in the figure 2.16. The XXX address bits indicate which of the delay25 chip internal register is being accessed.

2.5. SPECS slaves

SPECS is a single master multi-slave bus, designed to allow a simple, fast and cheap means of communication between electronics systems [1]. It is also designed to be efficiently protected against errors, and to be flexible.

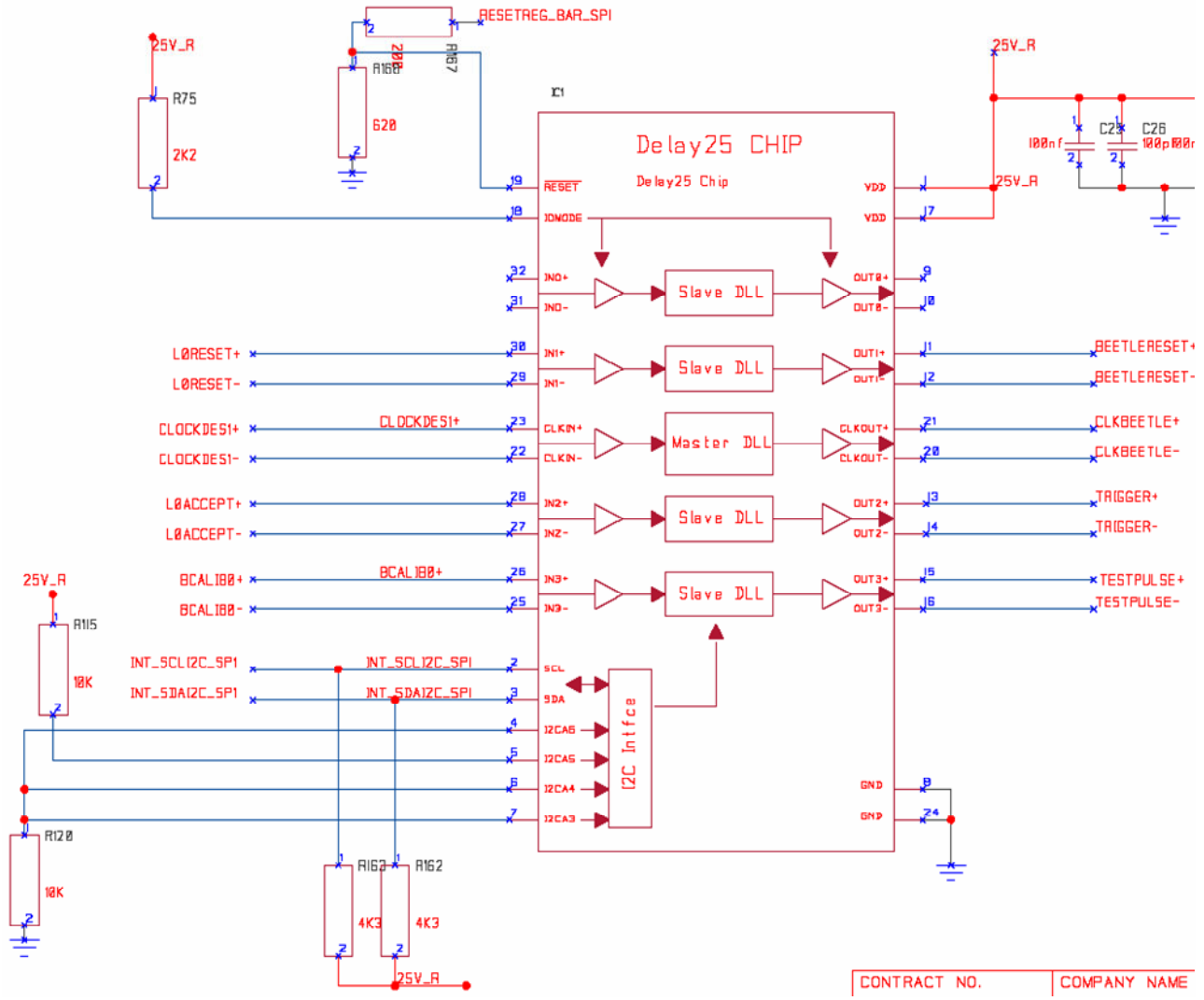


Figure 2.16: Delay25 chip schematic connections

The SPECS slaves are the devices that allow interfacing all our chips in the service boxes and detector boxes. They are implemented as mezzanine cards which provide several communication interfaces such as I2C, JTAG and parallel bus, and also other features like TTC channelB decoding, programmable I/O registers … The list of features that a mezzanine can provide is next:

- One long distance point to point differential SPECS interface (coming from the SPECS master).
- One unipolar SPECS local interface for multi-load bus applications.
- Two local I2C buses of 2.5V and 3.3V.
- One output for long distance I2C.
- One JTAG bus.
- 12 JTAG or 12 I2C chip-select control bits for external drivers.
- 12 JTAG or 12 I2C direction control bits for external drivers.
- One parallel bus offering 16 data bits and 8 address bits.
- One decoder for the channel B of the TTCrx, decoding:
    - L0 front-end reset,
    - Calibration pulse type 0, which can be delayed with a programmable counter.
- One 32-bit static register to control or read back the local environment. The bits [31:24] can be individually configured either in output or in input mode. In input mode, they may be configured as

an interrupt vector, each of them being then able to generate a SPECS interrupt. The bits [23:0] can be individually programmed in input or output mode. This register does not need any external clock to be written by the SPECS. After a hardware reset, all I/Os are configured in input mode by default for safety reasons. Thus pull-up resistors may be necessary if some levels are mandatory at power-up.

- One reset signal. This output can be triggered without the need of any clock on the board.
- One local 40MHz oscillator. It is also provided as an output of the mezzanine and can be enabled by the software.
- One EEPROM which will allow the ECS system to obtain some information about the front-end element housing the mezzanine. It can be read and written by one dedicated I2C bus.
- One DCU chip with 6 ADC channels of 12 bit resolution and 1 non calibrated temperature channel.

The figure 2.17 represents the block diagram of the SPECS slaves use in the CB. The functionalities we use are the following:

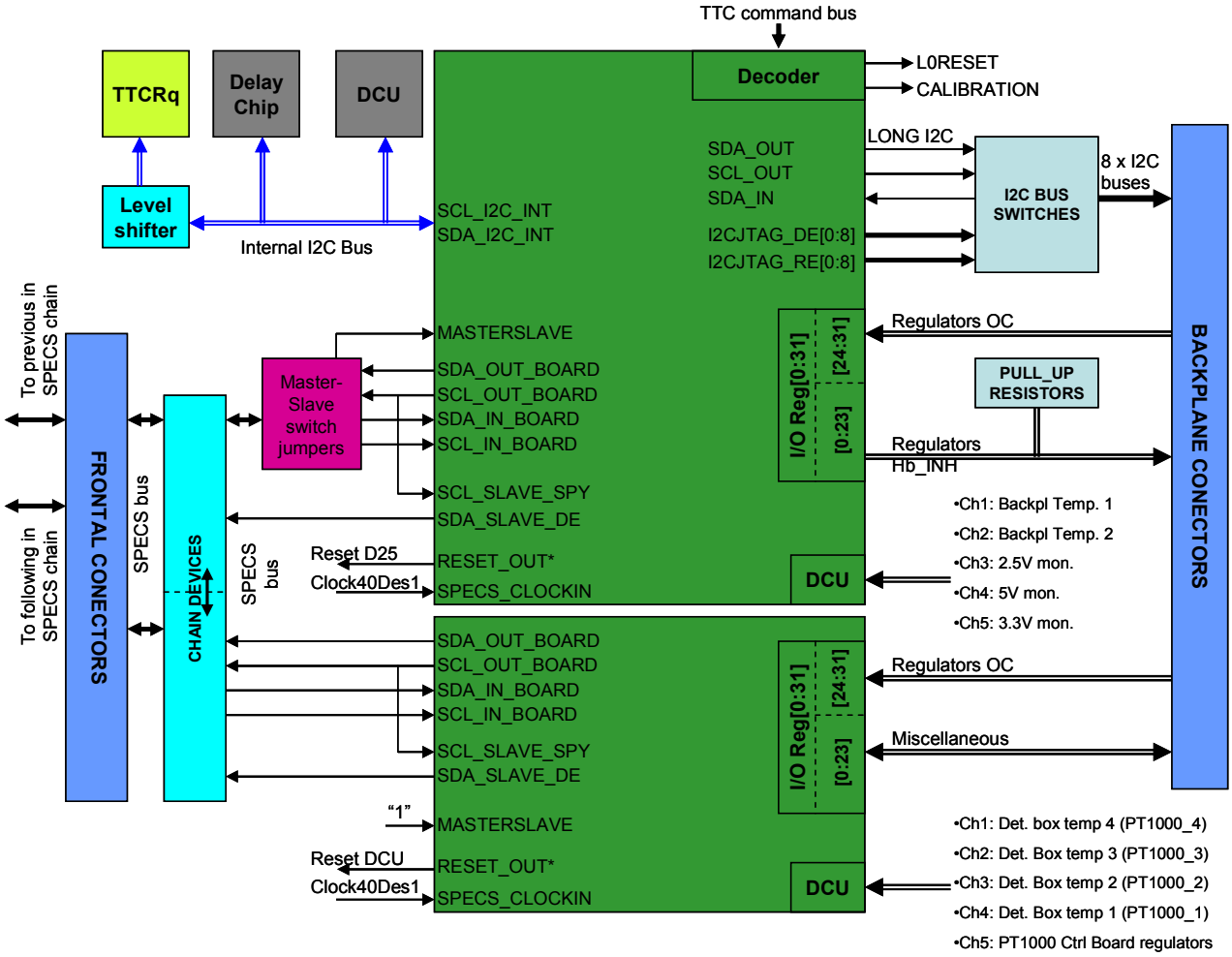


Figure 2.17: SPECS slaves block diagram

- The internal I2C of the Slave1 for interfacing the TTCrq, the Delay25 chip and the CB DCU.
- The ChanB decoder of the Slave1.
- The long distance I2C lines together with the first 8 I2C chip-select and direction control bits of slave1.
- The single-ended SPECS local interface for multi-load bus applications of both slaves.
- The reset outputs of both slaves

- The I/O configurable register of both slaves.
- The DCU's of both slaves.

Although it's not show in the diagram, also the internal oscillator and the PROM will be used.

2.5.1. The internal I2C bus

For onboard I2C slaves, an I2C bus is implemented by the mezzanine. It is based on the 2 SPECS signals: *scl_i2c_int* and *sda_i2c_int*. This implies that a 2.5 V logic level has to be used instead of the usual 3.3 V level on this SDA line.

The Delay25 chip, the DCU and the TTCrq hosted in the CB will be controlled using this internal I2C bus. Both the Delay25 chip and the DCU can not work with I2C levels other than 2.5V, so that's why we use this bus for them. However, the TTCrq works at 3.3V and this is the reason for the addition of a level shifter (see section 2.10). The possibility of directly using a 3.3V I2C bus coming from the SPECS slave has been left open. In principle two lines have been reserved in the SPECS mezzanine for a 3.3V bus, so they have been routed to a switch made of jumpers where we can chose either using the level shifter or the internal 3.3V SPECS I2C bus. By default the jumpers are set for using the level shifter (see figure 2.18).

This bus must work at frequencies not much higher than 100Khz, so attention must be paid when using the SPECS slaves internal I2C bus which is set to work at 1Mhz by default. Neither the devices nor the level shifter and even the bus layout has been thought to work at higher rates, so this restriction must always kept in mind when using the CB.

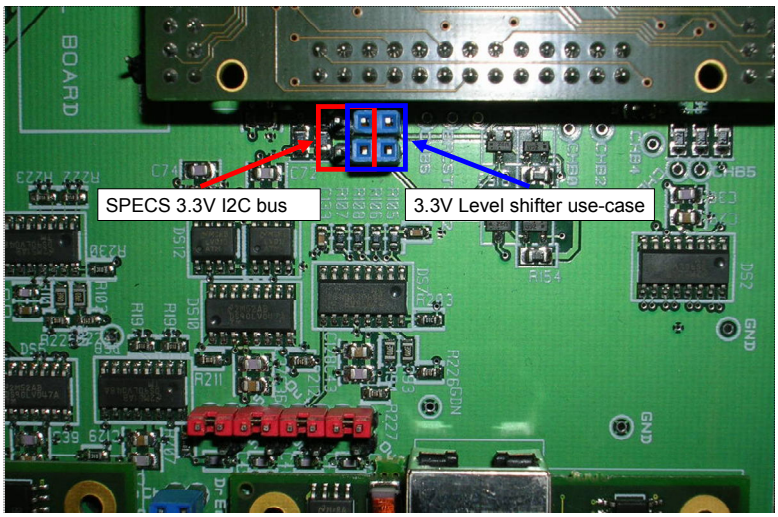


Figure 2.18: Jumper position for the selection of the TTCrq 3.3V I2C bus. In the figure the jumpers are set for using the 3.3V I2C level shifter (blue box position). For using the SPECS 3.3V I2C bus they must be moved to the red box position.

2.5.2. The ChanB decoder

All Brcst[7:2] and the two broadcast strobe signals BrcstStr1 and BrcstStr2 are connected from the TTCrx to the SPECS slave to permit decoding and synchronization. Two commands are decoded:

1) L0 Front-end Reset, which is validated with the BrcstStr1 broadcast strobe signal as shown in Figure 2.19. A pulse of 25 ns, synchronous to the failing edge of the selected clock is delivered. The Clock40Des1 clock from the TTCrx the used one.

2) Bit 0 of Calibration pulse: this signal can be delayed with a programmable delay up to 255ns, in steps of 25ns, as shown in figure 2.20, by writing the value of the delay in the mezzanine register CHANB_DELAY. The clock of the counter is the selected mezzanine clock which must also be the Clock40Des1. A pulse of one clock cycle is generated.

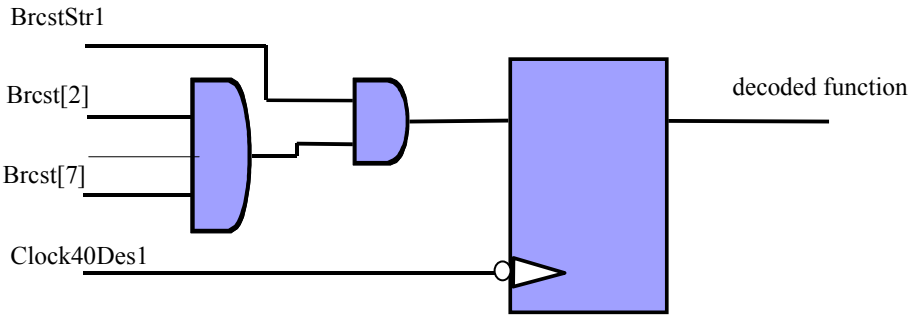


Figure 2.19: ChannelB decoding diagram

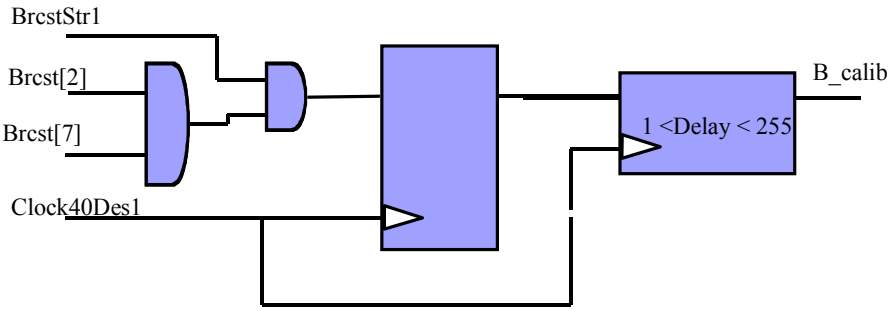


Figure 2.20: Calibration pulse decoding and delaying diagram

It also implements the additional feature of enabling/disabling the decoding of each of the signals individually. This feature is mandatory for the calibration command because the calibration pulse injection command is a global TTC broadcast to all systems, and in case we don't disable it, it could affect the Beetles data while data taking since it will be pulsing whenever a command is sent .

2.5.3. The long distance I2C

One can implement on this board up to 12 long distance I2C outputs. The SPECS system is seen in this case as an I2C provider, and its internal features can be completely ignored. The use of the long distance I2C provided by the SPECS slave is mandatory to communicate with boards situated in high radiation areas, like the Beetles, since it is not possible to put the SPECS FPGA at these locations.

The long distance I2C bus is based on 3 unidirectional signals: scl_i2c, sda_i2c, and sda_i2c_in. These signals must be buffered by drivers, and the equivalent of an open collector circuit must be implemented. The frequency of the I2C signals can be selected by a register in the master and thus decreased for slow I2C slaves (1 MHz, 500 kHz, 250 kHz, 125 kHz, 65 kHz, or 33 kHz). To implement additional busses, 12 selection signals and 12 direction signals (i2cjtag_de and i2cjtag_re) are provided. The i2cjtag_de signals (but not the i2cjtag_re signals) can also be commanded statically (e.g. for external multiplexer commands) thanks to a 16 bit internal register. This mode has to be selected in the MEZZA_CTRL register.

The way this long I2C is used for commanding the Beetles in the Hybrids and the GOLs and DCUs in the Dig. Boards is explained in detail in the section 2.9.

2.5.4. The single-ended SPECS local interface

On the SPECS mezzanine, 2 SPECS interfaces are provided: one point to point for long distance interconnection and one for local bus connection. Thanks to this feature, we can handle several mezzanines on the same SPECS bus.

The mezzanine can be configured in master mode or in slave mode. In master mode, the mezzanine can deal with 2 SPECS busses:

- 1 point to point long distance bus. This bus is implemented with RJ45 connectors on the mezzanine, which permits a direct connection to the master through an Ethernet cable. It can also make use of the SMC connectors if the RJ45 plug cannot be used for mechanical or any other reason.

- 1 multi-drop SPECS bus, located on the SMC connector. On this bus one can connect up to 31 slaves, respecting always the signal integrity on it.

In slave mode, the mezzanine controls the SPECS bus on the SMC connector, applying the same signal integrity rules as before.

In order to avoid any signal integrity problems with the SPECS bus signaling the use of drivers located next to the connectors is recommended. The figures 2.21 and 2.22 show how to implement a multi-mezzanine SPECS bus using LVDS drivers.

The point to point distance bus implemented in the RJ45 connector of the mezzanine implements pole-zero compensation for long distance (100m) communications, so using the mezzanine in master mode also permits getting profit of this extra feature. The LVDS driving stage of the mezzanine uses two smd air coils (one for SDA and one for SCL) which act as a pre-emphasis filter for compensating the high frequency attenuation caused by the cable length, which improves the signal quality in the receiver.

The design of the CB SPECS chaining stage has been done in a way which makes possible using either the slave1 mezzanine in master mode or slave mode, although for mechanical reasons the slave mode is recommended. A thorough explanation of this part is done in section 2.6.

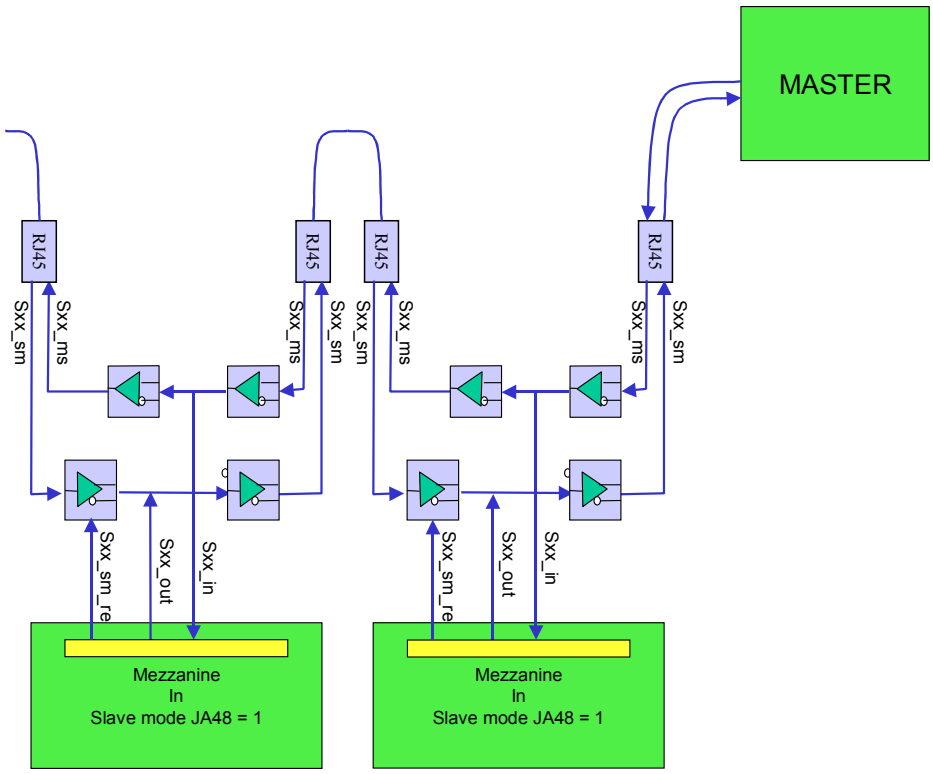


Figure 2.21: Chaining with all mezzanines in slave mode

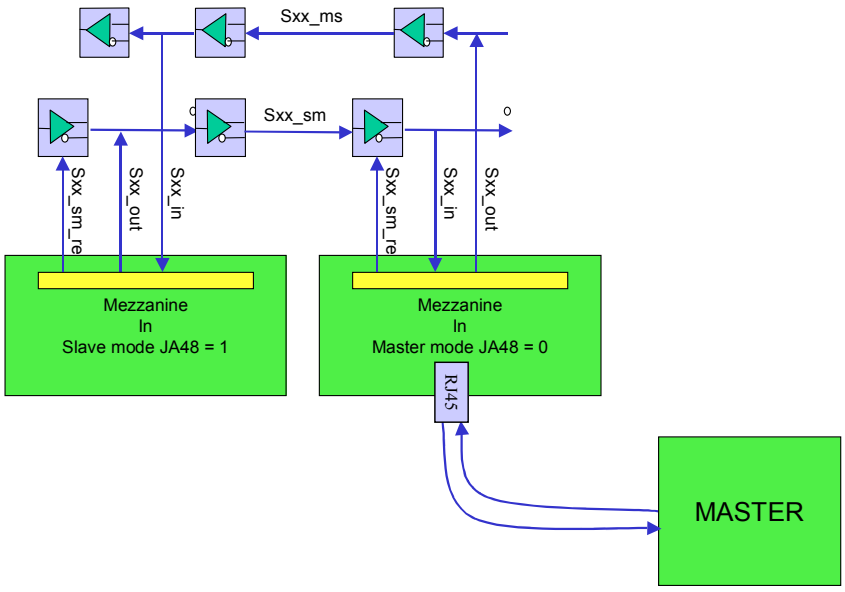


Figure 2.22: Chaining with one mezzanine in master mode

2.5.5. The reset outputs

The asynchronous reset signal of the slave1 is used for resetting the delay25 chip, whereas the reset from the slave2 resets the CB DCU. The reset signal is active at low level. They can be used in case of chip malfunctioning.

2.5.6. The I/O configurable register

On each mezzanine 32 user configurable I/O are implemented. They can be read or controlled by two 16 bit registers, REGOUT_MSB and REGOUT_LSB. These registers can be configured either in output or in input mode by 2 internal registers, CONFREGOUT_LSB and CONFREGOUT_MSB. By default (at power on or after Reset), the registers are configured in input mode to avoid any conflict with the signal. The logic is LVTTL (3.3V).

The 32 I/O of the slave1 are basically used for the backplane regulators control, whereas the I/O lines from the slave2 are used for the regulators control and other miscellaneous purposes. The lines used for the regulators inhibit (INH) control are pulled-up to 2.5V, hence they are disabled at start-up or after a slave reset. The lines for reading the OCM (Over Current Monitoring) signals of the 3.3V and 5V regulators are scaled using voltage divider in order to assure high levels less than 3.3V in the SPECS inputs (see figure 2.23).

The figures 2.24 and 2.23 show the distribution of the backplane regulators OCM and INH signals for the IT and TT in relation to the svce. box slot and partition number. The representation, and therefore the slot and partition numbering has been done supposing the svce box is observed from the frontal side (which means looking at the backplane from the back). It also shows the SPECS I2C bus numbering for the different partitions.

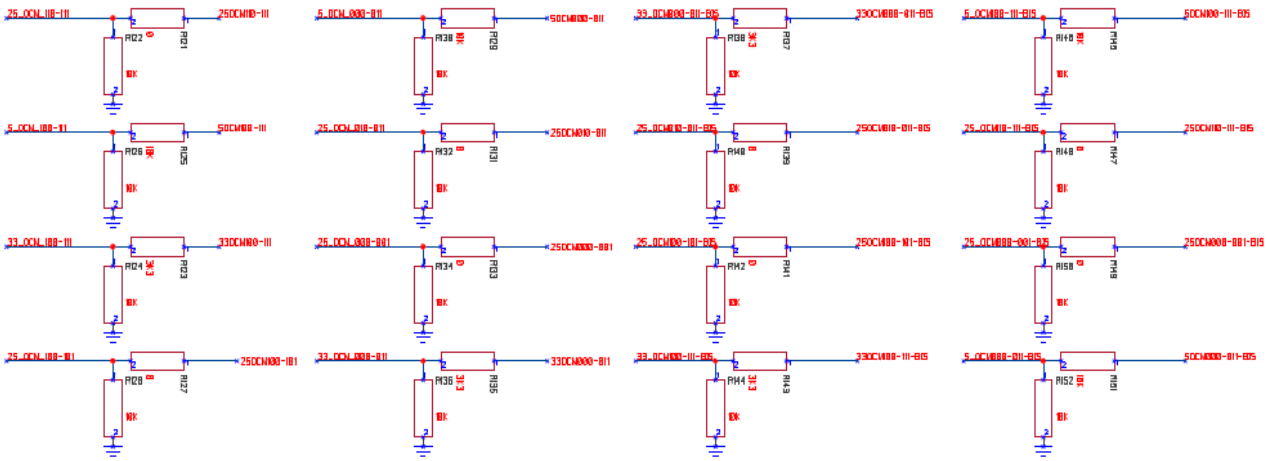


Figure 2.24: Voltage dividers for the OCM signals

The I/O register signals assignment for the IT and TT is next (in parenthesis is indicated if the signal must be programmed as input or output):

IT I/O register assignment:	**TT I/O register assignment:**
Slave1 bit-signal assignment: 1) Hb_INH_7 (O) 2) Hb_INH_6 (O) 3) Hb_INH_5 (O) 4) P1_DBs_INH (O) 5) Hb_INH_4 (O) 6) P0_DBs_INH (O) 7) Hb_INH_2 (O) 8) Hb_INH_3 (O) 9) Hb_INH_0 (O) 10) Hb_INH_1 (O) 11) Hb_INH_9 (O) 12) Hb_INH_8 (O) 13) Hb_INH_11 (O) 14) Hb_INH_10 (O) 15) P2_DBs_INH (O) 16) Hb_INH_12 (O) 17) P3_DBs_INH (O) 18) Hb_INH_13 (O) 19) Hb_INH_14 (O) 20) Hb_INH_15 (O) 21) TTCrq RESET (O) 22) TTCrq_QPLL RESET (O) 23) QPLLs reset (O) 24) RST_GOLs (O) 25) P0_OC25V_#2 (I)	**Slave1 bit-signal assignment:** 1) Not used in backplane 2) Hb_INH_5 (O) 3) Hb_INH_4 (O) 4) P1_DBs_INH (O) 5) Hb_INH_3 (O) 6) P0_DBs_INH (O) 7) Hb_INH_2 (O) 8) Not used in backplane 9) Hb_INH_0 (O) 10) Hb_INH_1 (O) 11) Hb_INH_7 (O) 12) Hb_INH_6 (O) 13) Not used in backplane 14) Hb_INH_8 (O) 15) P2_DBs_INH (O) 16) Hb_INH_9 (O) 17) P3_DBs_INH (O) 18) Hb_INH_10 (O) 19) Hb_INH_11 (O) 20) Not used in backplane 21) TTCrq RESET (O) 22) TTCrq_QPLL RESET (O) 23) QPLLs reset (O) 24) RST_GOLs (O) 25) P0_OC25V_#2 (I)

[3] These signals where foreseen for extending the control of the I2CMEZZ board.

[4] These signals come from the TYCO-electronics connector in the frontal.

[5] These I/O have been routed to the backplane connector for any general purpose.

IT I/O register assignment:	TT I/O register assignment:
26) P0_OC5V (I) 27) P0_OC33V (I) 28) P0_OC25V_#1 (I) 29) P1_OC5V (I) 30) P1_OC25V_#2 (I) 31) P1_OC25V_#1 (I) 32) P1_C33V (I)	26) P0_OC5V (I) 27) Not used in backplane 28) P0_OC25V_#1 (I) 29) P1_OC5V (I) 30) P1_OC25V_#2 (I) 31) P1_OC25V_#1 (I) 32) Not used in backplane
Slave2 assignment: 1) OCM_25V_CtrlBoard (I) 2) L0ACCEPT_DE_Ctrl (O) 3) OCM_5V_CtrlBoard (I) 4) I2CSwitch_Ctrl4 (O)[3] 5) Amp_Con4 (I) [4] 6) I2CSwitch_Ctrl3 (I) [3] 7) DRV_DOWN_EN (O) 8) X9-C1 (I/O) [5] 9) X9-A2 (I/O) [5] 10) X9-B2 (I/O) [5] 11) X9-A3 (I/O) [5] 12) DRV_UP_EN (O) 13) Not Connected in CB 14) Not Connected in CB 15) TTCrqREADY (I) 16) TTCrqLOCKED (I) 17) TTCrqERROR (I) 18) I2CSwitch_Ctrl2 (O) [3] 19) Amp_Con3 (I) [4] 20) I2CSwitch_Ctrl1 (O) [3] 21) Amp_Con2 (I) [4] 22) CtrlExt1 (O) [3] 23) Amp_Con1 (I) [4] 24) CtrlExt2 (O) [3] 25) P3_OC33V (I) 26) P3_OC25V_#1 (I) 27) P3_OC25V_#2 (I) 28) P3_OC5V (I) 29) P2_OC25V_#1 (I) 30) P2_OC33V (I) 31) P2_OC5V (I) 32) P2_C25V_#2 (I)	**Slave2 assignment:** 1) OCM_25V_CtrlBoard (I) 2) L0ACCEPT_DE_Ctrl (O) 3) OCM_5V_CtrlBoard (I) 4) I2CSwitch_Ctrl4 (O) [3] 5) Amp_Con4 (I) [4] 6) I2CSwitch_Ctrl3 (I) [3] 7) DRV_DOWN_EN (O) 8) X9-C1 (I/O) [5] 9) X9-A2 (I/O) [5] 10) X9-B2 (I/O) [5] 11) X9-A3 (I/O) [5] 12) DRV_UP_EN (O) 13) Not Connected in CB 14) Not Connected in CB 15) TTCrqREADY (I) 16) TTCrqLOCKED (I) 17) TTCrqERROR (I) 18) I2CSwitch_Ctrl2 (O) [3] 19) Amp_Con3 (I) [4] 20) I2CSwitch_Ctrl1 (O) [3] 21) Amp_Con2 (I) [4] 22) CtrlExt1 (O) [3] 23) Amp_Con1 (I) [4] 24) CtrlExt2 (O) [3] 33) Not used in backplane 34) P3_OC25V_#1 (I) 35) P3_OC25V_#2 (I) 36) P3_OC5V (I) 37) P2_OC25V_#1 (I) 38) Not used in backplane 39) P2_OC5V (I) 25) P2_C25V_#2 (I)

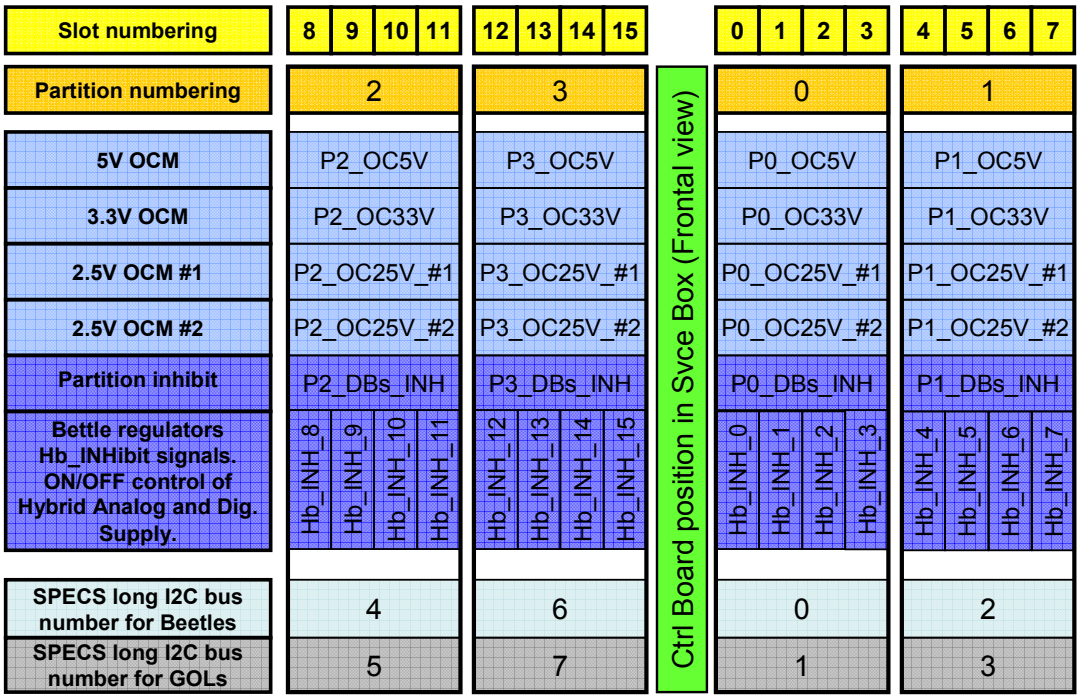


Figure 2.25: Logical distribution for the OCM and inhibit signals and also I2C buses according to the slot and partition numbering shown (looking at the svce box from the frontal) for the IT subdetector.

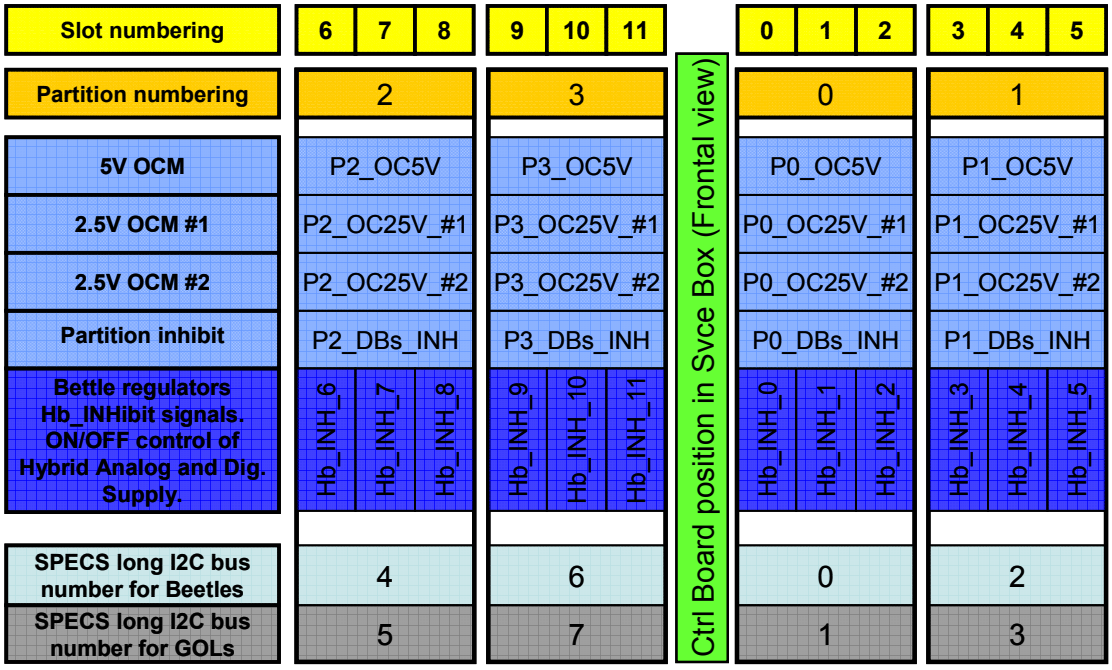


Figure 2.26: Logical distribution for the OCM and inhibit signals and also I2C buses acording to the slot and partition numbering shown (looking at the svce box from the frontal) for the TT.

2.5.7. The DCU

A DCU2 chip is implemented on each mezzanine. One 10Ω resistor is implemented on each input. The input range of the analog channels are 0 to 2.5 V and the reference resistor is set to 120KΩ, giving a conversion factor of 2.1 mV^{-1} [8]. Channel 7 is a non calibrated temperature channel.

The SPECS internal DCUs channels are used for monitoring several Detector Box and backplane temperatures, and also for monitoring the control board regulators voltages and even an additional input has been foreseen for monitoring the regulators temperature.

DCU slave1:

- Channel 0 → Not used (10 µAcurrent source).
- Channel 1 → Backplane temperature 1.
- Channel 2 → Backplane temperature 2.
- Channel 3 → CB 2.5V monitoring.
- Channel 4 → CB 5V monitoring.
- Channel 5 → CB 3.3V monitoring.

DCU slave2:

- Channel 0 → Not used (10 µAcurrent source).
- Channel 1 → Detector box temperature 4 (PT1000_4).
- Channel 2 → Detector box temperature 3 (PT1000_3).
- Channel 3 → Detector box temperature 2 (PT1000_2)
- Channel 4 → Detector box temperature 1 (PT1000_1).
- Channel 5 → PT1000 for the Ctrl Board regulators temperature monitoring.

In section 2.7 a more detailed description about the PT1000 temperature sensors conditioning and readout can be found.

The figure 2.26 shows the simple circuit foreseen for an eventual smd PT1000 sensor in the opposite side of the 3.3V voltage regulator. Also 2 pins have been added so that instead of using a smd sensor an aerial one attached to the heatsinks could be used by means of a small twisted cable.

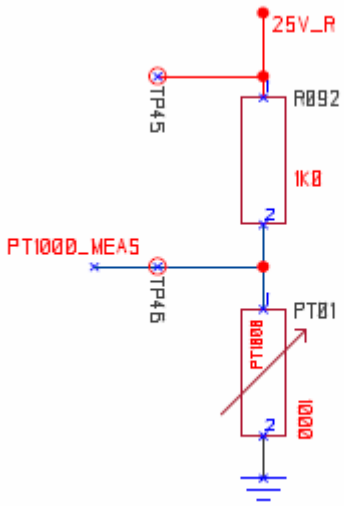


Figure 2.27: Extra PT1000 sensor and polarization circuit

2.6. SPECS chaining circuitry

In order to allow many slaves share the same SPECS master link additional electronics is necessary. In our system we want to connect up to 6 control boards to the same master link, which means interconnecting 12 SPECS slaves.

The four signals that connect the SPECS master to the slaves: SDA_MS, SDA_SM, SCL_MS, SCL_SM are LVDS, whereas the SPECS slaves FPGAs I/O are single ended, so a translation from LVDS to TTL/CMOS in the CB is necessary.

Figure 2.27 shows the devices interconnection system implemented in the CB in order to perform the SPECS chaining within the CB and with the other Control Boards and master.

In first term, the diagram shows 3 different types of LVDS transmitters/receivers:

- The DS90LV047 (grey) and DS90LV048 (grey) are LVDS quad line driver and receivers respectively.

- The SN65LVDS32 (blue) is a quad line receiver the receiver with a higher CMRR than the DS90LV048, and for this reason it is used as the LVDS external link receiver in order to cope with common mode voltage differences among the several service boxes connected to the same SPECS link and between the control room and the detector location.

- The DS92LV010 (brown) is a BLVDS transceiver that we use in transmitter mode. Since it is BLVDS its current swing is twice than LVDS, which is necessary in order to deal with the attenuation introduced by the 100m cable between cavern and control room.

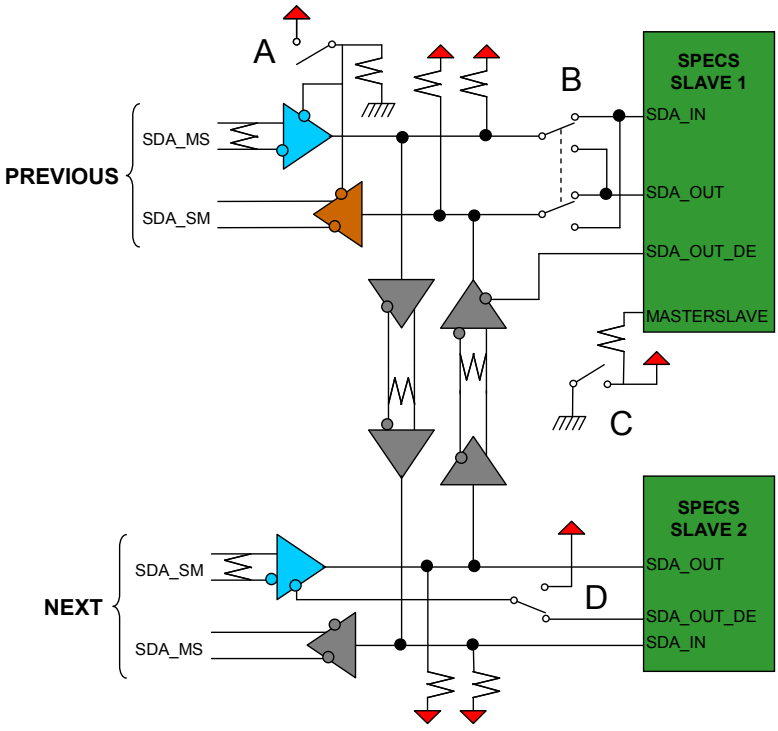


Figure 2.28: SPECS chaining block diagram for the SDA signal

Many switches, which are realized with jumpers, are also necessary:

- The "A" is for disabling the LVDS receivers in case we decide to use the 1st slave in master mode, and therefore we connect the input cable directly to the SPECS slave RJ45 connector.

- The "B" pair of switches is used for changing the interconnection of the SDA_IN and SDA_OUT signals depending on the MASTERSLAVE status of the SPECS slave. If we decide to use the 1st mezzanine in master mode the jumpers must be plugged as shown in figure 2.29, while for working in slave mode they must be set as in figure 2.28.

- The "C" is for setting the slave to work either in master mode or in slave mode. The slave 2 is by default set to slave mode.

- The "D" switch which can be set to two different positions: the situation shown in the block diagram (and in parallel in the picture 2.28) is the normal one and permits the slave "isolating" the link from the previous slaves in the chain and thus can send a transmission to the master; in the other position (see yellow box in picture 2.29), the LVDS receiver is disabled and this is useful in case that is the last slave in the chain.

Figures 2.28 and 2.29 show the jumpers and its use.

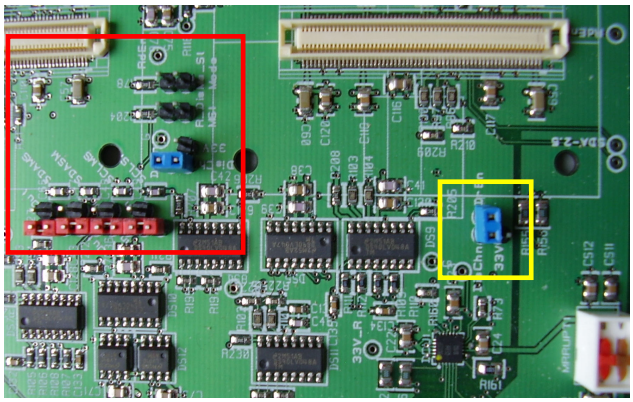


Figure 2.29: Inside de red box the jumper positions for using the mezzanine1 in slave mode. In yellow the jumper position for enabling the link to other boards in the chain.

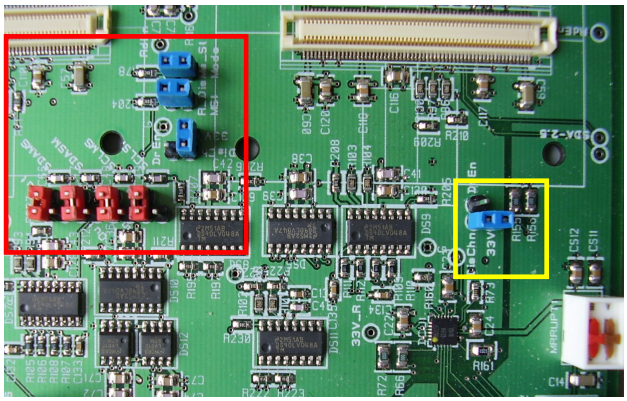


Figure 2.30: Within the red box the jumper positions for using the mezzanine1 in master mode. In the yellow box the jumper position for "cutting" the SPECS link.

2.7. Signal conditioning devices

Signal conditioning of the temperature and humidity signals before digitization is necessary in order to have a proper measurement. The temperature sensors signals are configured in a wheatstone bridge and amplified using the radiation tested AD8129 differential amplifier [10] (Figure 2.30). The humidity sensor is by itself a wheatstone bridge sensor, so the its output signal is differential, and it is also amplified with the AD8129, but with a different gain.

The radiation tested voltage reference AD780 [11] is used for the amplifiers reference voltage and also for the humidity sensor biasing (figure 2.31). The voltage reference goes to a double toggle switch and then to the instrumentation amplifiers reference pins and humidity sensor bias line (figure 2.32). This switch permits choosing between the voltage reference and the 2.5V regulator supply. The 2.5V from the regulator will give a more imprecise measurement for several reasons: the regulator output voltage is noisier; the regulator output voltage value cannot precisely be set; and it is also more temperature dependent (bang-gap voltage references are auto-compensated).

The AD8129 is not a rail to rail differential amplifier, so the input and output voltage swing for any of the terminals is only guarantied to work properly from 1.1V to 3.9V. The gain of the amplifier is set to 11 for the temperature signals and to 51 for the humidity sensor. The output of the instrumentation amplifier goes to a 1:3 voltage divider and the to the DCU input. This voltage divider has been implemented in order to ensure that the input voltage at the DCU is in the range from 0-1.25V, so we use the DCU in LIR mode (Low Input Range) and hence the ADC value is referenced to ground.

The readout value for the temperature sensors is calculated as follows:

$$\Rightarrow V_{inDCU} = \left[\left(V_{in+} - V_{in-}\right)\times G + V_{ref}\right]\times A_{div}$$

$$\Rightarrow V_{in+} = V_{25V\_PT1000} \times \left(R_{8K25} \Big/ R_{8K25+} R_{909} \right)$$

$$\Rightarrow V_{in-} = V_{25V\_PT1000} \times \left(R_{8K25} \Big/ R_{8K25+} R_{PT1000} \right)$$

$$\Rightarrow G = 1 + R_{3K4} \Big/ R_{340}$$

$$\Rightarrow A_{div} = R_{2K0} \Big/ R_{2K0+} R_{1K0}$$

$$\Rightarrow V_{ref} = 2.5V$$

$$\Rightarrow V_{25V\_PT1000} = 2.5V$$

Merging everything together we finally get:

$$\Rightarrow \boxed{R_{PT1000} = \frac{8250\times\left(19158 - 10990{,}8\times V_{inDCU}\right)}{81591 + 10990{,}8\times V_{inDCU}} \quad \Omega}$$

And from PT1000 resistance we get the temperature value as follows:

$$\Rightarrow \boxed{T_0 = \frac{\left(R_{PT1000} - 1000\right)}{3.85} \quad ^{\circ}C}$$

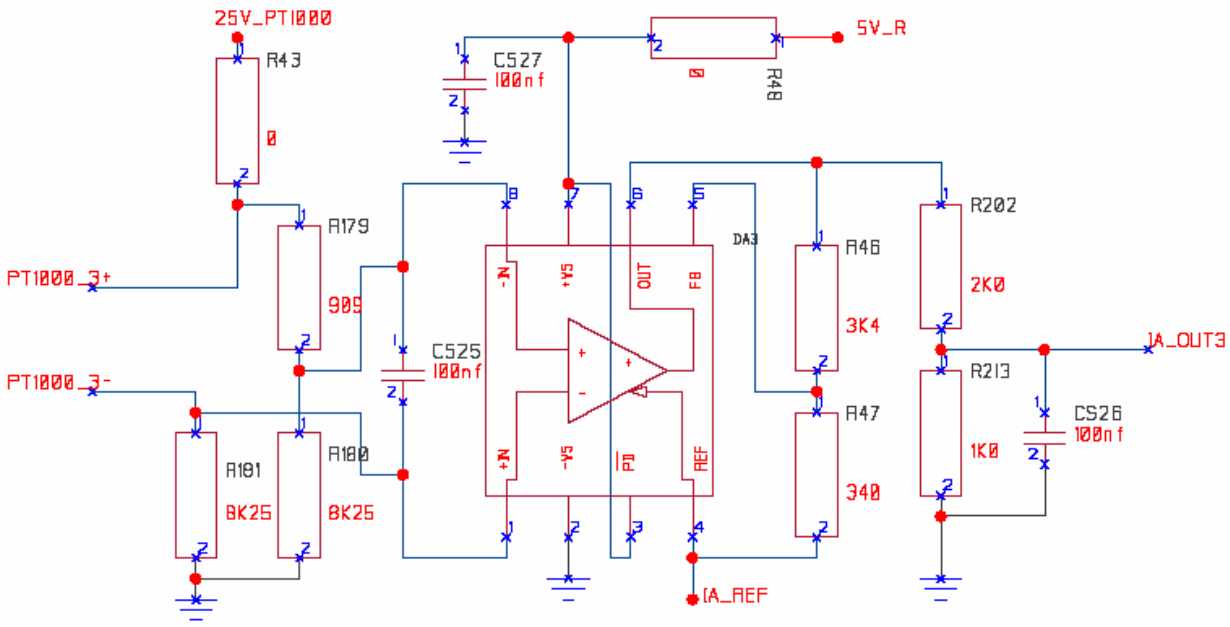


Figure 2.31: PT1000 sensor signal conditioning

High precision (%0.1) and low temperature coefficient (± 25ppm/ºC) resistors are used for the wheatstone bridge, the amplifier gain and the voltage divider. However, the error in the measurement is dominated by the DCU, which shows deviations up to 10% from the ideal value.

A way to accomplish a precision measurement is performing a calibration of every DCU with known resistance values. The idea is calibrating the DCU temperature channels using several resistance values, for instance 1KΩ, 1K039Ω and 1K077Ω, which correspond to PT1000 temperatures of 0ºC, 10ºC and 20ºC respectively. We read the DCU output values for each resistance and then we create the calibration curve for each DCU temperature channel. A custom made board with some precision resistors and specific software has been developed for calibrating the DCU channels.

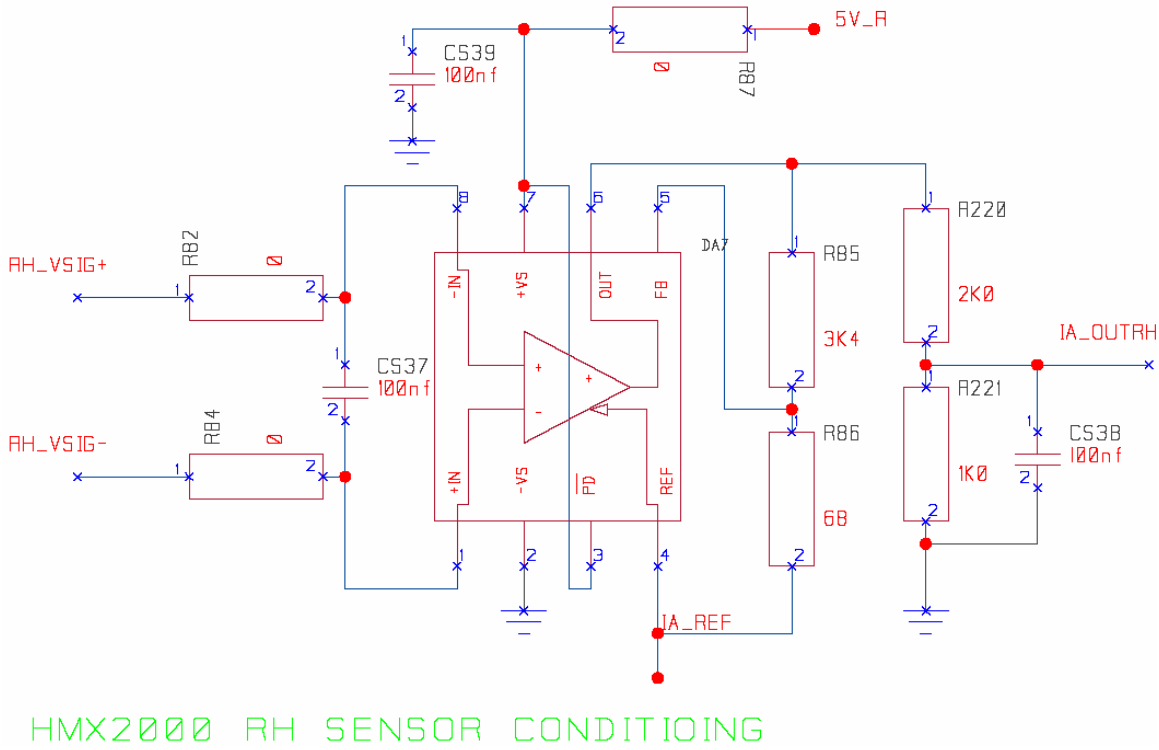


Figure 2.32: HMX2000 bridge output signal conditioning circuit

The HMX2000 is a radiation hard humidity sensor [12] tested and characterized by the CMS pixel group. The sensor output value doesn't follow a general standard equation, so the manufacturer provides a sheet of calibration data for each sensor (see appendix A) on demand. The sensor output depends not only in the humidity, but also depends slightly on the environmental temperature. The output voltage also scales with the bias voltage and can go up to 5V, as stated from the company.

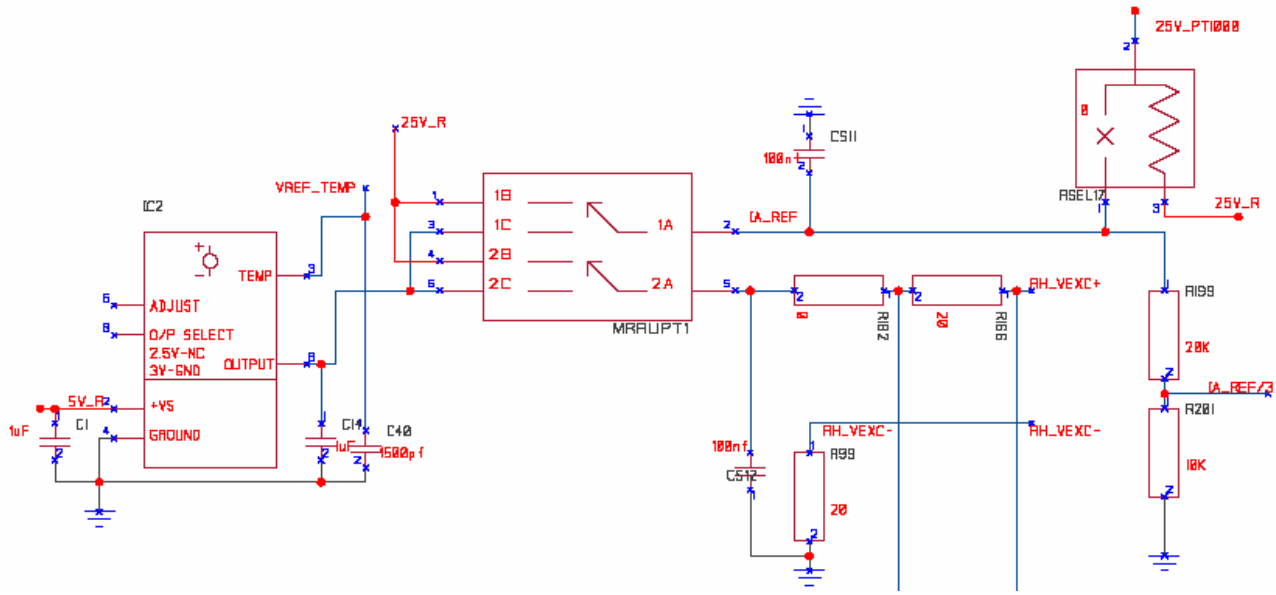


Figure 2.33: Schematic diagram of the voltage reference together with the toggle switch and the humidity sensor biasing resistors.

From the calibration data, and assuming temperatures from 5 to 10ºC, we find that the lowest output voltage value is around -12.5mV for 0%RH. As we will supply the sensor with 2.5V instead of 1.25V, the output scales to ~-25mV, which multiplied by a gain of 51 produces and output value of -1.275V. As the amplifier output is mounted on a 2.5V offset, the resulting output value is 1.225V which is above the 1.1V minimum

output voltage required for the amplifier. This output is divided by 3 in the voltage divider at the DCU input so we will work with the DCU in LIR mode.

2.8. DCU

Together with 2 DCUs in the SPECS slaves, the CB hosts an extra DCU. This DCU is basically used for the reaout of the HMX2000 humidity sensor:

- Channel 1 → IA_IMEAS: estimation of the current through the HMX2000 sensor.
- Channel 2 → HIH_RH/4: input divided by 4 for a HIH-3610 humidity sensor signal (for debugging purposes)
- Channel 3 → IA_OUTRH: humidity sensor signal after being conditioned.
- Channel 4 → IA_REF/3: value divided by 3 of the voltage reference output (for monitoring the AD780).
- Channel 5 → RH_VEXC-: excitation voltage in the negative terminal of the HMX2000.

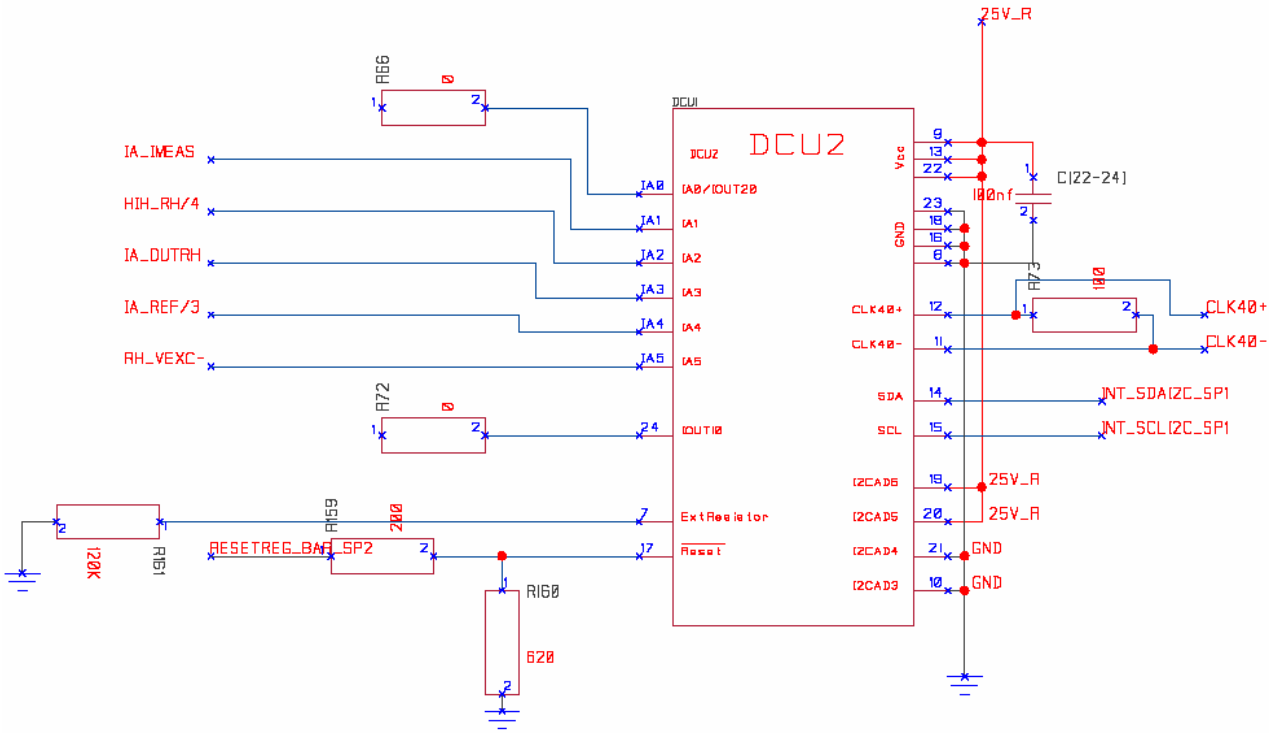


Figure 2.34: Control Board DCU schematic

As mentioned earlier, this DCU can be accessed using the SPECS internal I2C bus. The DCU address is set to “bx1100XXX”, where the XXX are used for addressing the different DCU registers.

The reset line is connected to the slave2 external reset through a voltage divider. The external reference resistor is set to 120KΩ , giving a conversion factor of 2.1 mV^{-1}. The 40Mhz differential clock needed by the DCU comes from the TTCrq.

2.9. I2C bus switches

The long I2C bus from the SPECS consists of 3 unidirectional lines for SDA and SCL signals and 8 bus select lines. In the standard I2C, SDA and SCL are bidirectional lines (they are open drain or open collector), whereas the SPECS long I2C consists of SDA_OUT, SDA_IN and SCL_OUT (SCL_IN is not available since the SCL is an unidirectional clock line). Therefore interface circuitry is necessary in order to build eight I2C "standard compatible" buses from the SPECS signals.

From this SPECS long I2C we build four 3.3V I2C buses that will go to the ladder hybrids and four 2.5V that will go to the Dig. Boards, based on a partitioning scheme that follows the read-out partitioning described in [13](see also figures 2.25 and 2.26). The Dig. Board links need to be 2.5V because the GOLs and DCU are not compatible with other voltage levels. However, the hybrid links need necessarily to be 3.3V since the Beetles I2C lines are 3.3V compatible and some test showed up that working at 2.5V could compromise the reliability of the link connection due to the cable length and its associated capacitance and voltage drop along it.

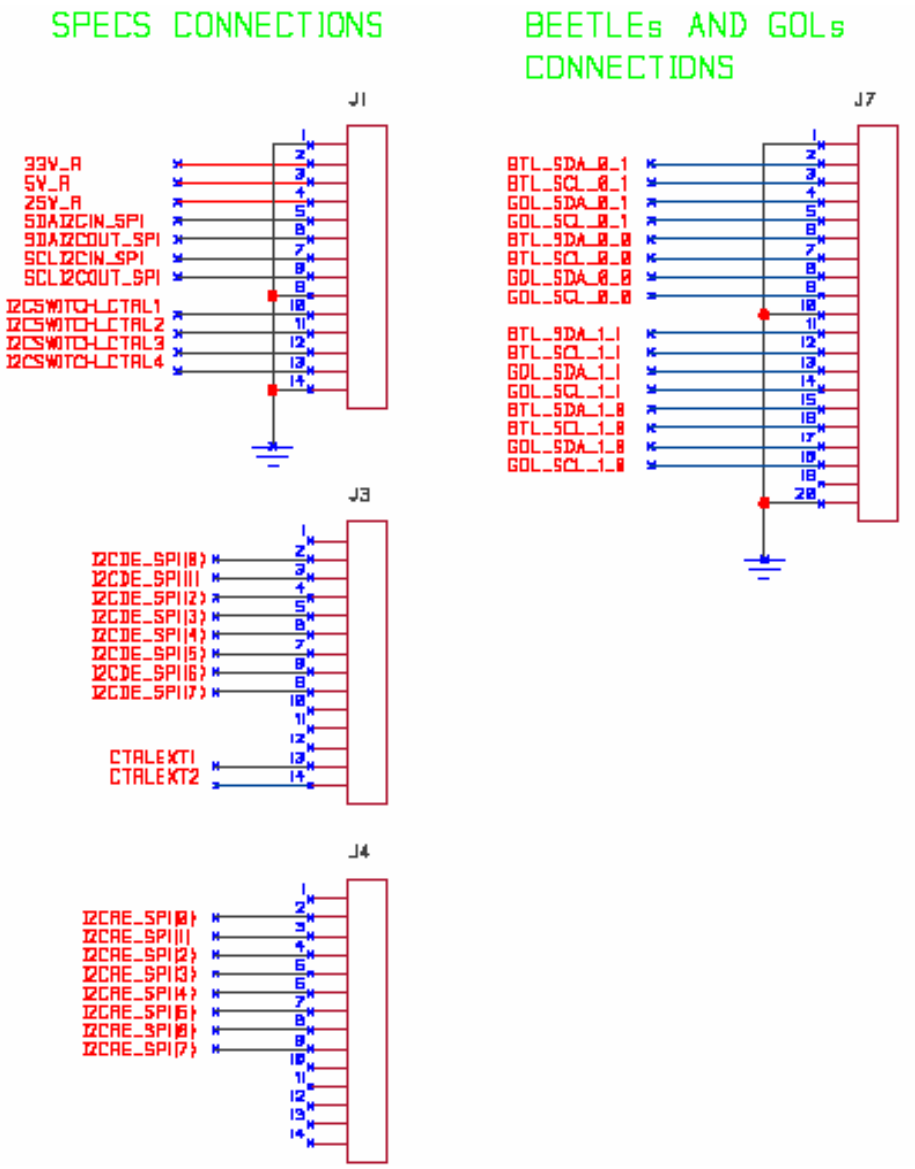


Figure 2.35: I2C bus MUX/DEMUX interface connectors

This interface circuitry is implemented in a mezzanine card, so the CB features some pin connectors with the signals shown in figure 2.35. In the left hand of the picture we can observe the mentioned signals SDA_OUT, SDA_IN, SCL_OUT and I2C_DE_SP1[0:7] (the bus selection signals) are together with the power supply lines and some other control lines (I2CSWITCH_CTRL[1:4] and CTRLEXT[1:2]), and in the right hand we can find the I2C bus outputs that go to the Hybrids and Dig Boards.

The figure 2.35 shows the mezzanine behavioural model in a normalized way. From the DEMUX block follows that all the outputs are tri-state and are connected either to the SDA or to the SCL lines. Each output pair SDA-SCL is also controlled by one of the I2C_DE input lines, and the odd pairs are also controlled by EN signals. The output lines are pulled-up to 3.3V or 2.5V depending on whether they connect to a Hybrid or to a Dig Board. There are also two CtrlExt lines (8 and 9) which could also control the whole I2C DEMUX. As I2C is a bidirectional bus, feedback from SDA the outputs must be sent back to the SPECS SDA_IN input line, and this is done in the MUX block.

The aim of the I2CSWITCH_CTRL[1:4] lines is pulling to 0V the GOLs I2C lines and thus avoid the GOL start-up problem. These lines should be pulled up or down in the mezzanine depending on the default initial state we desire at the SPECS start-up (at SPECS startup all these lines are configured in input mode).

The CTRLEXT1 and CTRLEXT2 I/O lines have just been added in case additional functionalities want to be implemented in the I2C mezzanine.

The initial idea was building this mezzanine using an anti-fuse radhard FPGA implementing the described blocks. A first implementation in VHDL together with the logical and timing test has been done. Minor tests of this implementation have also been performed in an APA150 test-board, but not a real test with the actual hardware.

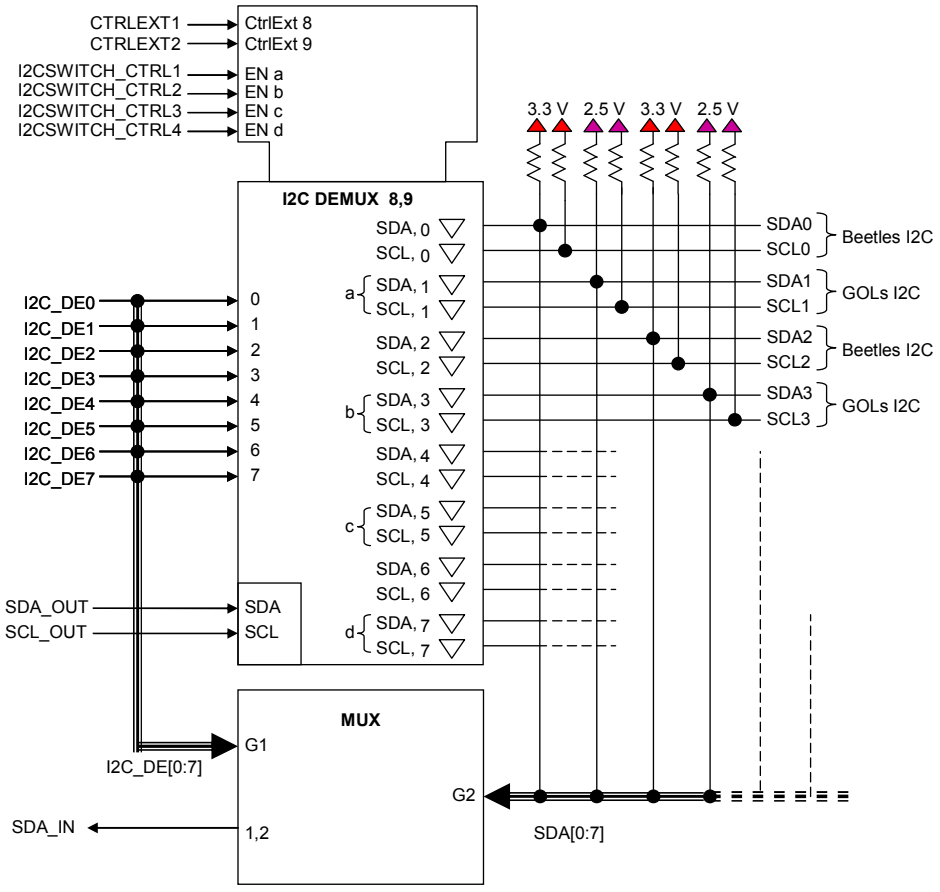


Figure 2.36: I2C DEMUX and MUX normalized symbols

In parallel to the FPGA mezzanine development a simple one based on tri-state drivers that fulfils all the basic requirements has been built. The figure 2.36 shows the schematic for a SDA-SCL pair, and the figure X the prototype PCB plugged in the CB. The complete mezzanine replicates by 8 the number of pairs keeping in mind that four of the output pairs are 3.3V and the other four are 2.5V. It uses the 74F125SC (bipolar technology) quad buffer tri-state drivers from Fairchild and BSR117 NPN transistors for inverting the I2C_DE bus select lines.

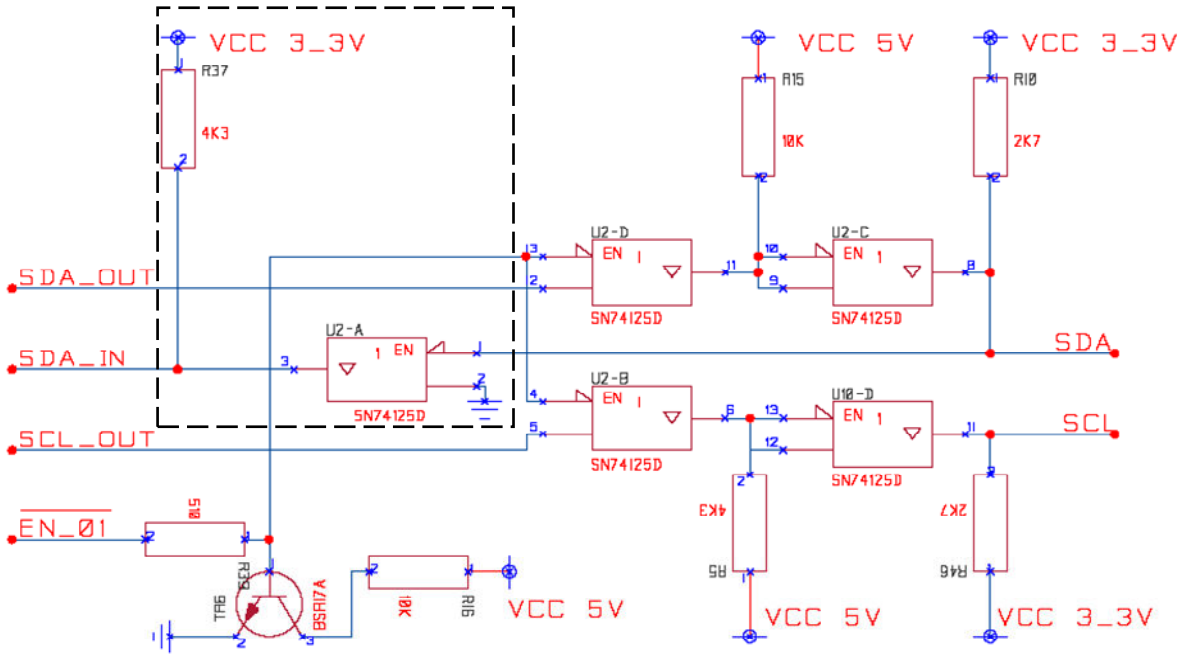


Figure 2.37: 2C DEMUX and MUX implementation based on tri-state drivers

This tri-state based mezzanine just implements the basic functionalities. The components comprised in the dashed area implement the MUX while the other ones implement the DEMUX. The drawbacks of this mezzanine are:

- The tri-state drives work properly at least till 24.5Krad radiation dose and the maximum expected dose in the svce boxes is ~15krad, but applying safety factors, the devices should withstand till 60 krad. This means that for reliability reasons, they should be changed after ~5 years.

- They don't implement GOL I2C lines disable capability. It should be also mentioned that the Silicon Tracker detector has never suffered this start-up problem for the long time that it has been using the GOLs.

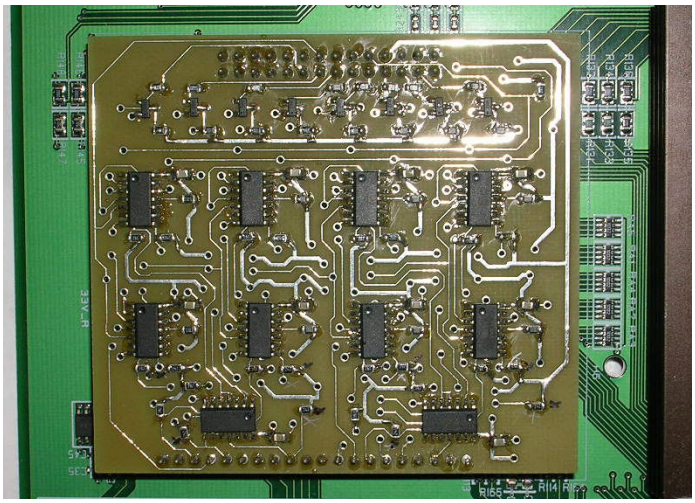


Figure 2.38: I2C mezzanine based on 74F125SC tri-state drivers

The initial idea of the FPGA based mezzanine is still ongoing (but with quite limited manpower and effort in the current times) and it is considered to be a future upgrade of the tri-state based one, which fulfils the task effectively.

2.10. Level shifter

The level shifter just consists of two head-to-head NPN transistors [9] working in saturation mode, together with the pull-up resistors mandatory for the I2C bus. It is used translate the I2C voltage level from 2.5V to 3.3V, keeping in mind that the I2C bus is bidirectional. The figure 2.38 shows the scheme, where the 2.5V I2C lines are on the left side (INT_SDAI2C_SP1 and INT_SCLI2C_SP1) and the 3.3V ones on the right (SDA_33V, SCL_33V) and the 4K3 pull-up resistor at both sides are not shown.

I2C signals come from open-collector or open-drain outputs, so can only pull down. As the transistors base voltage is set to 2.5V, when one of the input terminals goes low, the opposite transistor acts as a common base amplifier that saturates, pulling the other terminal low to within one V_{cesat}. This action also pulls the emitter of the input transistor low, to within one V_{cesat} of its collector, thereby cutting off collector current (although base current flows) and preventing latch-up.

For our application, BSR17A NPN switching transistors have been chosen, which allow working at rates of some hundreds of Khz, enough for TTCrq I2C communication. The maximum V_{eb} that the transistor can withstand is 6V, which is high enough since we will have 2.5V in the base and 3.3V in one of the emitters.

The transistor has been tested for radiation by the CERN AB-BI (Accelerators and Beams Department – Beam instrumentation) up to 87.5 Krad in their WBTN (Wide Band Time Normalizer) board and no abnormal behaviour has been found.

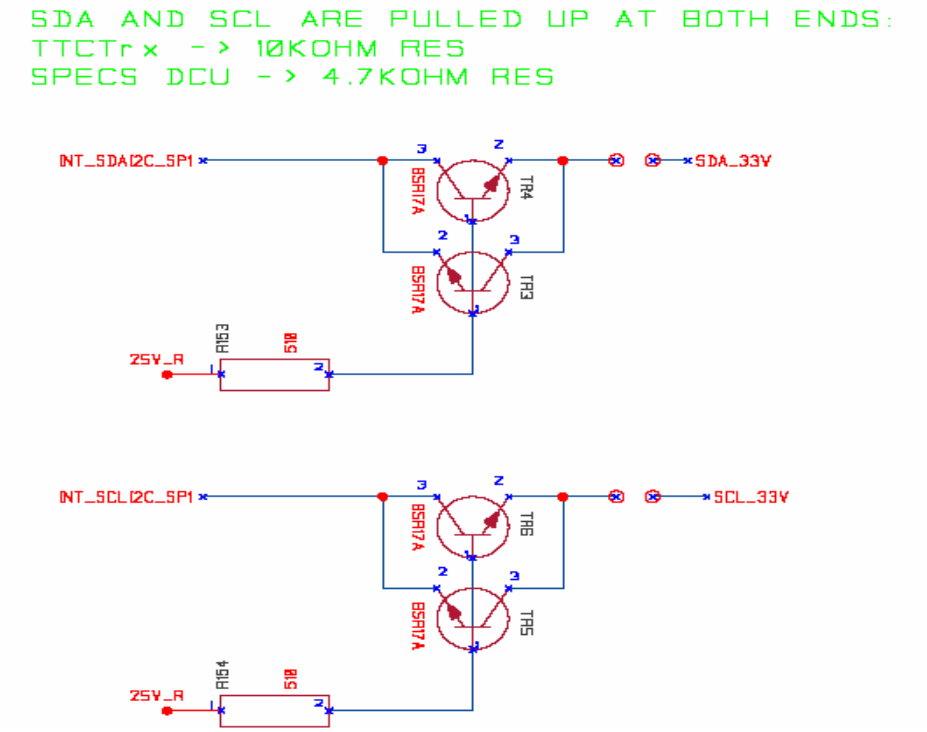


Figure 2.39 : I2C level shifter schematic

3. Control board PCB design and construction.

The CB is produced in a multilayer technology with impedance controlled traces. The structure of the PCB is shown in Figure 3.1. The thicknesses were chosen to provide controlled impedance traces for the layers 2 and 5 (from top to bottom).

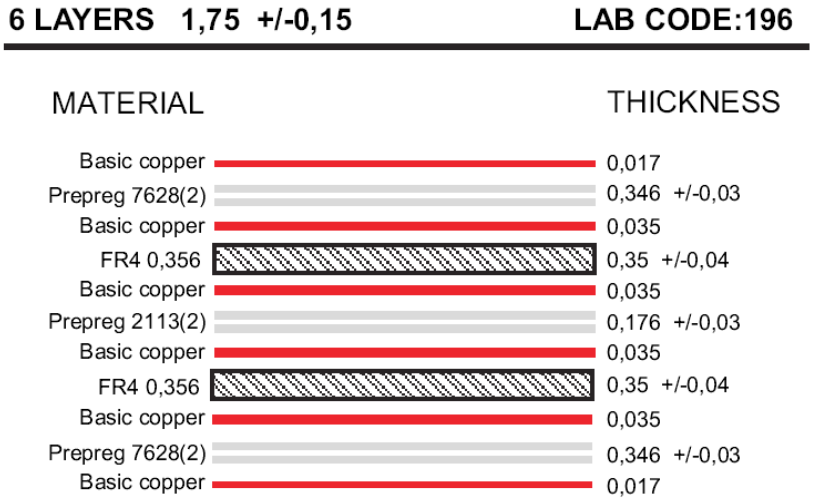


Figure 3.1: PCB structure

It has been designed using Zuken-Cadstar program.

Copper layer from top to bottom:

1. Top Layer: signal layer flooded with ground copper.
2. Signal 1: signal layer.
3. PW: splitted power plane layer.
4. GND: ground layer.
5. Signal2: signals + fast signals.
6. Bottom layer: signal layer flooded with ground copper.

The layers layout can be seen in appendix C.

The images in the appendix D show the controlled impedance tracks, which are highlighted in red. Also the manufacturer track impedance solver results are shown.

The drills are all of them through hole. Below is shown the drilling report for all the tools:

Plated through hole:

Drill No.	Tool No.	Size(mils)	Count	File Name
0	1	12.0	1288	
1	2	28.0	225	
2	3	32.0	55	
3	4	35.0	112	
4	5	39.0	70	
5	6	43.0	4	
6	7	51.0	4	

```
         7          8      122.0          2
         8          9      125.0         10
-------------------------------------------------------------
                          TOTAL       1770
```

Non plated through hole:

```
Drill No.  Tool No.      Size(mils)    Count    File Name
-------------------------------------------------------------
         0          1       71.0          8
         1          2      126.0          8
-------------------------------------------------------------
                          TOTAL         16
```

3.1. I2C mezzanine PCB

The I2C mezzanines that plug in the CB are simple two layer PCBs. The layer layout can be seen in the appendix E.

The drills are all plated through hole:

Plated through hole:

```
Drill No.  Tool No.      Size(mils)   Count    File Name
-------------------------------------------------------------
         0          1         20        167
         1          2    39.37007874    48
-------------------------------------------------------------
                          TOTAL        215
```

3.2. Components radiation tolerance

Due to the relatively high radiation levels present in the service boxes, some care must be taken when choosing the components for the CB. The devices response must be characterized for Total Ionizing Dose (TID) effects, for Single Event Effects (SEE) and Non Ionizing Energy Loss (NIEL), and they'll have to survive for the foreseen 10 years of experiment running.

After 10 years of running at nominal LHCb luminosity, the following radiation levels are expected at the location of the ST service boxes:

LOCATION	TID (rad)	NIEL (1MeV equivalent neutrons)	SEE (>20 MeV hadron/cm^2)
T1 service box	$13 \cdot 10^3$	$1.2 \cdot 10^{12}$	$7.4 \cdot 10^{10}$
T2 service box	$14 \cdot 10^3$	$1.5 \cdot 10^{12}$	$8.1 \cdot 10^{10}$
T3 service box	$15 \cdot 10^3$	$1.6 \cdot 10^{12}$	$9.3 \cdot 10^{10}$
TT service box	$14 \cdot 10^3$	$2 \cdot 10^{12}$	$1.2 \cdot 10^{11}$

Table 3.1 : Expected radiation levels for ST service boxes

Including the safety factors:

- Radiation qualification uncertainty → ×2
- TID/NIEL – component variations on the same fabrication line → ×2

The following radiation test levels have to be reached:

TID (rad)	NIEL (n/cm^2)	SEE (p/cm^2)
$60 \cdot 10^3$	$80 \cdot 10^{11}$	$4 \cdot 10^{11}$

Table 3.2 : Radiation levels to be reached

Active components radiation assurance:

- TTCrq : CERN rad-hard development. The 2.5V regulator must be removed from the board.

- Delay25: CERN rad-hard development.

- LHC4913 regulators: CERN rad-hard development.

- DCU: CERN rad-hard development.

- SPECS: tested successfully up to ~30krad.

- AD8129 diff amplifier: tested successfully by the ST group.

- AD780 voltage reference: tested by NASA for TID (up to 100krad) and Agapito et al. [Y] for neutrons (up to $5 \cdot 10^{12}$, when it should withstand for safety up to $8 \cdot 10^{12}$). It has been mounted on DIP socket so it can be replaced.

- DS90LV047A and DS90LV048A lvds transmitter and receiver: tested by Atlas and LHCb.

- DS92LV010A transceiver: tested by Atlas and LHCb.

- BSR17A(Fairchild) NPN transistor: tested by Eva Calvo till 80krad in her WBTN (Wide Band Time Normalizer) board for the beam position monitoring.

- SN74125D quad tristate gate: tested by Orasy Calo group up to 24.5krad.

4. Control Board testing, results and installation

4.1. Control board tests

Extensive tests have been performed in the 2 first versions of the CB. In order to perform a complete testing of the CB functionalities a complex setup with all the ST readout and DAQ electronics and special software has been developed. The setup is being used for the Inner Tracker ladder production test and consists of the following elements:

- 1 Control board.
- 1 svce box with backplane.
- 8 Dig boards.
- 1 TELL1 (old firmware with L1 trigger).
- 1 Readout Supervisor (old firmware with L1 trigger) and the VME electrical to optical translator boards (TTCvi and TTCtx).
- Crate for the TELL1 and the Readout Supervisor.
- 1 SPECS master.
- A Temperature Cycling Box where up to 6 IT ladders can be tested.
- LV and HV power supplies.
- Copper and optical cables.

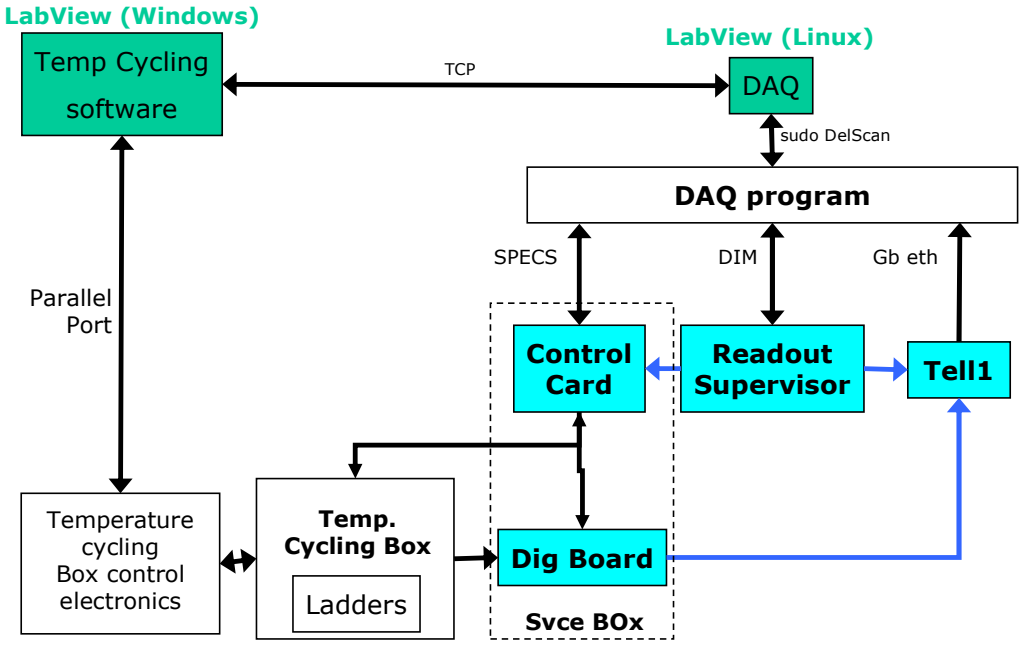


Figure 4.1: Setup simplified scheme.

With the described setup different run acquisitions have been developed:

- Run a delay scan in order to look the signal peak.
- Run pedestal acquisitions.

- Run channel scans in the peak position pulsing 1 out of every 8 strips.
- Perform S/N tests on the electronics.
- Perform ADC timing scans.
- …

Below is shown the sequence of commands we use for performing a delay scan:

1. Start up ReadOut supervisor and TELL1 via ssh command call. This is the only step which is not executed by our IT data acquisition program.

2. Initalize SPECS comunications.

3. Initialize Svce Box electronics with default values. We set the phase of the trigger and reset signals), Beetles and GOLs. In this case, the I2C bus for the TTCrx and the Delay25 chip is the internal one in the Control Board and the buses for the Beetles and GOLS are the ones going out from the I2C demultiplexer mezzanine.

   a. Reset the SPECS master and slaves calling the SPECS libraries functions:
   ```
   if (rc = specs_master_reset( theMaster ))
   if (rc = specs_slave_external_reset( theSlave1 ))
   if (rc = specs_slave_internal_reset( theSlave1 ))
   ```

   b. Initialize the SPECS Input Output register
      - Configure bits 0-23 in output mode and also
      - Set the bits 0 to 19 (regulator INH signals to 0). Set bit 20, 21 and 23 (TTCrq reset, TTCrqQPLL reset and GOL reset) to “0” since these signals are inverted later. Set bit 22 (/QPLL reset) to “1”.

   c. Sleep 1 second.

   d. Initialize the TTCrq. The I2C base address is 0x5E.
      - First, we perform a TTCrq reset via I2C. Write in the TTCrq pointer register address (0x5E) the value TTCrq_STATUS_REGISTER (0x16) and then send another I2C command to the data register address (0x5F) the value (0x05) in order to perform the reset.
      - Write back again a 0x00 to the same register in case the watchdog reset flag has been activated.
      - Enable the Clk2 output and set the Clk1 as the synchronization clock. We write into the TTCrq_CONTROL_REGISTER (0x03) the data value 0x08 in order to enable the CLK2 output.

   e. Initialize the SPECS channel B decoder and the Delay 25 chip.
      - First we program the SPECS to work synchronous with Clock1, not with the SPECS local oscillator.
      - Set the Delay chip frequency mode to 40 Mhz, force the DLL resynchronization, and enable the several outputs in the next order: Testpulse, Trigger, L0reset and clock. Code below:

```
8 * delay25Address = new U8(DELAY25CHIP_I2C_ADD);
U8 * regAddress = new U8(0x5);
U8 * regValue   = new U8(0x0) ;
U8 * data   = new U8(0x0) ;

// First we set clock frequency mode in the CGR register: [M1 M0] = [0 0] ->
40 MHz
// CGR : [GRST IDLL nu nu nu nu M1 M0]
rc  =  specsDelay25Write(  &theSlave1  ,  *delay25Address  ,  *regAddress  ,
*regValue ) ;
if(rc){
    printf(" Error with code = %X \n\n", rc);
    return((int)rc);
}

// Secondly we reset the ASIC and force the resinchronization of the DLL. This
action resets
```

```
// the value of the CR4 register (Control Register for clock channel), but not
the contents
// of the  GCR (General Control Register)
*regValue = 0x80;
rc  =  specsDelay25Write(  &theSlave1  ,  *delay25Address  ,  *regAddress  ,
*regValue ) ;
if(rc){
    printf(" Error with code = %X \n\n", rc);
    return((int)rc);
}

// We enable the channel 3 which is the channel for the TestPulse signal and
set the delay to 0
*regValue = 0x40 | TP_INICIAL_DELAY;
*regAddress = DELAY25CHIP_CR3;

rc  =  specsDelay25Write(  &theSlave1  ,  *delay25Address  ,  *regAddress  ,
*regValue ) ;

// We enable the channel 2 which is the channel for the Trigger signal and set
the delay to 0
*regValue = 0x40 | TRIG_INICIAL_DELAY;
*regAddress = DELAY25CHIP_CR2;

rc  =  specsDelay25Write(  &theSlave1  ,  *delay25Address  ,  *regAddress  ,
*regValue ) ;
if(rc){
    printf(" Error with code = %X \n\n", rc);
    return((int)rc);
}

// We enable the channel 1 which is the channel for the L0Reset signal and set
the delay to 0
*regValue = 0x40 | L0_RESET_INICIAL_DELAY;
*regAddress = DELAY25CHIP_CR1;

rc  =  specsDelay25Write(  &theSlave1  ,  *delay25Address  ,  *regAddress  ,
*regValue ) ;
if(rc){
    printf(" Error with code = %X \n\n", rc);
    return((int)rc);
}

// We enable the channel 4 which is the channel for the Clock1 signal and set
the delay to 0
*regValue = 0x40 | CLOCK1_INICIAL_DELAY;
*regAddress = DELAY25CHIP_CR4;

rc  =  specsDelay25Write(  &theSlave1  ,  *delay25Address  ,  *regAddress  ,
*regValue ) ;
if(rc){
    printf(" Error with code = %X \n\n", rc);
    return((int)rc);
}
```

f. Program all the Beetles using the next default values.

- This is the I2C frame we use for the Beetle register parameters

```
#define BEETLE_VFS00

    0x00,/* Register number*/            \
    0x2C,   /* Itp, test pulse bias current, = 2MIPS */             \
    0x4C,   /* Ipre, preamplifier bias current */          \
    0x0A,   /* Isha, shaper bias current */            \
    0x0A,   /* Ibuf, front-end buffer bias current */      \
    0x00,   /* Vfp, preamplifier feedback voltage */       \
    0x00,   /* Vfs, shaper feedback voltage */         \
    0x05,   /* Icomp, comparator bias current */           \
    0x00,   /* Ithdelta, current defining incremental comparator threshold */\
    0x00,   /* Ithmain, current defining common comparator threshold */ \
    0x00,   /* Vrc, comparator RC time constant */         \
    0x0D,   /* Ipipe, pipeamp bias current */          \
    0x82,   /* Vd, pipeamp reset potential */          \
    0x69,   /* Vdcl, pipeamp reference voltage */          \
    0x14,   /* Ivoltbuf, pipeamb buffer bias current */    \
    0x1A,   /* Isf, multiplexer buffer bias current */     \
    0x66,   /* Icurrbuf, output buffer bias current */     \
    0x5C,   /* Latency, trigger latency */             \
```

```
    0x1C,   /* R0Ctrl, readout control, 1A = 1 port, 1C = 4 ports */ \
    0x00,   /* RclkDiv, ratio between Rclk and Sclk */      \
    0x0A    /* CompCtrl, comparator control */
```

- And this is the I2C frame for the test pulse mask

```
// BEETLE_TPSELECT_DATA RegisterAddress, Ch7-0, Ch15-8, ... Ch127-120
#define BEETLE_TPSELECT_DATA
0x16,0xff,0xff,0xff,0xff,0xff,0xff,0xff,0xff,0xff,0xff,0xff,0xff,0xff,0xff,0xf
f,0xff
```

g. Program all the GOLs :
- Program in the Configuration register 3 the value 0x81, so we set the laser driver current to 1,4mA and also enable the utilization of the configuration register3 and 2. Set in the Config register 2 the value 0x16. The code is below:

```
/* Programming GOL config register 3 for setting the laser-diode bias
   current and the PLL charge pump curren */
*nValues = 1;
data[0] = GOL_CONF3_REG;
rc = specs_i2c_write( &theSlave1 , *outputSelect , *i2cAddress2 ,*nValues ,
data ) ;
if(rc){
  printf(" Error with code = %X \n\n", rc);
  return((int)rc);
}
data[0] = GOL_CONF3_REG_DATA; //(0x81)
rc      =      specs_i2c_write(      &theSlave1      ,      *outputSelect      ,
(*i2cAddress2)+1 ,*nValues , data ) ;
if(rc){
  printf(" Error with code = %X \n\n", rc);
  return((int)rc);
}

/* Now we set in the values for the GOL conf register 2: PLL charge-pump
current
   and other thigs ... */
*nValues = 1;
data[0] = GOL_CONF2_REG;
rc = specs_i2c_write( &theSlave1 , *outputSelect , *i2cAddress2 ,*nValues ,
data ) ;
if(rc){
  printf(" Error with code = %X \n\n", rc);
  return((int)rc);
}

data[0] = GOL_CONF2_REG_DATA; // (0x16)
rc      =      specs_i2c_write(      &theSlave1      ,      *outputSelect      ,
(*i2cAddress2)+1 ,*nValues , data ) ;
if(rc){
  printf(" Error with code = %X \n\n", rc);
  return((int)rc);
}
```

h. Sleep 1 second.

4. Set the timing for the ADC clock shifting the TTCrx clock2. Here is the code:

```
// Select the register of the clock which is going to be deskewed
if (clockNum == 1)
    regClockSelected = TTCrq_FINE_DELAY1_REG;
else if (clockNum == 2)
    regClockSelected = TTCrq_FINE_DELAY2_REG;
else{
    printf( " TTCrq Clock selected doesn't exist, select 1 or 2");
    return(-35);
}

data[0] = regClockSelected;

rc = specs_i2c_write( &theSlave1 , outputSelect , i2cAddress ,nValues ,data) ;
if (rc) {
   printf(" Error with code = %X \n\n", rc);
```

```
   return((int)rc);
}

// Write the selected delay into the TTCrq acording to the conversion formula
// fineDelay is the number of 104 ps steps
fineDelayMSB = fineDelay % 15;
fineDelayLSB = ((fineDelay/15) - fineDelayMSB + 14) % 16;
fineDelayRegValue = 16*fineDelayMSB + fineDelayLSB;

rc = specs_i2c_write( &theSlave1 , outputSelect , i2cAddress+1 ,nValues ,
&fineDelayRegValue ) ;
if(rc){
   printf(" Error with code = %X \n\n", rc);
   return((int)rc);
}
```

5. We initialize the RS parameters using our TFC DIM client.

6. Initialize the event building libraries.

7. Run a delay scan in order to look the signal peak:
   a. Program the Beetles with the proper TestPulse mask and read them back just to confirm that they have been properly programmed.
   b. Send a L0 and L1 reset.
   c. We loop for every delay point in which we do:
      i. Delay the test pulse signal.
      ii. Run the desired number of events from the RS/TELL1: we program the RS for working with single shots, so we won't lose any event due to GBE card buffer overflows. After programming it, we send a L0 and L1 reset. Then we start the RS run and send as many single shots as we want and stop the RS run.
   d. We analyze the data looking for the signal peak.

8. Run a pedestal acquisition in the peak position. We don't loop for every delay point, we just get data in the position where we found the peak.

9. Run a new “fine” delay scan but focusing around values next to the peak.

10. Run channel scan in the peak position pulsing 1 out of every 8 channels. We loop eight times since we are pulsing in every loop just one out of eight channels. This means that at the beginning of every loop we have to program the Beetles with the proper test pulse mask and then we get the events.

11. We switch OFF the regulators, electronics and close all the connections (SPECS, odin ...).

For testing and calibrating the temperature sensors and the DCU acquisition a specific program has been developed (figure 4.7). Also a custom home made PCB has been built. With this PCB we can connect to each temperature and humidity channel 3 different resistances using some jumpers. In the program we choose in which of the positions the jumpers are set and then we run a data acquisition of hundreds of events. This average and standard deviations of each channel for each jumper position is stored into a text file in csv format.

4.2. Some results

Next figures show analyzed data taken with the setup.

The figure 4.2 shows a typical delay scan using the calibration signal. We can observe how the Beetle signal amplitude evolves with time. We can also observe the pedestal behaviour. The calibration signal permits looking for shorted or opened sensor strips, that’s the reason for performing channel scans. In the bottom plot of the figure we can observe how strips 247 and 251 seem to be unbonded: the signal height is higher since the capacitance seen by the Beetle channel is lower.

Figure 4.3 represents the raw noise, the noise distribution, the Beetle pedestals and the S/N analysis for one Beetle. In each row are represented the mentioned subjects respectively, and each column represents one Beetle port.

The figure 4.4 represents an ADC timing scan for the S/N of one Beetle chip. The test consists of shifting the "Clock40Des2" from the TTCrq. The first plot (top left corner) shows the S/N averaged for all the Beetle channels. The following ones represent the S/N for individual channels. We can find that some channels seem to be noisier and that for sampling points next to the signal edge the S/N is better. The x-axis units (the delay) is 104ps.

The figure 44.5 shows the noise behavior when using data cables of 2.7m and 5.5m, and the figure 4.6 shows the noise relation with respect to different ADC timings.

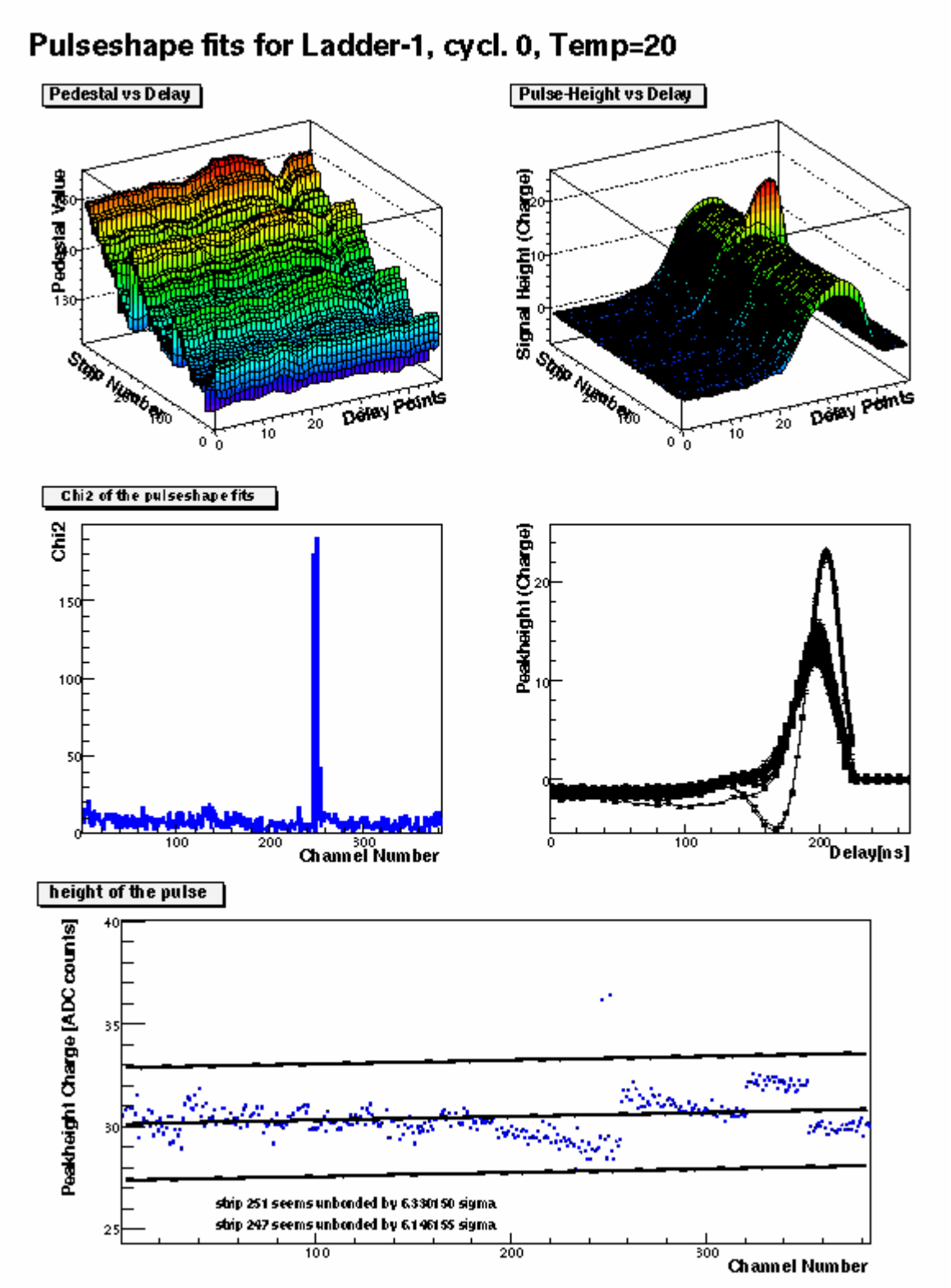


Figure 4.2: The top plots represent pedestal and signal height values vs delay using the calibration signal. The plot at the bottom shows the ADC read value at the signal peak time position for all the channels.

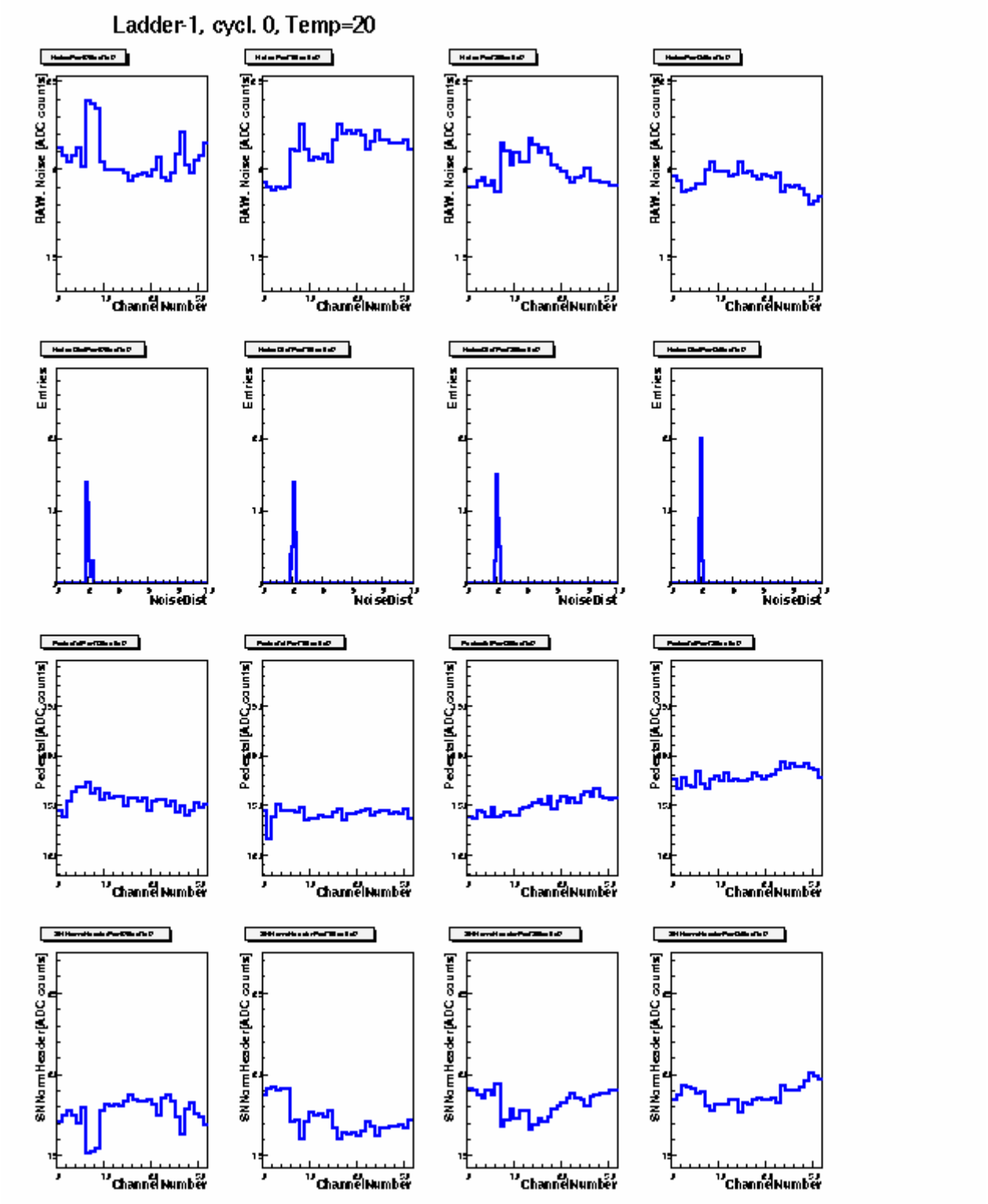


Figure 4.3 : The figures in the first row show the raw noise (ADC counts) for the 4 ports of one Beetle. The second row shows the noise distribution for the 4 ports. In the row 3 we can see the pedestal values and in the bottom row the S/N in the 4 ports.

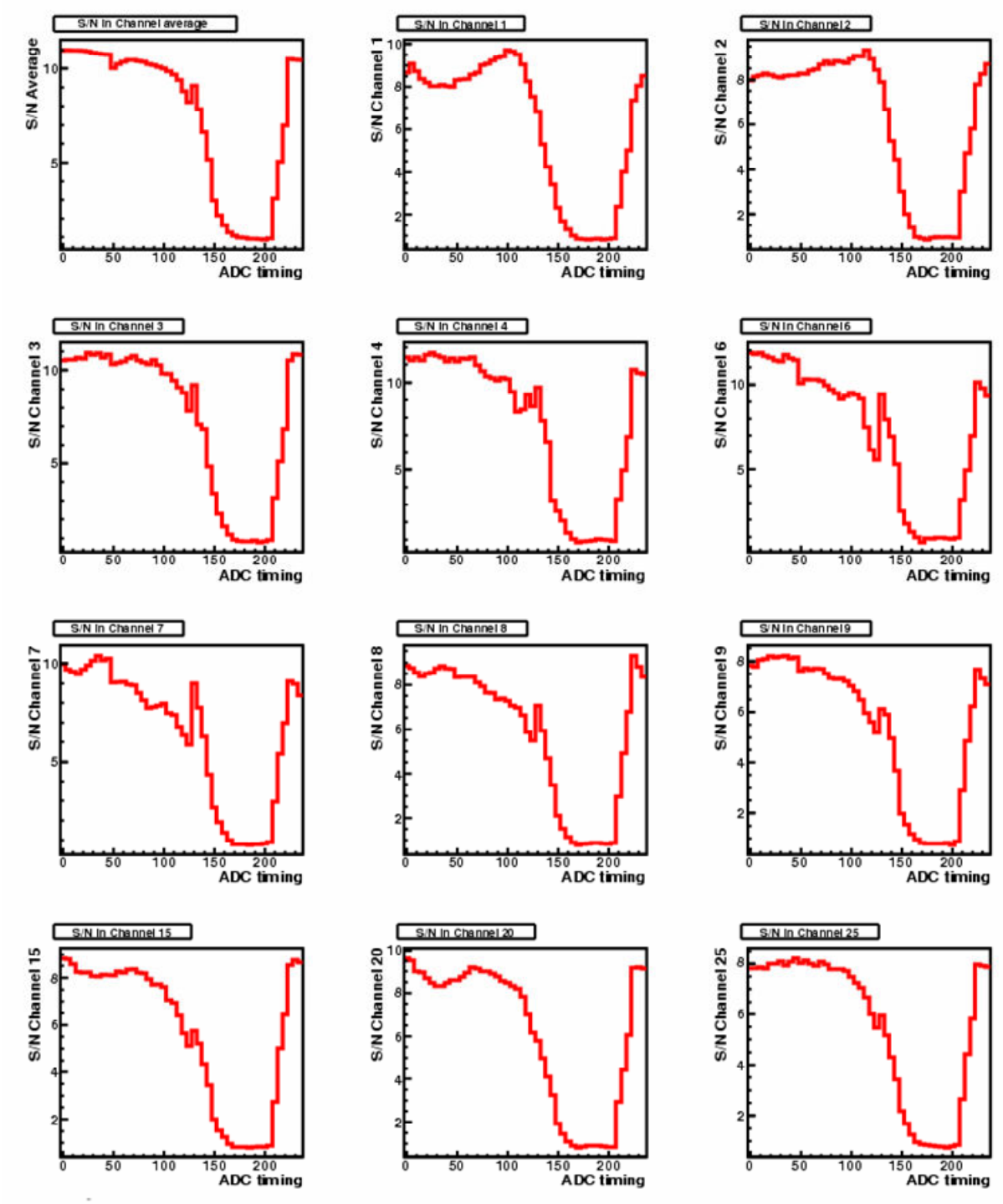


Figure 4.4 : ADC timing for the S/N. The first plot (top left corner) show an ADC timing scan of the S/N on one Beetle (averaged for all the channels). The other plots are for individual channels. As it can be seen there are channels which are slightly more noisy than others.

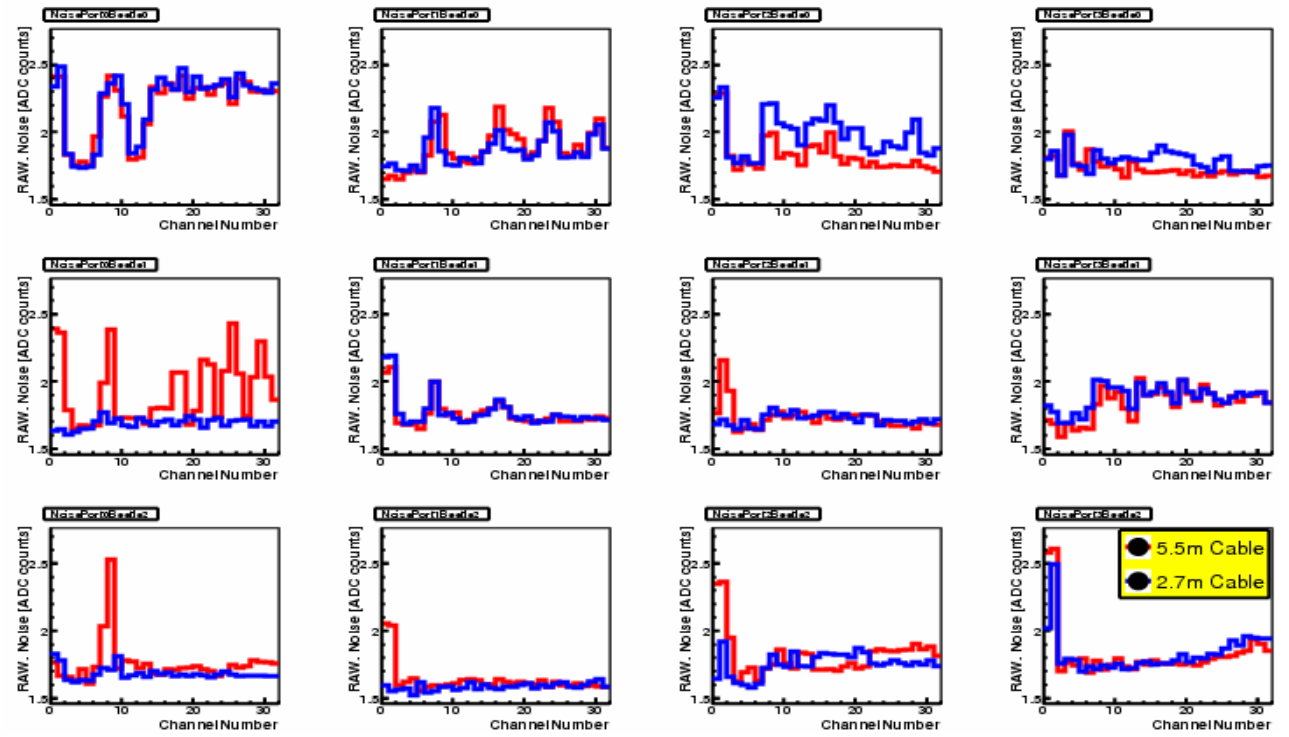


Figure 4.5 : raw noise for the 3 Beetles of one ladder. Each column is for each Beetle port, and the red line is for a 5.5m data cable (cable from DB to Hybrid) and the blue line is for a 2.7m one.

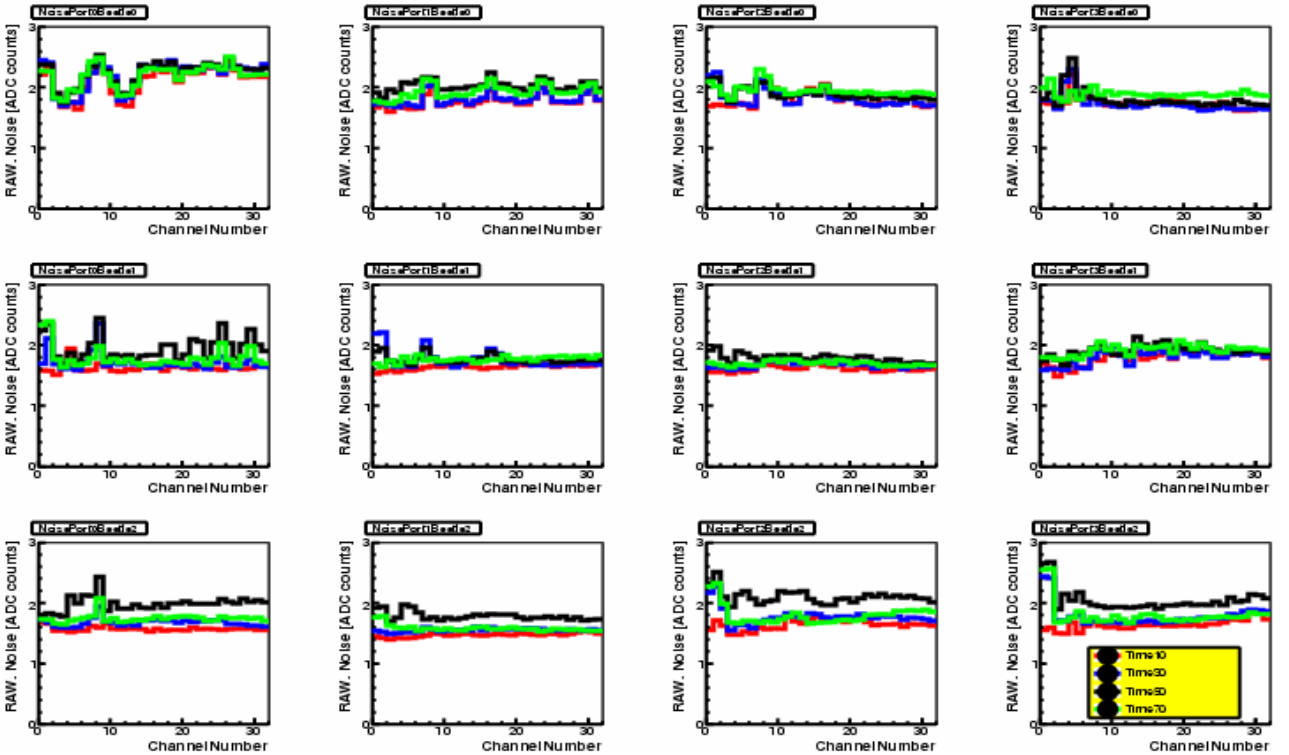


Figure 4.6: raw noise for different ADC timings. A tiny improvement in the noise can be obtained by adjusting the ADC clock timing.

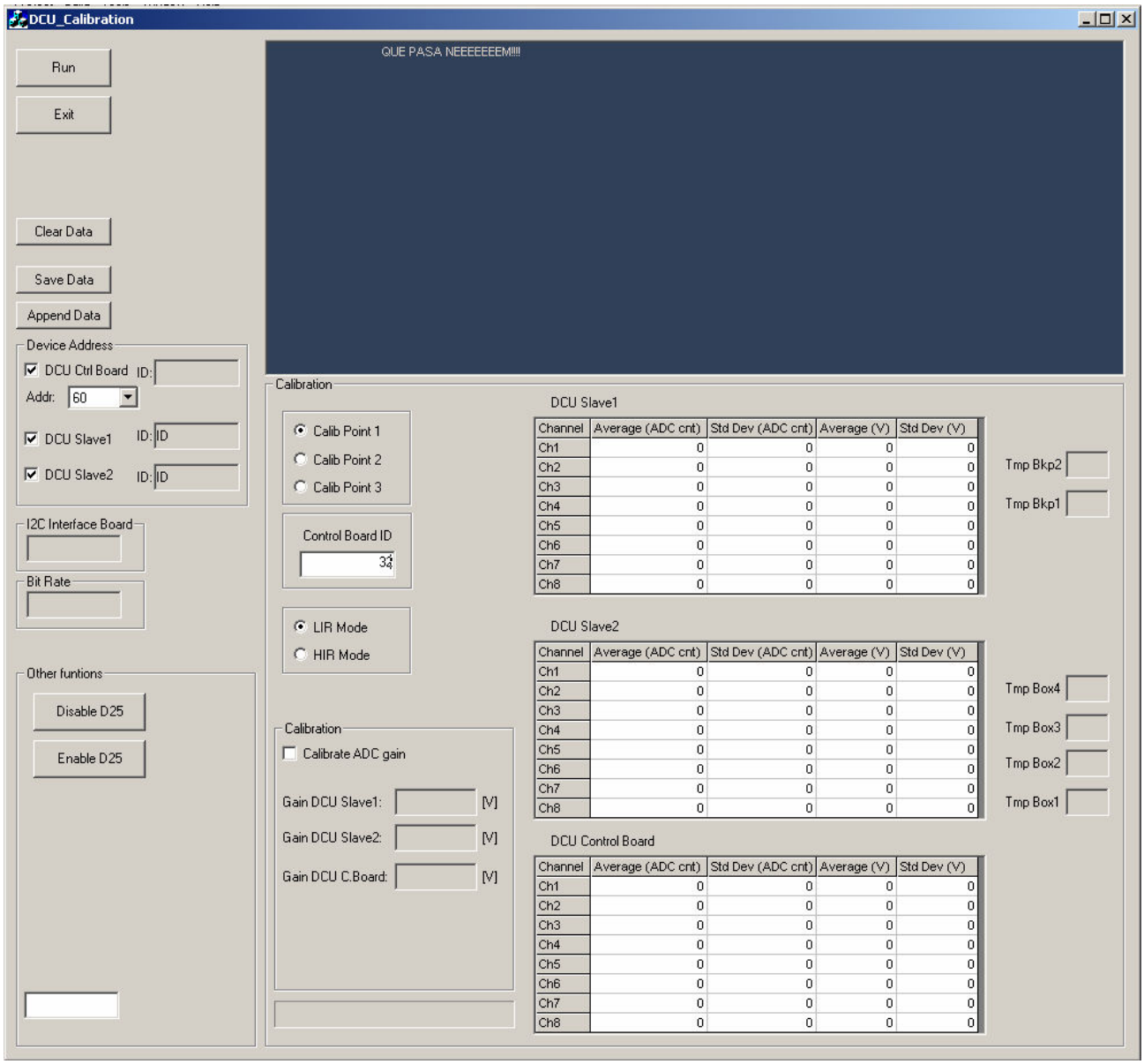


Figure 4.7: DCU calibration program

4.3. Control Board installation

For the installation of the CB in the svce box some few things should always be kept in mind.

- All the SPECS slaves in the same SPECS bus need to have different addresses. The address is set in the mezzanine by means of a micro-switch. As a general convention we can assign consecutive numbers from 1 to N to the mezzanines, with the address number increasing as the SPECS bus grows: 1 and 2 addresses for the 1st CB, 3 and 4 for the 2nd and so on. This implies that whenever a mezzanine is replaced, the same address as the previous one must be set.

- The jumpers need to be plugged as explained in sections 2.5.1(for connecting the TTCrq I2C bus) and 2.6 (for the SPECS bus).

- The upper RJ45 in the CB is for connecting the cable coming from the master or the previous CB, and therefore the bottom one is for continuing the SPECS chain.

- In case the 1st mezzanine is used in master mode, the RJ45 cable from the master will connect to the mezzanine connector. In this case, the resistors that connect the connector case to ground in the mezzanine must be removed. Like this the cable shield is just connected to ground in the master side, so a little bit of "bricolage" has to be done for connecting the cable shield to ground in the svce box. Also the mezzanine needs to be fastened to the CB using screws in order to avoid cable tensions that could unplug it. For this reason is recommended to use all the mezzanines in slave mode, but due to signal integrity problems maybe is not possible.

- Due to the SPECS link configuration, whenever exists a problem which implies switching off the CB, that is, the low voltage power supply lines for the svce. box, the whole SPECS link is lost since the SPECS chaining devices will be off. This implies loosing half station in the IT detector and one quadrant in the TT. Re-cabling of the SPECS link must be done as soon as access to the svce. boxes is granted.

- The cable shields must be connected to the svce box case using the dedicated pins in the CB as shown in section 2.2.2.

- It is necessary to keep track of every installed HMX2000 sensor since their calibration curves are unique.

- In case the I2C mezzanines described in 2.9 are not upgraded to the rad-hard FPGA version, for safety reasons they should be replaced after 5 years of experiment running.

- The same applies to the AD780 voltage reference, although in this case they can most probably survive for the 10 years. Anyhow using the dual switch we can get rid of the AD780 and use the 2.5V from the regulator.

- A hole in the CB frontal has been foreseen for hooking a tool for easing the extraction of the board.

Appendix A: HMX2000 calibration data

Sensor Pos	S/N	Bridge Output (mV)	Vref (excitation)	%RH@Pc	Chamber %RH @ PcTc	Satur PSI	Chmbr PSI	Satur T	Chmbr T	Flow l/m	Reading #
13	43-0652	-4,59924	1,251	10,2134	9,99328	141,085	14,0566	9,99753	10,3241	19,5188	1
13		-2,75345	1,251	20,3914	19,9523	69,7181	14,0617	10,0048	10,33	19,8883	2
13		-1,12944	1,251	30,69	30,0227	46,1258	14,0668	10,003	10,3315	20,2686	3
13		-4,90199	1,251	10,3565	10,0044	139,369	14,0857	5,00097	5,49806	20,0578	4
13		-3,05654	1,251	20,6452	19,9525	68,9714	14,0867	5,00386	5,49425	19,7399	5
13		-1,26521	1,251	31,0597	29,9992	45,6505	14,0911	5,00445	5,50363	19,7681	6
13		-5,18234	1,251	10,4359	10,0453	139,066	14,0487	-0,00399	0,5204	20,2812	7
13		-3,2706	1,251	20,7122	19,9442	68,5355	14,0437	0,00505	0,52574	19,6493	8
13		-1,59962	1,251	31,1223	29,9931	45,416	14,0473	0,00289	0,51187	20,2202	9
13		-5,59647	1,251	10,6265	10,0163	137,188	14,1099	-4,98945	-4,29685	20,0535	10
13		-3,67131	1,251	21,1611	19,952	67,6188	14,1053	-5,00617	-4,31606	20,326	11
13		-1,94111	1,251	31,7691	29,9512	44,7708	14,1067	-5,00743	-4,31628	19,7234	12
13		-6,10248	1,251	10,8288	9,99942	134,413	14,0861	-10,0094	-9,10886	20,0139	13
13		-4,35654	1,251	21,5878	19,9719	66,2179	14,0912	-9,99835	-9,11898	20,1191	14
13		-2,74065	1,251	32,3884	30,0318	43,8838	14,0963	-9,99227	-9,13853	20,355	15
14	43-0604	-6,14791	1,251	10,2134	9,99272	141,084	14,0565	9,99753	10,3241	19,5179	1
14		-4,36302	1,251	20,3939	19,9548	69,7091	14,0617	10,0047	10,33	19,8864	2
14		-2,77049	1,251	30,69	30,0227	46,1258	14,0668	10,003	10,3315	20,2686	3
14		-6,47423	1,251	10,3565	10,0044	139,369	14,0857	4,99862	5,49806	20,0578	4
14		-4,68355	1,251	20,6452	19,9525	68,9714	14,0867	5,00386	5,49425	19,7399	5
14		-2,92772	1,251	31,0666	30,0023	45,6403	14,0911	5,00269	5,50354	19,7665	6
14		-6,77049	1,251	10,4359	10,0472	139,066	14,0488	-0,00203	0,52013	20,2803	7
14		-4,90584	1,251	20,7122	19,9442	68,5355	14,0437	0,00505	0,52574	19,6493	8
14		-3,26084	1,251	31,1236	29,9943	45,414	14,0473	0,00328	0,51234	20,2207	9
14		-7,19395	1,251	10,6264	10,0172	137,188	14,1098	-4,98945	-4,29685	20,0535	10
14		-5,30806	1,251	21,1611	19,952	67,6188	14,1053	-5,00617	-4,31606	20,326	11
14		-3,60193	1,251	31,7691	29,9512	44,7706	14,1067	-5,00919	-4,3162	19,7216	12
14		-7,71942	1,251	10,8288	9,99942	134,411	14,0862	-10,0075	-9,1077	20,0157	13
14		-6,00146	1,251	21,5878	19,9719	66,2179	14,0912	-9,99835	-9,11898	20,1191	14
14		-4,4077	1,251	32,3812	30,0182	43,8936	14,0963	-9,99468	-9,13832	20,3547	15
15	43-0591	-7,99037	1,251	10,2134	9,99272	141,084	14,0565	9,9982	10,3241	19,5179	1
15		-6,2551	1,251	20,3939	19,9548	69,7091	14,0617	10,0047	10,33	19,8864	2
15		-4,70473	1,251	30,69	30,0227	46,1258	14,0668	10,0023	10,3324	20,2681	3
15		-8,36772	1,251	10,3568	10,0027	139,367	14,0858	4,99862	5,49847	20,0609	4
15		-6,62104	1,251	20,6452	19,9525	68,9714	14,0867	5,00396	5,49425	19,7399	5
15		-4,90615	1,251	31,0666	30,0023	45,6403	14,0911	5,00269	5,50354	19,7665	6
15		-8,69717	1,251	10,4359	10,0472	139,066	14,0488	-0,00025	0,5208	20,2798	7
15		-6,88485	1,251	20,7106	19,9416	68,5405	14,0437	0,00527	0,52679	19,649	8
15		-5,29081	1,251	31,1236	29,9943	45,414	14,0473	0,00328	0,51234	20,2207	9
15		-9,16159	1,251	10,6264	10,0172	137,188	14,1098	-4,98945	-4,29685	20,0535	10
15		-7,32626	1,251	21,1601	19,9524	67,6219	14,1053	-5,00534	-4,31601	20,3266	11
15		-5,6714	1,251	31,7693	29,9467	44,7706	14,1067	-5,00919	-4,3162	19,7216	12
15		-9,73405	1,251	10,8291	10,0004	134,411	14,0862	-10,0075	-9,1077	20,0157	13
15		-8,0691	1,251	21,5931	19,9763	66,2014	14,0912	-9,99749	-9,11783	20,1193	14
15		-6,52043	1,251	32,3812	30,0182	43,8936	14,0963	-9,99778	-9,13903	20,3547	15
16	43-0595	-7,69339	1,251	10,2135	9,99339	141,082	14,0564	9,9982	10,3238	19,515	1
16		-5,94488	1,251	20,397	19,9578	69,6982	14,0617	10,0047	10,33	19,8862	2
16		-4,3748	1,251	30,6908	30,0204	46,1245	14,0668	10,0023	10,3324	20,2681	3
16		-8,06339	1,251	10,3568	10,0016	139,366	14,0858	4,99738	5,49884	20,0633	4
16		-6,30896	1,251	20,6463	19,9539	68,9682	14,0868	5,00396	5,49409	19,7397	5
16		-4,55533	1,251	31,0738	30,0062	45,6296	14,0911	5,00109	5,50346	19,7646	6
16		-8,33804	1,251	10,436	10,0482	139,066	14,0488	-0,00025	0,5208	20,2798	7
16		-6,53559	1,251	20,7106	19,9416	68,5405	14,0437	0,00527	0,52679	19,649	8
16		-4,92515	1,251	31,1245	29,9951	45,4128	14,0473	0,00363	0,51276	20,22	9
16		-8,83901	1,251	10,6265	10,0181	137,189	14,11	-4,98742	-4,29584	20,0549	10
16		-7,01765	1,251	21,1601	19,9524	67,6219	14,1053	-5,00534	-4,31601	20,3266	11
16		-5,35081	1,251	31,7693	29,9467	44,7703	14,1067	-5,00989	-4,31613	19,7191	12
16		-9,3839	1,251	10,8291	10,0004	134,411	14,0862	-10,0058	-9,1077	20,0157	13
16		-7,72765	1,251	21,5931	19,9763	66,2014	14,0912	-9,99749	-9,11783	20,1193	14
16		-6,17315	1,251	32,3741	30,0053	43,9034	14,0963	-9,99778	-9,13903	20,3571	15
17	43-0661	-8,95675	1,251	10,2135	9,99339	141,082	14,0564	9,99881	10,3238	19,515	1
17		-7,18182	1,251	20,397	19,9578	69,6982	14,0617	10,0047	10,33	19,8862	2
17		-5,60139	1,251	30,6917	30,0184	46,1232	14,0668	10,0007	10,3322	20,2678	3
17		-9,26977	1,251	10,3568	10,0016	139,366	14,0858	4,99738	5,49884	20,0633	4
17		-7,49484	1,251	20,6463	19,9539	68,9658	14,0866	5,00314	5,49396	19,7393	5
17		-5,76595	1,251	31,0738	30,0062	45,6296	14,0911	5,00109	5,50346	19,7646	6
17		-9,59371	1,251	10,436	10,0482	139,066	14,0488	-0,00025	0,5208	20,2798	7
17		-7,75147	1,251	20,7094	19,9391	68,5455	14,0438	0,00456	0,52684	19,6501	8
17		-6,1229	1,251	31,1245	29,9951	45,4128	14,0473	0,00363	0,51276	20,22	9
17		-9,99088	1,251	10,6266	10,019	137,189	14,1101	-4,98559	-4,29492	20,0535	10
17		-8,13436	1,251	21,1594	19,9514	67,6241	14,1053	-5,00459	-4,31507	20,3257	11
17		-6,44965	1,251	31,7695	29,9449	44,7703	14,1067	-5,00989	-4,31613	19,7191	12
17		-10,5092	1,251	10,8294	10,002	134,408	14,0863	-10,0058	-9,10755	20,0176	13
17		-8,8287	1,251	21,5987	19,9777	66,1841	14,0912	-9,99852	-9,11678	20,1201	14
17		-7,25694	1,251	32,3741	30,0053	43,9034	14,0963	-9,99878	-9,13903	20,3571	15
18	43-0584	-4,03235	1,251	10,2136	9,99414	141,079	14,0563	9,99881	10,3235	19,5133	1
18		-2,56433	1,251	20,4007	19,9614	69,6851	14,0616	10,0038	10,3291	19,8849	2
18		-1,24845	1,251	30,6917	30,0184	46,1232	14,0668	10,0007	10,3322	20,2678	3
18		-4,27725	1,251	10,357	10,0016	139,363	14,0857	4,99807	5,49918	20,0661	4
18		-2,8021	1,251	20,6468	19,9534	68,9658	14,0866	5,00314	5,49396	19,7393	5
18		-1,34646	1,251	31,081	30,0122	45,6189	14,0911	5,00145	5,50429	19,7639	6

Sensor Pos	S/N	Bridge Output (mV)	Vref (excitation)	%RH@Pc	Chamber %RH @ PcTc	Satur PSI	Chmbr PSI	Satur T	Chmbr T	Flow l/m	Reading #
18		-4,40276	1,251	10,3521	9,96829	139,067	14,0489	0,00135	0,52138	20,28	7
18		-2,86565	1,251	20,7094	19,9391	68,5455	14,0438	0,00456	0,52684	19,6501	8
18		-1,50946	1,251	31,125	29,9954	45,4121	14,0473	0,00395	0,51315	20,221	9
18		-4,82277	1,251	10,6266	10,019	137,189	14,1101	-4,98559	-4,29492	20,0535	10
18		-3,25359	1,251	21,1594	19,9514	67,6241	14,1053	-5,00459	-4,31507	20,3257	11
18		-1,83754	1,251	31,7695	29,9449	44,7698	14,1067	-5,00961	-4,31515	19,7159	12
18		-5,23125	1,251	10,8294	10,002	134,406	14,0864	-10,0043	-9,10833	20,0195	13
18		-3,80497	1,251	21,5987	19,9777	66,1841	14,0912	-9,99852	-9,11678	20,1201	14
18		-2,4781	1,251	32,3671	29,9954	43,913	14,0963	-9,99878	-9,13876	20,3575	15
19	43-0747	-5,3122	1,251	10,2136	9,99414	141,079	14,0563	9,99881	10,3235	19,5133	1
19		-3,5002	1,251	20,4007	19,9614	69,6851	14,0616	10,0038	10,3291	19,8849	2
19		-1,89564	1,251	30,6926	30,0167	46,1219	14,0668	9,99934	10,3321	20,2665	3
19		-5,649	1,251	10,357	10,002	139,363	14,0857	4,99807	5,49918	20,0661	4
19		-3,82791	1,251	20,6468	19,9534	68,963	14,0865	5,0024	5,49383	19,739	5
19		-2,07195	1,251	31,081	30,0122	45,6189	14,0911	5,00145	5,50429	19,7639	6
19		-6,011	1,251	10,3521	9,96829	139,067	14,0489	0,0028	0,52192	20,2811	7
19		-4,11904	1,251	20,708	19,9381	68,5507	14,044	0,00392	0,52598	19,6518	8
19		-2,45844	1,251	31,125	29,9954	45,4121	14,0473	0,00395	0,51315	20,221	9
19		-6,45123	1,251	10,6266	10,019	137,189	14,1101	-4,98482	-4,29409	20,053	10
19		-4,53605	1,251	21,1589	19,9522	67,6256	14,1053	-5,0039	-4,31512	20,3251	11
19		-2,81208	1,251	31,7698	29,9435	44,7698	14,1067	-5,00961	-4,31515	19,7159	12
19		-6,99992	1,251	10,8296	10,0042	134,406	14,0864	-10,0043	-9,10833	20,0195	13
19		-5,26175	1,251	21,6044	19,9781	66,1663	14,0912	-10,0004	-9,11583	20,1211	14
19		-3,64625	1,251	32,3671	29,9954	43,913	14,0963	-9,99878	-9,13876	20,3575	15
20	43-0730	-7,80315	1,251	10,2138	9,99486	141,078	14,0564	10,0003	10,3241	19,5142	1
20		-6,0109	1,251	20,4048	19,9642	69,6709	14,0616	10,002	10,3283	19,8846	2
20		-4,41424	1,251	30,6926	30,0167	46,1219	14,0668	9,99934	10,3321	20,2665	3
20		-8,14523	1,251	10,357	10,002	139,363	14,0857	4,99868	5,49918	20,0661	4
20		-6,34844	1,251	20,6474	19,9531	68,963	14,0865	5,0024	5,49383	19,739	5
20		-4,59558	1,251	31,0885	30,0204	45,6078	14,0911	5,00178	5,50415	19,7631	6
20		-8,47365	1,251	10,3521	9,96915	139,067	14,0489	0,0028	0,52192	20,2811	7
20		-6,63664	1,251	20,7067	19,9355	68,5559	14,0441	0,00334	0,5261	19,652	8
20		-5,0013	1,251	31,1244	29,9949	45,4129	14,0473	0,00425	0,51351	20,2212	9
20		-8,89384	1,251	10,6265	10,0189	137,191	14,1102	-4,98482	-4,29409	20,053	10
20		-7,04175	1,251	21,1589	19,9522	67,6256	14,1053	-5,0039	-4,31512	20,3251	11
20		-5,34899	1,251	31,7698	29,9435	44,7698	14,1067	-5,00847	-4,31515	19,7159	12
20		-9,43706	1,251	10,8296	10,0042	134,406	14,0864	-10,0029	-9,10833	20,0195	13
20		-7,75629	1,251	21,6044	19,9781	66,1663	14,0912	-10,0004	-9,11583	20,1211	14
20		-6,1804	1,251	32,36	29,9858	43,9227	14,0963	-9,99969	-9,13853	20,3583	15
21	43-0767	-5,98406	1,251	10,2138	9,99486	141,078	14,0564	10,0003	10,3241	19,5142	1
21		-4,23581	1,251	20,4048	19,9642	69,6709	14,0616	10,002	10,3283	19,8846	2
21		-2,6917	1,251	30,6926	30,0167	46,1203	14,0668	9,99898	10,3329	20,2646	3
21		-6,35205	1,251	10,3572	10,0024	139,361	14,0859	4,99868	5,49947	20,0689	4
21		-4,59423	1,251	20,6474	19,9531	68,9605	14,0864	5,00173	5,49372	19,7392	5
21		-2,89492	1,251	31,0885	30,0204	45,6078	14,0911	5,00178	5,50415	19,7631	6
21		-6,61235	1,251	10,3521	9,96915	139,067	14,0489	0,0028	0,52192	20,2811	7
21		-4,78956	1,251	20,7067	19,9355	68,5559	14,0441	0,00334	0,5261	19,652	8
21		-3,18873	1,251	31,123	29,9933	45,415	14,0473	0,00361	0,51293	20,2226	9
21		-7,1294	1,251	10,6265	10,0189	137,191	14,1102	-4,98482	-4,29409	20,053	10
21		-5,28637	1,251	21,1585	19,9529	67,6269	14,1053	-5,00237	-4,31425	20,3253	11
21		-3,62225	1,251	31,7704	29,9446	44,769	14,1067	-5,00847	-4,31429	19,7126	12
21		-7,67985	1,251	10,8297	10,0063	134,405	14,0865	-10,0029	-9,10902	20,0222	13
21		-5,99928	1,251	21,6099	19,977	66,149	14,0912	-10,003	-9,11496	20,12	14
21		-4,446	1,251	32,36	29,9858	43,9227	14,0963	-9,99969	-9,13853	20,3583	15
22	43-0687	-6,74403	1,251	10,2138	9,99542	141,076	14,0563	10,0007	10,3238	19,5123	1
22		-5,06471	1,251	20,4094	19,9675	69,6548	14,0616	10,0005	10,3276	19,8848	2
22		-3,5655	1,251	30,6936	30,0154	46,1203	14,0668	9,99898	10,3329	20,2646	3
22		-7,0901	1,251	10,3572	10,0024	139,361	14,0859	5,00015	5,49947	20,0689	4
22		-5,40558	1,251	20,648	19,9529	68,9605	14,0864	5,00173	5,49372	19,7392	5
22		-3,75132	1,251	31,0962	30,0306	45,5964	14,0911	5,00208	5,50311	19,7622	6
22		-7,41214	1,251	10,3521	9,96918	139,067	14,0489	0,00322	0,5224	20,2813	7
22		-5,65809	1,251	20,7067	19,9355	68,5559	14,0441	0,00334	0,5261	19,652	8
22		-4,11634	1,251	31,123	29,9933	45,415	14,0473	0,00361	0,51293	20,2226	9
22		-7,8457	1,251	10,6264	10,0187	137,193	14,1103	-4,98412	-4,29333	20,0514	10
22		-6,06515	1,251	21,1585	19,9529	67,6269	14,1053	-5,00237	-4,31425	20,3253	11
22		-4,4645	1,251	31,771	29,9446	44,7681	14,1067	-5,00653	-4,3126	19,7095	12
22		-8,39195	1,251	10,8299	10,0065	134,403	14,0865	-10,0025	-9,10876	20,0246	13
22		-6,76734	1,251	21,6099	19,977	66,149	14,0912	-10,003	-9,11496	20,12	14
22		-5,26958	1,251	32,3531	29,979	43,9322	14,0963	-10,0005	-9,13921	20,3602	15
23	43-0766	-8,49056	1,251	10,2138	9,99542	141,076	14,0563	10,0007	10,3238	19,5123	1
23		-6,91453	1,251	20,4094	19,9675	69,6548	14,0616	10,0005	10,3276	19,8848	2
23		-5,51998	1,251	30,6936	30,0154	46,1186	14,0668	9,99956	10,3336	20,2642	3
23		-8,7807	1,251	10,3575	10,0041	139,359	14,086	5,00015	5,49883	20,0719	4
23		-7,19882	1,251	20,648	19,9529	68,9605	14,0864	5,00112	5,49372	19,7392	5
23		-5,67195	1,251	31,0962	30,0306	45,5964	14,0911	5,00208	5,50311	19,7622	6
23		-9,05165	1,251	10,3521	9,96918	139,067	14,0489	0,0036	0,52285	20,28	7
23		-7,4084	1,251	20,7053	19,9318	68,5611	14,0442	0,00281	0,52713	19,6517	8
23		-5,97647	1,251	31,123	29,9933	45,415	14,0473	0,00361	0,51293	20,2226	9
23		-9,43245	1,251	10,6264	10,0187	137,193	14,1103	-4,98349	-4,29263	20,0514	10
23		-7,76439	1,251	21,1583	19,9522	67,6276	14,1052	-5,00189	-4,31346	20,3262	11
23		-6,27506	1,251	31,771	29,946	44,7681	14,1067	-5,00653	-4,3126	19,7095	12
23		-9,90895	1,251	10,8299	10,0065	134,403	14,0865	-10,0025	-9,10876	20,0246	13
23		-8,39149	1,251	21,6157	19,98	66,1311	14,0912	-10,0044	-9,11508	20,1201	14
23		-6,99302	1,251	32,3531	29,979	43,9322	14,0963	-10,0005	-9,13921	20,3602	15
24	43-0763	-6,88635	1,251	10,2139	9,99538	141,073	14,0562	10,0011	10,3244	19,5124	1

Sensor Pos	S/N	Bridge Output (mV)	Vref (excitation)	%RH@Pc	Chamber %RH @ PcTc	Satur PSI	Chmbr PSI	Satur T	Chmbr T	Flow l/m	Reading #
24		-5,16322	1,251	20,4142	19,9713	69,638	14,0616	9,99903	10,3269	19,8848	2
24		-3,62011	1,251	30,6947	30,0163	46,1186	14,0668	9,99956	10,3336	20,2642	3
24		-7,22843	1,251	10,3576	10,0041	139,357	14,0859	5,00057	5,49916	20,0751	4
24		-5,50008	1,251	20,6485	19,9539	68,9583	14,0863	5,00112	5,49271	19,7385	5
24		-3,79365	1,251	31,1046	30,0394	45,584	14,0911	5,00145	5,50216	19,7606	6
24		-7,5102	1,251	10,3522	9,9692	139,066	14,049	0,0036	0,52285	20,28	7
24		-5,75386	1,251	20,7053	19,9318	68,5611	14,0442	0,00281	0,52713	19,6517	8
24		-4,18205	1,251	31,1207	29,9885	45,4184	14,0473	0,00212	0,5124	20,2228	9
24		-7,9537	1,251	10,6261	10,0184	137,197	14,1103	-4,98349	-4,29263	20,0494	10
24		-6,18003	1,251	21,1583	19,9522	67,6276	14,1052	-5,00189	-4,31346	20,3262	11
24		-4,55406	1,251	31,771	29,946	44,7669	14,1067	-5,00385	-4,31196	19,7068	12
24		-8,48664	1,251	10,8299	10,0065	134,401	14,0866	-10,0021	-9,10851	20,0258	13
24		-6,87588	1,251	21,6157	19,98	66,1311	14,0912	-10,0044	-9,11508	20,1201	14
24		-5,36435	1,251	32,3464	29,9724	43,9414	14,0963	-10,0013	-9,13984	20,3592	15
25	43-0589	-8,46593	1,251	10,2139	9,99538	141,073	14,0562	10,0011	10,3244	19,5124	1
25		-6,7269	1,251	20,4142	19,9713	69,638	14,0616	9,99903	10,3269	19,8848	2
25		-5,17995	1,251	30,6947	30,0163	46,117	14,0668	10,0001	10,3334	20,2615	3
25		-8,81	1,251	10,3576	10,0043	139,357	14,0859	5,00057	5,49916	20,0751	4
25		-7,06062	1,251	20,6485	19,9539	68,9562	14,0864	5,00147	5,4927	19,7382	5
25		-5,35354	1,251	31,1046	30,0394	45,584	14,0911	5,00145	5,50216	19,7606	6
25		-9,08883	1,251	10,3522	9,9692	139,066	14,049	0,00395	0,52325	20,2792	7
25		-7,27555	1,251	20,7037	19,9267	68,567	14,0443	0,00143	0,52806	19,6515	8
25		-5,68515	1,251	31,1207	29,9885	45,4184	14,0473	0,00212	0,5124	20,2228	9
25		-9,54305	1,251	10,6261	10,0184	137,197	14,1103	-4,98291	-4,29263	20,0494	10
25		-7,70694	1,251	21,1581	19,9516	67,6282	14,1052	-5,00235	-4,31365	20,3259	11
25		-6,0551	1,251	31,7719	29,952	44,7669	14,1067	-5,00385	-4,31196	19,7068	12
25		-10,0758	1,251	10,8301	10,0068	134,401	14,0866	-10,0021	-9,10851	20,0258	13
25		-8,40416	1,251	21,6214	19,9832	66,1132	14,0912	-10,0048	-9,11428	20,1194	14
25		-6,85842	1,251	32,3464	29,9724	43,9414	14,0963	-10,0013	-9,13984	20,3592	15
26	43-0669	-7,97696	1,251	10,214	9,99532	141,071	14,0561	10,0014	10,3249	19,5139	1
26		-6,16497	1,251	20,4192	19,9764	69,6205	14,0615	9,99863	10,3263	19,8849	2
26		-4,55085	1,251	30,6958	30,0189	46,117	14,0668	10,0001	10,3334	20,2615	3
26		-8,35243	1,251	10,3576	10,0043	139,357	14,0859	5,00096	5,49916	20,0751	4
26		-6,5281	1,251	20,6492	19,9552	68,9562	14,0864	5,00147	5,4927	19,7382	5
26		-4,74302	1,251	31,1134	30,0447	45,571	14,0911	5,00088	5,50312	19,7594	6
26		-8,68625	1,251	10,3522	9,96924	139,066	14,049	0,00395	0,52325	20,2792	7
26		-6,78188	1,251	20,7037	19,9267	68,567	14,0443	0,00143	0,52806	19,6515	8
26		-5,11353	1,251	31,1179	29,9838	45,4224	14,0473	0,00168	0,51283	20,2227	9
26		-9,16915	1,251	10,6259	10,0174	137,201	14,1104	-4,98291	-4,2911	20,0468	10
26		-7,23556	1,251	21,1581	19,9516	67,6282	14,1052	-5,00235	-4,31365	20,3259	11
26		-5,50197	1,251	31,7719	29,952	44,7669	14,1067	-5,00385	-4,31196	19,7068	12
26		-9,74052	1,251	10,8301	10,0068	134,4	14,0867	-10,0018	-9,10738	20,0274	13
26		-7,97395	1,251	21,6214	19,9832	66,1132	14,0912	-10,0048	-9,11428	20,1194	14
26		-6,34825	1,251	32,3402	29,9664	43,95	14,0963	-10,002	-9,1404	20,3592	15
27	43-0764	-7,20641	1,251	10,214	9,99532	141,071	14,0561	10,0014	10,3249	19,5139	1
27		-5,55644	1,251	20,4192	19,9764	69,6205	14,0615	9,99863	10,3263	19,8849	2
27		-4,10036	1,251	30,6958	30,0189	46,1153	14,0668	10,0015	10,3331	20,262	3
27		-7,54513	1,251	10,3577	10,0045	139,355	14,0858	5,00096	5,49946	20,0785	4
27		-5,89174	1,251	20,6492	19,9552	68,9562	14,0864	5,0027	5,4927	19,7382	5
27		-4,29928	1,251	31,1134	30,0447	45,571	14,0911	5,00088	5,50312	19,7594	6
27		-7,89861	1,251	10,3522	9,96924	139,066	14,049	0,00395	0,52325	20,2792	7
27		-6,1776	1,251	20,7751	19,9907	68,5729	14,0444	-0,00074	0,5289	19,6506	8
27		-4,68058	1,251	31,1179	29,9838	45,4224	14,0473	0,00168	0,51283	20,2227	9
27		-8,31873	1,251	10,6259	10,0174	137,201	14,1104	-4,98291	-4,2911	20,0468	10
27		-6,57173	1,251	21,1579	19,9509	67,6287	14,1052	-5,00277	-4,31383	20,3255	11
27		-5,01436	1,251	31,7739	29,9653	44,7639	14,1067	-4,99921	-4,31176	19,7007	12
27		-8,85527	1,251	10,8303	10,0063	134,4	14,0867	-10,0018	-9,10738	20,0274	13
27		-7,25835	1,251	21,6272	19,9882	66,0953	14,0912	-10,0052	-9,11446	20,1207	14
27		-5,79795	1,251	32,3402	29,9664	43,95	14,0963	-10,0026	-9,1404	20,3592	15
28	43-0704	-9,04039	1,251	10,2142	9,99539	141,07	14,0562	10,0018	10,3254	19,5129	1
28		-7,32099	1,251	20,4244	19,9818	69,6025	14,0615	9,99918	10,3266	19,8845	2
28		-5,79765	1,251	30,6969	30,0232	46,1153	14,0668	10,0015	10,3331	20,262	3
28		-9,43175	1,251	10,3577	10,0045	139,352	14,086	5,00132	5,49973	20,0811	4
28		-7,70563	1,251	20,6499	19,9587	68,9543	14,0864	5,0027	5,49179	19,738	5
28		-6,00915	1,251	31,1221	30,0481	45,5582	14,0911	4,99854	5,50308	19,7587	6
28		-9,7507	1,251	10,3523	9,96857	139,066	14,049	0,00334	0,5236	20,2791	7
28		-8,00193	1,251	20,7751	19,9907	68,5729	14,0444	-0,00074	0,5289	19,6506	8
28		-6,44795	1,251	31,1151	29,9793	45,4266	14,0473	0,00128	0,51323	20,2208	9
28		-10,2404	1,251	10,6256	10,0148	137,205	14,1105	-4,9842	-4,2897	20,0435	10
28		-8,47275	1,251	21,1581	19,9508	67,6282	14,1052	-5,00225	-4,31308	20,3262	11
28		-6,86272	1,251	31,7739	29,9653	44,7639	14,1067	-4,99921	-4,31176	19,7007	12
28		-10,8093	1,251	10,8303	10,0063	134,399	14,0867	-10,0024	-9,10637	20,029	13
28		-9,20903	1,251	21,6272	19,9882	66,0953	14,0912	-10,0052	-9,11446	20,1207	14
28		-7,70985	1,251	32,3346	29,9608	43,9578	14,0963	-10,0026	-9,14091	20,3592	15
29	43-0750	-7,5546	1,251	10,2142	9,99539	141,07	14,0562	10,0018	10,3254	19,5129	1
29		-5,78115	1,251	20,4244	19,9818	69,6025	14,0615	9,99918	10,3266	19,8845	2
29		-4,20688	1,251	30,6969	30,0232	46,1135	14,0668	10,0018	10,332	20,2616	3
29		-7,9711	1,251	10,3579	10,0048	139,352	14,086	5,00132	5,49973	20,0811	4
29		-6,18742	1,251	20,6499	19,9587	68,9543	14,0864	5,00382	5,49179	19,738	5
29		-4,45345	1,251	31,1221	30,0481	45,5582	14,0911	4,99854	5,50308	19,7587	6
29		-8,4394	1,251	10,3523	9,96857	139,066	14,049	0,00334	0,5236	20,2791	7
29		-6,58792	1,251	20,7731	19,9842	68,5799	14,0445	-0,00363	0,52875	19,6514	8
29		-4,95977	1,251	31,1151	29,9793	45,4266	14,0473	0,00128	0,51323	20,2208	9
29		-8,88549	1,251	10,6253	10,0125	137,21	14,1105	-4,98627	-4,28934	20,0391	10
29		-7,01374	1,251	21,1581	19,9508	67,6282	14,1052	-5,00225	-4,31308	20,3262	11

Sensor Pos	S/N	Bridge Output (mV)	Vref (excitation)	%RH@Pc	Chamber %RH @ PcTc	Satur PSI	Chmbr PSI	Satur T	Chmbr T	Flow l/m	Reading #
29		-5,32572	1,251	31,7739	29,9653	44,7639	14,1067	-4,99921	-4,31176	19,7007	12
29		-9,49335	1,251	10,8304	10,0049	134,399	14,0867	-10,0024	-9,10637	20,029	13
29		-7,78732	1,251	21,6331	19,9934	66,0769	14,0912	-10,0055	-9,11462	20,1207	14
29		-6,20996	1,251	32,3346	29,9608	43,9578	14,0963	-10,0026	-9,14091	20,3592	15
30	43-0751	-4,62834	1,251	10,2144	9,99545	141,069	14,0563	10,0021	10,3259	19,5138	1
30		-2,9808	1,251	20,4298	19,9885	69,5839	14,0615	10,0006	10,327	19,8841	2
30		-1,52444	1,251	30,698	30,0274	46,1135	14,0668	10,0018	10,332	20,2616	3
30		-4,95969	1,251	10,3579	10,0048	139,352	14,086	4,99983	5,49973	20,0811	4
30		-3,30676	1,251	20,6506	19,961	68,9521	14,0865	5,00382	5,49187	19,7377	5
30		-1,70659	1,251	31,1294	30,0491	45,5474	14,0911	4,99642	5,50396	19,7574	6
30		-5,25286	1,251	10,3523	9,9679	139,065	14,0491	0,00279	0,52392	20,2786	7
30		-3,53044	1,251	20,7731	19,9842	68,5799	14,0445	-0,00363	0,52875	19,6514	8
30		-2,02976	1,251	31,1124	29,9794	45,4306	14,0473	0,00273	0,51358	20,2205	9
30		-5,71135	1,251	10,6253	10,0125	137,21	14,1105	-4,98627	-4,28934	20,0391	10
30		-3,95977	1,251	21,1581	19,9508	67,6282	14,1052	-5,00225	-4,31308	20,3262	11
30		-2,39876	1,251	31,7751	29,9678	44,7622	14,1067	-4,9981	-4,3112	19,6975	12
30		-6,23148	1,251	10,8304	10,0049	134,397	14,0867	-10,003	-9,10547	20,0304	13
30		-4,63266	1,251	21,6331	19,9934	66,0769	14,0912	-10,0055	-9,11462	20,1207	14
30		-3,16544	1,251	32,3296	29,9559	43,9646	14,0963	-10,0031	-9,14138	20,3603	15
31	43-0651	-8,8939	1,251	10,2144	9,99538	141,067	14,0562	10,0023	10,3263	19,5144	1
31		-7,10007	1,251	20,4298	19,9885	69,5839	14,0615	10,0006	10,327	19,8841	2
31		-5,52323	1,251	30,698	30,0274	46,1135	14,0668	10,0013	10,332	20,2616	3
31		-9,27142	1,251	10,3581	10,0037	139,35	14,0859	4,99983	5,49998	20,0832	4
31		-7,46824	1,251	20,6506	19,961	68,9495	14,0864	5,00393	5,49103	19,738	5
31		-5,73445	1,251	31,1294	30,0491	45,5474	14,0911	4,99642	5,50396	19,7574	6
31		-9,62783	1,251	10,3523	9,9679	139,065	14,0491	0,00229	0,52331	20,2786	7
31		-7,74825	1,251	20,7707	19,9793	68,5884	14,0446	-0,00535	0,52861	19,6519	8
31		-6,11678	1,251	31,1099	29,9796	45,4342	14,0473	0,00405	0,51391	20,2185	9
31		-10,0599	1,251	10,625	10,0103	137,215	14,1106	-4,98815	-4,289	20,0349	10
31		-8,15134	1,251	21,1586	19,9508	67,6265	14,1052	-5,00177	-4,31239	20,3265	11
31		-6,45398	1,251	31,7751	29,9678	44,7622	14,1067	-4,9981	-4,3112	19,6975	12
31		-10,6377	1,251	10,8305	10,0037	134,397	14,0867	-10,003	-9,10547	20,0304	13
31		-8,90057	1,251	21,639	19,9986	66,0585	14,0912	-10,0049	-9,11386	20,12	14
31		-7,30635	1,251	32,3296	29,9559	43,9646	14,0963	-10,0031	-9,14138	20,3603	15
32	43-0630	-6,19705	1,251	10,2144	9,99538	141,067	14,0562	10,0023	10,3263	19,5144	1
32		-4,54884	1,251	20,4351	19,9951	69,5654	14,0615	10,0019	10,3273	19,8836	2
32		-3,0786	1,251	30,6992	30,0275	46,1118	14,0668	10,0013	10,3319	20,2611	3
32		-6,59885	1,251	10,3581	10,0037	139,35	14,0859	4,99757	5,49998	20,0832	4
32		-4,94656	1,251	20,6512	19,9628	68,9495	14,0864	5,00393	5,49103	19,738	5
32		-3,30929	1,251	31,1353	30,049	45,5387	14,0911	4,99449	5,50475	19,7551	6
32		-6,91937	1,251	10,3523	9,96798	139,065	14,0491	0,00229	0,52331	20,2781	7
32		-5,26084	1,251	20,7707	19,9793	68,5884	14,0446	-0,00535	0,52861	19,6519	8
32		-3,76523	1,251	31,1099	29,9796	45,4342	14,0473	0,00405	0,51391	20,2185	9
32		-7,39952	1,251	10,625	10,0103	137,215	14,1106	-4,98815	-4,289	20,0349	10
32		-5,72852	1,251	21,1586	19,9508	67,6265	14,1052	-5,00177	-4,31239	20,3265	11
32		-4,18265	1,251	31,7765	29,968	44,7603	14,1067	-4,99801	-4,31069	19,6945	12
32		-7,97453	1,251	10,8305	10,0037	134,396	14,0868	-10,0036	-9,10467	20,0323	13
32		-6,46306	1,251	21,639	19,9986	66,0585	14,0912	-10,0049	-9,11386	20,12	14
32		-5,03441	1,251	32,325	29,9515	43,9709	14,0963	-10,0036	-9,1418	20,3605	15
33	43-0640	-8,73773	1,251	10,2144	9,99538	141,067	14,0562	10,0023	10,3263	19,5144	1
33		-7,0884	1,251	20,4351	19,9951	69,5654	14,0615	10,0019	10,3273	19,8836	2
33		-5,6213	1,251	30,6992	30,0275	46,1118	14,0668	10,0007	10,3319	20,2611	3
33		-9,09145	1,251	10,3582	10,0027	139,347	14,0858	4,99757	5,4993	20,0845	4
33		-7,43925	1,251	20,6512	19,9628	68,9466	14,0863	5,00312	5,49118	19,7382	5
33		-5,82095	1,251	31,1353	30,049	45,5387	14,0911	4,99449	5,50475	19,7551	6
33		-9,40824	1,251	10,3523	9,96798	139,065	14,0491	0,00184	0,52331	20,2781	7
33		-7,70312	1,251	20,7678	19,9755	68,5978	14,0445	-0,006	0,52848	19,6519	8
33		-6,20605	1,251	31,1081	29,9823	45,437	14,0473	0,00614	0,51419	20,2164	9
33		-9,86396	1,251	10,625	10,0103	137,215	14,1106	-4,98815	-4,289	20,0349	10
33		-8,1334	1,251	21,1594	19,9529	67,6245	14,1054	-5,00043	-4,31177	20,3266	11
33		-6,57635	1,251	31,7765	29,968	44,7603	14,1067	-4,99801	-4,31069	19,6945	12
33		-10,41	1,251	10,8307	10,0026	134,396	14,0868	-10,0036	-9,10467	20,0323	13
33		-8,83519	1,251	21,6449	20,0054	66,0402	14,0912	-10,0043	-9,11407	20,1199	14
33		-7,37807	1,251	32,325	29,9515	43,9709	14,0963	-10,0041	-9,14219	20,3614	15
34	43-0700	-9,06252	1,251	10,2146	9,99485	141,066	14,0563	10,0017	10,3267	19,5114	1
34		-7,24084	1,251	20,4406	20,0004	69,5464	14,0615	10,0021	10,3275	19,8824	2
34		-5,63204	1,251	30,7004	30,0296	46,11	14,0668	10,0007	10,3309	20,2604	3
34		-9,43065	1,251	10,3582	10,0027	139,345	14,0858	4,99551	5,49868	20,0861	4
34		-7,60256	1,251	20,6519	19,9622	68,9466	14,0863	5,00312	5,49118	19,7382	5
34		-5,84104	1,251	31,1398	30,0481	45,532	14,0911	4,99274	5,50548	19,7537	6
34		-9,7551	1,251	10,3524	9,96744	139,064	14,0491	0,00184	0,52366	20,2798	7
34		-7,84691	1,251	20,7678	19,9755	68,5978	14,0445	-0,006	0,52848	19,6519	8
34		-6,18184	1,251	31,1081	29,9823	45,437	14,0473	0,00614	0,51419	20,2164	9
34		-10,2392	1,251	10,6246	10,0074	137,219	14,1105	-4,98987	-4,28779	20,0298	10
34		-8,3021	1,251	21,1594	19,9529	67,6245	14,1054	-5,00043	-4,31177	20,3266	11
34		-6,57449	1,251	31,778	29,9685	44,7582	14,1067	-4,99882	-4,31113	19,6922	12
34		-10,81	1,251	10,8307	10,0026	134,396	14,0868	-10,0036	-9,10467	20,0323	13
34		-9,04157	1,251	21,6449	20,0054	66,0402	14,0912	-10,0043	-9,11407	20,1199	14
34		-7,41596	1,251	32,321	29,9475	43,9764	14,0963	-10,0041	-9,14219	20,3614	15
35	43-0761	-8,69191	1,251	10,2146	9,99485	141,066	14,0563	10,0017	10,3267	19,5114	1
35		-6,87982	1,251	20,4406	20,0004	69,5464	14,0615	10,0021	10,3275	19,8824	2
35		-5,2808	1,251	30,7016	30,0315	46,1082	14,0668	10,0002	10,33	20,2606	3
35		-9,04038	1,251	10,3583	10,0018	139,345	14,0858	4,99551	5,49868	20,0861	4
35		-7,21688	1,251	20,6519	19,9622	68,9435	14,0862	5,00239	5,49131	19,7376	5
35		-5,4609	1,251	31,1398	30,0481	45,5269	14,0911	4,99206	5,50523	19,7518	6

Sensor Pos	S/N	Bridge Output (mV)	Vref (excitation)	%RH@Pc	Chamber %RH @ PcTc	Satur PSI	Chmbr PSI	Satur T	Chmbr T	Flow l/m	Reading #
35		-9,31661	1,251	10,3524	9,96744	139,064	14,0491	0,00184	0,52366	20,2798	7
35		-7,41625	1,251	20,765	19,9736	68,6074	14,0445	-0,00569	0,52837	19,6518	8
35		-5,7651	1,251	31,1081	29,9823	45,437	14,0473	0,00614	0,51419	20,2164	9
35		-9,80203	1,251	10,6246	10,0074	137,219	14,1105	-4,99142	-4,28669	20,0245	10
35		-7,86675	1,251	21,1603	19,9533	67,6216	14,1054	-5,00012	-4,31121	20,3266	11
35		-6,14981	1,251	31,778	29,9685	44,7582	14,1067	-4,99882	-4,31113	19,6922	12
35		-10,3553	1,251	10,8308	10,0017	134,395	14,0868	-10,0041	-9,10394	20,034	13
35		-8,58489	1,251	21,6506	20,0134	66,0224	14,0912	-10,0038	-9,11517	20,1205	14
35		-6,96886	1,251	32,321	29,9475	43,9764	14,0963	-10,0041	-9,14219	20,3614	15
37	43-0601	-7,018	1,251	10,2148	9,99444	141,063	14,0564	10,0011	10,327	19,512	1
37		-5,298	1,251	20,4459	20,0056	69,5281	14,0614	10,0024	10,3278	19,8819	2
37		-3,76605	1,251	30,7016	30,0315	46,1082	14,0668	10,0002	10,33	20,2606	3
37		-7,36785	1,251	10,3583	10,0018	139,345	14,0858	4,99551	5,49868	20,0861	4
37		-5,64071	1,251	20,6527	19,9617	68,9435	14,0862	5,00239	5,49131	19,7376	5
37		-3,94104	1,251	31,1433	30,0507	45,5269	14,0911	4,99206	5,50523	19,7518	6
37		-7,66784	1,251	10,3525	9,96691	139,063	14,0491	0,00016	0,52398	20,2791	7
37		-5,89583	1,251	20,762	19,9728	68,6177	14,0446	-0,0045	0,52827	19,6518	8
37		-4,32113	1,251	31,1067	29,9831	45,4389	14,0473	0,00714	0,51445	20,2148	9
37		-8,11872	1,251	10,6243	10,0049	137,223	14,1105	-4,99374	-4,28669	20,0245	10
37		-6,32686	1,251	21,1615	19,9541	67,6184	14,1055	-4,99983	-4,31069	20,3276	11
37		-4,69051	1,251	31,7816	29,9635	44,7531	14,1067	-5,00114	-4,31016	19,6844	12
37		-8,652	1,251	10,8308	9,99992	134,394	14,0869	-10,0046	-9,10237	20,0353	13
37		-7,02439	1,251	21,6562	20,0212	66,0052	14,0912	-10,0043	-9,11707	20,1215	14
37		-5,50362	1,251	32,3177	29,9419	43,981	14,0963	-10,0085	-9,14254	20,3622	15
38	43-0587	-9,75175	1,251	10,2148	9,99444	141,063	14,0564	9,99957	10,327	19,512	1
38		-8,02277	1,251	20,4459	20,0056	69,5281	14,0614	10,0024	10,3278	19,8819	2
38		-6,48508	1,251	30,7016	30,0315	46,1062	14,0668	9,99981	10,3301	20,2582	3
38		-10,1184	1,251	10,3584	10,001	139,343	14,0857	4,99365	5,49812	20,0885	4
38		-8,38691	1,251	20,6527	19,9617	68,9435	14,0862	5,00082	5,49131	19,7376	5
38		-6,68856	1,251	31,1433	30,0507	45,5269	14,0911	4,99206	5,50523	19,7518	6
38		-10,4441	1,251	10,3524	9,96624	139,063	14,049	0,00016	0,52336	20,2791	7
38		-8,62265	1,251	20,7592	19,9735	68,6277	14,0447	-0,00251	0,52818	19,651	8
38		-7,02978	1,251	31,1058	29,9837	45,4403	14,0473	0,00805	0,51468	20,2134	9
38		-10,9106	1,251	10,624	10,0025	137,228	14,1106	-4,99374	-4,2866	20,0188	10
38		-9,06196	1,251	21,1615	19,9541	67,6184	14,1055	-4,99983	-4,31069	20,3276	11
38		-7,4075	1,251	31,7816	29,9635	44,7531	14,1067	-5,00114	-4,31016	19,6844	12
38		-11,4868	1,251	10,8308	9,99992	134,394	14,0869	-10,0046	-9,10237	20,0353	13
38		-9,80006	1,251	21,6562	20,0212	66,0052	14,0912	-10,0043	-9,11707	20,1215	14
38		-8,24765	1,251	32,3147	29,9295	43,9851	14,0963	-10,0085	-9,14195	20,3629	15
39	43-0697	-6,12997	1,251	10,2149	9,99333	141,063	14,0565	9,99957	10,3273	19,5144	1
39		-4,42491	1,251	20,4512	20,0107	69,5097	14,0614	10,0026	10,328	19,8817	2
39		-2,92177	1,251	30,7029	30,0318	46,1062	14,0668	9,99981	10,3301	20,2582	3
39		-6,42342	1,251	10,3584	10,001	139,343	14,0857	4,99365	5,49812	20,0885	4
39		-4,71761	1,251	20,6538	19,9605	68,94	14,0863	5,00082	5,49144	19,7386	5
39		-3,08456	1,251	31,1449	30,0532	45,5245	14,0911	4,99325	5,50592	19,75	6
39		-6,69465	1,251	10,3524	9,96624	139,063	14,049	0,00016	0,52336	20,2791	7
39		-4,90574	1,251	20,7592	19,9735	68,6277	14,0447	-0,00251	0,52818	19,651	8
39		-3,3488	1,251	31,1058	29,9837	45,4403	14,0473	0,00805	0,51468	20,2134	9
39		-7,0829	1,251	10,624	10,0025	137,228	14,1106	-4,99374	-4,2866	20,0188	10
39		-5,264	1,251	21,1625	19,9547	67,615	14,1055	-4,99957	-4,31022	20,3276	11
39		-3,64635	1,251	31,7816	29,9635	44,7531	14,1067	-5,00114	-4,31016	19,6844	12
39		-7,58814	1,251	10,8308	9,99746	134,395	14,0869	-10,0068	-9,10186	20,0359	13
39		-5,92184	1,251	21,6618	20,0271	65,9879	14,0912	-10,0047	-9,11789	20,1206	14
39		-4,39989	1,251	32,3147	29,9295	43,9851	14,0963	-10,0085	-9,14195	20,3629	15
40	43-0611	-5,25861	1,251	10,2149	9,99333	141,063	14,0565	9,99914	10,3276	19,5144	1
40		-3,55688	1,251	20,4512	20,0107	69,5097	14,0614	10,0026	10,328	19,8817	2
40		-2,05765	1,251	30,7029	30,0318	46,1042	14,0668	9,99942	10,3293	20,2554	3
40		-5,63018	1,251	10,3585	10,0009	139,342	14,0857	4,99286	5,49762	20,0903	4
40		-3,91925	1,251	20,6538	19,9605	68,9369	14,0862	5,0003	5,49155	19,7379	5
40		-2,28625	1,251	31,1449	30,0532	45,5245	14,0911	4,99325	5,50592	19,75	6
40		-5,9982	1,251	10,4363	10,0457	139,062	14,0488	-0,00191	0,5228	20,2795	7
40		-4,30975	1,251	20,7592	19,9735	68,6277	14,0447	-0,00251	0,52818	19,651	8
40		-2,79308	1,251	31,1053	29,9849	45,4411	14,0473	0,00887	0,5149	20,2123	9
40		-6,41335	1,251	10,6236	10,001	137,232	14,1104	-4,99585	-4,28742	20,0138	10
40		-4,71675	1,251	21,1638	19,9555	67,6108	14,1055	-4,99933	-4,30979	20,3287	11
40		-3,14849	1,251	31,7835	29,9605	44,7503	14,1067	-5,00348	-4,31065	19,6809	12
40		-6,9871	1,251	10,8308	9,99746	134,395	14,0869	-10,0107	-9,10186	20,0359	13
40		-5,45673	1,251	21,6672	20,0311	65,9711	14,0912	-10,006	-9,11864	20,1204	14
40		-4,00347	1,251	32,3125	29,9188	43,9882	14,0963	-10,0112	-9,14141	20,3629	15
41	43-0754	-4,14198	1,251	10,215	9,99301	141,061	14,0566	9,99914	10,3276	19,5134	1
41		-2,36899	1,251	20,4565	20,0147	69,4915	14,0614	10,0019	10,3282	19,8821	2
41		-0,80264	1,251	30,7042	30,034	46,1042	14,0668	9,99942	10,3293	20,2554	3
41		-4,50044	1,251	10,3585	10,0009	139,342	14,0857	4,99286	5,49762	20,0903	4
41		-2,71865	1,251	20,6546	19,9603	68,9369	14,0862	5,0003	5,49155	19,7379	5
41		-1,0061	1,251	31,1448	30,056	45,5247	14,0911	4,99524	5,50654	19,7479	6
41		-4,86598	1,251	10,4363	10,0457	139,062	14,0488	-0,00379	0,5228	20,2795	7
41		-3,04544	1,251	20,6837	19,9054	68,6362	14,0447	0,0002	0,5281	19,6516	8
41		-1,43162	1,251	31,1053	29,9849	45,4411	14,0473	0,00887	0,5149	20,2123	9
41		-5,29164	1,251	10,6236	10,001	137,232	14,1104	-4,99585	-4,28742	20,0138	10
41		-3,45425	1,251	21,1638	19,9555	67,6108	14,1055	-4,99933	-4,30979	20,3287	11
41		-1,78161	1,251	31,7835	29,9605	44,7503	14,1067	-5,00651	-4,31065	19,6809	12
41		-5,83059	1,251	10,8307	9,99435	134,396	14,0869	-10,0107	-9,10231	20,0341	13
41		-4,16418	1,251	21,6672	20,0311	65,9711	14,0912	-10,006	-9,11864	20,1204	14
41		-2,60248	1,251	32,3125	29,9188	43,9882	14,0963	-10,0128	-9,14141	20,3629	15
42	43-0698	-4,24096	1,251	10,215	9,99301	141,061	14,0566	9,99965	10,3276	19,5134	1

Sensor Pos	S/N	Bridge Output (mV)	Vref (excitation)	%RH@Pc	Chamber %RH @ PcTc	Satur PSI	Chmbr PSI	Satur T	Chmbr T	Flow l/m	Reading #
42		-2,5628	1,251	20,4619	20,0189	69,4727	14,0614	10,0013	10,3284	19,8821	2
42		-1,07687	1,251	30,7042	30,034	46,1042	14,0668	9,99997	10,3293	20,2554	3
42		-4,55728	1,251	10,3586	10,0021	139,34	14,0856	4,99305	5,49625	20,0921	4
42		-2,87766	1,251	20,6546	19,9603	68,9369	14,0862	4,99983	5,49155	19,7379	5
42		-1,25826	1,251	31,1448	30,056	45,5247	14,0911	4,99524	5,50654	19,7479	6
42		-4,848	1,251	10,4363	10,0445	139,061	14,0487	-0,00379	0,5223	20,2798	7
42		-3,07955	1,251	20,6815	19,9047	68,6439	14,0448	0,00177	0,52893	19,6523	8
42		-1,53669	1,251	31,1052	29,9862	45,4412	14,0473	0,0096	0,51508	20,213	9
42		-5,24442	1,251	10,6232	9,99963	137,237	14,1103	-4,99777	-4,28816	20,0095	10
42		-3,44581	1,251	21,1638	19,9555	67,6108	14,1055	-4,99933	-4,30979	20,3287	11
42		-1,84698	1,251	31,7855	29,9558	44,7475	14,1067	-5,00651	-4,31109	19,6775	12
42		-5,74944	1,251	10,8307	9,99435	134,396	14,0869	-10,0132	-9,10231	20,0341	13
42		-4,10558	1,251	21,6672	20,0311	65,9711	14,0912	-10,006	-9,11864	20,1204	14
42		-2,59874	1,251	32,3107	29,9116	43,9907	14,0963	-10,0128	-9,14092	20,3628	15
43	43-0642	-5,30325	1,251	10,2152	9,99335	141,06	14,0566	9,99965	10,3278	19,5142	1
43		-3,7932	1,251	20,4619	20,0189	69,4727	14,0614	10,0013	10,3284	19,8821	2
43		-2,46463	1,251	30,7056	30,0362	46,1021	14,0668	9,99997	10,3294	20,2526	3
43		-5,63358	1,251	10,3586	10,0021	139,34	14,0856	4,99413	5,49592	20,0921	4
43		-4,1159	1,251	20,6558	19,9606	68,9335	14,0863	4,99983	5,49166	19,7375	5
43		-2,65612	1,251	31,1432	30,059	45,527	14,0911	4,99704	5,50618	19,7458	6
43		-5,90737	1,251	10,4363	10,0442	139,06	14,0486	-0,00459	0,52184	20,2804	7
43		-4,31	1,251	20,6815	19,9047	68,6439	14,0448	0,00177	0,52893	19,6523	8
43		-2,92228	1,251	31,1061	29,9861	45,4399	14,0473	0,00937	0,51524	20,2134	9
43		-6,33195	1,251	10,6232	9,99963	137,237	14,1103	-4,99951	-4,28816	20,0095	10
43		-4,7013	1,251	21,1651	19,9549	67,6064	14,1054	-5,00002	-4,3094	20,3286	11
43		-3,25425	1,251	31,7855	29,9558	44,7475	14,1067	-5,01017	-4,31149	19,6775	12
43		-6,82417	1,251	10,8306	9,99153	134,398	14,0869	-10,0132	-9,1018	20,0316	13
43		-5,33226	1,251	21,6726	20,0337	65,9541	14,0912	-10,0089	-9,12022	20,1202	14
43		-3,96895	1,251	32,3107	29,9116	43,9907	14,0963	-10,0128	-9,14092	20,3628	15

Appendix B: Control Board Schematics

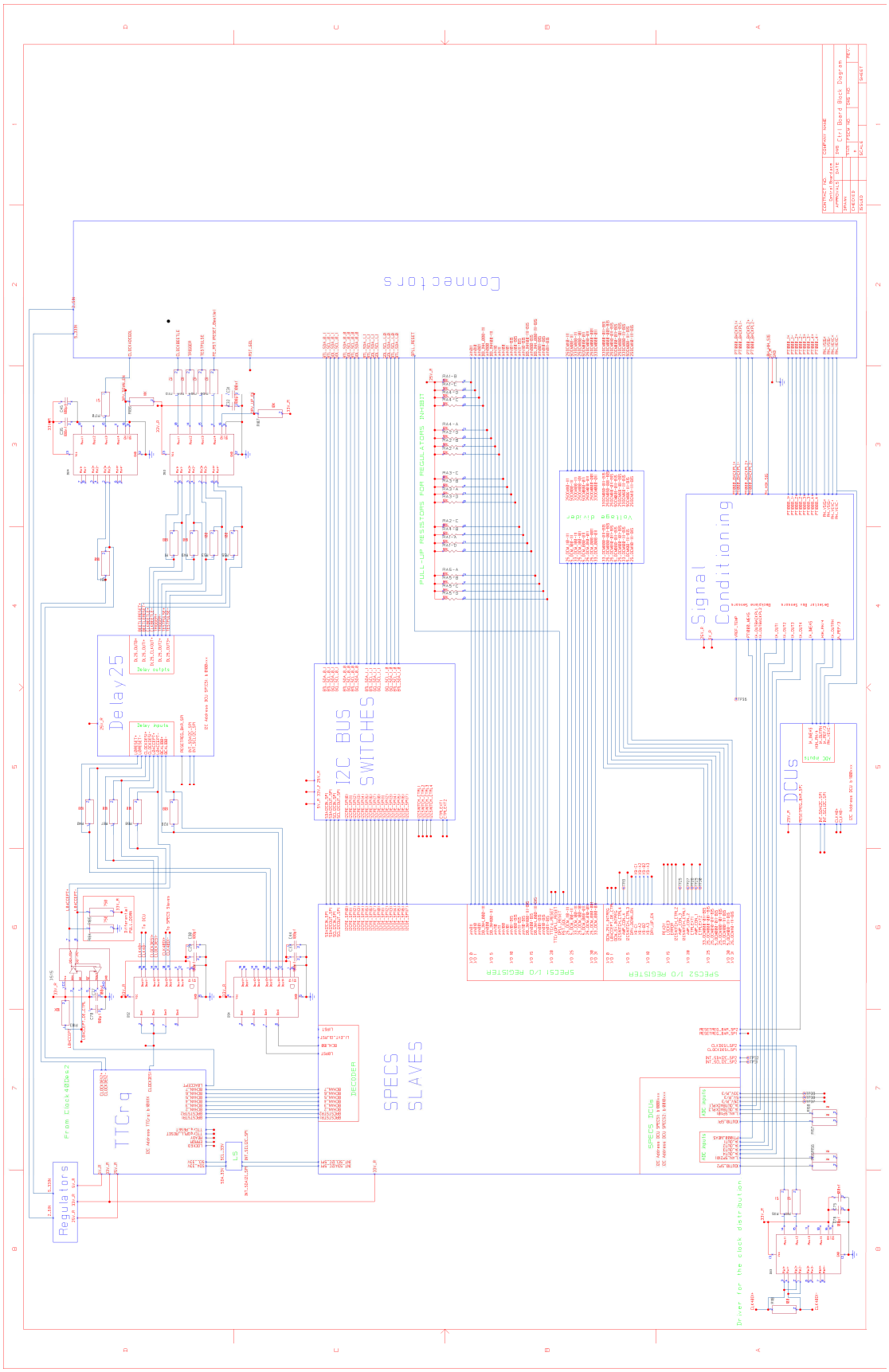


Image 1 : Control Board block diagram

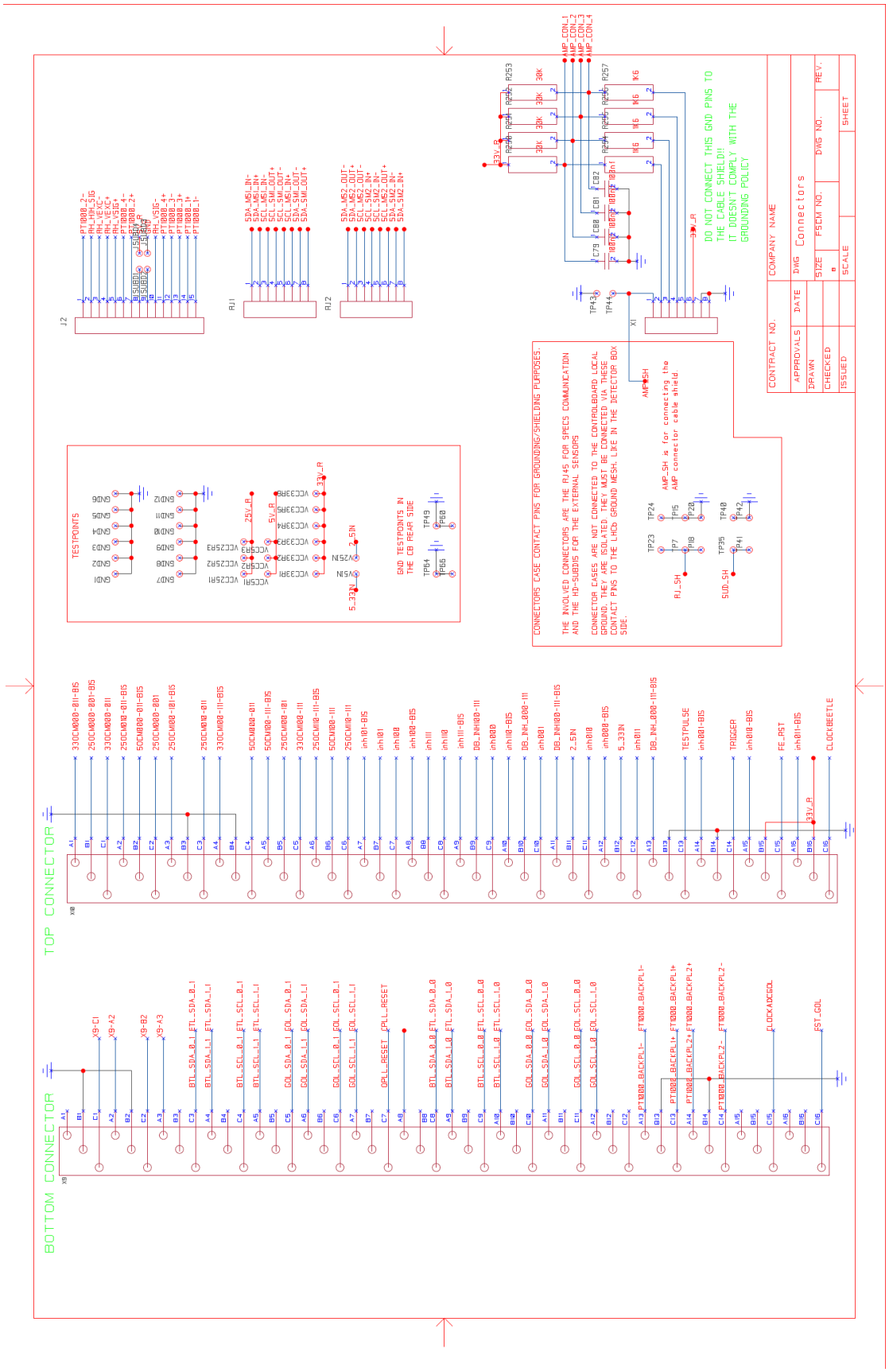


Image 2: Connectors

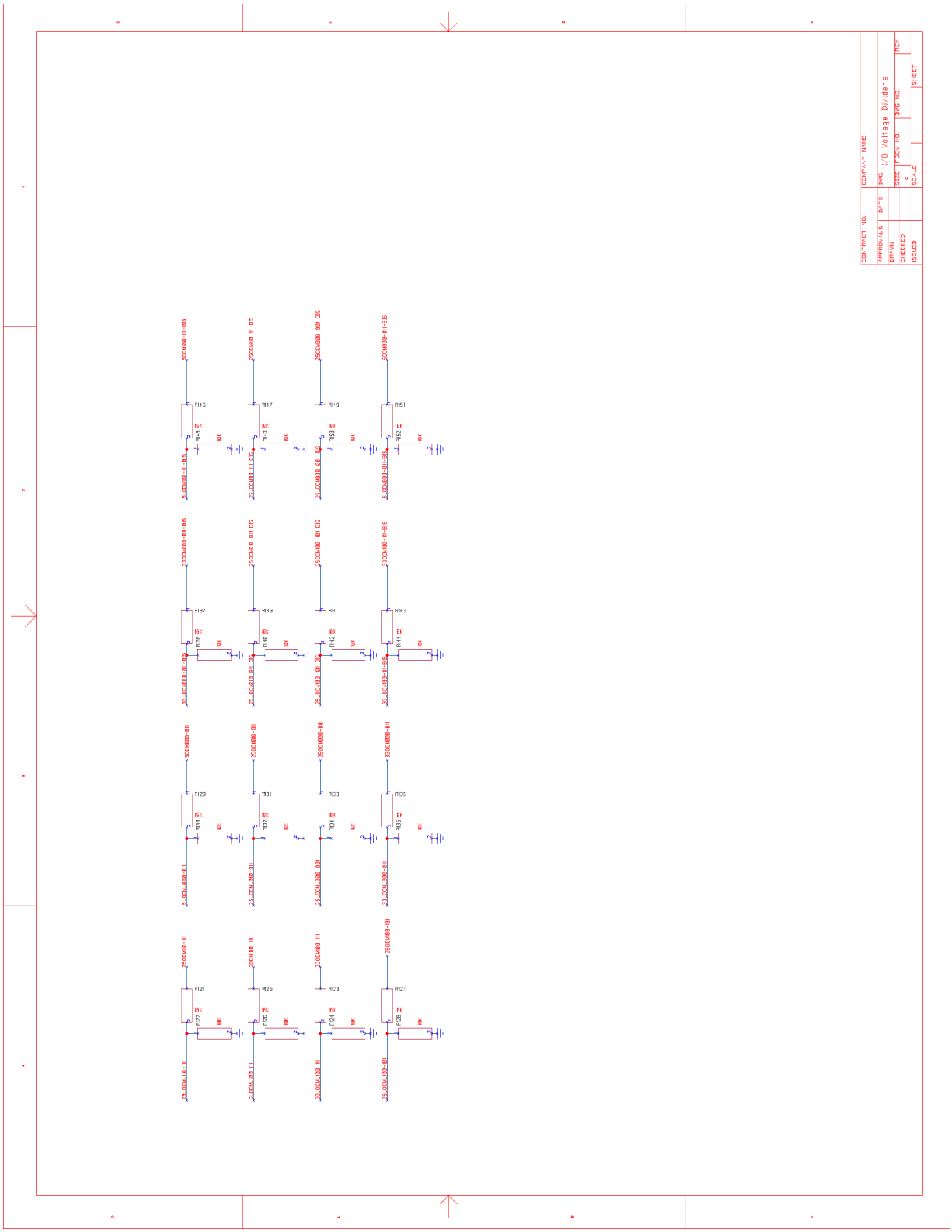


Image 3: I/O voltage dividers

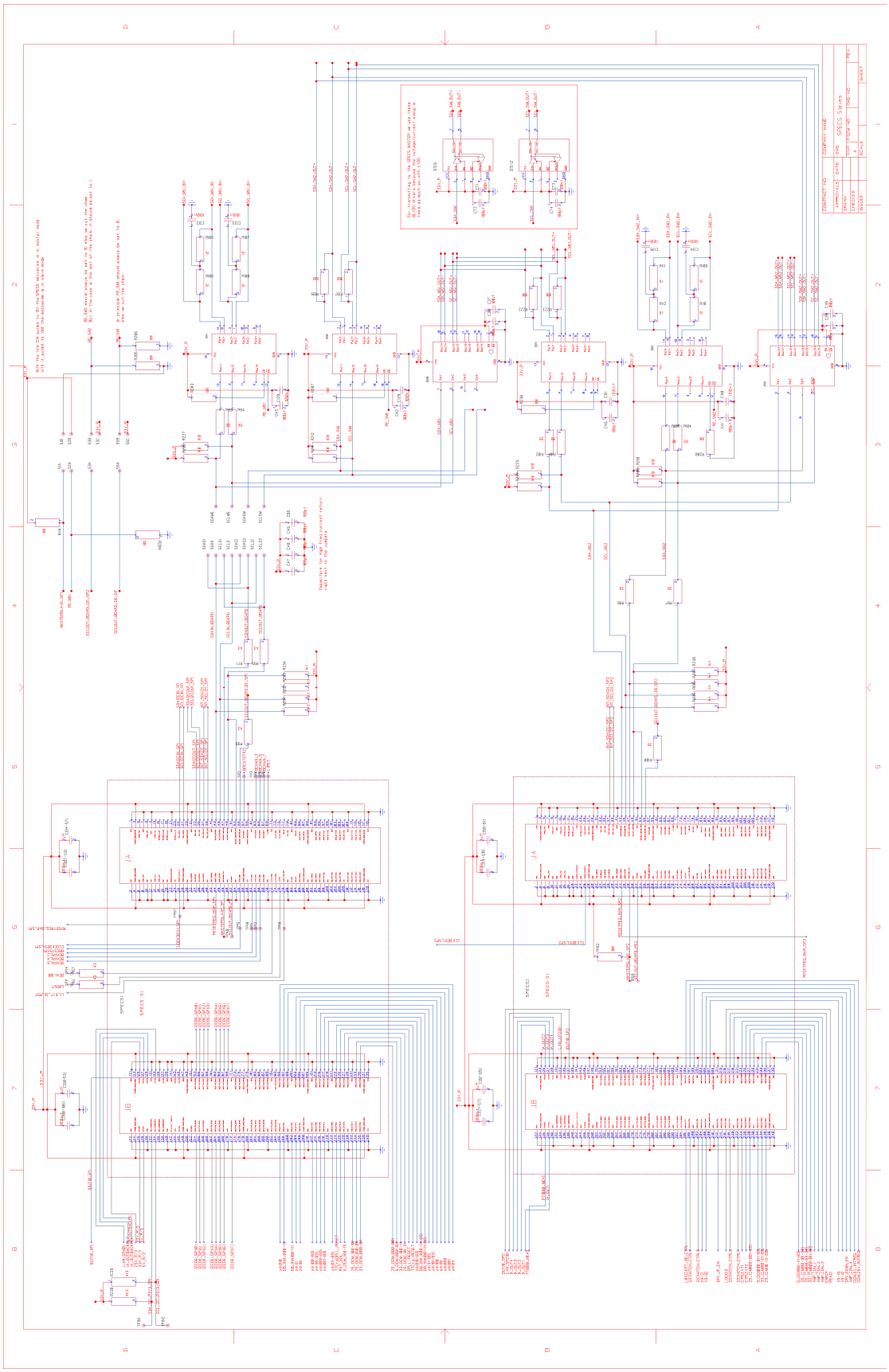


Image 4: Specs slaves + SPECS bus chaining

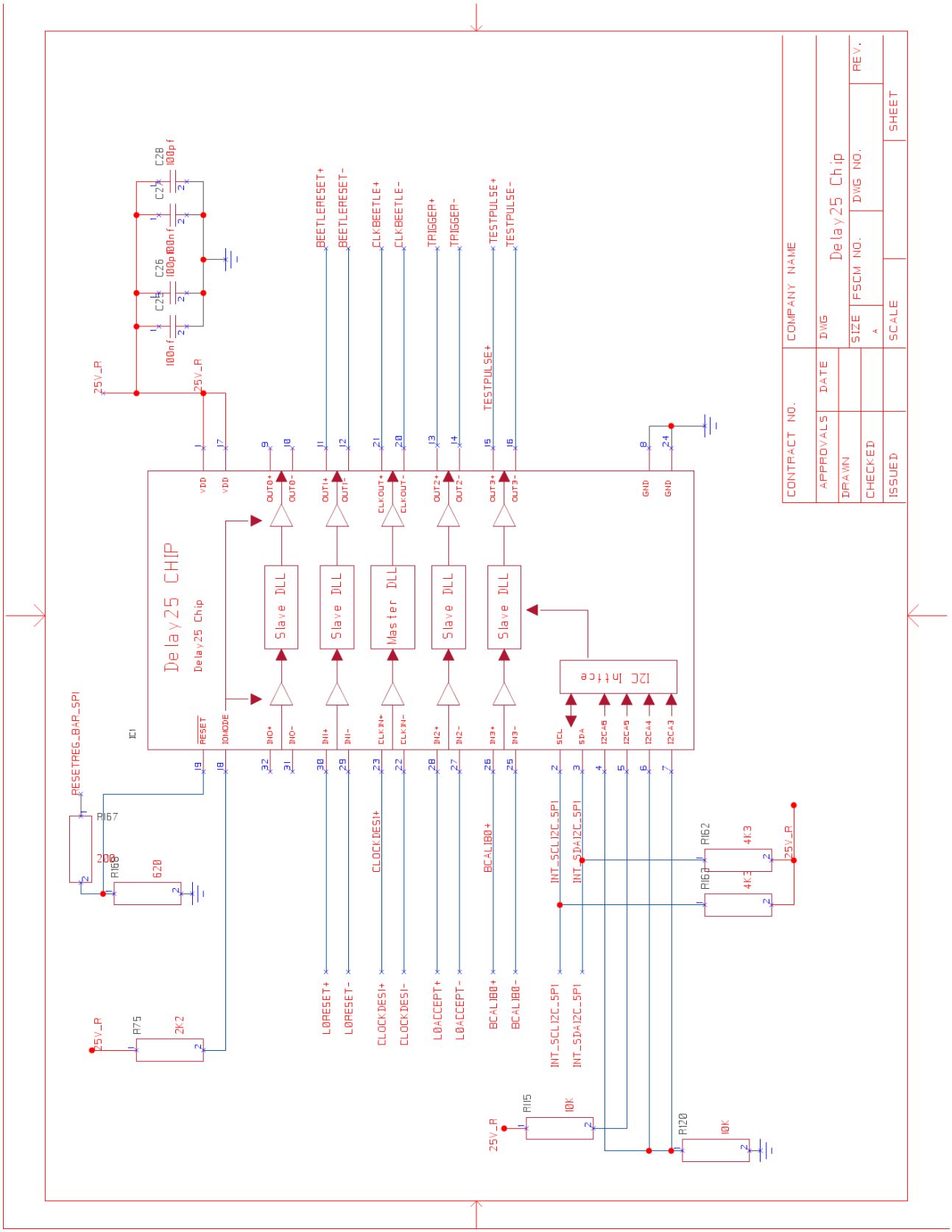


Image 5: Delay25 chip

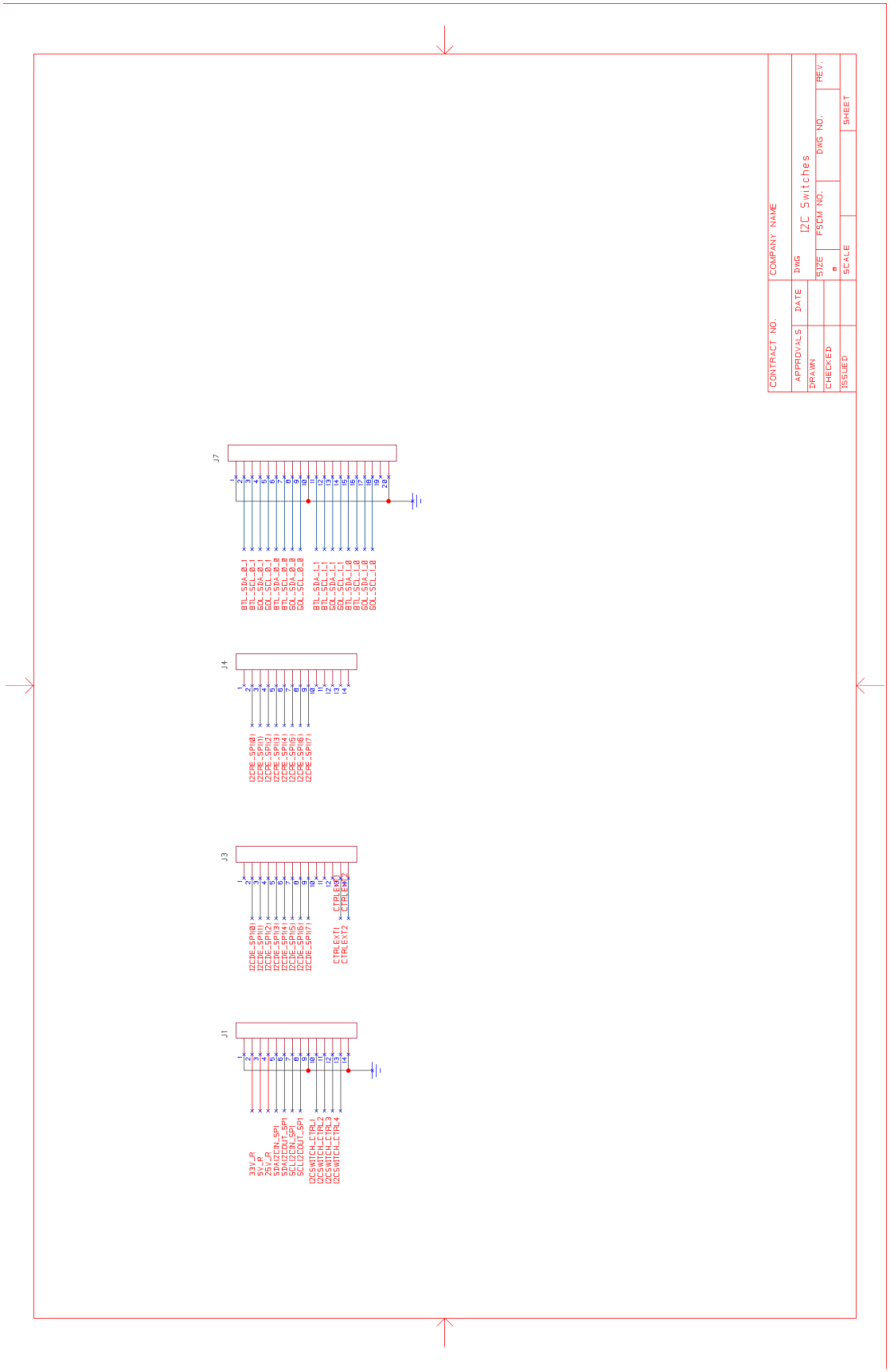


Image 6: I2C mezzanine connectors interfacing

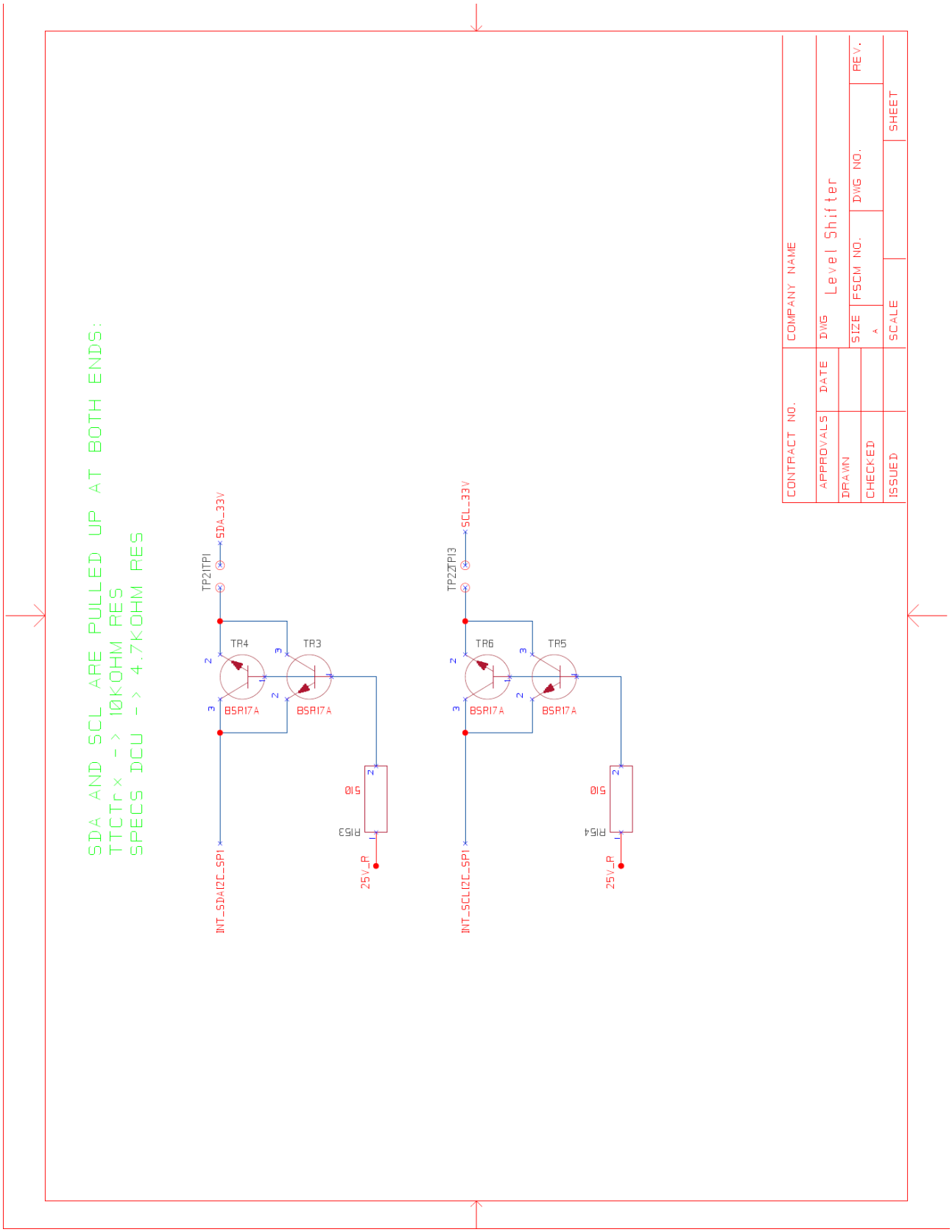


Image 7: Level shifter

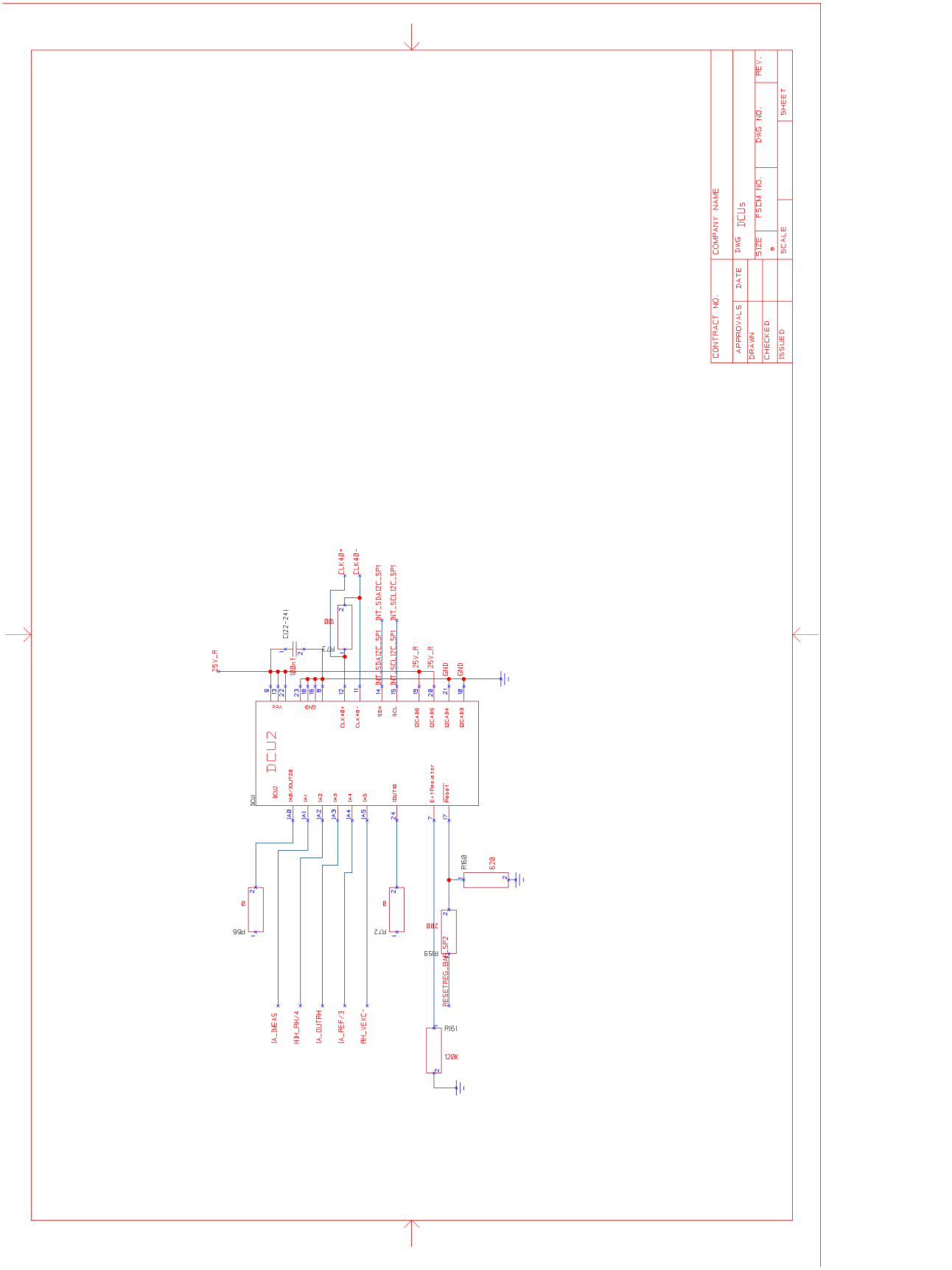

COMPANY NAME
DWG DCUs
SIZE B
FSCM NO.
DWG NO.
REV.
SHEET
SCALE
CONTRACT NO.
DATE
APPROVALS
DRAWN
CHECKED
ISSUED
DCU2
CLK40+
CLK40-
INT_SDA12C_SP1
INT_SCL12C_SP1
25V_R
GND
C122-241
R160
620
R161
120K
RESETREG_BAR_SP2
A_IMEAS
HYH_PHY4
A_OUTPH
A_REF/3
PH_VEXC-

Image 8: DCU2

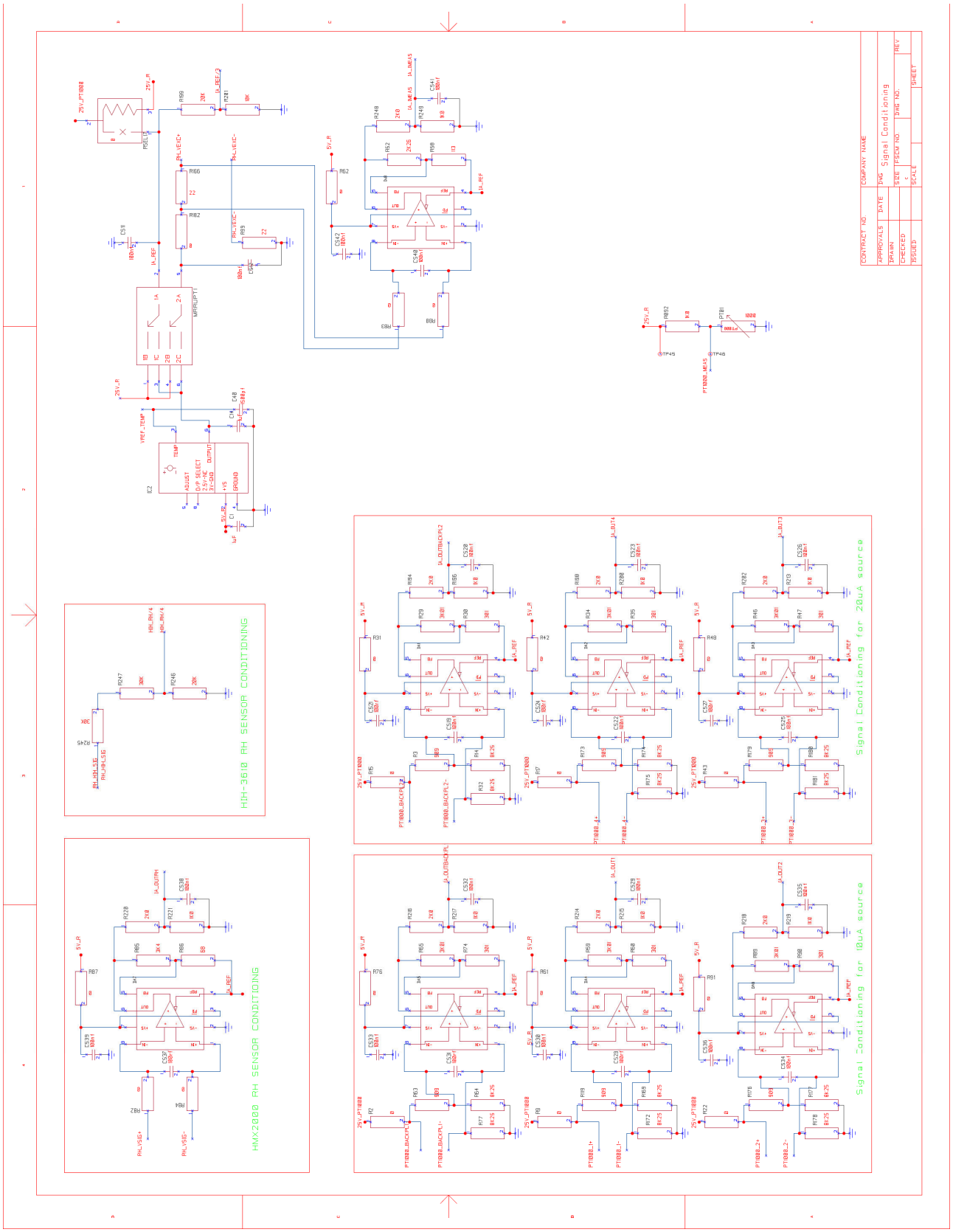


Image 9: Signal conditioning

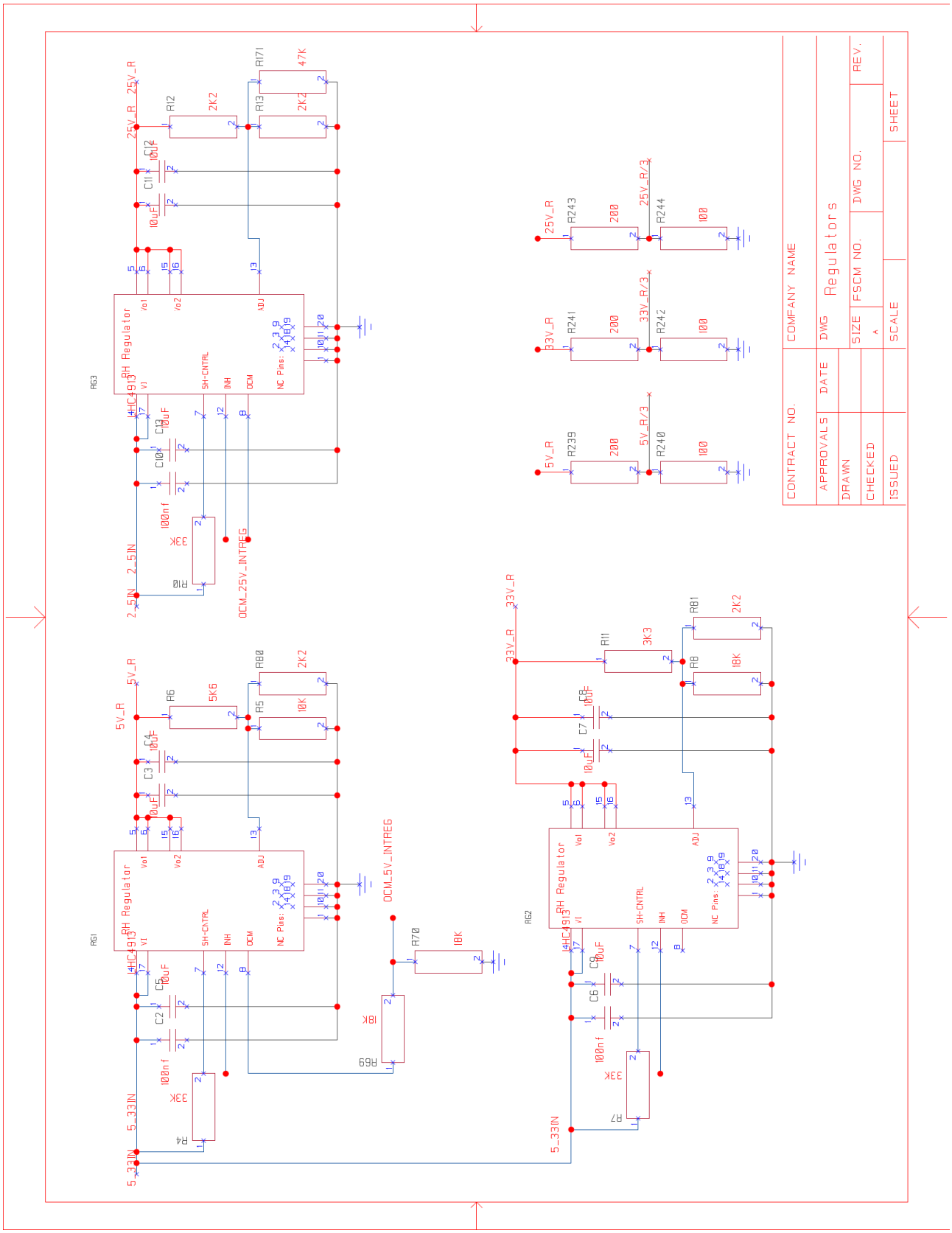


Image 10: Voltage regulators

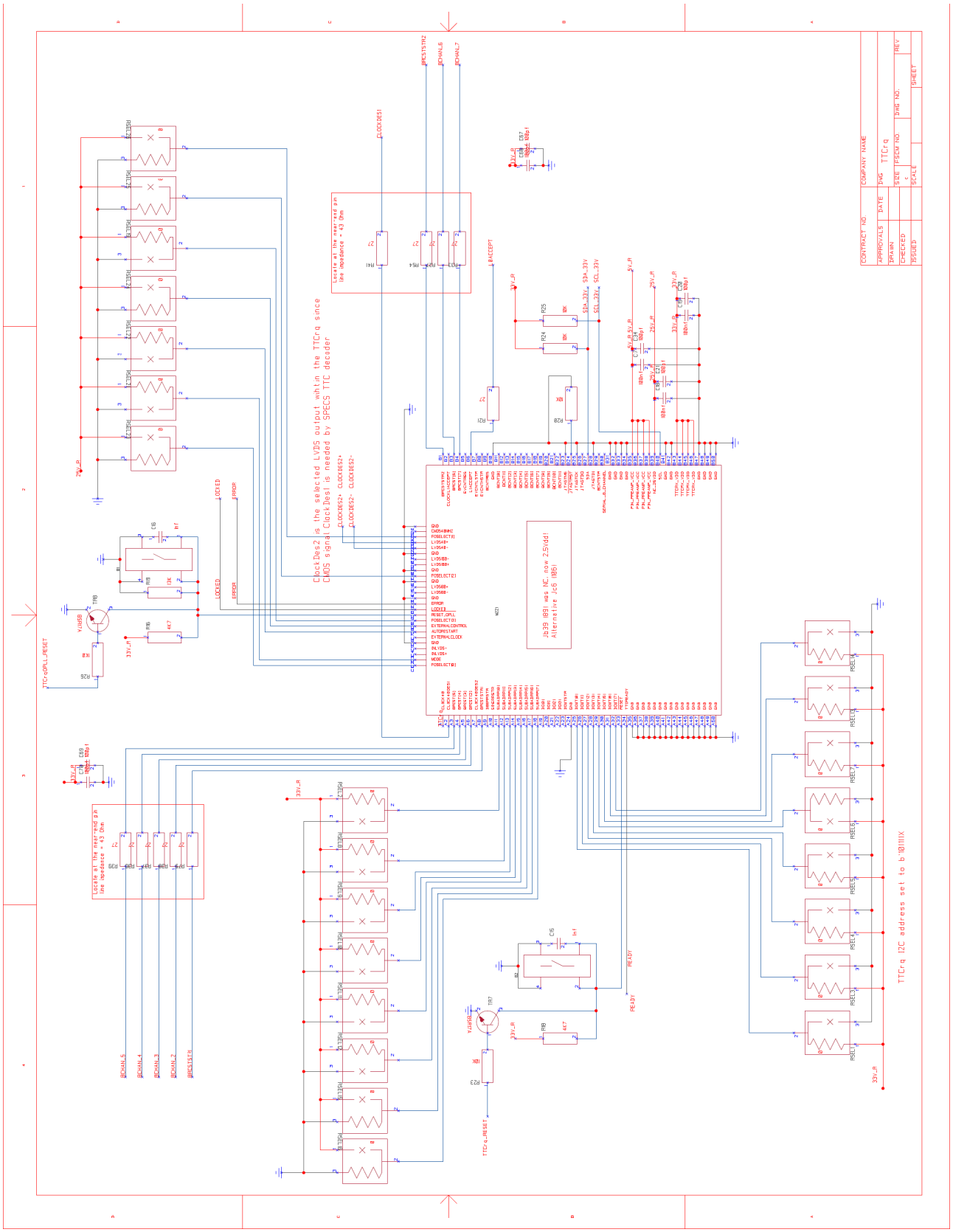
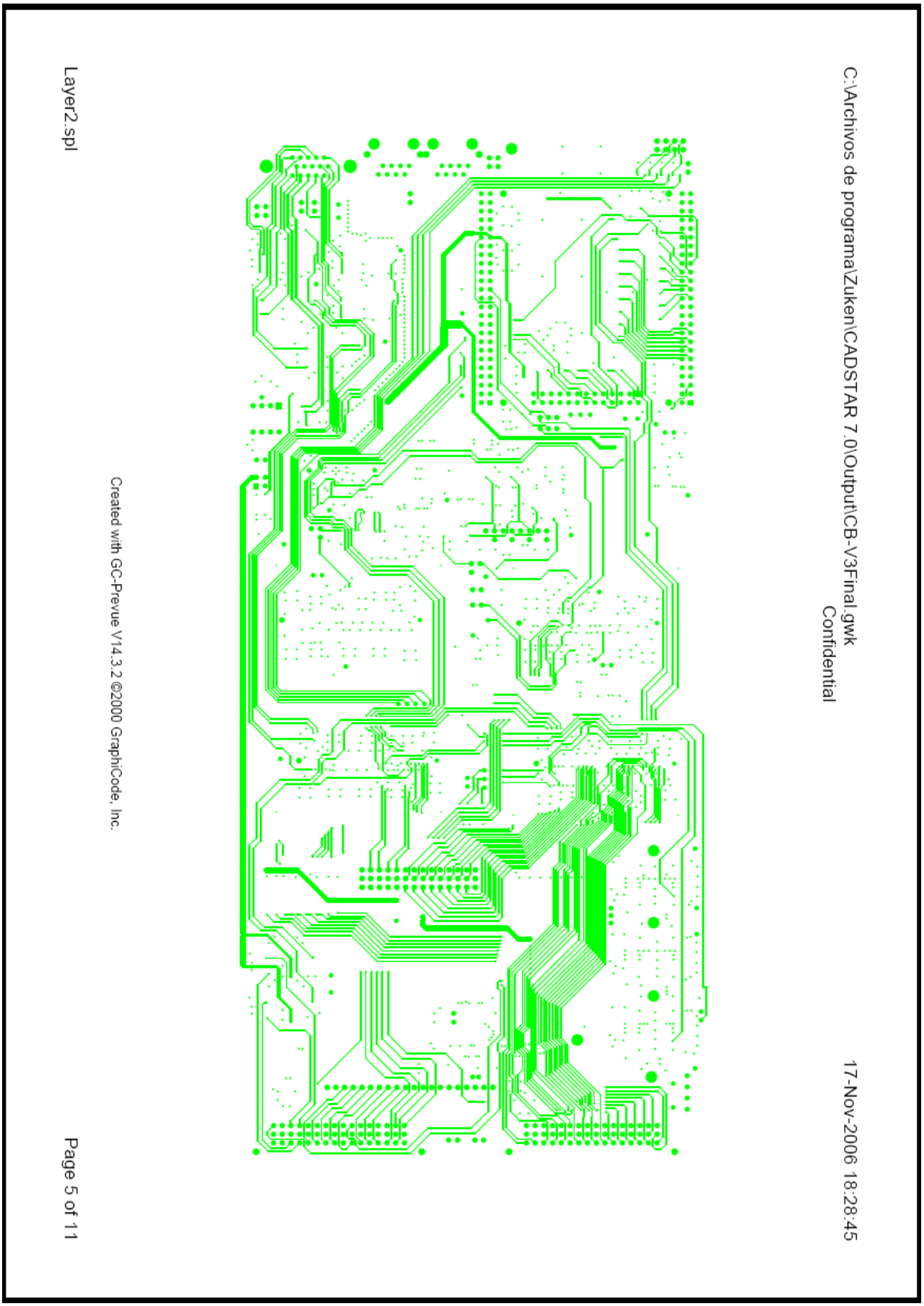
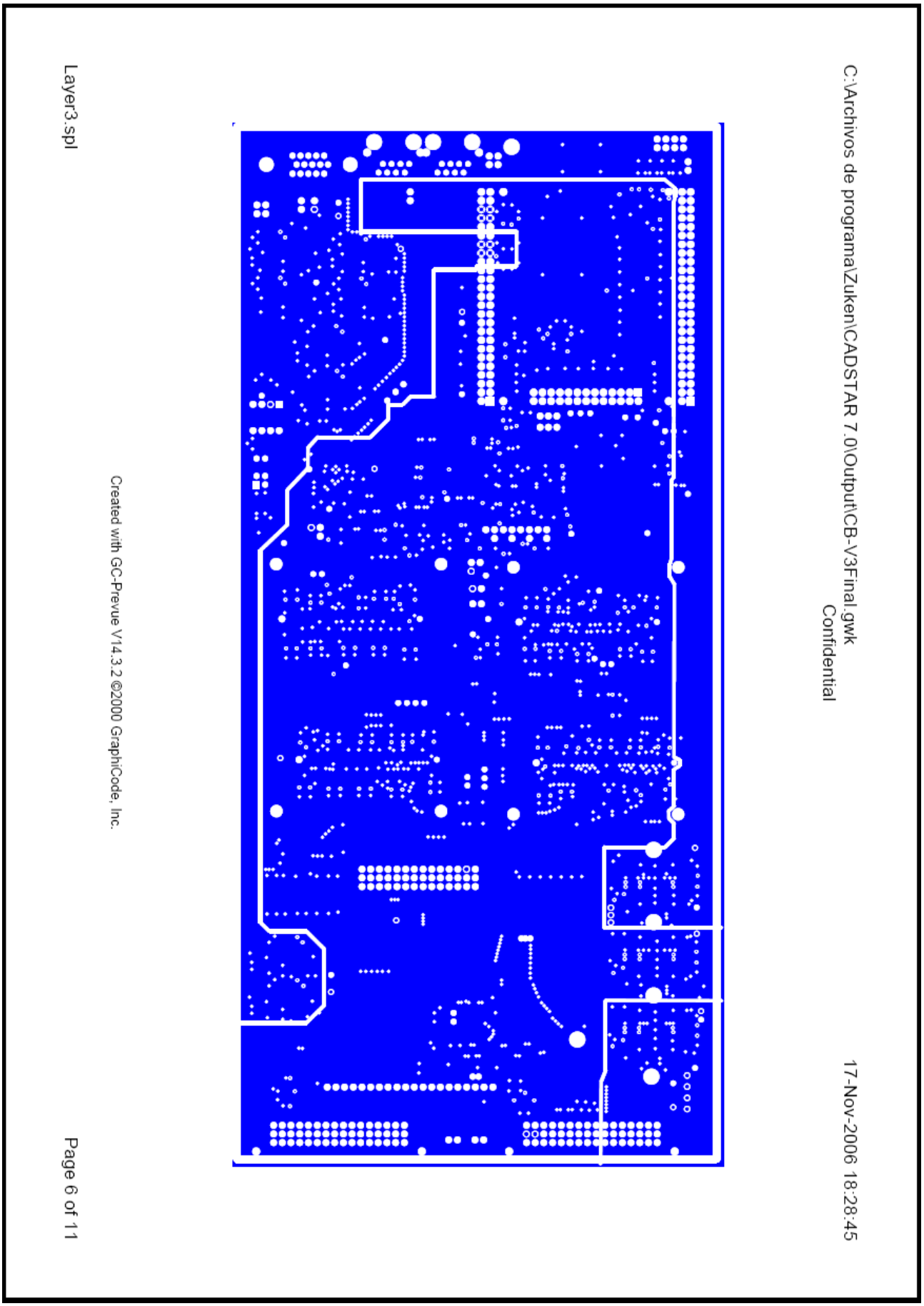
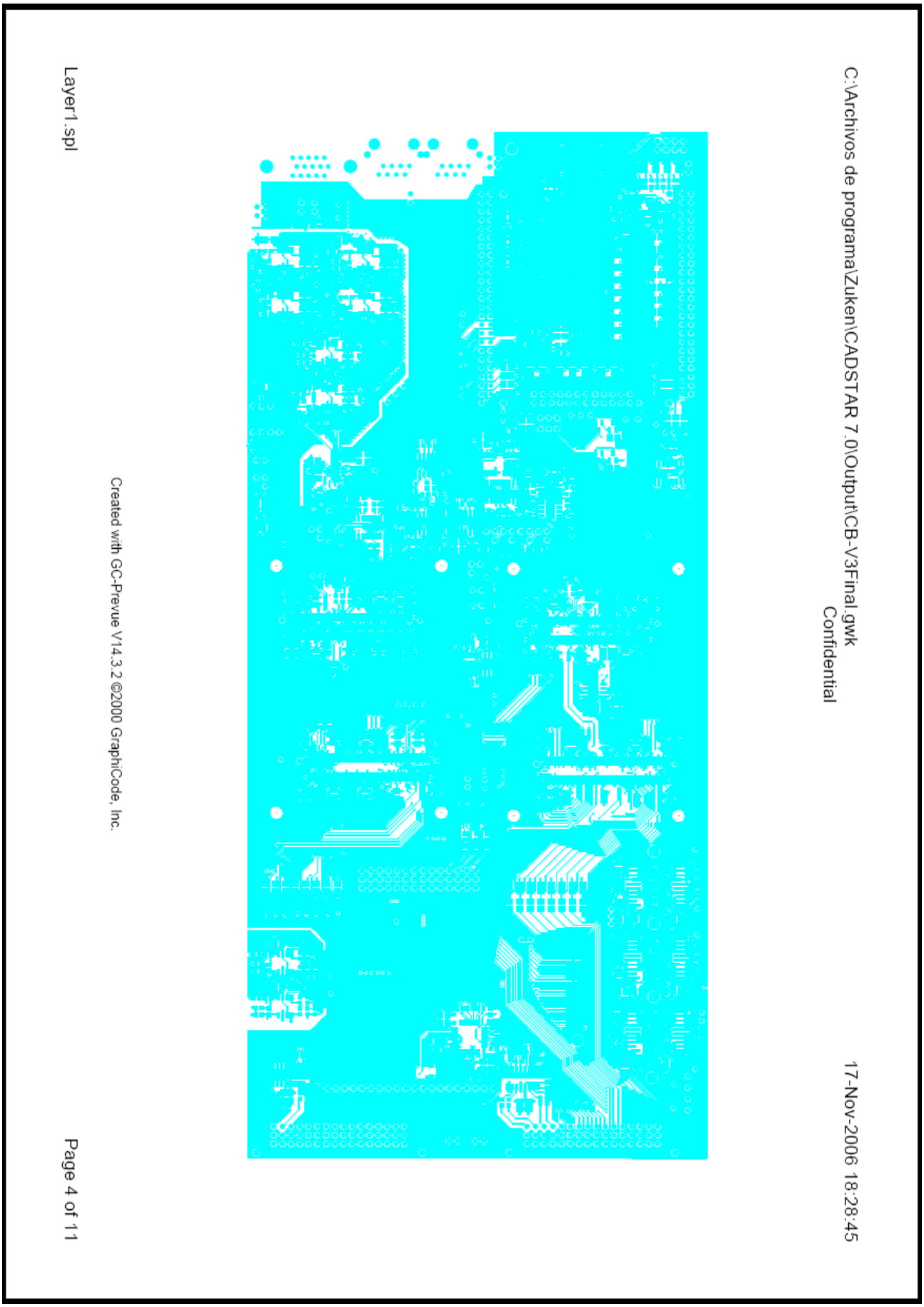


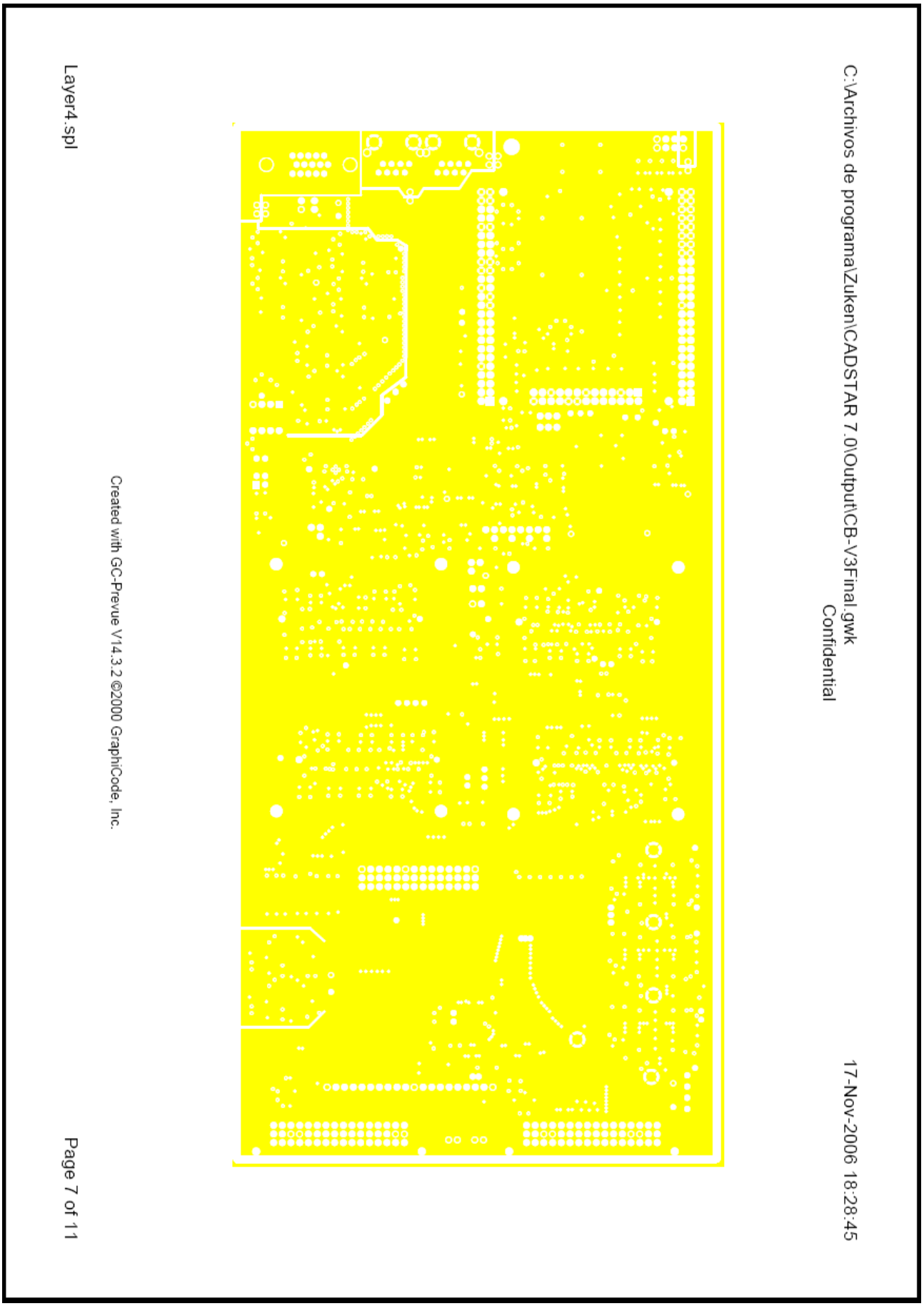
Image 11:TTCrq

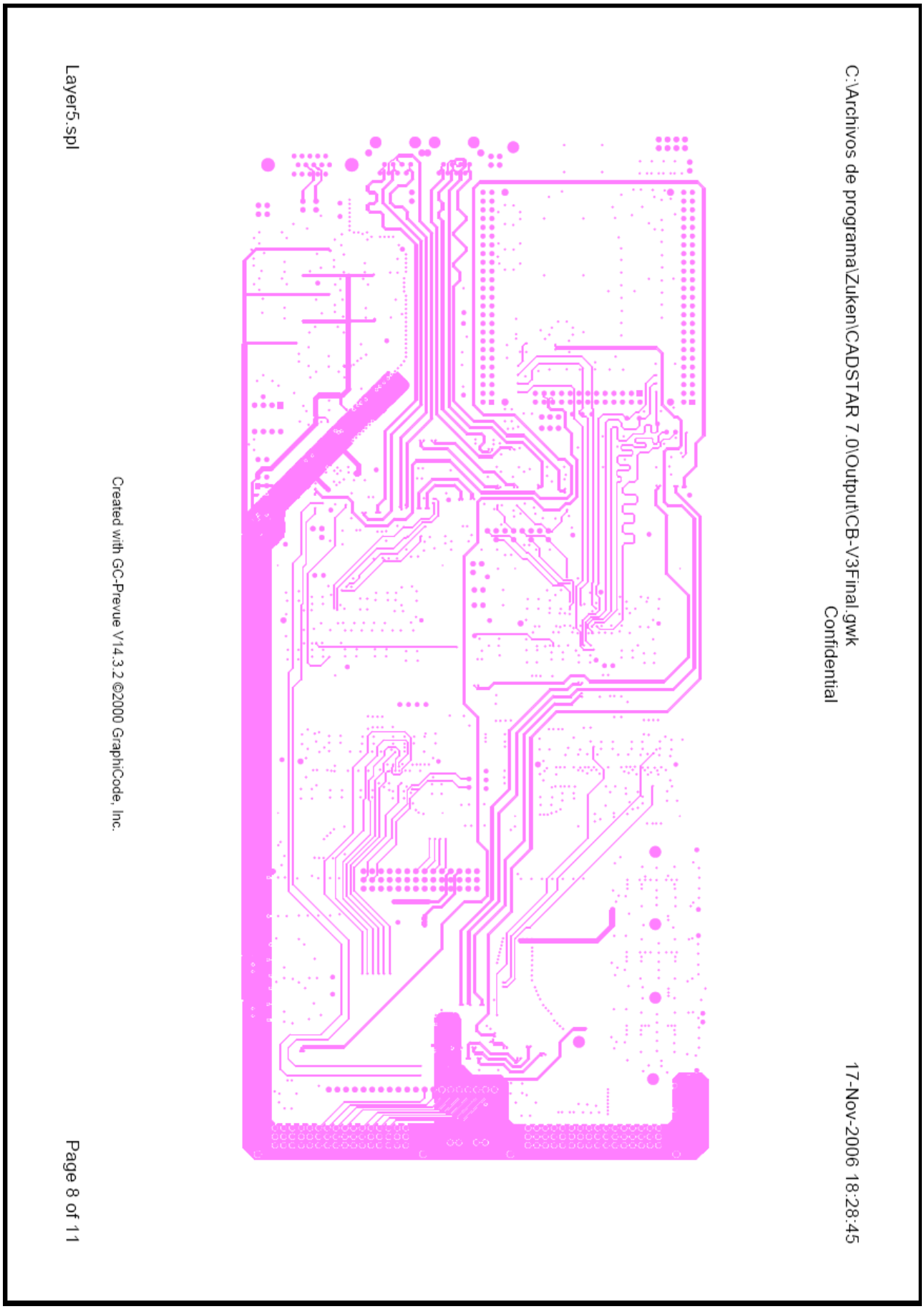
Appendix C: Control Board PCB layers

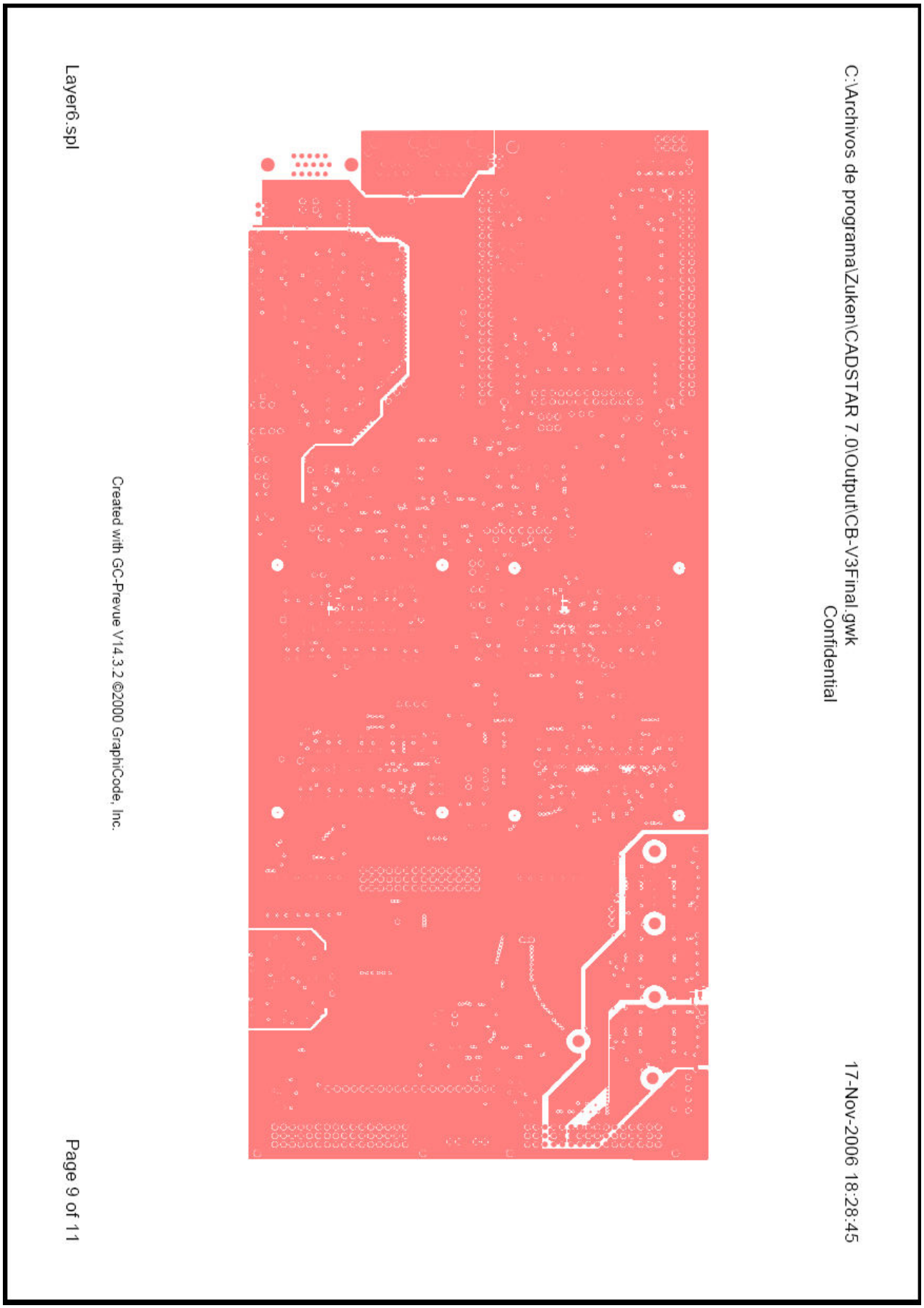

Layer2.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 5 of 11
C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45

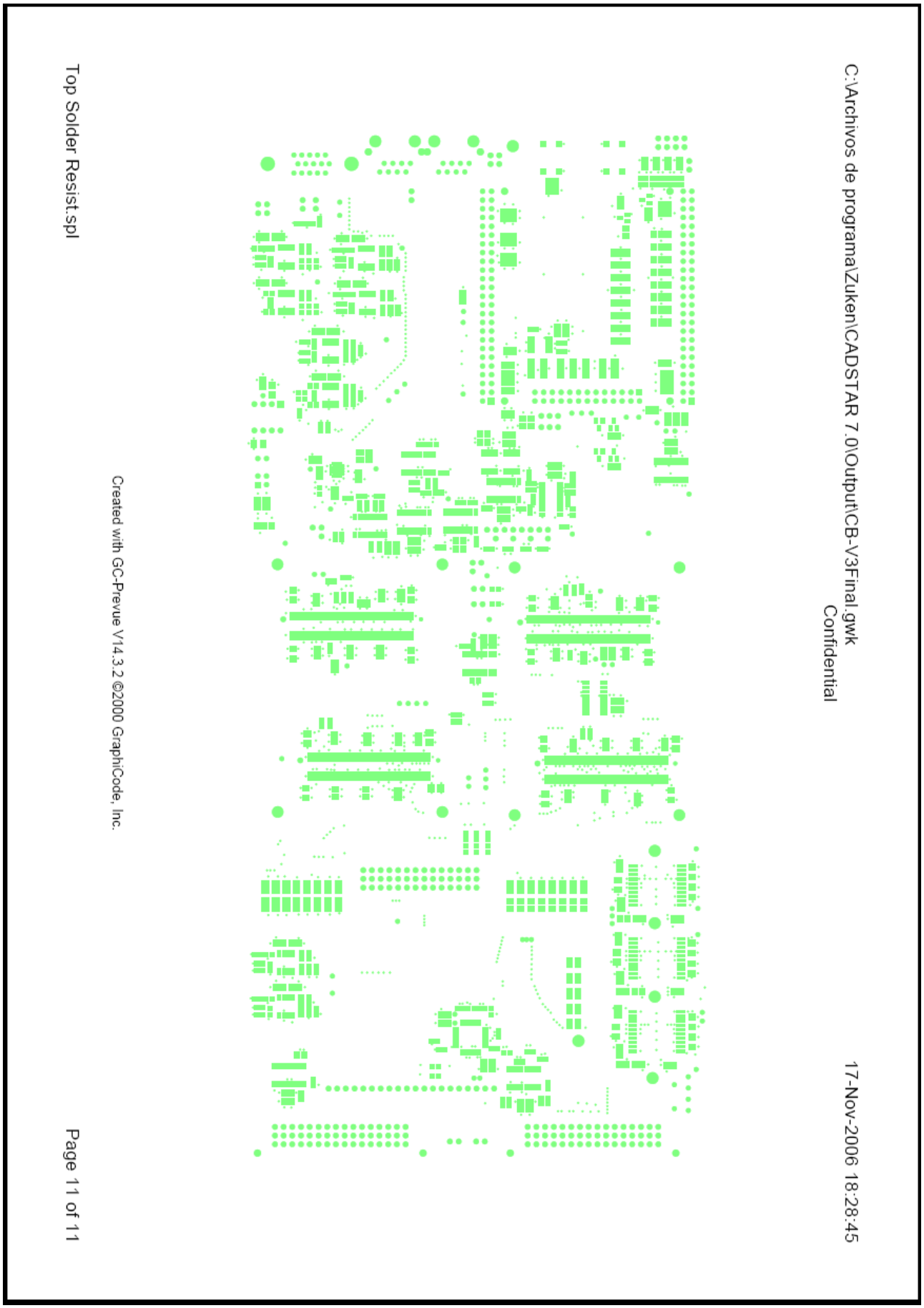

C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45
Layer3.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 6 of 11

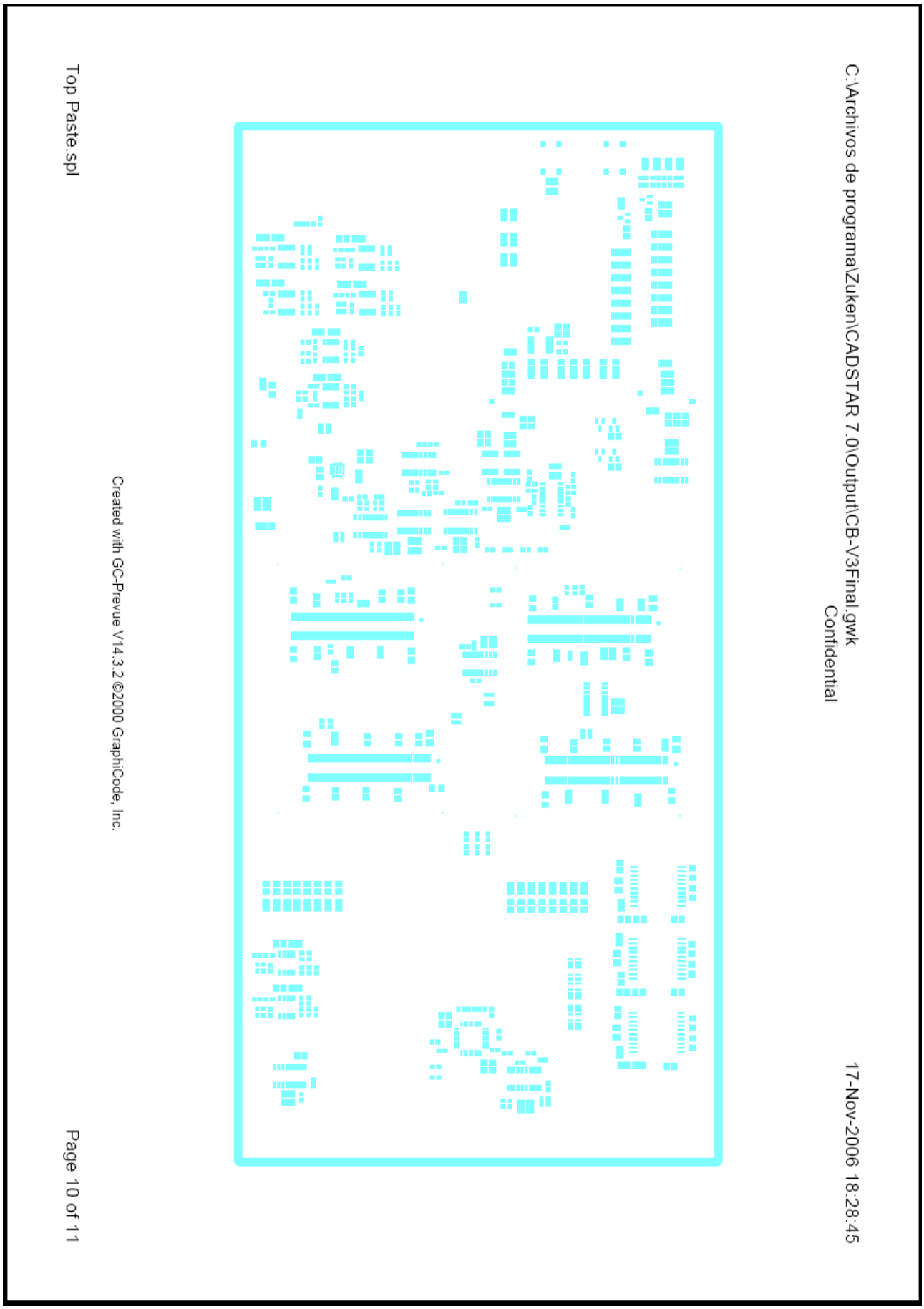

C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45
Layer1.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 4 of 11


C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45
Layer4.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 7 of 11

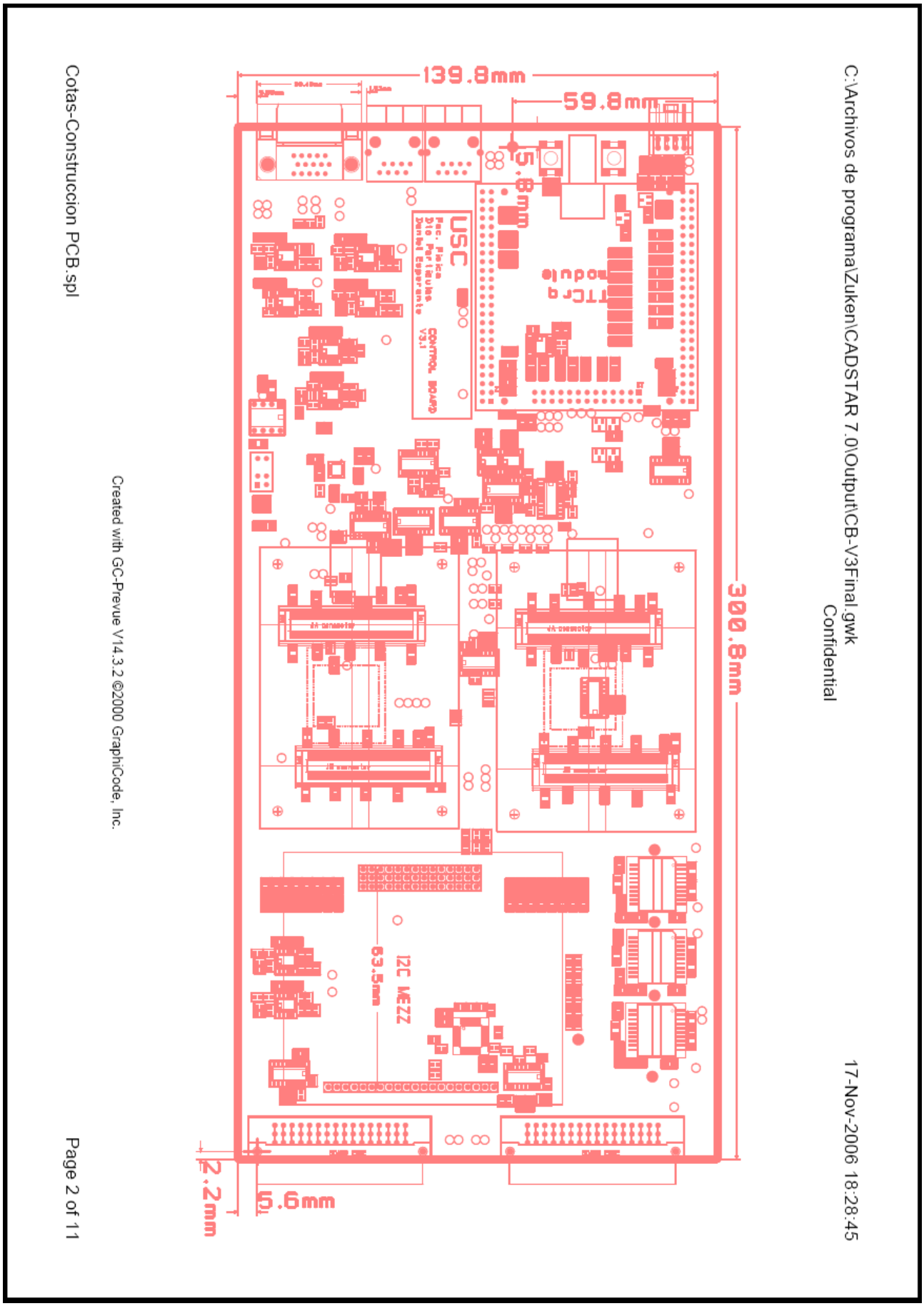

Layer5.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 8 of 11
C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45


Layer6.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 9 of 11
C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45


C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45
Top Solder Resist.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 11 of 11


C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45
Top Paste.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 10 of 11


Bottom Solder Resist.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 3 of 11
C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45


139.8mm
59.8mm
5.8mm
USC
CONTROL BOARD
V3.1
300.8mm
I2C MEZZ
63.5mm
12.2mm
5.6mm
C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\CB-V3Final.gwk
Confidential
17-Nov-2006 18:28:45
Cotas-Construccion PCB.spl
Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.
Page 2 of 11

Appendix D: Ctrl Board controlled impedance routes

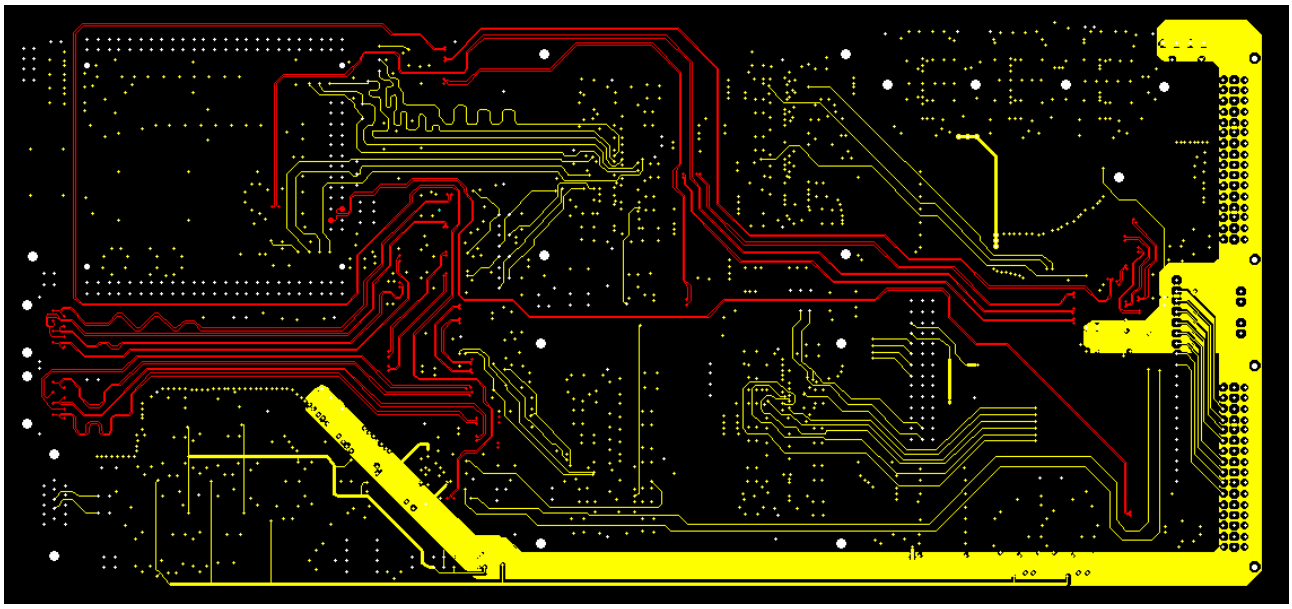


Image 12 : 100Ω differential impedance tracks. “Signal2” layer.

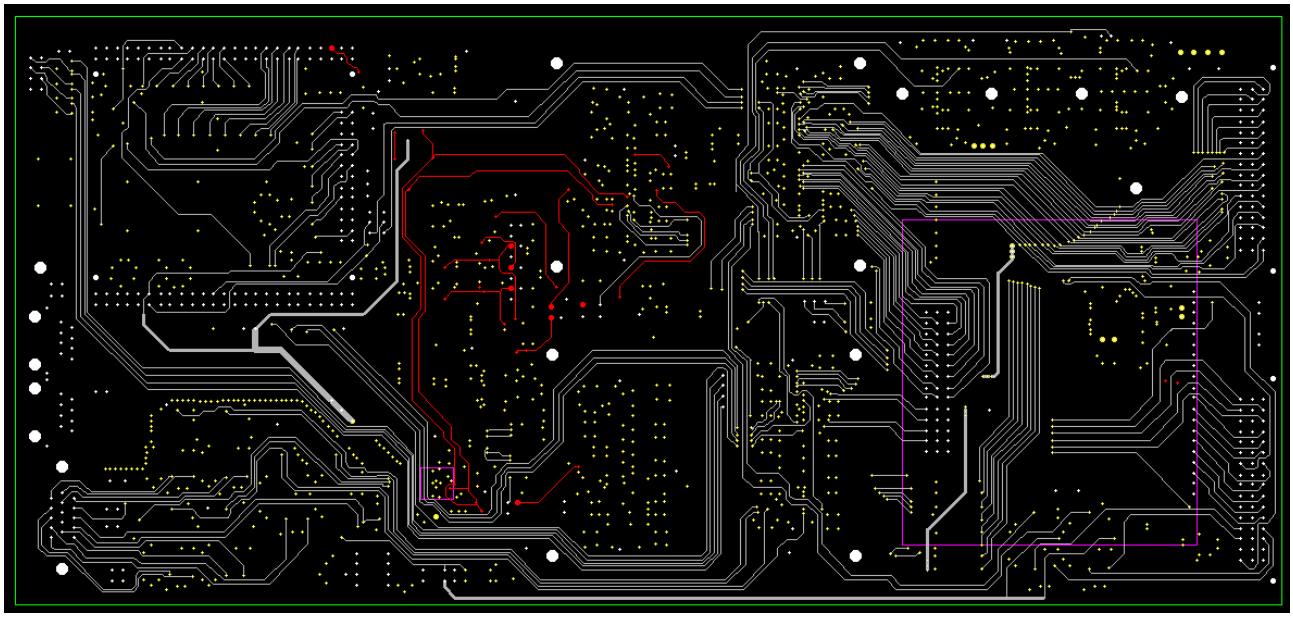


Image 13 : 60Ω impedance tracks. “Signal1” layer.

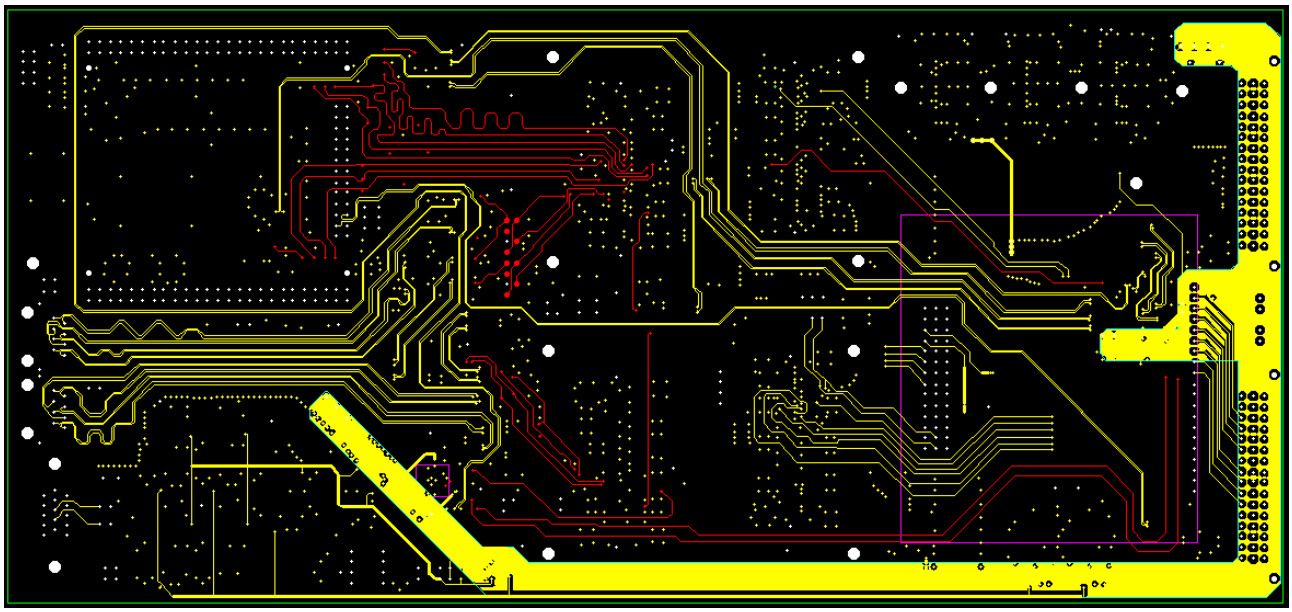


Image 14 : 60Ω impedance tracks. “Signal2” layer.

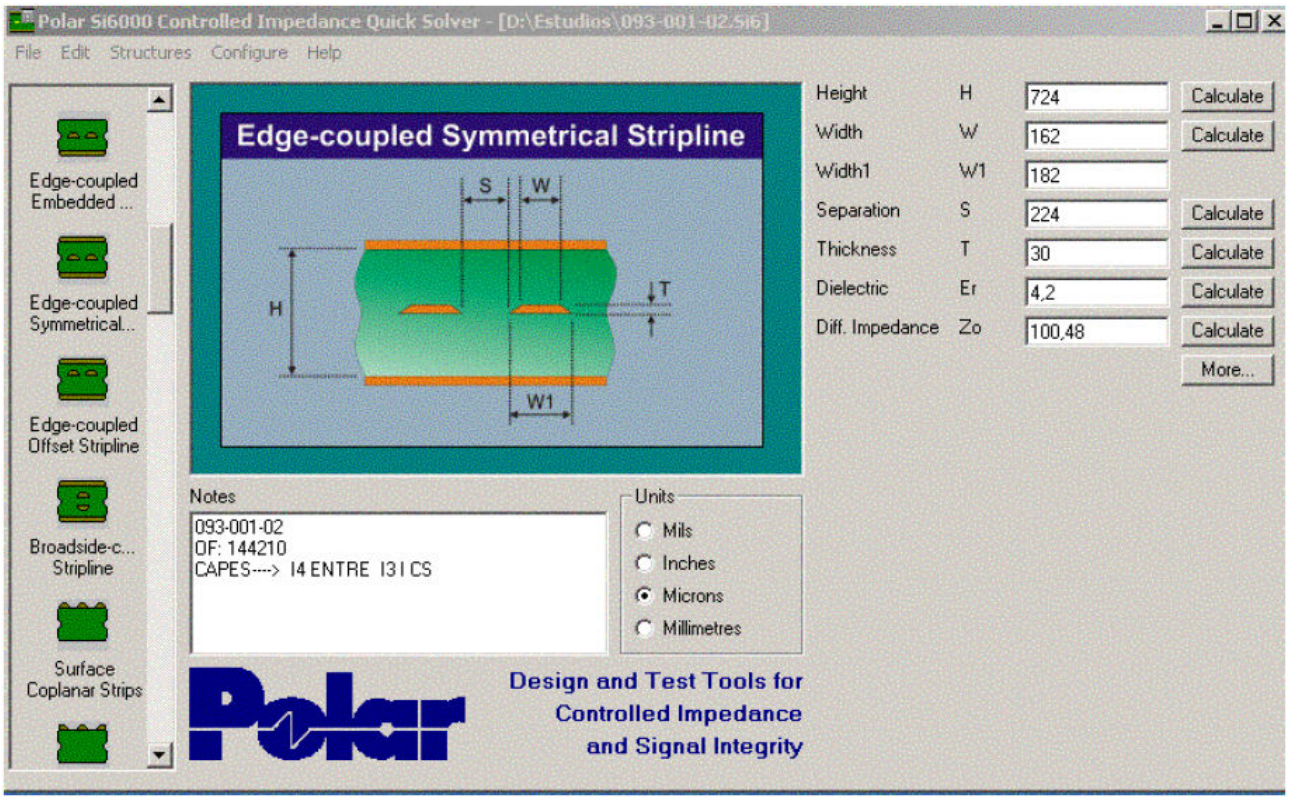


Image 15: Manufacturer controlled impedance solver result for 100Ω differential impedance

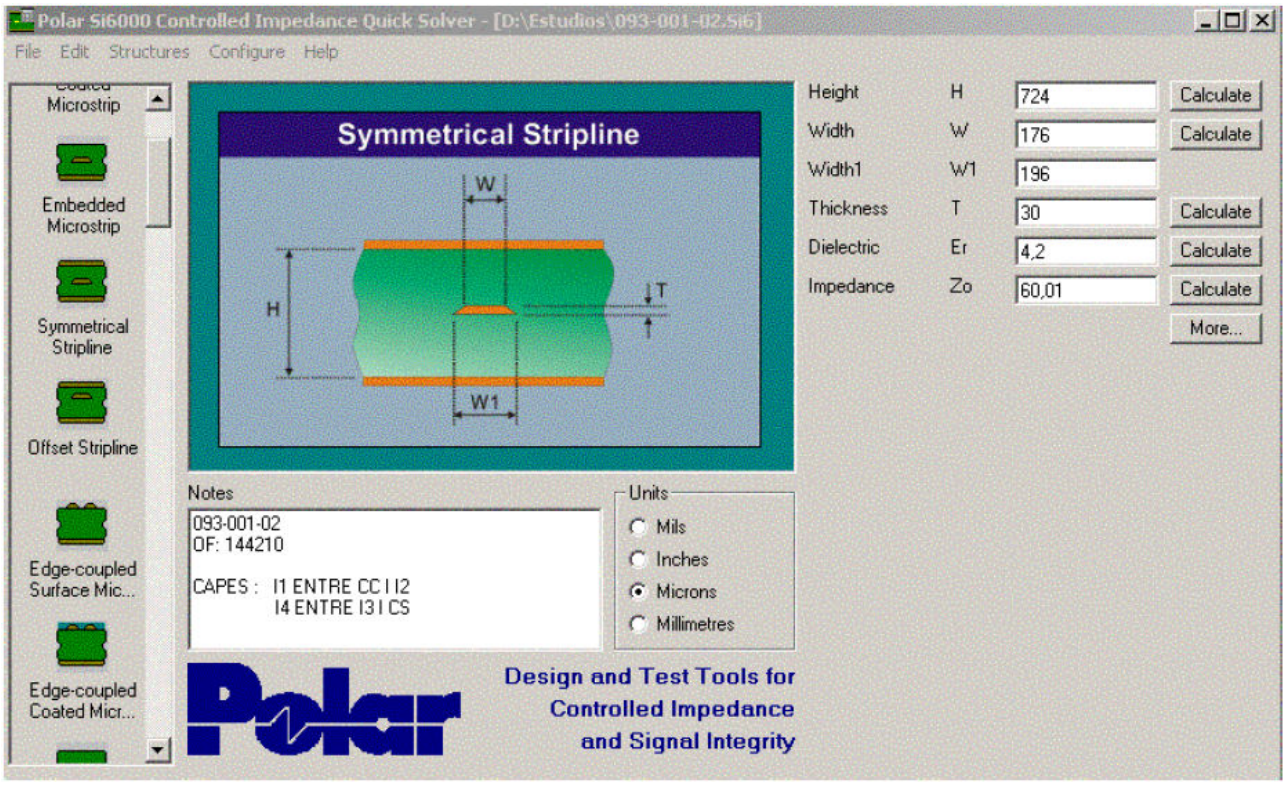


Image 16 : Manufacturer controlled impedance solver result for 60Ω impedance

Appendix E: I2C mezzanine schematic

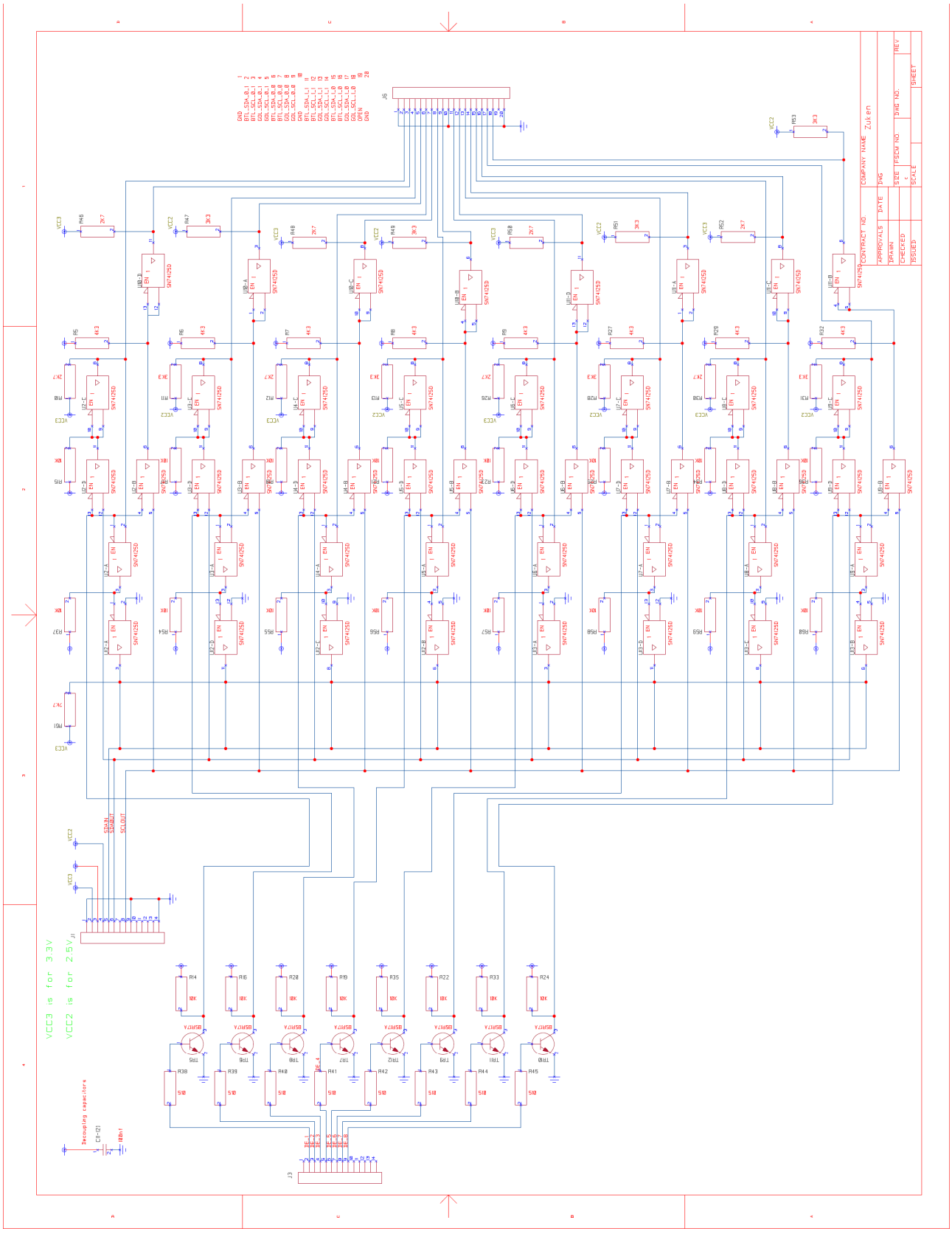
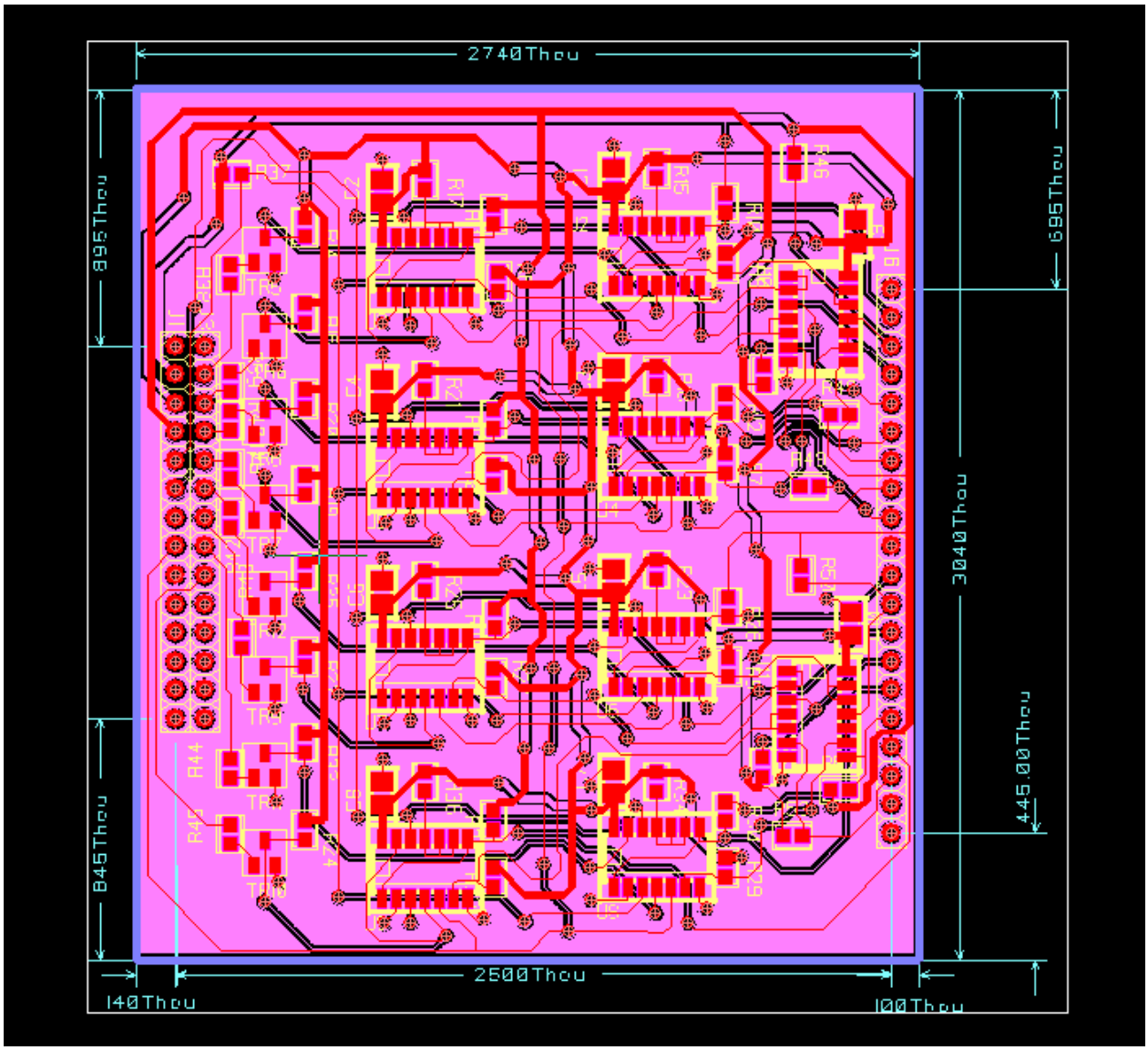


Image 17: I2C 8 buses mezzanine based in F125 tri-state gates

Appendix F: I2C mezzanine PCB layers

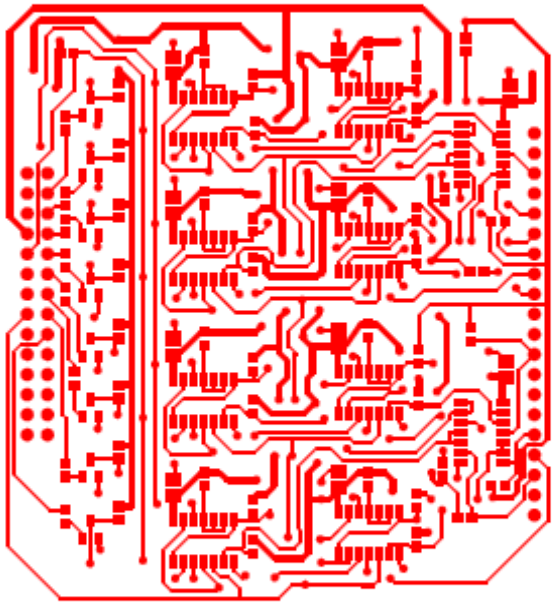


C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\I2CMEZZ.gwk 20-Nov-2006 12:34:50
Confidential

Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.

Top Silk Screen.spl Page 6 of 9

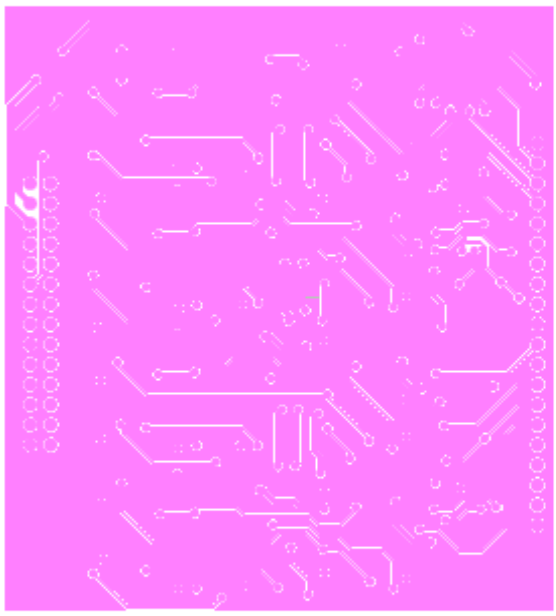
C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\I2CMEZZ.gwk 20-Nov-2006 12:34:50
Confidential



Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.

TopElec.spl Page 8 of 9

C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\I2CMEZZ.gwk 20-Nov-2006 12:34:50
Confidential

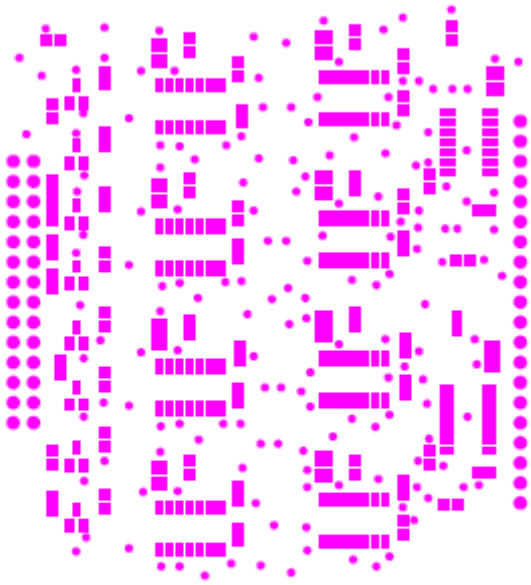


BottomElec.spl Page 2 of 9

C:\Archivos de programa\Zuken\CADSTAR 7.0\Output\I2CMEZZ.gwk 20-Nov-2006 12:34:50
Confidential

Created with GC-Prevue V14.3.2 ©2000 GraphiCode, Inc.

MechanicalDimensions.spl Page 3 of 9



Top Solder Resist.spl

Page 7 of 9

Appendix H: Svce box I2C addressing scheme.

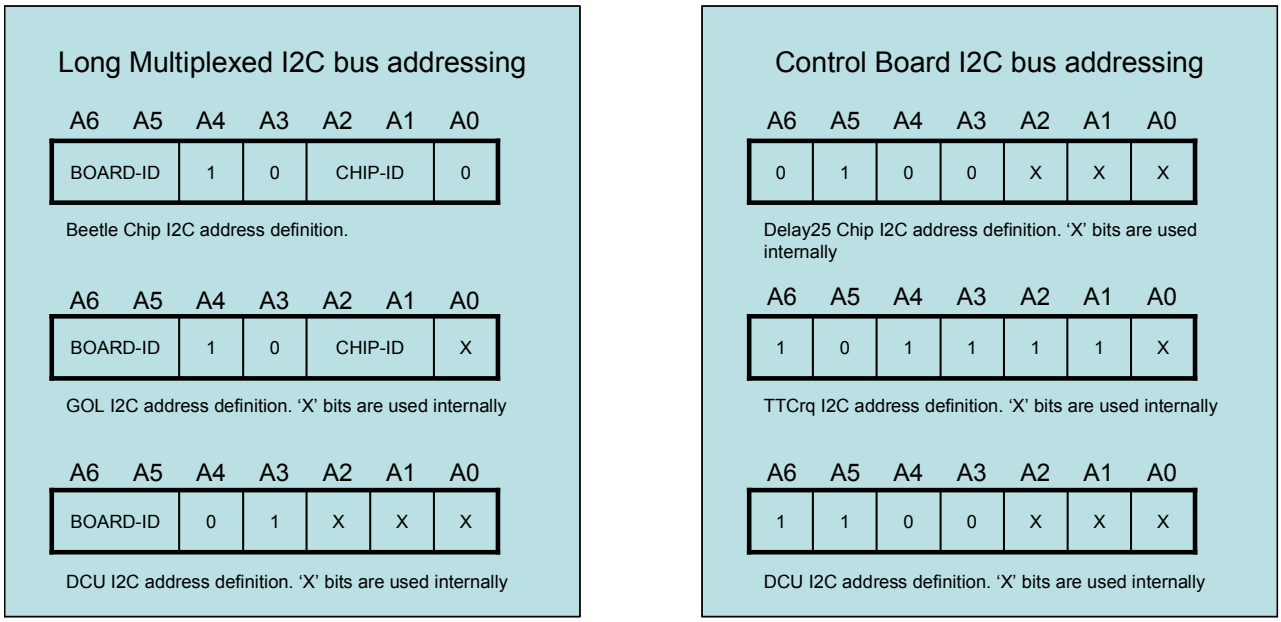


Image 18 : ST I2C addressing scheme

As each readout hybrid is associated with a Digitizer Board, a Board-ID is defined, ranging from 0 to 3 and set by the I2C address bits A6 and A5. All devices (Beetle, GOL, DCUF) linked to a specific board will be programmed with the same Board-ID. This is done with the common lines I2C ADR5 and I2C ADR6, which are connected to all I2C devices.

The logic state of these lines is determined for each Digitizer Board and its associated readout hybrid by the backplane slot, in which the Digitizer Board has been placed.

For the GOL/DCUF I2C us, address Bit A4 determines the device type, where '1' is associated with a GOL chip and '0' with a DCUF.

The GOL bits A2 and A1 are used for the Chip-ID, ranging from 0 to 3, which corresponds to the consecutive numbering of the Beetle chips on a given hybrid. In addition, associating bits A2 and A1 on the readout hybrid to the four Beetle readout chips creates identical addresses for each Beetle/GOL pair. No address conflict occurs since the I2C buses are held separate. As the bit A0 is used for programming internal GOL registers, the matching of addressed can not be extended to the full I2C address. The remaining bit A0 of every Beetle is connected to '0' as no further addresses are needed for the Beetle I2C bus.

SPECS internal DCUs have its own I2C bus each. The I2C address is 0x00 for both.

5. References

[1] Dominique Breton, Daniel Charlet, Patrick Robbe, Ioana Videau, "A Serial Protocol for the Experiment Control System of LHCb".

[2] P. Moreira, "TTCrq Manual", version 1.5. CERN-EP/MIC.

[3] LHC4913 series regulator datasheet. STMicroelectronics.

[4] L6225, "DMOS DUA

[5] L FULL BRIDGE DRIVER" datasheet. STMicroelectronics.

[6] C. Bauer, D. Esperante, R. Frei, U. Straumann, P. Vazquez, A. Vollhardt, "Grounding, Shielding and Power Distribution for the LHCb Silicon Tracking". LHCb note 2004-101.

[7] http://ttc.web.cern.ch . Timing, Trigger and Control (TTC) Systems for the LHC.

[8] G. Magazzu, A. Marchioro, and P. Moreira, "DCU User Guide", CERN, http://cmstrackercontrol.web.cern.ch/CMSTrackerControl/documents/Magazzu/DCU2_User_Manual v2.12.pdf

[9] Hagerman, Jim, "Two transistors form bidirectional level translator", EDN, Nov 7, 1996, pg 114.

[10] Achim Vollhardt, Daniel Esperante, Yuri Ermoline, "Results of proton irradiation of components for the LHCb Silicon Tracker". LHCb note 2004-037.

[11] Agapito et al. "Instrumentation Amplifiers and Voltage Controlled Current Sources for the LHC Cryogenic Instrumentation". Proceedings of 6th Workshop for LHC Experiments (LEB2000).

[12] HMX2000, Hygrotron-MEMS Hygro/Thermal Sensor, www.hygrometrix.net.

[13] M.Needham, "Channel numbering and readout partitioning for the Silicon Tracker", LHCb note 2006-033.