Production of the front-end boards of the LHCb muon system

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Abstract

This note describes the production of the front end boards CARDIAC, for the 1368 MWPC, and CARDIAC-GEM, for the 12 triple-GEM chambers, of the LHCb muon system. The PCB structure and component layout and the production issues, such as component soldering, quality assurance at the company and delivery rates, are described.
The performance of these boards will be the subject of a future publication.

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1 Introduction

The LHCb muon system is equipped with 1368 Multi Wire Proportional Chambers (MWPC) and 12 triple-GEM chambers.
In stations 2 to 5 the MWPCs are four gap chambers. Signals from pairs of consecutive gas gaps are summed by connecting the gaps together to one front-end channel and the two front end channels are then OR-ed, after discrimination. In station 1 the MWPC are two-gap chambers and each gap is connected to one front-end channel.
The triple-GEM chambers are made of two superimposed single gap chambers whose signals are digitally OR-ed.
This readout structure is achieved by plugging the front-end boards on chamber sides, as will be discussed in section 2.2.
Both the PCB structure and component layout and the circuitry of the front-end boards including the integrated circuits, are the result of many years of development, starting from the first boards conceived with the ADSQ chips [1] and going through the many prototypes of both chips and boards, involving many people from different groups.
This note describes the production of the final front-end boards, for both the MWPC and the triple-GEM chambers.

2 Integrated circuits on the boards and board positioning on the chambers

This section describes the main charateristics of the chips which are on the front-end boards and the board positioning on the chambers. These two issues are discussed here only for the sake of completeness and they are not a result of the work described in this note.

2.1 Integrated circuits on the front-end boards

The front-end boards, named CARDIAC for the MWPC and CARDIAC-GEM for the triple-GEM detector, house three CMOS, IBM 0.25 μm technology, chips: two ASD (amplifier-shaper-discrimnator) chips, CARIOCA [3] for the MWPC and CARIOCAGEM [4] for the triple-GEM detector, and a DIALOG [5] chip. The latter mainly performs the OR of the two ASD output signals.
The CARIOCA chip has eight identical channels. The input of the CARIOCA circuit is pseudo - differential, consisting of two identical current-mode amplifiers. One amplifier is connected to the chamber pad. The other one has a floating input and is used to provide DC balance to the shaper and common mode rejection to pickup, crosstalk and noise on the power supply lines. After the amplifier, there is a shaper circuit and a differential amplifier which provide further gain together with signal and amplifier tail cancellation. The differential amplifier output is fed to the discriminator. The discriminator output is sent to the LVDS driver that provides the chip output signal. A baseline restoration circuit, realized as a nonlinear feedback loop around the second differential amplifier, limits the baseline fluctuations at high rate. Two different amplifiers are implemented for each channel, one for positive signals, i.e. for cathode readout and one for negative signals, i.e. for anode readout. A polarity switch allows to select one or the other amplifier, depending on the use for anode or cathode readout.
The charatcteristics of this chip is a charge sensitivity of about 14mV/fC at 0 pF of input capacitance, decreasing to 7 mV/fC at 220 pF and an equivalent noise charge of 2240+42e-/pF (1880+45e-/pF) for the positive (negative) amplifier, linearity of the response up to 200 fC, peaking time of 10 ns and pulse width of 20 ns at 15 pF of detector capacitance.
The CARIOCA-GEM circuit is very similar to the CARIOCA, but for the removal of the ion tail cancellation circuit in the shaping amplifier and an increased gain of this stage by a factor 1.5; the peaking time rises to 14 ns and the pulse with to about 30 ns at 15 pF of detector capacitance.
For both of these chips the cross-talk among channels was measured to be smaller than 0.5 %.
DIALOG (DIagnostic, time Adjustment and LOGics) performs the reduction from the 121,112 front-end channels (which are called Physical Channels) to the 25,920 trigger channels (called Logical Channels). The CARIOCA chip has eight binary outputs, hence DIALOG manages 16 input Physical Channels, with an output of at most 8 Logical Channels. Another key task of the circuit is to make it possible

proper detector time alignment channel by channel, which is also necessary for a correct operation of the muon trigger. It also performs, independently for each channel, threshold level generation for the front-end chip and has front-end monitoring facilities dedicated to system debug and diagnostics. All DIALOG functions are configured by the I2C protocol.
The CARIOCA and CARIOCA-GEM were inserted into the TQFP100 package while the DIALOG was inserted into the TQFP120 package.
The front-end board is therefore a mixed analog-digital signal board. Given the high current sensitivity of the amplifier channels, the readout architecture was orgnanised so that the configuration logic signals, such as the ones for threshold setting and time alignment, were only generated on the board outside of the run time of the experiment. The only function which has to be active during the run time is the readout of the internal scalers of the DIALOG.
Still, the simultaneous presence of very low analog input signals and comparatively large digital LVDS signal running between the front-end chips and the DIALOG and at the DIALOG output represents a serious challenge for the designer.

2.2 Front-end board positioning on the chambers

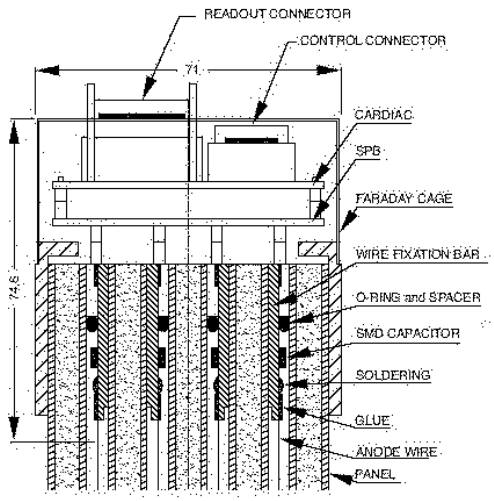


Figure 1 Schematic drawing of a four gap MWPC showing the connection of the detector to the front-end.

The readout structure for the MWPC is shown in Fig. 1 and consists of a spark protection board (SPB) [1] to protect the electronics from sparking in the chamber and a CARDIAC board. For the four gap MWPCs with cathode readout another intermediate board, OR Pad Board, was added to perform the analog summing of signals from nearby gaps.
Due to space requirements, the CARDIAC-GEM board was produced with a slightly different layout from the CARDIAC. One board was designed which performs the previously mentioned functions altogether. Its placement on the chamber sides is shown in Fig. 2.

3 Front-end board functions

The functions of the CARDIAC board are shown in Fig. 3a). Eight analog signals, coming from the SPB, are sent to the CARIOCA input; the discriminated signals are sent to the DIALOG, as LVDS signals. The DIALOG performs the OR of the two CARIOCA input and sends the output LVDS signals to the off-detector boards. The DIALOG performs also threshold setting independently for all CARIOCA channels and sends injection pulses to all channels of one CARIOCA chip simultaneously. DIALOG functions can be accessed using the I2C protocol. Moreover a polarity switch is set in order to exploit

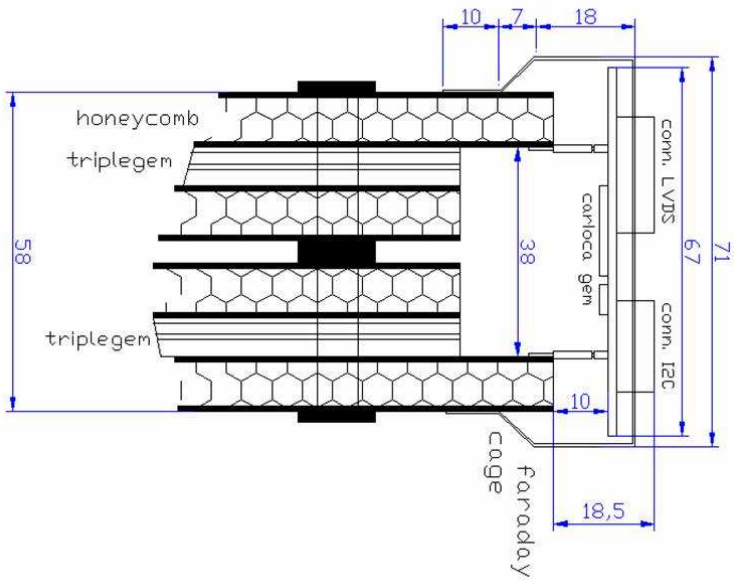


Figure 2 Schematic drawing of a triple-GEM chamber showing the connection of the detector to the front-end.

Table 1 Number of boards for equipping the chambers of the experiment, number of requested spares [2] and total number of needed boards.

	needed on detector	spares	total
CARDIAC(+)	4032	416	4448
CARDIAC(-)	3312	180	3492
CARDIAC-GEM	288	48	336

the CARIOCA property, described in section 2.1 of benefitting from a dedicate preamplifier, depending of its use for wire or cathode readout.
For the CARDIAC-GEM the space requirement made it mandatory to concentrate all functions on one board, as shown in Fig. 3b), including the spark protection circuit.
The number of needed boards for equipping the chambers together with the requested spare boards [2] is shown in table 1.

4 PCB structure and component layout

Both types of boards are made of 6 layers, approximately 1.6 mm thickness, gold plated FR4. The dimensions are 62.23x48.26 mm for the CARDIAC board and 67.31x46.99 mm for the CARDIAC-GEM board.
To minimise the interaction of the digital signals with the input channels, the CARIOCA chips in the CARDIAC board are placed on the inner PCB layer, i.e. towards the chamber, while the DIALOG is placed on the outer PCB layer. For the CARDIAC-GEM all chips were placed on the external layer.

4.1 PCB layer structure

The six layers are organized as follows:

1. TOP (external layer). DIALOG chip (also the two CARIOCAs in the GEM version), digital lines and LVDS output lines.

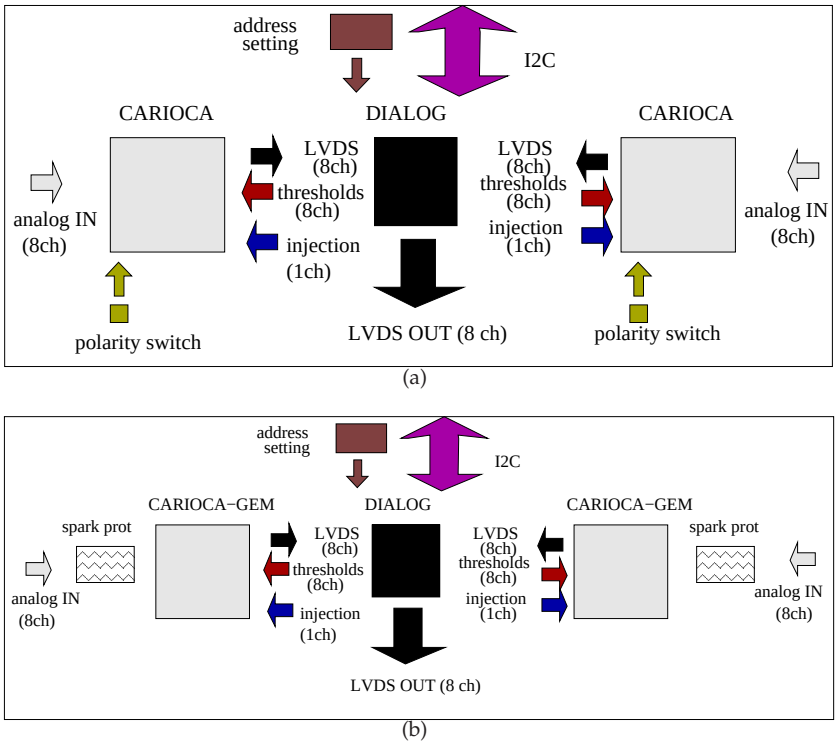


Figure 3 Functions of the CARDIAC board (a) and of the CARDIAC-GEM board(b)

2. GND1. Ground plane unique for analog and digital
3. INNER. Digital lines
4. PWR. Power plane unique for analog and digital
5. GND2. Ground plane identical two GND1
6. BOT (close to the detector). CARIOCA chips (spark protection circuitry for the GEM version), analog lines and input lines.

The PCB [9] are made of three FR4 sheets of 0.4 mm thickness, with insulation between the sheets of 0.18 mm. Cu thickness is 30 μm, Au thickness for the TOP and BOT layers is 0.1 μm; the nominal width of the lines is 6 mils (150 μm).
The connectors used are 3M (CH87102V100 and CH87162V100) and MOLEX (53324-0460) for the CARDIAC and the FTSH series of SAMTEC for the CARDIAC-GEM.
Signal injection from DIALOG to CARIOCA was fixed to an input step voltage of 2.5 V which corresponds to an input charge of 125 fC, and it can be used to verify if one amplifier channel is alive or not. One pad per chip accessing the analog output of the eighth channel was also designed on the board and is accessible for readout using a probe terminated into a 50 Ω load.

4.2 Grounding and low voltage distribution

The final grounding layout has been determined experimentally from several prototypes testing different solutions. Different ground schemes with separate ground/power for analog and digital where also tested, but the chosen layout gave the lower noise and better stability. Ground and power are common to analog and digital parts. Ground copper areas are added two the top layer to shield the LVDS outputs and to the bottom layer to shield the input lines (CARIOCA version only). The electrical connection between the different ground areas is ensured by several vias. For ground pads were also designed on the corners of the top layers to make a soldered ground connection with the Faraday cage

of the chambers.
To avoid ground loops with the I2C lines, the ground pin of the I2C input and output connector was not connected to the GND for the boards.
All bias lines were bypassed as close as possibile to the input pads of the chips with 100 nF capacitors. A large bypass capacitor of 10 μF was also added very close to the input pin of the low voltage connector.
A fraction of the positive CARDIAC boards were provided with additional shielding on top of the chips when mounted on high capacitance MWPC's.This turned out to be useful to reduce the (coherent) noise rate on these boards to an acceptable level.
The supply voltage is 2.5 V and the current consumption around 450 mA per board.

4.3 Spark protection circuit on the CARDIAC-GEM board

The spark protection circuit for the CARDIAC-GEM board has to stand potentially dangerous 500 V discharges and protect the CARIOCA-GEM input. The circuit is made of the series of a high power 10 Ω resistor [8], a small signal BAV99 diode and a standard surface mount 8 Ω resistor, as shown in Fig. 4. This circuit acts on the very fast transient discharge pulse as a nonlinear voltage divider. It was

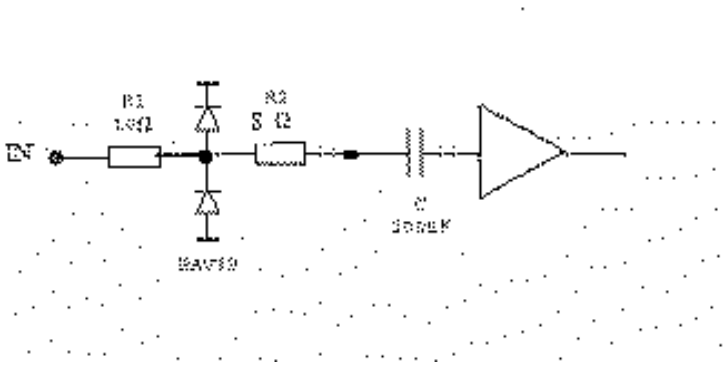


Figure 4 Schematic drawing of the spark protection circuit of the CARDIAC-GEM board.

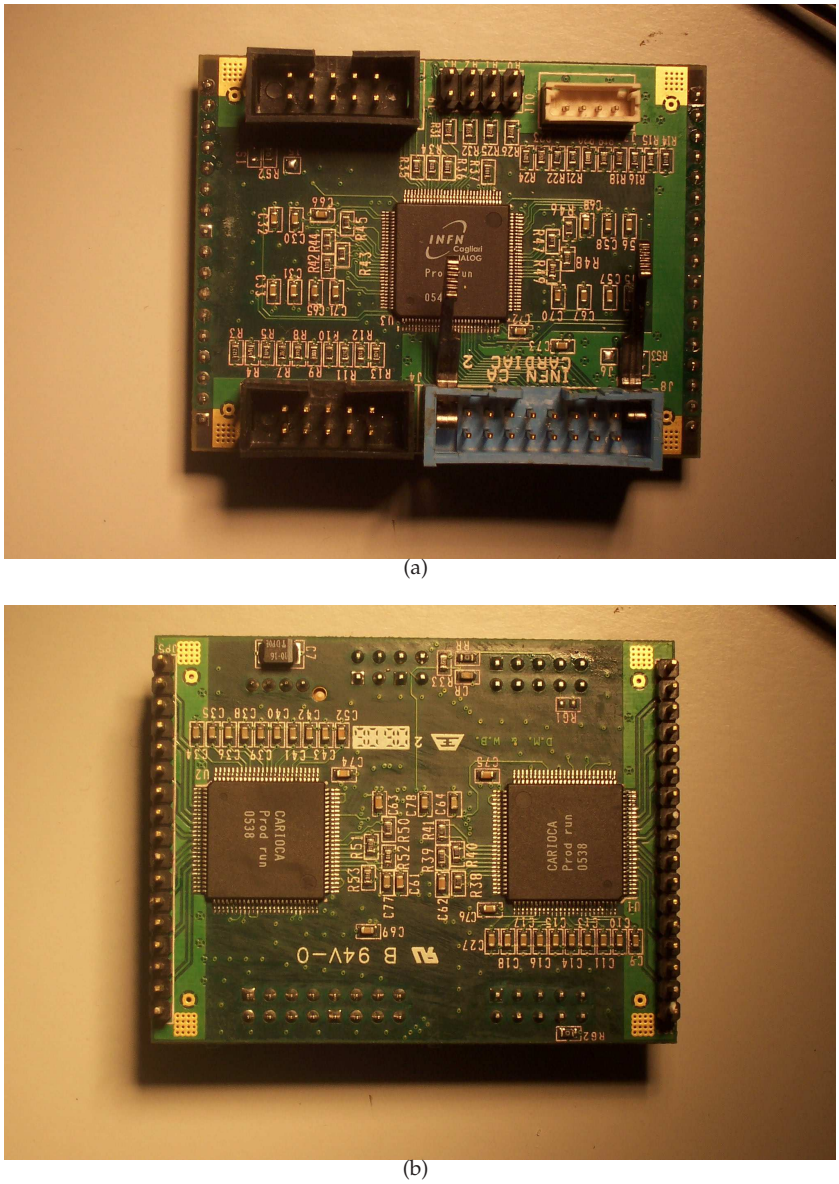
shown by tests that, at 500 V, the pulse amplitude at CARIOCA-GEM input (input impedance of 50 Ω) is reduced by a safe factor of 50. The high power resistor was tested for discharges with a needle setup at 500 V and its resistance value did not show any deviation from the nominal values even with a million discharges.
A picture of the CARDIAC board is shown in Fig. 5 while a picture of the CARDIAC-GEM board is shown in Fig. 6.

5 Component soldering on the PCB

Surface mount components were soldered with the reflow soldering process. The paste [11] was forced through the apertures of an Alpaca stencil, laser cut, 200 μm thick, onto the solder lands on the PCB, passing by hand a metal squeegee. The boards were then passed through a convection reflow oven with transport speed of 180 mm/min and a peak temperature of 225^0C. The reflow temperature of the paste was 183^0C and the thermal cycle above this temperature lasted for about 40 s.

6 Quality assurance at production site and yield

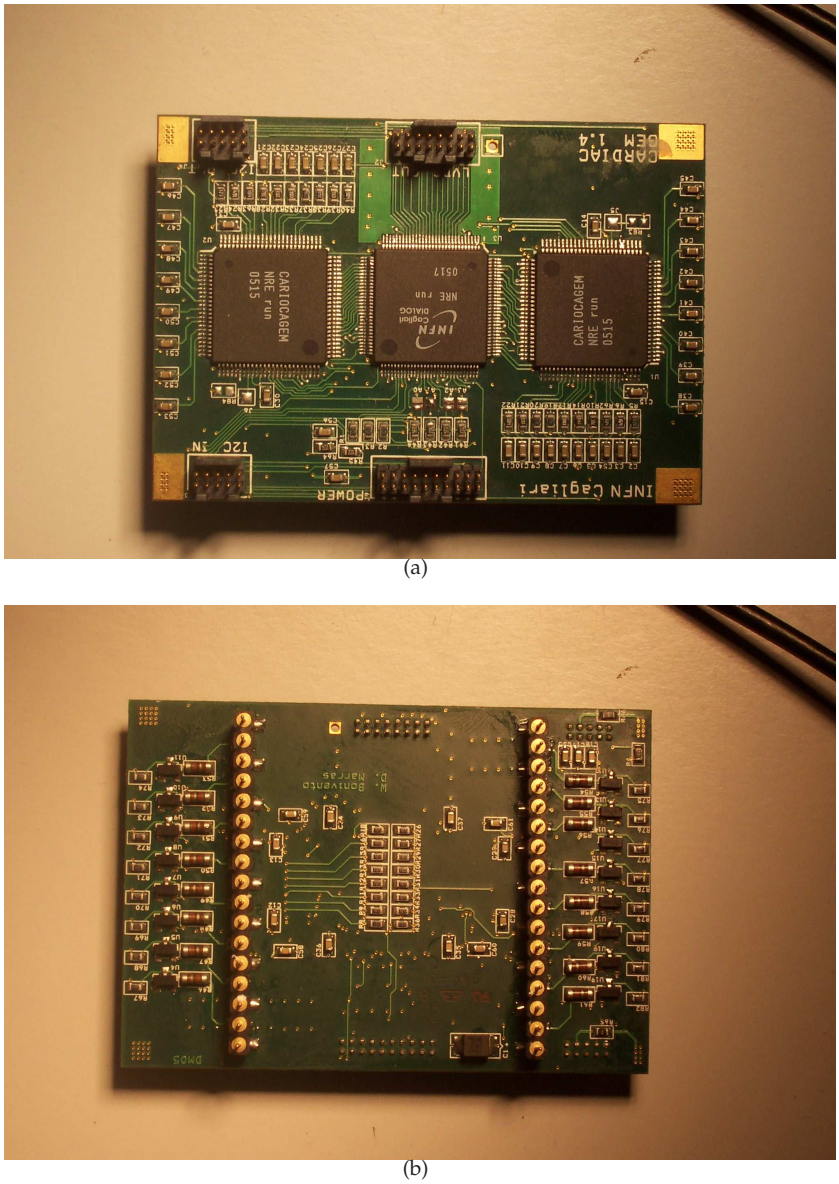
Only chips positively tested after packaging were assembled on the boards. The test [6] consisted of a full charatcterisation in terms of noise and linearity at a fixed input capacitance of 100 nF, simulating the detector. A current leakage test on all the pins was also performed.



(a)

(b)

Figure 5 A picture of the CARDIAC board. In Fig(a) the top layer is shown; the connectors of the upper row are from left to right the input I2C, the I2C address setting and the low voltage; the connectors of the lower row are the output I2C and the output LVDS; the DIALOG chip is in the middle. In Fig.(b) the bottom layer is shown; the left and right connectors are the input connectors from the SPB; the two CARIOCA chips are in the middle.



(a)

(b)

Figure 6 A picture of the CARDIAC-GEM board. In Fig(a) the top layer is shown; the connectors of the upper row are from left to right the output I2C and the output LVDS; the connectors of the lower row are the input I2C and the low voltage; the chips from the left to the right are the CARIOCA-GEM, the DIALOG and the other CAROCA-GEM. In Fig.(b) the bottom layer is shown; the left and right connectors are the input connectors from the triple-GEM chamber.

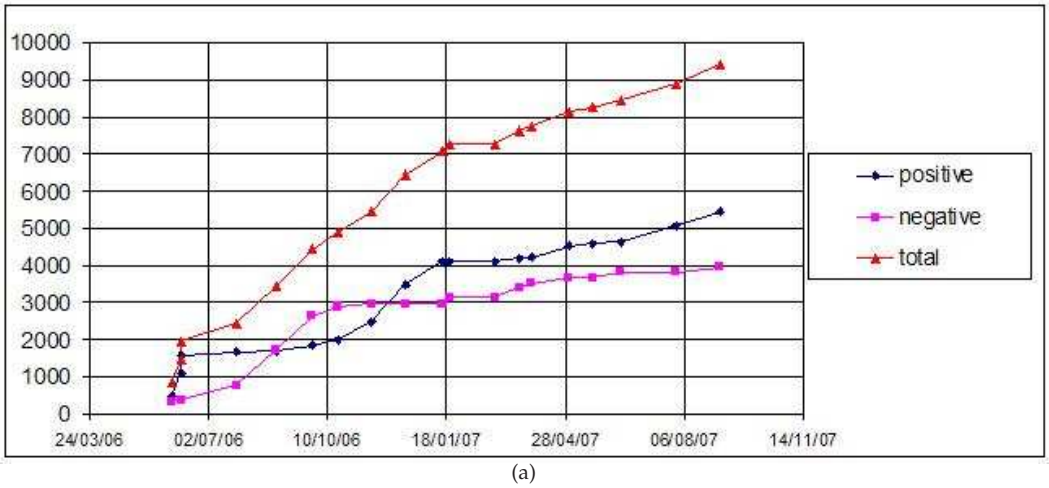
Table 2 Total number of needed boards including spares as in table 1, number of produced boards, number of boards delivered to the laboratories for installation, with the rejected boards subctracted out, and percentage of unrecoverable boards over the total produced. (*)=for the CARDIAC-GEM the last production batch of 100 boards was not included. (**)=the number of delivered and unrecoverable boards is obtained assuming conservatively that a recent batch of 480 boards rejected by the assembling sites are all unrecoverable. The recovery procedure will take place at the beginning of the year 2008.

	total needed	produced	delivered	unrecoverable
CARDIAC(+)	4448	5430	4716(**)	13.1 %(**)
CARDIAC(-)	3492	3969	3558(**)	10.3 %(**)
CARDIAC-GEM	336	332(*)	294(*)	11.4 %

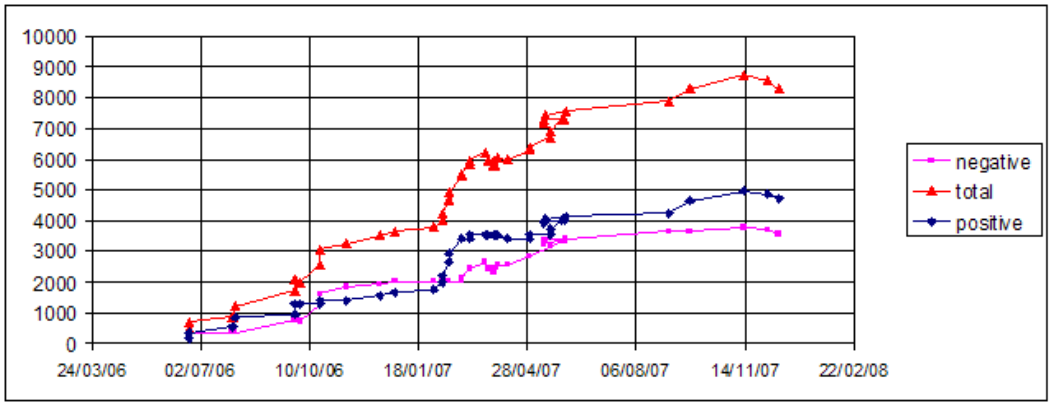
Component placement on the boards was checked by visual inspection with a microscope.
The boards after production were subject to a thermal cycle to spot potential problems due to bad soldering. A thermal run consisted of four cycles inside a climatic chamber [7], each one consisting of four thermal treatments: 20 min at $0\ ^0$, 20 min of linearly rising temperature to $100\ ^0$C, 40 min at $100\ ^0$C and 20 min of linearly falling temperature to $0\ ^0$C .
After that, they underwent a full characterisation with a test bench. Four boards were tested simultaneously for linearity, noise and cross-talk up to 100 fC of imput charge, with detector capacitance, simulated with a variable capacitor, varying from 30 to 150 pF, injecting a step voltage into a 4.5 pF series capacitor on all channels. The bias current was also measured using Hall probes.
Boards were rejected from this test if dead channels or channels shorted together, either in the input or in the output stage, and if a bias current of less than 400 mA, were found. On the contrary, given the wide range of detector capacitances and grounding schemes, it was left to the users to validate the boards in terms of noise.
The rejected boards were visually inspected again and repaired or definitively rejected, depending on the outcome of the inspection. In case the second test failed, the boards were declared unrecoverable. This happened to about 10 % of the boards.
A fraction of the boards was found defective by tests done at installation sites; this included not only boards with noisy channels but also boards with faulty CARIOCA or DIALOG channels, probably due to bad handling of the boards. These boards followed the same path as described above and were repaired or definitively rejected.

7 Production delivery rates

Fig. 7a) shows the production rate vs time of the CARDIAC boards, while Fig. 7b) shows the delivery rate vs time to the end users, after burn-in and testing.
The plots start with an offset since there is pre-production batch of negative boards (350) produced during 2/2006, which is not included in the plot.
After that, as seen from the first plot, the production went rather smoothly with a rate of about 700 boards/month. The delivery rates have sometimes a negative slope in the plot since rejects coming back from the production centers for repair are counted with negative sign.
The CARDIAC-GEM boards were produced almost alogether during the year 2007.
Table 2 shows the total number of needed boards including spares as in table 1, the number of produced boards, the number of boards delivered to the laboratories for installation, with the rejected boards from the laboratories subctracted out, and the percentage of unrecoverable boards over the total produced. The number of delivered and unrecoverable boards is obtained assuming conservatively that a recent batch of 480 boards rejected by the assembling sites are all unrecoverable. The recovery procedure will take place at the beginning of the year 2008.
Altogether the produced CARDIAC and CARDIAC-GEM boards are enough to satisfy all needs. However, to cope with the so called *premature deaths* of chips, some margin is needed. We expect this effect to be small but not completely negligible and it could probably amount to a few per mil.



(a)



(b)

Figure 7 Production rate vs time of the CARDIAC boards(a) and delivery rate vs time to the end users, after burn-in and testing(b).

8 Acknowledgments

We would like to thank A.Cardini and A.Lai of INFN Cagliari, A.Kashchuk of PNPI and M.Newcomer of University of Pennsylvania for the many disucssions and suggestions on board layout issues, G. Corradi of LNF for his invaluable help with the tuning of the soldering process, which made the production at the Eletis Company possible, S.Cadeddu and D.Raspino of INFN Cagliari for the measurements of noise induced by the I2C signal lines, A.Golyatsch of PNPI Institute, Russia, for his deep testing of spark protection circuits during his stay at INFN-Cagliari, G.Paoluzzi e R.Messi of Rome Tor Vergata University for the thermal cycling of all the boards and the many people from the different chamber dressing centers whose tests provided invaluable feedback on the production and quality control at the company.

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[7] At Dipartimento di Fisica, Università di Roma2, Tor Vergata, Via della Ricerca Scientifica 1, Roma, Italy

[8] VISHAY, thin film MELF resistor MMA0204

[9] Baselectron S.R.L. Produzione Circuiti Stampati 27020 Travaco' Siccomario (PV) - 7, VIA EINAUDI

[10] Eletis s.r.l., Via I. Alfonso, Cagliari, Italy

[11] Solder paste:Sn62 RMA FMQM/12A