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LHCb Preshower Front-End Electronics Board

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Abstract

This note describes the digital part of the fully synchronous solution developped for the LHCb preshower detector Front-End electronics. The general design and the main features of this board are given including trigger part.

1 Introduction

The LHCb preshower detector (PS) provides the longitudinal segmentation of the electromagnetic shower detection. It is used to reject the high background of charged pions and is part of the L0 trigger. It is used in conjunction with the ECAL/HCAL to search for clusters of 2×2 cells and to identify e, γ, π^0, hadron of highest E_{T}. The preshower is located immediately upstream from the electromagnetic calorimeter (ECAL), with one-to-one correspondence between ECAL towers and PS cells. It is made of a 15 mm thick lead ($2.5\,\mathrm{X}_0$) followed by a detection plane of 15 mm thick scintillator pads. A description can be found in reference [1]. 6016 cells constitute this plane, it is subdivided into inner, middle and outer sections with approximatively $4{\times}4$, $6{\times}6$ and $12{\times}12$ cm^2 cell dimensions. The scintillation light is collected with helicoidal wavelength shifting fluorescent fiber held in a groove in the scintillator. Both fiber ends are connected to long clear fibers which send the light to photomultiplier tubes (MAPMT) with 64 channels that are located above or below the detector. The main characteristics of the signal at the output of a phototube are described in reference [2] as well as the preshower requested performances.

On average, about 25 photoelectrons in response to a minimum ionising particle (MIP) are provided and about 85 % of the charge is obtained in 25 ns. Furthermore, to avoid MAPMT aging problems [3], MAPMT are operated with very low gain (a few thousand). The HV of a MAPMT is common to all 64 channels and there is a non-adjustable gain dispersion among these channels of up to a factor four. It has therefore been decided to sub-divide the front-end electronics in two parts. The "Very Front End" (*VFE*) part described in reference [4], is placed the closest possible to the MAPMT, on its back. It comprises amplification, integration and holding operation of the signal. As there are very large fluctuations in the signal pulse shape, it is important to integrate the signal over a time as long as possible within the 25 ns limitation. This is performed by alternating two integrators in integration, respectively reset modes. The signal is sampled by track-and-hold circuits and the output of the active integrator is chosen by a multiplexer. A dedicated ASIC has been designed for this purpose with a 10-bit dynamic range. All circuits elements are functioning in differential mode to improve stability and pickup-noise rejection. Four channels per chip are implemented leading to 16 chips per board. The final iteration of the chip has two gains (the larger one being the double of the smaller), the selection between them being made with a mechanical switch (jumper). This allows to compensate the cell to cell gain variation by a factor two.

The analog signal is then sent with twisted-pair cables of 27 meters length to the front end board (*FEB*) located in racks above the detector. Another gain adjustment up to a factor two can be obtained on the *FEB* digitally. Thus the PS electronics is ab compensate up to a factor 4 in gain variation. In this board, the

signal is digitized with a 10-bit ADC and stored in a FIFO pipeline until level 0 trigger decision.

The deposited energy in the preshower is measured for two purposes. First, every 25 ns, a Yes/No signal for the L0 calorimeter trigger system is produced by comparing the measured value to a threshold. Second, the same energy value is used to correct the energy measurements in ECAL. For preserving both the trigger threshold accuracy and the full dynamic range necessary for the energy corrections, a 10 bits digitisation is required for the PS signals. The phototube chosen to detect the light from the PS is a multi anode photomultiplier tube (MAPMT) with 64 channels, leading to 64 channels *FE* electronics for the PS. Some of the MAPMTs (and implicitly *FEB*s) in the central area have only 32 used channels. The ECALhas 32 channels *FE* boards, a PS *FEB* accounting therefore for two ECAL boards.

Another task assured by the PS *FEB* is the reception of 64 bits from the scintillator pad detector (SPD), one per channel, signaling whether a SPD cell has been hit by a charged particle.

This note is an update of the LHCb notes [5] describing the *FE* part of the PS electronic system is. The requirements for the PS *FEB* are the following:

- a synchronization signal is provided to the *VFE*;
- the analog signals from the *VFE* are digitized and processed in order to produce the PS data;
- the PS trigger bits are computed;
- the SPD data are collected;
- the SPD multiplicity is determined;
- it receives at 40 MHz, from ECAL *FEB*s the cell addresses of the trigger candidates;
- it searches through all PS and SPD data the neighbours for all hit cells ;
- PS trigger bits and SPD data are sent synchronously to the calorimeter trigger; validation board;
- the PS and SPD data are stored while waiting for a L0 trigger request, in which case they are sent to the daq .

Each process implemented on the *FEB* is done without any dead time with a fully synchronously pipe-line architecture.

2 General overview

The PS/SPD *FEB*s handle 64 preshower data channels for raw data read-out and trigger purpose, and 64 SPD trigger channels. The raw data dynamic range corresponds to 10 bits, coding energy from 0.1 MIP (1 ADC count) to 100 MIPs. A general overview of the board is given on figure 1. Its general architecture is similar to the ECAL/HCAL boards [9] with five major components:

1. an analog block receiving the 64 analog PS channels from the *VFE* part and digitizing them. Each channel is composed of a fully differential operational amplifier followed by a 10-bit 40 MHz differential ADC.

   A synchronization signal (clock and reset) is sent to the *VFE*.

2. a processing block made of eight identical *FE_PGA*s. Each is in charge of processing eight PS channels. Three corrections are applied : pedestal subtraction, gain adjustment and pile-up correction[1] (named "α" correction) then the 10-bit data are coded into a 8-bit floating format.

   A trigger bit is produced for each channel by applying a threshold on the corrected data. Eight SPD channels are also received. Two PS and SPD channels are packed together, stored and retrieved after L0. Two blocks of memory per two channels are used in each *FE_PGA* for the Level-0 pipeline and derandomiser.

   The processing block is very resource consuming. Since the *VFE* comprises two interleaved integrators working in alternance [4], the gain and offset corrections have to be applied differently for two consecutive events, leading to two "effective" subchannels per physical channel. Also the data inputs — eight channels of 1 SPD bit and eight channels of 10 PS bits— are important. Consequently, the *FE_PGA* chosen was the AX1000 of the ACTEL anti-fuse technology.

3. a trigger block made of one *TRIG_PGA*. It handles the processing for the production of the L0 information. It receives the address of each cell being a local maximum of transverse energy from a ECAL *FEB*. As the ECAL electronics is organized per 32 channel boards, each 64 channel PS/SPD *FEB* is seen by the system as two 32 channel half boards, each receiving its own request address.

   The *TRIG_PGA* is APA450 of the ACTEL ProASIC plus Flash based FPGA family.

[1] About 15% of the signal collected during the 25 ns after a bunch crossing BCID_n arrives during the next 25 ns of BCID_{n+1}. Consequently the measured energy in BCID_{n+1} is corrected for a fraction (denoted α) of the energy measured in BCID_n.

4. a *SEQ_PGA* mainly building the data block after L0-Yes, and sending it to the CROC. It also issues control and synchronisation signals for the other eight *FE_PGA*s, and the *TRIG_PGA*.

5. a SPECS slave called *GLUE_PGA* handling all the I2C communication of the board.

The last two blocks, *SEQ_PGA* and *GLUE_PGA*, are identical to the ones of the ECAL/HCAL *FE* electronics and are described in reference [9]. They are respectively APA300 and APA150 of the ACTEL ProASIC plus Flash based FPGA family.

All registers holding permanent information are radiation protected in static mode by triple voting and during data transfers by hamming.

The schematic of PS and SPD data processing inside a PS/SPD *FEB* is given in Figure 2.

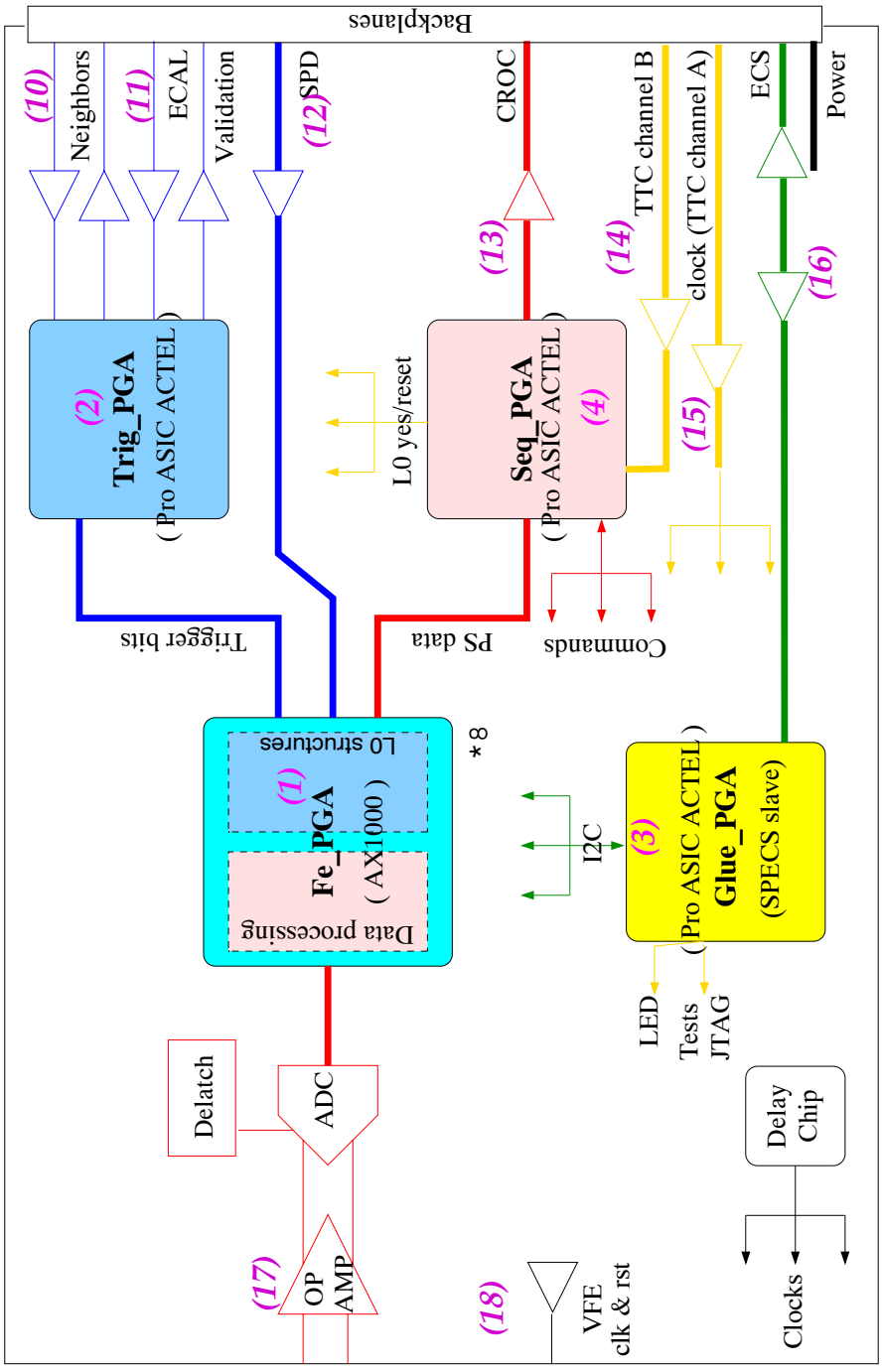

Figure 1: PS *FEB* synopsis.

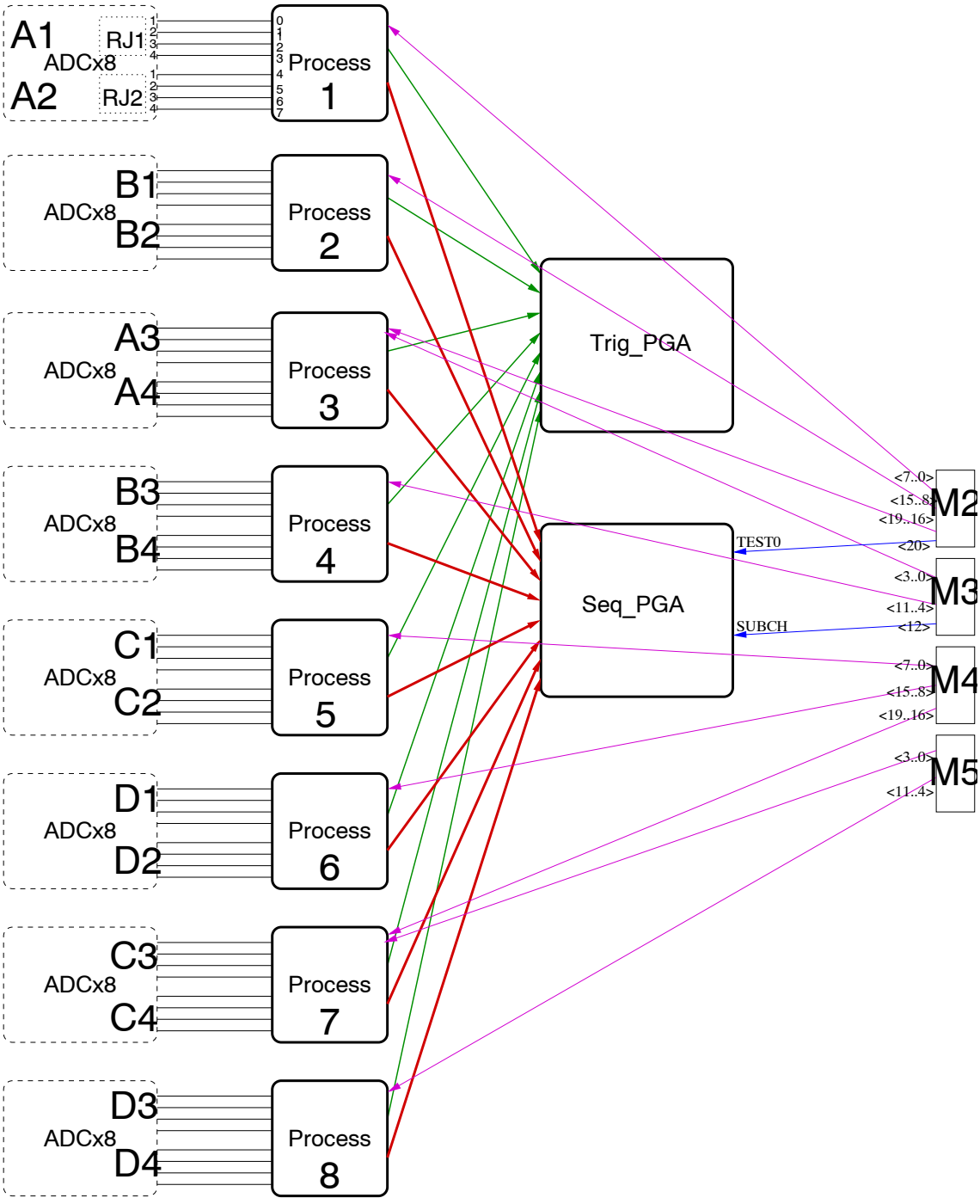

Figure 2: Schematic of PS and SPD data processing inside a PS FE card. **U***i* (U∈{A, B, C, D}; $i \in \{1, 2, 3, 4\}$) is the name of the RJ45/chip PS VFE channel connected to the FE-FGA. **M***i* ($i \in \{1, 2, 3, 4\}$) are the deserialisors for SPD data

3 Analog part

3.1 *VFE* signals reception and ADCs processing

The *VFE* chip output signal is unipolar, with a 2 V amplitude and a common mode voltage of -0.6 volt. We plan to use the AD9203 ADC since it has differential inputs, a small package and is low power consuming (3.3 V, 74 mW) [5]. Its inputs are bipolar with a common mode voltage of +0.5 V.

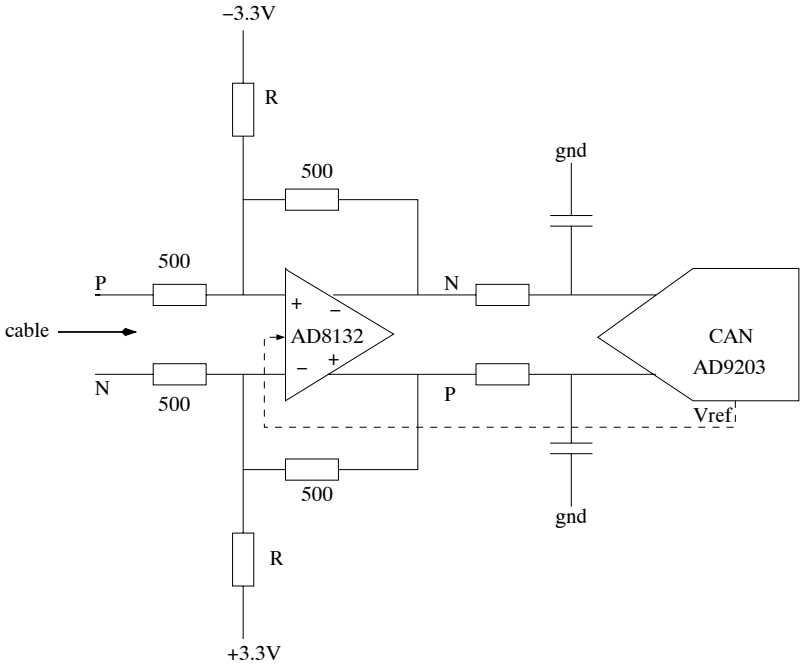

Figure 3: ADC driver

This ADC has been carefully tested, in order to validate its utilisation with an unipolar differential signal shifted by a constant offset without extra noise. A both end cable adaptation with pole zero correction is used to allow the use of simple, cheap Ethernet cable up to 20 m without reflection.

To adapt the cable and the very front-end chip specifications to the AD9203 ADC inputs characteristics the optical amplifier AD8132 is used; it has differential input/output opamp and a separate common mode feedback.

As shown on figure 3 a balanced differential offset is used to shift the dynamic range of the input signal from 1 V to ±0.5 V, and the common mode feedback loop is used to fix the common mode voltage at the AD9203 reference value (+0.5 V), as proposed by the analog device application note. The ADC clock needs a little more care, due to the fact that it is not differential with TTL level. As we do not plan to carry a TTL 40 MHz clock on the 64 channel board, we decided to carry

it with LVDS levels and to convert it channel by channel as near as possible of the ADC's. In addition we take care to reduce the size of a full channel to one centimeter high to avoid the risk of clock digital noise. It should be noticed that this clock is the same for all the 64 channels due to the fact that all the channels of a same board are coming from the same MAPMT.

Under these conditions, a 8-channel prototype has been designed as a hierarchical block of the final front-end board, with a very careful PC board implementation.

The measured noise is about $\sigma = 0.4$ LSB (0.40 mV), as it can be seen in figure 4.

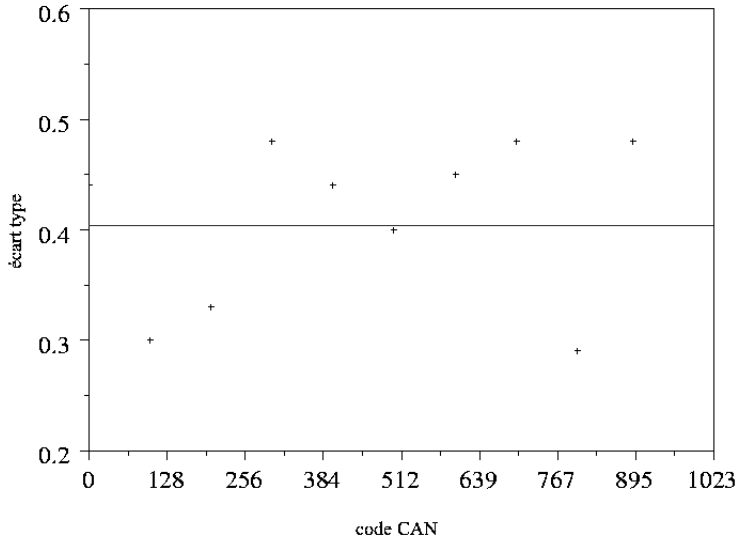

Figure 4: Static ADC noise (σ values) according to output code

The linearity errors are less than ± 2.5 mV along the full dynamic range. Part of these errors are due to the waveform generator characteristics. These results fit well with our requirements including linearity (see figure 5).

3.2 *VFE* synchronisation: clock and reset

The FE board sends two clocks and two resets signals to the VFE board. Each couple clock, reset feed one half of the VFE board. Electrical levels are ECL obtained by conversion of CMOS levels by the use of AD8132 differential amplifiers.

The clocks are generated by a Delay Chip, allowing the start of integration time to be tuned.

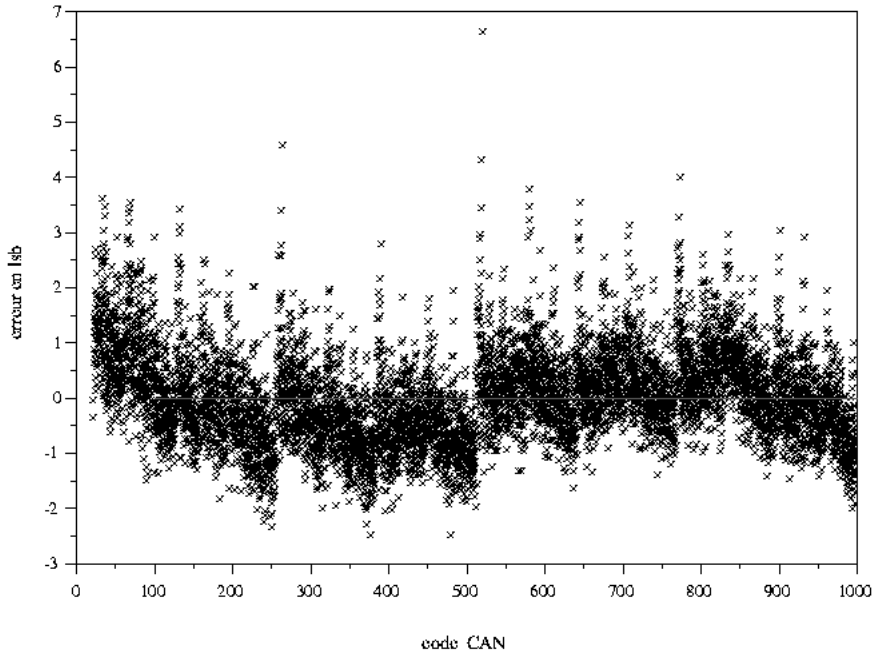

Figure 5: Error in lsb according to the ADC code

The resets are driven by one of the FEpga as the output of the computation of the logical or of the TTC BXID and L0ID resets. Resets signals are asynchronous.

4 FEPGA

As already discussed, after digitisation, several corrections are applied to the signal: electronic offset subtraction, subtraction of the estimated remnant from the previous 25 ns cycle ("α correction"), channel to channel dispersion of the gains. Their meaning and way of implementation are detailed in the following.

Trigger bits are calculated and the data are transcoded on 8 bits, precise enough for energy corrections, in order to gain transmission speed.

The data processing path is summarized in fig 4.

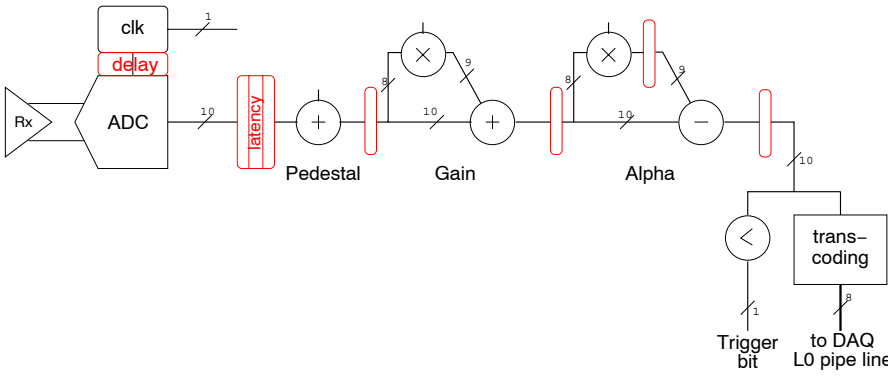

Figure 6: Data processing schematics

4.1 Offset correction

In the PSVFE board, sixteen chips, each handling four channels, perform the signal shaping of the 64 MAPMT outputs. The shaping method uses two interleaved fast integrators, each working at 20 MHz: while one integrates the MAPMT signal during 25 ns, the second is digitally reset. This leads to two different offsets per channel, depending on which integrator was used.

The chips offset was measured on the production chips and found to be on average 33 mV for the low gain and 54 mV for the high gain. Only chips with an offset less than 100 mV on high gain and more than 85 mV on low gain are accepted.

The offset correction in the *FE_PGA*s was therefore coded on 8 bits allowing a pedestal correction up to 255 LSB. A 10×8 subtracter without carry is used, since it is assumed that the offsets will be set such as to avoid any underflows

(underflow being 0). If D is the corrected data and D_r the raw one,

$$D = D_r - \mathit{offset}.$$

4.2 Gain correction

In order to avoid bit losses due to signed operations, the gain is coded as

$$G = 1 + \epsilon, \qquad 0 < \epsilon < 1.$$

For simplicity sake, we suppose that after the VFE correction of the gain dispersion, the lowest gain channel is still the lowest gain one and is assigned a relative gain of 1 in the following.

If the corrected data is D and the raw one D_r,

$$D = D_r + \epsilon \cdot D_r$$

ϵ is a non-signed, 8 bits number. Since it is small, it is not necessary to preserve all the 10 bits precision of D_r for the $\epsilon \cdot D_r$ multiplication. A 8×9 multiplier was chosen and it leads to a maximum error of 1 LSB on D. Precision is better than 1% at full scale. The overflows are assigned to 1023.

4.3 Event overlap correction

α, defined as the fraction between the remnant from the previous 25 ns cycle and the integrated charge in that previous 25 ns sample, was measured in the testbeam campaigns for MIPs and 15 different 12×12 and 4×4 PS cells (see fig. 7) [6]. It can be estimated that for these cell types, α is on average 0.19 and a range of 0 to 0.5 would cover any cell to cell dispersions. For smaller PS cells, α is expected to decrease, as the length of the WLS fibres in the scintillating tile is smaller.

Concerning the variation of the input signal shape with the signal amplitude, the tests performed in the lab and with pions, muons or electron beams, showed that the electronics does not change it over the full dynamical range. To estimate the precise variation of α over the full PS dynamic range (i.e. from 1 to 100 MIPS), fig. 8 shows the deviation of α for 100 MIPS signals from 1 MIP α, at different PMT output currents, or, equivalently, for different MAPMT voltages. As it can be noticed, for a PMT output current of 500 μA, the α drift is at full scale about 5%. Assuming that the linear fit can be extrapolated to the much lower PMT currents foreseen in the LHCb experiment (200 μA at full scale for the channels with the highest gain), the α drift can be estimated to 4%.

To ensure a precision of ~ 1 LSB for the α correction, the α drift at full scale should be known to better than 0.1%, which is practically not possible. However, knowing that the probability to have a cell hit subsequent to a trigger in the same

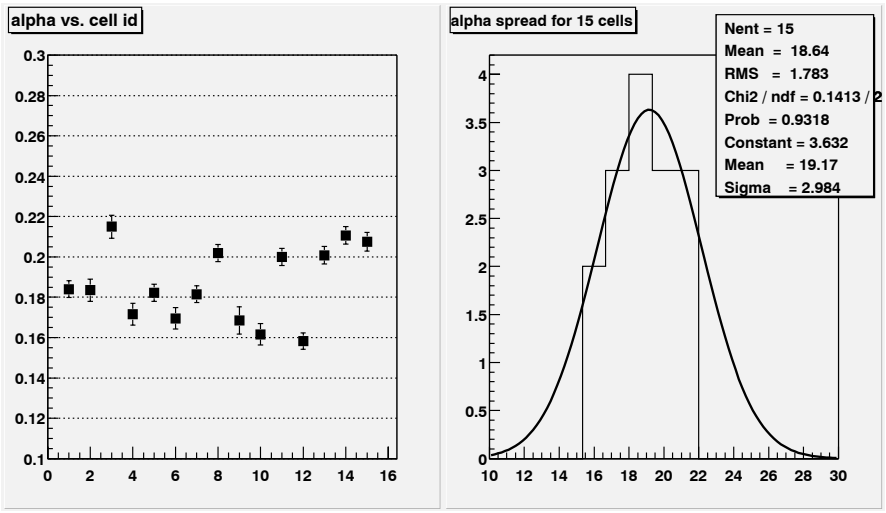

Figure 7: Variation of α from cell to cell, for outer module cells.

cell during the previous 25 ns cycle is rather low (less than 1% at $\mathcal{L} = 2 \cdot 10^{32}$ and less than 2% at $\mathcal{L} = 5 \cdot 10^{32}$, see [7]), it can be concluded that the systematic effect introduced – a possible artificial increase of the trigger rate after a cell saturation – is not significant. It was therefore decided against implementing an energy dependence for α.

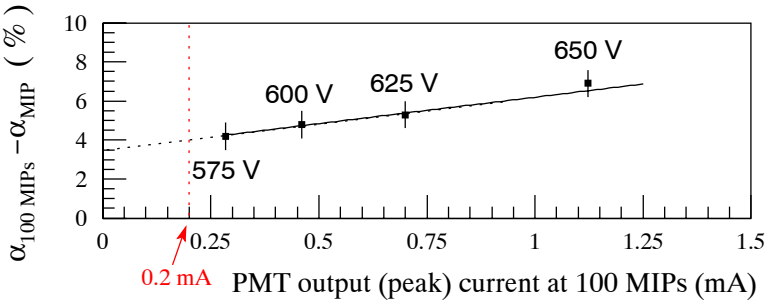

Figure 8: Variation of α with the PMT output current at 100 MIPS.

Implementation

If the corrected data is D and the raw ones in sample n and $n-1$ are D_r^n, respectively D_r^{n-1},

$$D = D_r^n - \alpha \cdot D_r^{n-1}, \qquad \text{with } 0 < \alpha < 0.5.$$

thus α is a non-signed, coded on 8 bits (1/512 LSB accuracy).

The underflows are detected in the case of $D_r^{n-1} >> D_r^n$ and D is then set to 0.

4.4 Trigger bit calculation and SPD data collection.

After calibration and α subtraction, the trigger bits are computed by comparing with predefined, 8 bits trigger thresholds. Noisy or defective channels for either PS or SPD are masked using a programmable 8 bits channel mask.

4.5 Data transcoding

The last operation performed is the transcoding of the 10 bits data to 8 bits, according to the algorithm described in table 1. Conversely, the 8-bit DAQ data have to be corrected in order to retrieve the original values according to table 2

	$d_{10} \leq 128$	$128 \leq d_{10} \leq 256$	$256 \leq d_{10} \leq 512$	$512 \leq d_{10}$
d_8	d_{10}	$128 + \frac{d_{10}-128}{2}$	$192 + \frac{d_{10}-256}{8}$	$224 + \frac{d_{10}-512}{16}$

Table 1: The trancoding algorithm depends on the signal value, in order to ensure constant relative precision over the full data range. d_{10} is the 10-bits original data value, whereas the d_8 is the transcoded value.

	$d_8 \leq 128$	$128 \leq d_{10} \leq 192$	$192 \leq d_{10} \leq 224$	$512 \leq d_{10}$
d_{10}	d_8	$2 \cdot d_8 - 126$	$8 \cdot d_8 - 1276$	$16 \cdot d_8 - 3064$

Table 2: Inverse transcoding algorithm

4.6 Data transmission to the SEQPGA - L0Seq block

Two 128 depth pipelines, for the PS and respectively SPD data are available for their synchronisation. The pipelines are automatically bypassed if their virtual depth is set by ECS to 0. The SPD bits and the PS trigger bits are subsequently added to the 8 bits PS data. At this point, the data path is send to the L0SEQ functional block (see figure 10) and mirrored toward a spy RAM described in section 4.9.

In the L0SEQ block, the 8 channels PS/SPD data are serialised into 4×20 bits with the format described in figure 9 and send to the *SEQ_PGA*, which stores the data and transmits them to the CROC if L0 request.

The synchronisation of the PS data with the L0 signal is obtained with a 256-depth pipeline, controlled by a programmable parameter.

Considering the *FE_PGA* s of the board numbered as in figure 2, the format of the data sent to the CROC by the *SEQ_PGA* is the following:

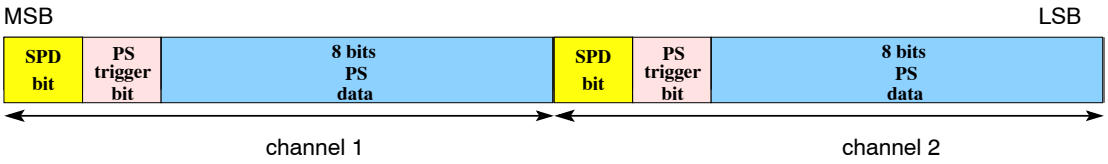

Figure 9: Ps — SPD data format.

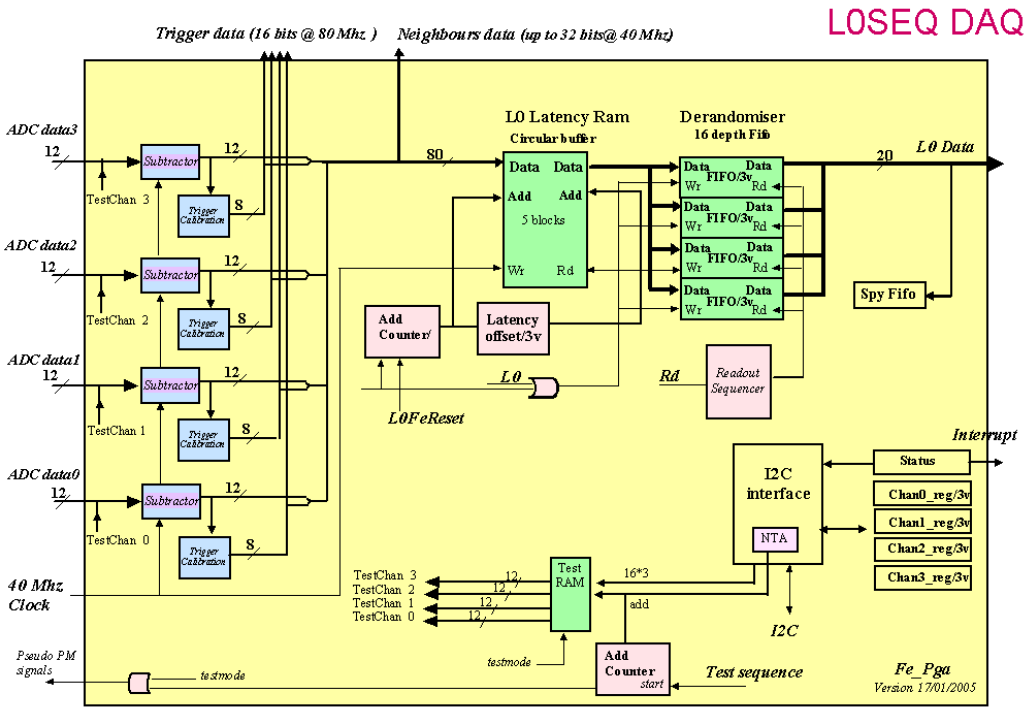

Figure 10: Block diagram for L0SEQ.

(FE[7]ch[0] ... FE[0]ch[0]) ... ... (FE[7]ch[7] ... FE[0]ch[7])

4.7 Channel mapping

Two channel mappings, imposed by Tell1 requirements, are implemented in the *FE_PGA* for the top and bottom configuration, according to the schemes defined in [8]. A programmable parameter allows the switch between the two schemes. The channel correspondence is given in table 3.

VFE channel (FE input channel)	0	1	2	3	4	5	6	7
FE output channel, top configuration	1	5	7	3	0	4	6	2
FE output channel, bottom configuration	6	2	0	4	7	3	1	5

Table 3: VFE-FE channel mapping

4.8 Injection RAM

Alternately to the ADCs output, digital data can be injected using an injection RAM, with a programmable depth up to 256. The injection RAM can be operated in synchronised mode, when the injection is started either by the L0 or the testsequence signals or non-synchronised mode, when the injection starts randomly. In both functioning modes, the charged data can be injected either in burst mode, ie with the (40 MHz) PS *FEB* ground clock frequency or with a frequency defined by the external L0 signals. In synchronised mode, the injection is unique, up to the last event charged in the INJRAM, whereas in non synchronised mode, the injection can also be continuous, in an infinite loop over the INJRAM addresses.

The synchronised mode of the INJRAM, both in burst mode or with an imposed external frequency, is going to be used extensively in the comissioning phase, for synchronising the different calorimeter subdetectors electronics, since the SPD *VFE* , the PS *FEB* and the ECAL can be triggered by a commun external signal and the commonly defined patterns retreived either in the DAQ or trigger pathes. It is also the most used configuration for inter-*FEB*s communication tests. The non synchronised mode is mainly used for the *FEB*s individual testing.

4.9 Acquisition (spy) RAMs

The board has a double acquisition, both through the L0SEQ block or through ECS using an acquisition (spy) RAM. It can be operated in burst mode (acquisition of 256 succesive patterns) or with a trigger signal frequency. The trigger signal (either L0 or testsequence signal) can be shaped using the leading edge or in gate mode.

5 The Trigger Path

As previously written in the introductory section, the FE board handles 64 PS and SPD data for both the general read-out of the experiment (DAQ path) and the level 0 trigger of the experiment. In the latter case, the elementary object is a trigger bit for each PS channel; it is computed in the FEPGA by comparing the ADC value to a given threshold aimed at selecting electron and photon responses in the detector. Though the value of the threshold is not frozen yet, the typical relevant cut lies in the range from 5 to 15 MIPs [5]. It has to be noticed that the comparison to the threshold is performed before the transcoding of the ADC data from 10 bits to 8 bits. Correspondingly, a trigger bit for the projective SPD channel, computed in the SPD VFE board, is transmitted to the FEPGA.

In order to build the calorimeter L0 information, all the sub-detectors responses must be combined. The overall procedure is described in [9]. The Figure 11 displays the overall scheme and the links between the subdetectors electronics.

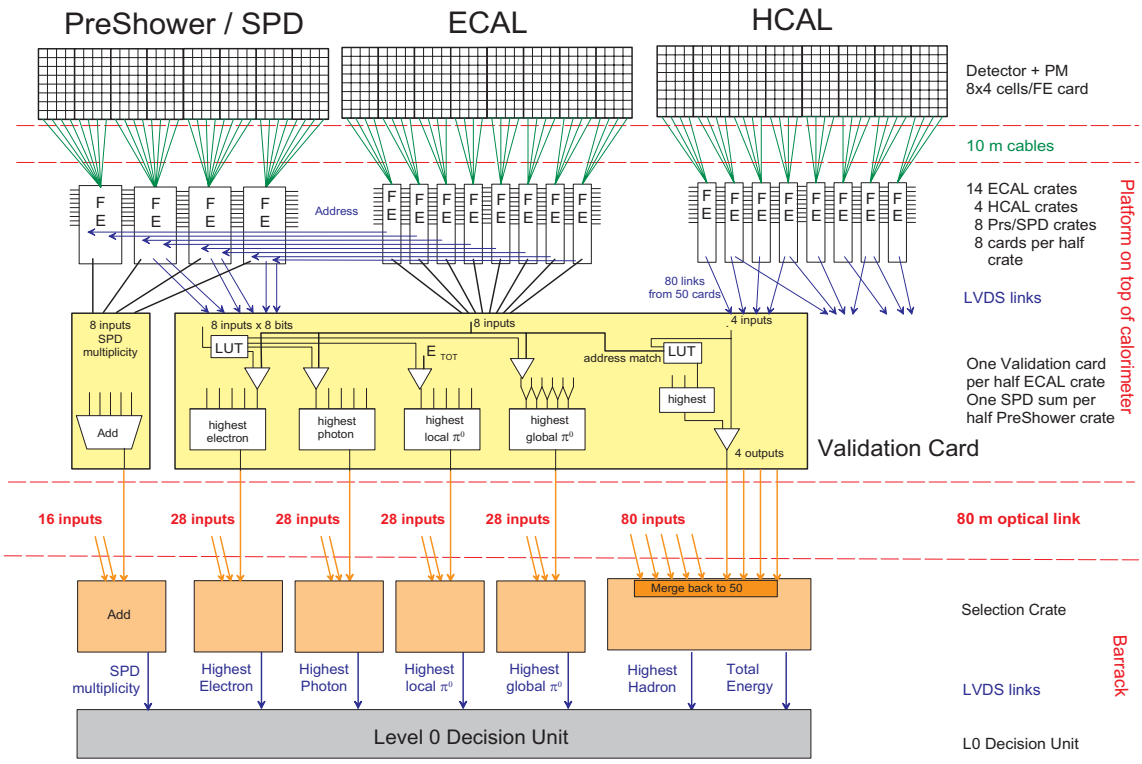

Figure 11: Overall view of the trigger calorimeter system.

Let's precise here the sequence of the operations relevant for the PS FE Board. The PS FE Board is seen by the trigger system as a 2×32 channels (*i.e* half boards, each receiving its own ECAL information. The maximum ECAL cell

response is searched for in each block of 32 channels (corresponding to one ECAL FE Board). Then, the ECAL address thus determined is sent to the corresponding PS FE Board and the trigger bits of the two corresponding PS and SPD cells are sent to the validation board as well as their neighbour cells in order to categorize the nature (electromagnetic or not) of the ECAL cluster. At the border of the 32 blocks, the neighbour cells belong to another board. As a consequence the PS FE Board receives also the information of other FE cards and reciprocally sends the border trigger bits to its neighbour card. The combination of the calorimeter trigger information is performed within the validation board. Let us notice that few PS FE Boards receive only 32 channels.

In addition to the largest transverse energy clusters, the calorimeter trigger information provides the hit multiplicity within the SPD detector. This multiplicity is computed within each PS FE board from the trigger bits determined in the SPD VFE board. The addition of the 64 trigger bits is sent to a dedicated board (SPD Multiplicity Board) in charge of summing the results of all the 64-channels blocks.

All these functionalities are implemented into a re-programmable PGA product from ACTEL (APA 450).

This section of the note will describe in details :

- the inputs and the outputs of the TRIG-PGA,
- the TRIG-PGA algorithms,
- the internal test facilities, control registers,injection RAMs etc...

5.1 Inputs and Outputs of the TRIG-PGA

It is first necessary to give the definitions related to how the one hundred boards are grouped and mapped in the electronics racks.

Each PS FE Board receives 64 bits of SPD data (1 bit per channel) from the backplane. In order to simplify the connectivity, there is a one-to-one correspondence of the channels between a SPD VFE Board and PS FE Board.

Two ECAL FE Boards are connected to one PS FE Board. The PS Board is therefore divided, from the trigger point of view, into two half Boards of 32 cells (8×4 cluster). One PS half FE Board corresponds to one ECAL FE Board.

Each ECAL FE Board is sending to the corresponding PS half FE Board the BCID and the address (coded with 5 bits) which identifies the ECAL channel with the maximal transverse energy out of the 32 channels of a board. It actually figures a 2×2 cluster as represented in Figure 12. The (x,y) coordinates are the transverse coordinates of the usual frame of the LHCb experiment.

Then the PS FE Board must send to the appropriate ecal validation board the trigger data of the addressed cell and of three of its neighbours, according to the

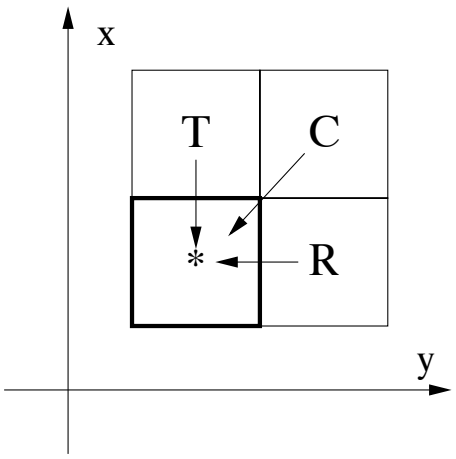

Figure 12: How a Region Of Interest (ROI) cluster is defined.

definition given in Figure 12. The same information is transmitted for PS and SPD, resulting in sending 8 bits for each ECAL address.

When a cell at the border of a card is involved, the Region Of Interest (ROI) cluster produced by the TRIG-PGA requires the information of other PS FE Boards (can be three at maximum when a corner cell is considered).

Because of the granularity change in the detector, the neighbours from a different region of the detector cannot be defined and are consequently set to '0'. This is also the case for the empty channels of a partially instrumented FE Board (outer and central regions).

The Figure 13 summarizes the relationship (mapping) between the detector and the FE electronics and shows how the boards are plugged into the crates. Each square (left part) corresponds to one Multi-anode Photomultiplier and hence one 64 channels FE Board.

The Figures 14 and 15 show the way the PS FE board is receiving the information from its neighbours and the way the cells are addressed, respectively.

Correlatively, each PS FE Board, when it's tagged *Right* or *Top*, must send its information by the backplane or by cables, respectively.

There are two other outputs for each FE Board, previously evoked in the introduction of the section. Firstly, the result of the search for the three neighbours must be sent to the adequate ECAL validation board. This is realised thanks to a dedicated point to point bus on the backplane (serial LVDS). Secondly, the SPD multiplicity computation (7 bits) is sent to the SPD control Board, through a point to point bus on the backplane, analogously to the neighbours.

The Figure 16 shows the internal architecture Cs the trigger chip and displays its inputs and outputs.

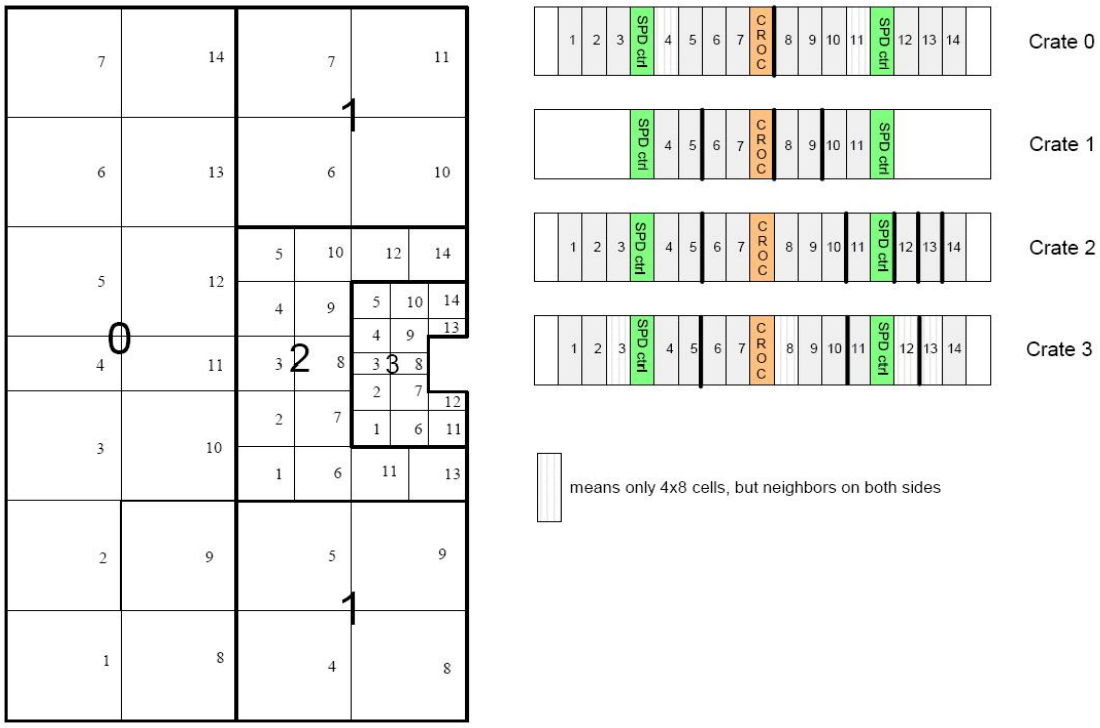

Figure 13: Sketch of one half of the detector displaying the inner, middle and outer regions of the PS. Each square corresponds to one Ma-PMT, i.e 64 detector channels. Four Boards in the inner region (quoted 4) are half boards (32 channels), two in the outer region of the detector. Also shown is the way the Boards are plugged in the crates.

5.2 Description of the algorithms

5.2.1 Search for the neighbours

The algorithm of the search for the 2×2 ROI was implicitly exposed throughout the lines of the previous subsection. Let's make clear in the following how it's practically implemented and the details of the different mappings of interest according to the bottom and top regions of the detector implied. There are actually two mappings of the detector, for the top and bottom part, respectively. They are displayed in figures 17 and 18. In addition, two other geometries must be taken into account for the half-instrumented boards.

As an illustration, the Figure 19 shows the PS cell corresponding to the ECAL address received by the board. In this configuration, the ROI is not strictly belonging to FE Board itself. A typical answer, according to the right part of Figure 19, will then be 00010001 if only the corresponding SPD and PS channels

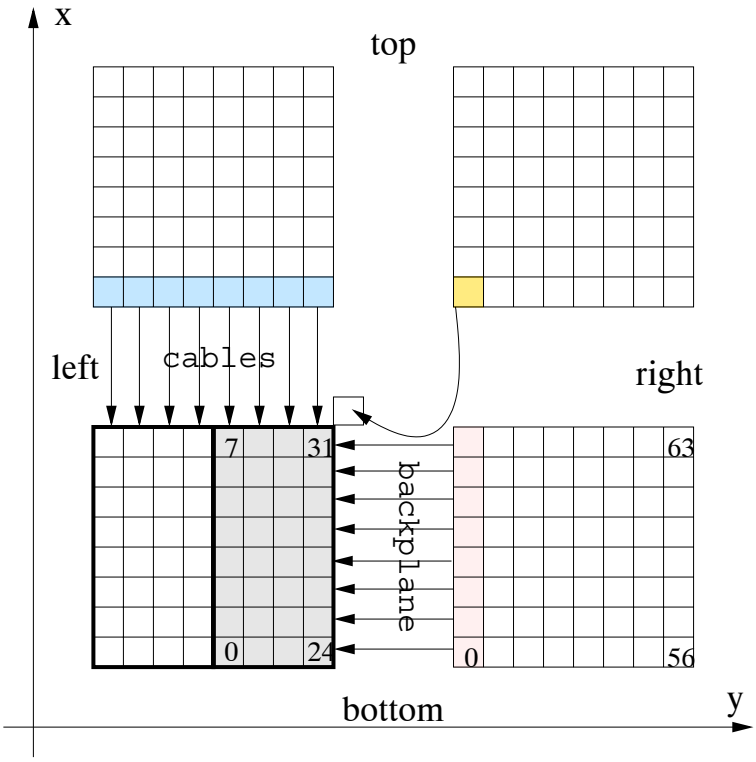

Figure 14: Relationships between all the boards potentially involved in the search for neighbours. The *Corner* information is transmitted to the *Right* Board through a cable, then sent to the *Left* Board through the backplane.

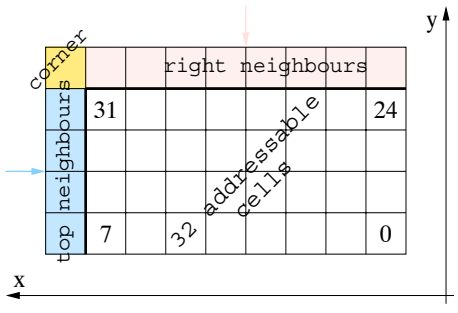

Figure 15: Definition of the addressable electronics channels within an half Board. One row corresponds to 1 FEPGA.

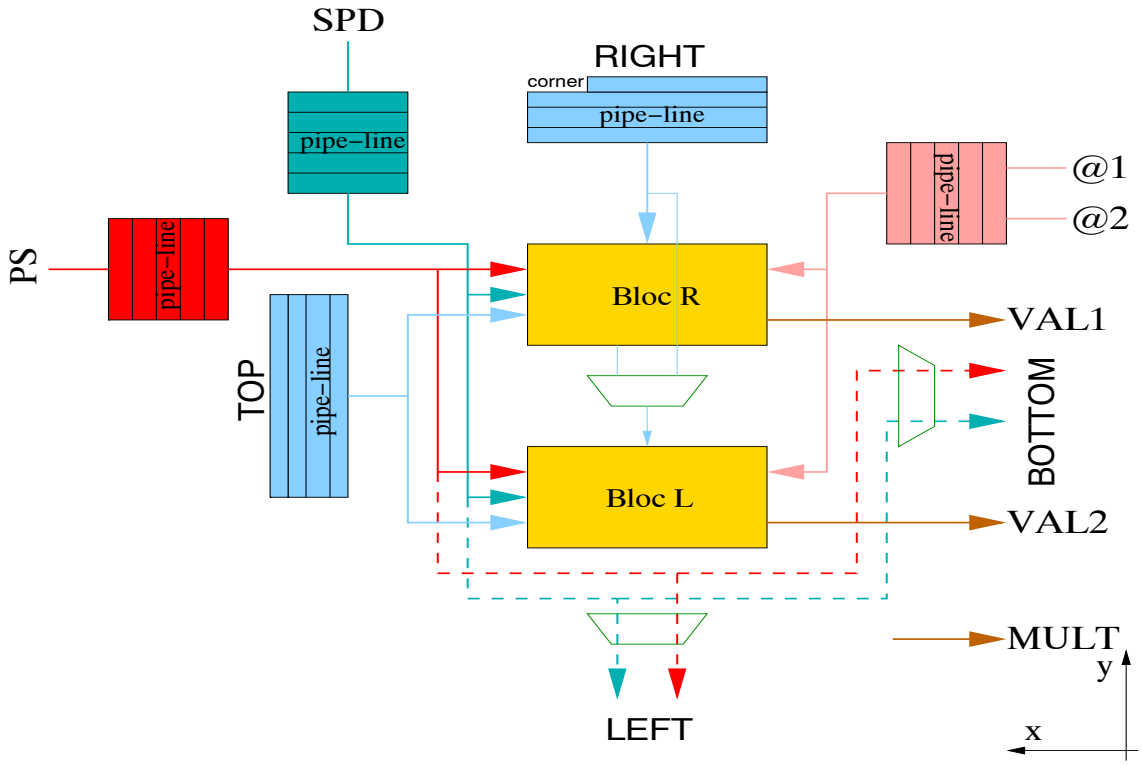

Figure 16: Internal architecture of the TRI-PGA. Are omitted in this sketch the memories for pattern injection dedicated to internally test the device.

were triggered. The initial ECAL address is also returned to the ECAL validation Board.

5.2.2 SPD Multiplicity

The SPD multiplicity computation solely consists in counting the number of bits set to "1" within the 64 SPD data transmitted from the SPD VFE Board to the PS FE Board. A number between 0 and 64 included (one word of 7 bits per FE Board) is then returned to the corresponding SPD control Board by means of a point to point bus on the backplane. A simple adder tree is providing the result. In order to reduce the size of the tree,

the data are partially processed before. In details, for each set of 4 bits, a combinatorial logic

function provides the number of bits set to "1" (3 bits). The associated electronics is synchronous and pipe-lined and the process takes one clock cycle.

A versatility of the system consists in the possibility of masking SPD trigger bits, (*i.e* setting their values to 0. As for the PS trigger bits, it might be useful, in the experiment operation, when a dysfunctional detector channel returns always a signal. It's useful also for the internal tests of the electronics device.

6 Trigger configuration

Analogously to the FEPGA, the TrigPGA (APA450) is configured by the set of control registers described in the appendix. Algorithms, injection of patterns, spy acquisition and synchronization functionalities are described in this part.

6.1 Algorithm modes

For each PS FE board, it is possible to set the mapping type (Top or Bottom) and to set the half-card configuration. For this latter case, only the neighbours transmission is modified to take into account the four instrumented FePGAs. In addition, some debug tools allow to take or not into account the Top and Right neighbours.

6.2 Injection and acquisition RAM

All input data can be injected by an injection RAM (52 bit length , 256 bit depth), divided in two parts : one for the ECAL addresses and BCID [1], the other for the Right and Bottom neighbour cells. Both can be injected independently. The depth of this RAM can be adjusted (*injdepth* register) and the injection can be continuous by looping the injection RAM. Therefore, for the purposes of commissioning or qualification tests, it is possible to emulate a missing board in front of

the PS FE board. As far as PS and SPD trigger bits are concerned, the injection is realised from FePGAs. However, there exists the possibility within the TrigPGA to all the SPD and PS trigger bits to 1.

The acquisition (80 bit length, 256 bit depth) allows to check the inputs and the outputs of the algorithm processing. According to bypass mode, PS and SPD data can be displayed. This mode is useful for checking the connectivity between FePGAs and TrigPGA. As the trigger bits are acquired after the mapping process, the mapping conformity can be checked. The other entries (ECAL and neighbours) allows to test the integration of the devices plugged to TrigPGA inputs. If the process is not bypassed, the acquisition RAM can contain all results of the trigger algorithms : the neighbours result corresponding to the two ECAL addresses, the ECAL addresses themselves, the SPD multiplicity computation and the local PS BCID.

Contrarily to the FePGAs implementation, injection and acquisition RAM counters cannot be displayed from the ECS.

6.3 Synchronization options

The TrigPGA has exactly the same injection and acquisition modes as FePGAs : injection/acquisition running at the frequency of a trigger signal, injection/acquisition at the PS clock and started with a trigger signal, etc. (see the corresponding section of the FePGAs part)

A pipe-line register is set for each input data of the TrigPGA. This feature is mandatory to synchronize all the companion calorimeter electronics Boards. The ECAL supervisor must guarantee that the alignment of the both ECAL board data is correct. Similarly, the data time alignment between PS and SPD is performed at the level of the FePGAs. The maximum latencies produced by these pipe-line registers are the following :

- PS-SPD trigger bits : 3 to 9 clock counts
- Top neighbours : 3 to 5 clock counts
- Right neighbours : 3 to 9 clock counts
- the both ECAL : 3 to 258 clock counts

[1]In order to minimize the resources in the device, ECAL1 BCID is equal to ECAL2 BCID in the TrigPGA injection RAM

In order to check online the time alignment between ECAL and PS-SPD data, the local BCIDs of theses boards have to be the same. Preshower trigger system supplies the difference between the PS BCID and the ECAL BCIDs (*deltaBXecal1* and *deltaBXecal2* registers). To adjust the PS BCID, the initial BCID value, loaded at each BCID reset signal, can be changed by the *BXlocalOFFSET* register. All these functionalities have been checked to work properly.

DETECTOR

A	8	7	6	5	4	3	2	1 C
	16	15	14	13	12	11	10	9
	24	23	22	21	20	19	18	17
	32	31	30	29	28	27	26	25
D	40	39	38	37	36	35	34	33 B
	48	47	46	45	44	43	42	41
	56	55	54	53	52	51	50	49
	64	63	62	61	60	59	58	57

VFE

A	8	24	7	23	6	22	5	21
	30	14	29	13	32	16	31	15
B	36	52	35	51	34	50	33	49
	58	42	57	41	60	44	59	43
C	4	20	3	19	2	18	1	17
	26	10	25	9	28	12	27	11
D	40	56	39	55	38	54	37	53
	62	46	61	45	64	48	63	47

Figure 17: Relationships table between the detector and VFE channels for the top part of the detector.

DETECTOR

A	57	58	59	60	61	62	63	64 C
	49	50	51	52	53	54	55	56
	41	42	43	44	45	46	47	48
	33	34	35	36	37	38	39	40
D	25	26	27	28	29	30	31	32 B
	17	18	19	20	21	22	23	24
	9	10	11	12	13	14	15	16
	1	2	3	4	5	6	7	8

VFE

A	57	41	58	42	59	43	60	44
	35	51	36	52	33	49	34	50
B	29	13	30	14	31	15	32	16
	7	23	8	24	5	21	6	22
C	61	45	62	46	63	47	64	48
	39	55	40	56	37	53	38	54
D	25	9	26	10	27	11	28	12
	3	19	4	20	1	17	2	18

Figure 18: Relationships table between the detector and VFE channels for the bottom part of the detector.

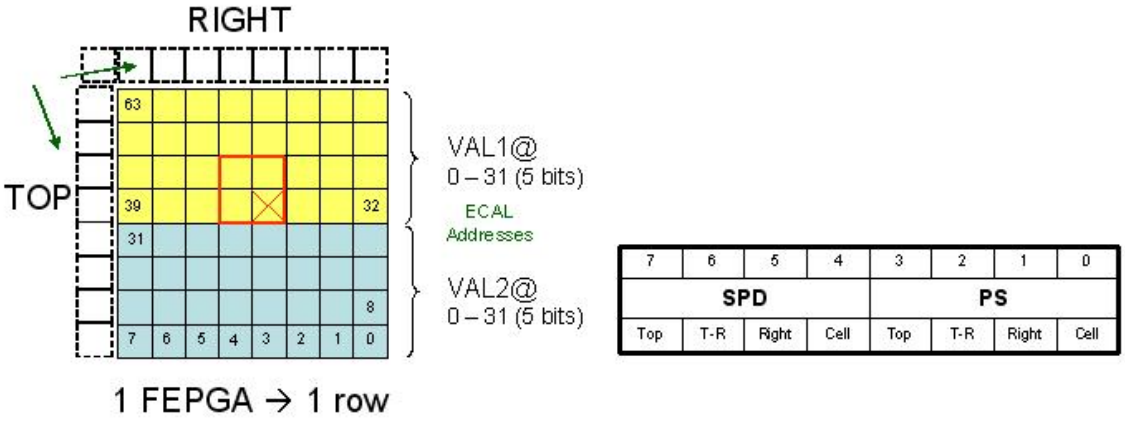

Figure 19: Left : The ECAL addresses received by the PS FE Board as well as the neighbour trigger bits. Right: the generic result of the search for the ROI.

7 Place and Route results(current versions)

To obtain the best results after place and route design steps the designs have been constrained as follow :

- 25% more performances asked on the 40 MHz clock ;
- relaxed constraints on SCL clock ;
- false path specifications to ease the place and route process.

The pin out was forced by the pcb design (no bus crossing, etc...) and can be considered as an overconstaint of the design. Both best and worst case timing reports have been checked in addition to HDL simulations (back-annotated or not). HDL simulations were performed at system level (i.e. at the chip level) includinf ECS, data flow and test structures within the same simulation (complementary other partial simulations have also been done).

7.1 Fepga

Constraint	Value	Results
Global clock	50 MHz	57 MHz (Worst case)
Global clock		slack : 230 ps (Best case)
SCL	25 MHz	62 MHz (Worst case)
SCL		slack : 330 ps (Best case)

Table 4: Timing report for FEpga

The table 4 sums up the timing results of FEpga. The maximum frequency margin is large enough. Tacking into account the clock tree delays, the slack is positive in the best case ensuring no hold time violations.

Resource	Results
Core cells	53%
RAM	70%
IOs	50%

Table 5: FEpga resource usage

Constraint	Value	Results
Global clock	50 MHz	52 MHz (Worst case)
Global clock		slack : 55 ps (Best case)
SCL	25 MHz	180 MHz (Worst case)
SCL		slack : 340 ps (Best case)

Table 6: Timing report for TRIGpga

7.2 TRIGpga

The table 6 sums up the timing results of FEpga. The maximum frequency margin is large enough. Tacking into account the clock tree delays, the slack is positive in the best case.

In addition to the global clock tree, 3 other local clock trees have been defined to route scl and clocks handling data from deserialisers. It ensure a minimum skew on the clock propagation delays.

Resource	Results
Core cells	38%
RAM	69%
IOs	90%

Table 7: TRIGpga resource usage

As shown in table 7, many core cells remain free inside TRIGpga. Nevertheless the number of internal net is critical for the routing steps : 5% more nets added to the design can lower the maximum frequency by 20% and make the place and route process results unpredictable. Special care is taken not to add too much net when design modification occurs.

8 ECS

ECS access to the board is given by the crate controler (CROC) connected to a SPECS slave on the PS *FEB*, called *GLUE_PGA*. Both the CROC and the *GLUE_PGA* are designed at LAL. The *GLUE_PGA* delivers 16 I2C buses, fourteen of which are individually used on the PS *FEB* for each of the eight *FE_PGA*s, *TRIG_PGA* and *SEQ_PGA* and four delay chips. This way, each component receives a dedicated I2C bus with no other component connected on it.

I2C addresses are then used as internal addresses for register banks or RAM access (in the case of the *FE_PGA*s and of the *TRIG_PGA*). As detailed in

appendices A and B, the *FE_PGA*s and of the *TRIG_PGA* react to four differents I2C addresses defining four internal channels. Each channel is internally associated to registers or the RAMs. The registers can not be accessed individually but within a whole I2C frame. Registers are written or read according to the data byte number, with an internal triple voting counter. The frame can then be partial, registers correponding to unsent bytes being simply not accessed. RAM access is done with autoincrement of the RAM address counter when the necessary number of bytes was received. An ECS access mode of the RAM is automatically set/unset when appropriate conditions are fulffiled, in case of troubles this can be done through ECS on a different channel.

9 Clock Distribution

9.1 Clock signals

The whole board electronics is synchronous and then clocked by an unique LHC frequency clock distributed through the crate backplane from the crate controller (CROC) in an isochronous way such as at the input of each FEB all the root clocks have the same phase.

Many external systems send data to the FEB. The incoming data are not supposed to be phase aligned with the FEB root clock as particles time of flight, cable length, TTC distribution, SER/DES chipsets etc, will affect the incoming data phase.

Thus the incoming data must be phase aligned to the FEB root clock to avoid sampling error or metastable states (t_{su} and t_h constraints). Consequently local phased 40 MHz clocks have to be generated on the FEB. Local phased clock are produced thanks to Delay Chips designed by LAL allowing the phase to range from 0 to 24 ns by 1 ns steps. With the same clock input a Delay Chips generates 4 independent phased clock channels allowing also their use as clock fanning circuits for some branches of the clock distribution tree on the board.

On the FEB, the clock tree is also based on multidrop LVDS signaling. Electrical levels are converted from differential CMOS to LVDS close to de Delay Chips outputs and from LVDS to LVTTL close to the FEB components clock inputs.

9.2 Clock domains

One clock domain is considered for each data input corresponding to a distant system (i.e. not in the same crate). Data coming from a board hosted into the same crate is clocked directly by the root clock, input and output registers are supposed to be implemented into the relevant components (PGAs) trying to minimize buffers propagation delay (typically 4 to 5 ns with high slew rate,

pad register mapping and highest output buffer current options enabled for an AXCELERATOR PGA).

9.2.1 VFE and ADC clock domains

Following a collision, the VFE electronics integrates the PMT signals by 25 ns time slices. The clock controlling the start of integration time is generated on the FEB and sent directly to the VFE electronics with a phase ϕ_{VFE}. This is implemented using 2 delay chip channels generating two clocks ϕ_{VFE1} and ϕ_{VFE2} each feeding an half VFE board. ϕ_{VFE1} and ϕ_{VFE2} should be identical (see fig 9.2.1).

Finally the VFE signals are sampled by the 64 ADCs on the FEB. The ADC clock has a phase ϕ_{ADC}. The falling edge samples the analogue data while the rising edge is used to refresh the ADC digital output. This is implemented using a full delay chip which delivers ϕ_{ADC1}, ϕ_{ADC2}, ϕ_{ADC3} and ϕ_{ADC4}. These 4 phases should be the same and each feeds 16 ADCs through multidrop LVDS fan-out tree.

Digital signals are sent to 8 PGAs (*FE_PGA*) where they are sampled a very first time with a clock phase ϕ_{FEADC} and then a second time with the FEB root clock. After this double layer register the detector data are fully synchronous with the FEB root clock domain. ϕ_{FEADC} is implemented using a single delay chip channel and a multidrop LVDS fan out tree to feed 8 FE_PGAs.

It is not necessary to set the value of ϕ_{FEADC} very precisely as it is used to sample digital data stable for at least 19 ns. This dedicated clock could have been replaced by the selection of the sampling edge of the root clock. In fact by using the appropriate settings of ϕ_{FEADC} these two ways are equivalent. Obviously ϕ_{FEADC} must be set to match setup and hold time requirement of the second register clocked by the root clock.

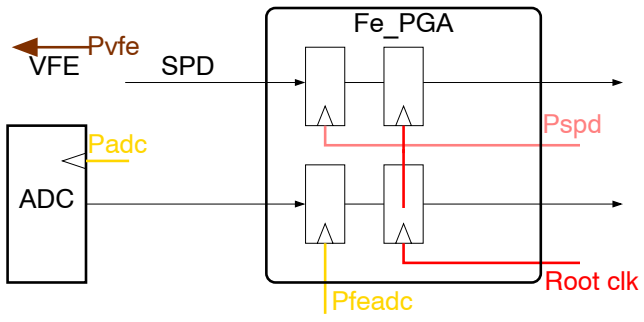

Figure 20: VFE anf ADC clock domain.

9.2.2 SPD clock domain

SPD digital signals (64 bits) are received by 3 LVDS deserializer (DS90CR216). Deserialized data are sent to FE_PGAs (8 bits per FE_PGA) where they are sampled with a phase ϕ_{SPD} (see figure 9.2.2). The same double register technique is used as for ADC data. The output clock signal delivered by the deserializer is also sampled by ϕ_{SPD} . The sampled value should always be the same, in this case it indicates that ϕ_{SPD} is set correctly. ϕ_{SPD} is implemented using a single delay chip channel and a multidrop LVDS fan out tree to feed 8 FE_PGAs.

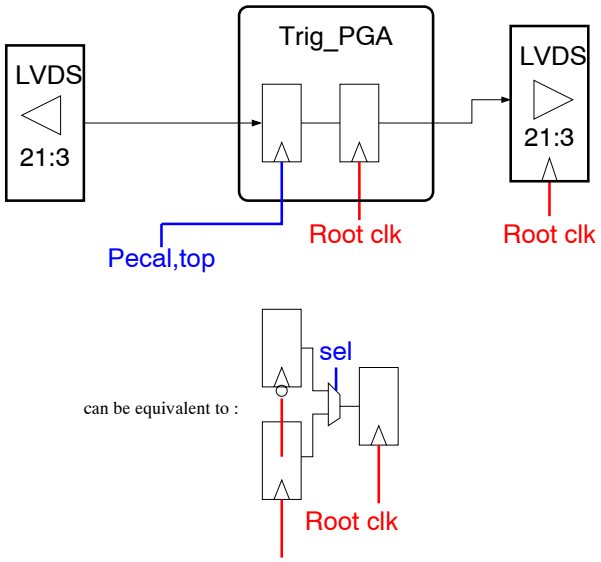

Figure 21: SPD clock domain

9.2.3 ECAL1 and ECAL2 clock domain

The same implementation is used for data sent by two ECAL FEB but with ϕ_{ECAL1} and ϕ_{ECAL2} (one delay chip channel each). ECAL data are sampled into the TRIG_PGA used for trigger algorithm.

9.2.4 PS (top neighbours) clock domain

Idem as for ECAL but with ϕ_{PS} . PS top neighbours are sent by TRIG_PGA on a first FEB and received by another TRIG_PGA on a second FEB thanks to DS90CR215/6 SER/DES chipset.

9.2.5 Output data clock domain

As said before every data output is controlled by the root clock (internal registers of PGA or serializers). A general schematics of the clock tree is presented in figure 9.2.5.

10 Radiation tolerance

10.1 Radiation tests

Most of components are common to ECAL/HCAL *FEB*s and have been qualified against SEU or SEL to be used in LHCb environment [10]. The specific components of the PS *FEB*, the ADC AD9203 and the operational amplifier AD8132, have also been tested at GANIL with Krypton beam [11].

The tested components are all qualified for what concerns cumulative effects: their consumptions and functionalities were found to be nominal after the irradiations. For what concerns SEL, the obtained limits are relatively good. SEL were observed only for the analogue part of the ADC. This corresponds to less than 10 SEL per year at 95% confidence level. They will be used in LHCb and to prevent any burn-out problem, the analogue part will be alimented through delatchers.

10.2 Radiation protection with delatchers

In case of SEL a current path is created through the integrated circuit (IC) die and can definitively damage it. To break this process the IC must be powered off (parasitic thyristor model).

The power consumption of the *FEB* ICs, grouped by partitions, is constantly checked with current limiting switches (MAX890L or MAX869L from Maxim). In case of current overrange a FAULT signal is asserted and the current is limited to a value set by an external resistor avoiding therefore any ICs damage.

To automate the powering down of the IC or of the group of ICs, the FAULT signal feeds back the ON pin of the current limiter cutting off the switch when active. The feed back loop is made up of three inverters (radiation tolerant 3 inputs NAND) with a *RC* time-constant for setting the power down time. Additionally, this *RC* filters also an unexpected small FAULT pulse when the switch is re-enabled.

The *FEB* partitions were defined as follows:

- eight groups of eight ADC's each, protected individually by an independent delatcher; the nominal consumption of the analogue part of one ADC is 20 mA, 160 mA for the eight ADCs (140 mA measured) and the threshold value was set to 415 mA.

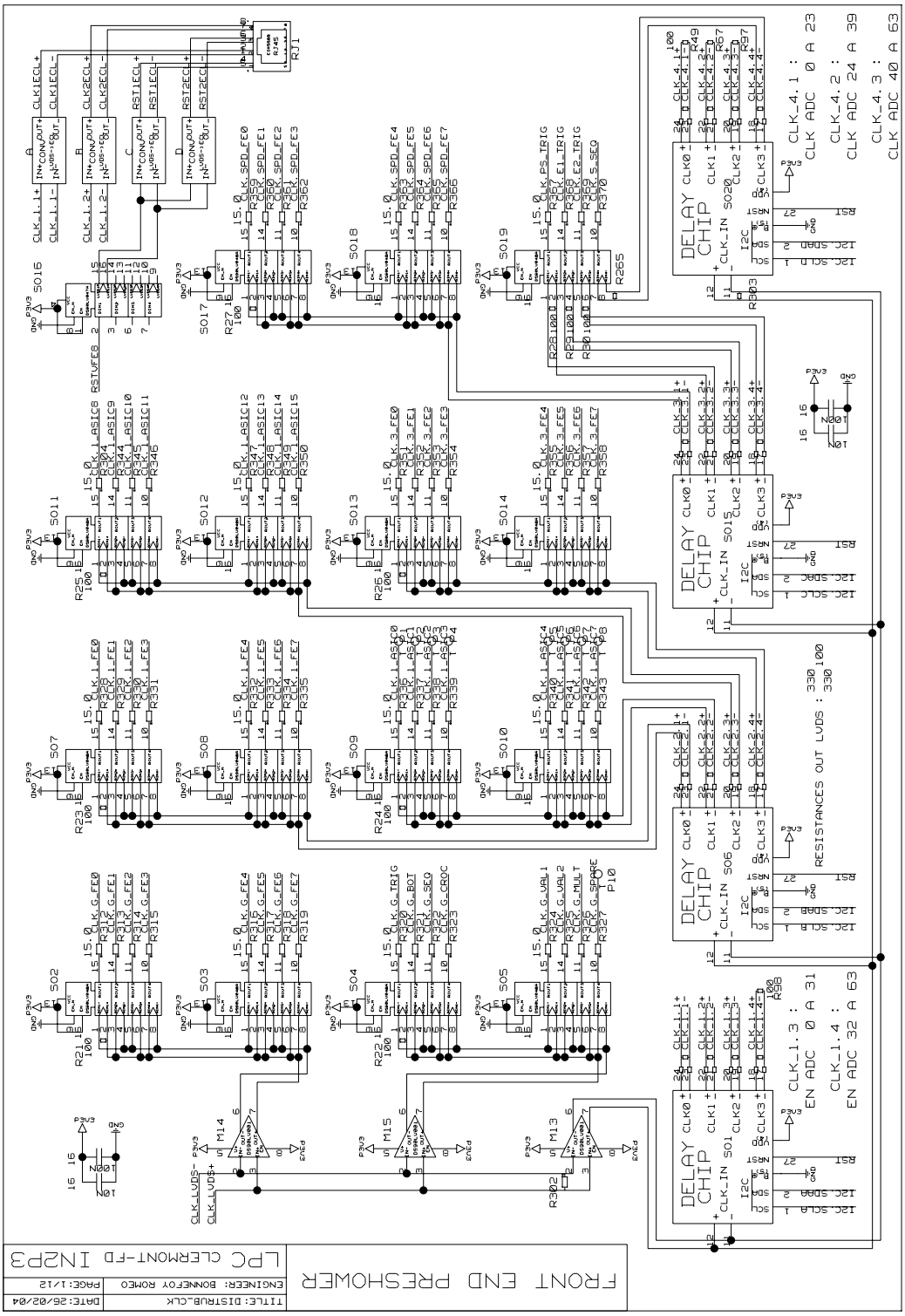

Figure 22: Clock tree schematics

- a delatcher for the *TRIG_PGA*, the *SEQ_PGA* and the *GLUE_PGA*; the measured current consumption was 770 mA and the threshold is set to two times the nominal current, i.e. 1500 mA
- two delatchers for the eight *FE_PGA*s of the *FEB*; the measured current consumption was 650 mA and the threshold is set to two times the nominal current, i.e. 1300 mA.
- a delatcher for the clock tree components (delay chips, etc...); the measured current consumption was 490 mA and the threshold is set to two times the nominal current, i.e. 1000 mA.

If the eight ADC's delatchers are independent, the last four are chained, as showed in figure 23. The tests performed on these chained *FE_PGA*s showed the

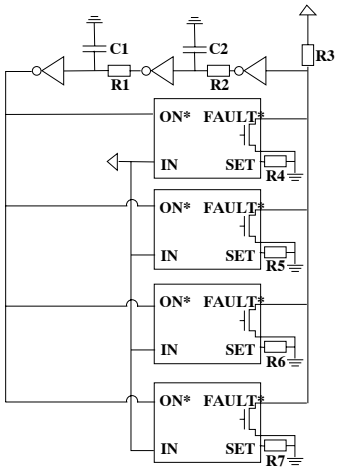

Figure 23: The schematics of the delatching circuit for the chained components.

necessity of doubling the *RC* filters in order to remain compatible with the CMOS electrical levels and within the noise margins. The figure 24 shows a screen shot of the measurement of the ON, SET and FAULT pins (from top to bottom) and last the command of a load to simulate a SEL.

For the *FE_PGA*s partitions the FAULT signal is monitored by ECS.

10.3 Radiation protection with coding

Each configuration or algorithm parameter register and finite state machine (FMS) state registers must be protected against radiation induced single event upsets (SEU). The data processing part is not SEU protected as the data flow constantly refreshes the electronic equipotentials.

This is achived by two design options :

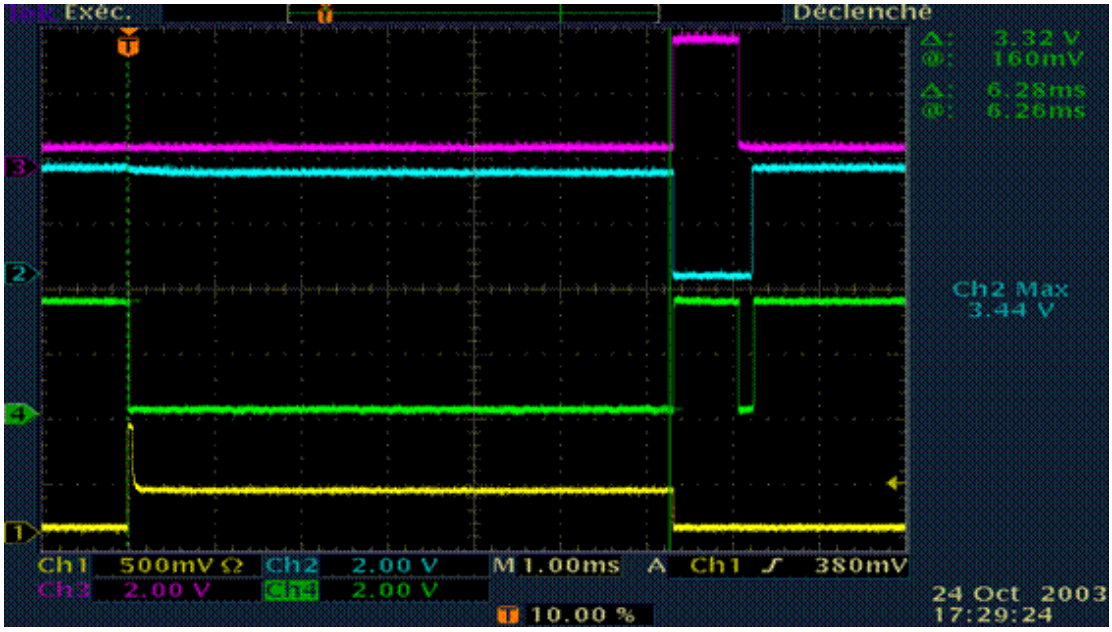

Figure 24: Screen shot of the measurement of the ON, SET and FAULT pins (from top to bottom) and last the command of a load to simulate a SEL.

- Triple module redundancy with triple voting to select valid data by a majority vote ;
- Hamming coding of data allowing a permanent correction of 1 erroneous bit and detection of two corrupted bits inside a 16 bits register (increased with 6 redundancy bits used for error detection and correction).

Every registers of FEpga and TRIGpga, including FSM, are based on triple module redundancy. Except for the FEpga algorithm parameters where the hamming coding lead to a better usage of internal ressources for a total of 544 bits of parameters data including redundancy bits.

The hamming decoder allowing error correction is shared among 16 registers and check data integrity cyclicaly except during ECS access where data are loaded by 8 bits slices uncompatible with the choosen hamming coding format.

11 Global monitoring of the board

16 LEDS are available on the card front panel and provide glimpses of the board functioning:

- power (2 LEDs)

- clock signal (4 LEDs)
- SPD signals (1 LED)
- VFE reset (1 LED)
- L0 requests (1 LED)
- readout request on the FPGA (FE-SEQ communication) (1 LED)
- ECAl validation request (2 LEDS)
- general reset of the board - TTC channel B decoding (1 LED)
- BCID reset (1 LED)
- ECS acces: SDA+SDL (2 LEDs)

12 Power consumption and partitions

The board is powered between +3.3 V and -5 V. No +5 V is available on the board which is therefore not compliant with standard ECAL or HCAL power supplies settings. Nevertheless, the same crate mecanics and power supplies modules are used. The 3.3 V comes from two power supplies, one being dedicated to analogue components of the board, the optical amplifier and the ADCs.

Except for the optical amplifier of the analogue input module, which is sufficiently radiation tolerant from the SEL point of view, the board components are powered through current limiter switches with automatic delatching capability (see section 10). Fuses are also added on the power lines.

The components are grouped in partitions (as described in section 10). Each partition is powered by a dedicated switch such as the power comsuption of the partition do not exceed 75% of the maximum current driving capability of the switch (1.5 A).

The measured board power consumption was

- for the digital +3,3 V: 2.42 A , ie 5.4 W
- for the analog -5.0 V: 0.84 A, ie 4.2 W,

leading to a total of 17.6 W.

#	Purpose	Year
1	Tests of neighbours algorithm	Q1 2001
2	Analogue module (ADC...)	Q2 2001
3	Analogue + FEpga, 16 channels, on VME board used for 2 Tests beams and MAPMT tests	Q3 2001
4	Digital pattern injector (LVDS)	Q3 2001
5	Digital ASIC (data processing)	Q2 2002
6	Digital ASIC with I2C	Q1 2003
7	First 64 channels prototype Actel AX + ASICs + DAQ and ECS	Q1 2004
8	Test bench for debugging and production tests	Q1 2004
9	(Almost final) 64 channels prototype updated with APA fpgas, final ECS	Q2 2005
10	Final design (minor updates)	Q1 2006

Table 8: Prototypes of PS FE electronics

13 PS *FEB* prototype

The hardware has been carefully checked through a large set of partial prototypes designed during the past years, as it can be seen in the table 8.

The radiation hard delay chip, the DAQ interface *SEQ_PGA*(Actel APA300) and the ECS interface *GLUE_PGA* (Actel APA150) have been designed by LAL and implemented without changes, except of course the physical position on the board.

Since April 2006 a full 64 channels prototype (figure 25) is available and it was extensively tested. The content and the results of these tests are detailed in the accompanying note [**?**].

Compared to the actual prototype, the changes to the final board are minimal:

- an extra *RC* constant was added to stabilize the chained delatchers;
- a pull up resistor was added on one of the *SEQ_PGA* entries, as requested by LAL;
- only four *SEQ_PGA*'s outputs distributing the *read commands* towards the *FE_PGA*s were used, whereas on the final board all available eight outputs will be used.
- on the prototype, it was possible to choose between two different gains, using

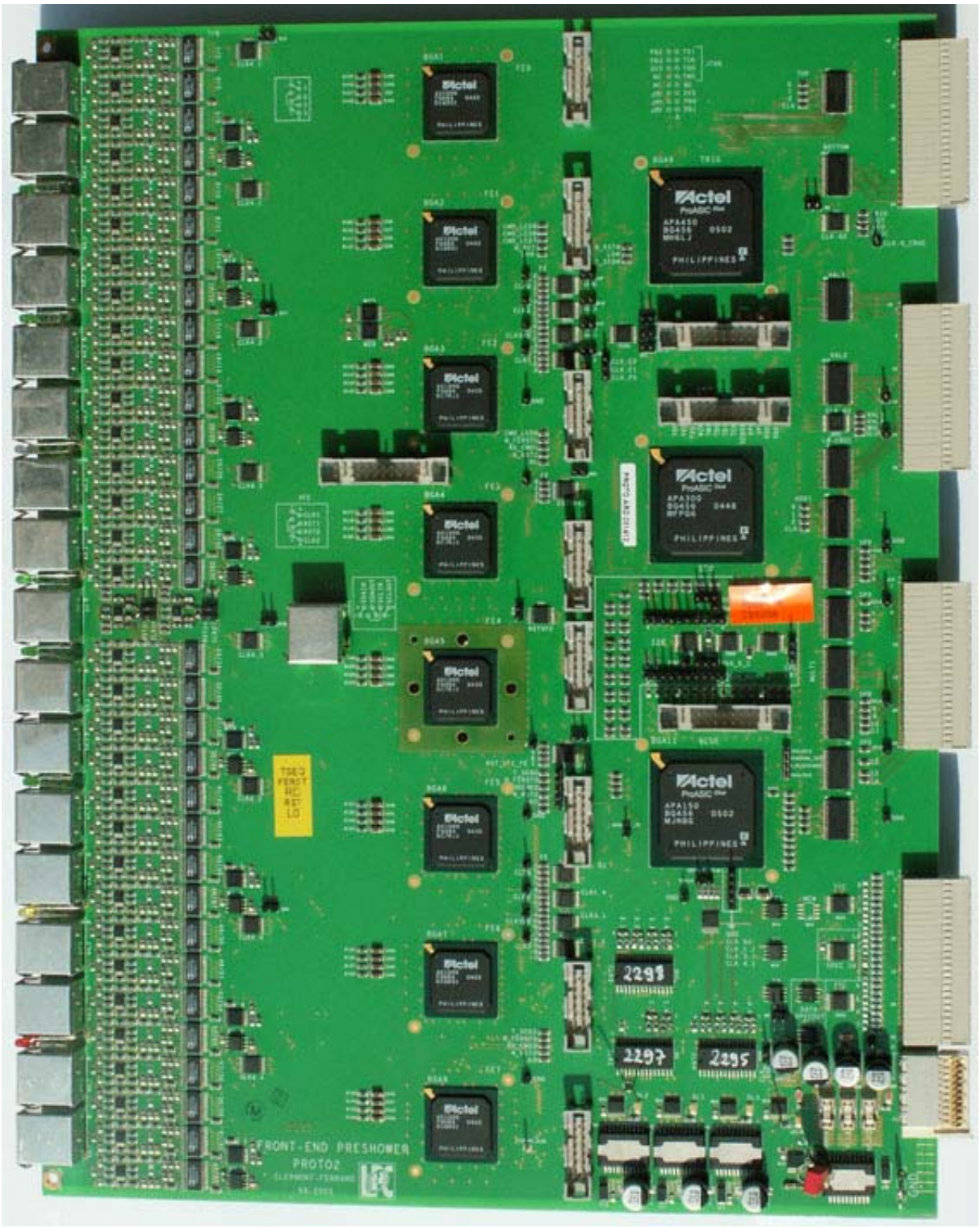

Figure 25: The PS/SPD Front-End board prototype

an optional 0 Ω resistor, possibily abandonned for the final board, where the gain is set to 1.07.

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A *FE_PGA* control registers — ECS control

I2C access to each PGA on four channels defined as base address+ 0...3. All the I2C frames may be incomplete.

A.1 Channel 00 — Status and Control Register

An up to nine words frame can be send to the FE_PGA for setting the Control Register:

CTRL, CMD, L0LAT, PSPIPE, SPDPIPE, MASK, ACQCTRL, INJDEPTH, TRIGDEL

with the parameter meaning explained in the following. Thirteen parameters are available in read mode:

CTRL, L0LAT, PSPIPE, SPDPIPE, MASK, ACQCTRL, INJDEPTH, FLAGS, STATUSCLK, ACQRAMCNT, INJRAMCNT, PSRAMCNT, TRIGDEL

- **CTRL:**

bit	7	6	5	4	3 | 2	1	0
	top or bottom mapping	Inj no synchronised	Inj sync selection	Inj sync mode	Bypass Processing	Data selection	Inj loop

  - **Inj loop:** infinite loop on the injection patterns if set to 0
  - **Data selection:** injection RAM patterns if set to 1, ADC output if set to 0
  - **Bypass processing:** 00 or 01 leads to normal processing, 10 = bypass processing , out data = 8 lsb of raw data 11 = bypass processing , out data = 8 msb of raw data
  - **Inj sync mode:** full RAM injection if set to 0, injection driven by trigger signal if set to 1
  - **Inj sync selection:** injection started by the testsequence signal if set to 0 and by the L0 signal if set to 1
  - **Inj no synchronised :** synchronised injection if set to 0, non synchronised otherwise
  - **top or bottom mapping :** mapping type bottom if 0, type top otherwise.

- **CMD:** 8b word, the bit 0 leads to the initialisation of the ACQRAM counter, whereas the bit 1 initialises the INJRAM counter.
- **L0LAT:** 8b RW word, gives the virtual depth of the L0 pipeline
- **PSPIPELEN:** 8b RW word, PS pipeline virtual depth, automatic bypass if set to 0
- **SPDPIPELEN:** 8b RW word, SPD pipeline virtual depth, automatic bypass if set to 0
- **MASK:** 8b RW word, mask for PS and SPD trigger outputs
- **ACQCTRL:**

bit	7	6	5	4	3	2	1 | 0
	Shaped L0 width	not used	not used	acq trig selection	not used	not used	ACQRAM mode

  - **ACQMode:** 00=mode raw trigger, 01=burst mode, 10=leading edge trigger, 11=shaped trigger (N samples)
  - **ACQ trig selection:** if 1, the testsequence signal replaces the L0 signal
  - **Shaped L0 width:** the L0 signal is shaped (in ACQ mode 11); 0 = 8 BX, 1=16 BX
- **FLAGS:** read only 8b word, gives the triple routing or hamming errors, delatches. It keeps the transitions and it is automatically reset when read.

bit	7	6	5	4	3	2	1	0
	hamming ch 1	hamming ch 2	ADC delatcher all other TR errors	TR error on 00 register	TR error on ACQ RAM	TR error on INJ RAM	TR error on ECS block	TR error on ECS interface

- **STATUSCLK:** read only 8b word, status for the clock sampling by the ground clock signal, normal values FF or $F7$. It gives the entry (general) clock quality, but should be noted that it does not work in absence of entry clock signal.

bit	7	6	5	4	3	2	1	0
	SPD clock lock	copy bit 2	copy bit 1	copy bit 0	SPD clock sampling by general clock	not used	ϕ_{FEADC}	PLL global clock lock (*)

- **INJRAMCNT:** read only 8b word, current value of the INJRAM counter
- **ACQRAMCNT:** read only 8b word, current value of the ACQRAM counter
- **INJDEPTH:** 8bit RW word, gives the virtual depth of the INJRAM
- **TRIGDEL:** 8bit RW word, gives the virtual depth of the trigger pipeline

A.2 Channel 01 and 10 — Read write of the processing parameters registers

The hamming coded values for the offsets, gains, alphas and trigger bits for the first four channels are programmed through the 01 channel, whereas the processing parameters for the last four channels are accessed through the channel 10. 33 bytes data frames are necessary on each cannel for parameters RW, which means that long I2C frames are used, contrary to the RW on the control channel.

A.3 Channel 11 — INJRAM and ACQRAM read

The INJRAM and the ACQRAM are read simultaneously through 256 frames of 24 8-bits words ($24 * 8$), where the frame structure is the following :

	ACQRAM	ACQRAM counter	INJRAM	INJRAM counter	debug value
byte#	0 : 7 | 8 | 9	10	11 : 20 | 21	22	23
	PS chans | PS trig bits | SPD bits		PS chans | SPD bits		1

The structure of the INJRAM is a bit more complex, since the injected values for the 8 PS channels are 10 bit values, which are re-organised as a frame of 10 8-bit words for the I2C transmission purposes.

Obviously only the INJRAM is available in write mode and the I2C frame mirrors the reading one, with the LSB to the right:

byte#	10	9 : 0
	SPD bits	PS chans

B *TRIG_PGA* control registers — ECS control

This description of the ECS control follows the last TrigPGA release : *PROTO1* . The TrigPGA is at the I2C address 0x0C of the FE board. Three channels allow to have access to the different items of the component :

- 0x0C + 0x0 : control registers
- 0x0C + 0x1 : injection RAM
- 0x0C + 0x3 : acquisition RAM

B.1 Control registers

The behaviour of the TrigPGA is totally determined by some 8 bit registers, accessible by software. These registers can be sorted by their access mode : read only, write only or read/write.

Read only registers :

- **FLAGS** : this register sums up the different triple-voting error flags of the TrigPGA. The zero value means no detected error.
  - bit 0 : error on ECALPIPE register
  - bit 1 : error on INJDEPTH register
  - bit 2-3 : error on I2C
  - bit 4 : error on ECAL pipe-line
  - bit 5 : error on CTRL register
  - bit 6 : error on ACQCTRL, INJCTRL or TALAT(PS-SPD part) registers
  - bit 7 : error on TALAT(neighbour part) register
- **DELTABXECAL1** : returns the difference between the first ECAL BCID and the PS local BCID.
- **DELTABXECAL2** : same register as the previous one but applied to the second ECAL board inputs.

Write only registers :

- **CMD** : the first LSB bit allows to reset the acquisition RAM counter (CMD=0x01) or the injection RAM counter (CMD=0x00).

Read/Write registers :

- **CTRL** : neighbour searching algorithm options
  - bit 0 : 0 = Bottom mapping, 1 = Top mapping
  - bit 1 : 0 = whole board, 1 = half-board

- bit 2 : 0 = Right neighbour used, 1 = Right neighbour disabled
- bit 3 : 0 = Top neighbour used, 1 = Top neighbour disabled
- bit 5-7 : Non-Affected (NA)

- **INJCTRL** : injection options
  - bit 0 : 0 = injection RAM looped, 1 = not looped
  - bit 1 : 0 = injection started with TestSequence pulse, 1 = with L0
  - bit 2-3 : 00 = injection @ PS clock + started with trigger signal
    01 = injection @ trigger
    10 = injection @ PS clock
    11 = reset counter RAMs by trigger
  - bit 4-5 : NA
  - bit 6 : 0 = effective ECAL inputs, 1 = ECAL part of the injection RAM
  - bit 7 : 0 = effective PS neighbours inputs, 1 = Neighbour part of the injection RAM
- **INJDEPTH** : injection RAM depth
- **ACQCTRL** : acquisition options
  - bit 1-0 : 00 = injection @ trigger
    01 = injection @ PS clock
    10 = injection @ leading edge trigger
    11 = injection @ shaped trigger
  - bit 2 : 0 = trigger, 1 = burst **WHAT IS IT ?**
  - bit 7-3 : if bit7=0, 0 = algorithm results acquired
    if bit7=1, 0 = Top neighbours and PS trigger bits acquired
    if bit7=1, 1 = Right neighbours and SPD trigger bits acquired
  - bit 4 : NA
  - bit 5 : 0 = trigger is L0, 1 = TestSequence
  - bit 6 : 0 = trigger shaped width of 8, 1 = 16
  - bit 7 : 0 = algorithm process, 1 = bypass mode
- **BXlocalOFFSET** : BCID initial value put at each BCID reset signal
- **ECALPIPE** : ECAL pipe-line depth [1]
- **TALAT** : Neighbours and PS-SPD trigger bits pipe-line depth [1]

[1] These delay options are bypassed if the register value is equal to 0

– bit 0-2 : PS-SPD pipe-line depth
– bit 3-4 : Top neighbour pipe-line depth
– bit 5-7 : Right neighbour pipe-line depth

The SPECS frames for writing and reading the configuration registers have the following structures :

Writing register frame :

63-56	55-48	47-40	39-32	31-24	23-16	15-8	7-0
INJDEPTH	INJCTRL	ACQCTRL	BXlocalOFFSET	TALAT	ECALPIPE	CTRL	CMD

Reading register frame :

79-72	71-64	63-56	55-48	47-40	39-32
DELTABXECAL1	DELTABXECAL2	INJDEPTH	INJCTRL	ACQCTRL	FLAGS

31-24	23-16	15-8	7-0
BXlocalOFFSET	TALAT	ECALPIPE	CTRL

B.2 Injection RAM

The injection RAM can contain the trigger algorithm inputs except of PS/SPD data. Nonetheless, if the bit called "PS/SPD TO ONE" is enable, all PS and SPD bits are set to one.

51-34	33-18	17	16-10	9-5	4-0
Right neighbours	Top neighbours	PS/SPD TO ONE	ECAL BCID	ECAL address 2	ECAL address 1

B.3 Acquisition RAM

The acquisition of the algorithm ouptut data depends on the value of the register ACQRAM (bit7 for bypass mode, bit3 for data selection). All possible modes are presented :

No bypass mode : ACQRAM bit7=0

79-75	74-57	56-41	40-34	33-29	28-21	20-16	15-8	7-0
0	Left neighbours	Bottom neighbours	SPD multiplicity	ECAL address 2	VAL2	ECAL address 1	VAL1	PS local BCID

Bypass mode : ACQRAM bit7=1, bit3=0

79-64	63-0
Top neighbours	PS inputs

Bypass mode : ACQRAM bit7=1, bit3=1

79-64	63-0
Right neighbours (no corner cells)	SPD inputs

The meaning of VAL1 and VAL2 bits is given by the following table

7	6	5	4	3	2	1	0
SPD				PS			
Top	Corner	Right	Cell	Top	Corner	Right	Cell