T1 Electronic Design Review

Saverio Minutoli

INFN Genova

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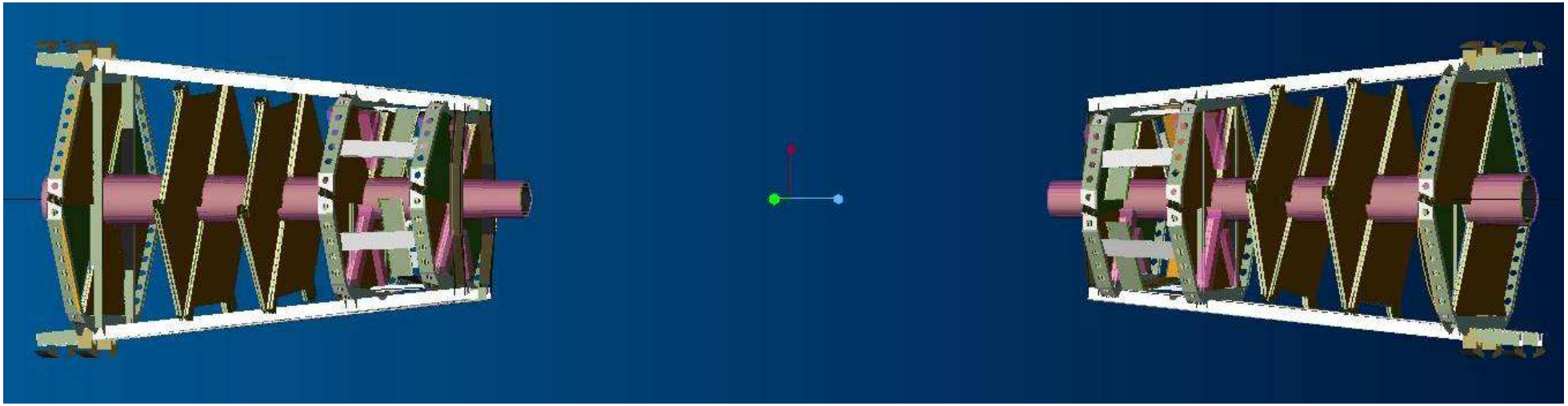
Talk overview:

- ✓ T1 detector structure
- ✓ CSC lab measures
- ✓ Radiation environment
- ✓ Anode FE system overview
- ✓ Anode vs VFAT measures
- ✓ Cathode FE overview
- ✓ Data and Trigger optical links
- ✓ Slow Control Ring
- ✓ H.V. and L.V. power distribution

Overview of T1 detector



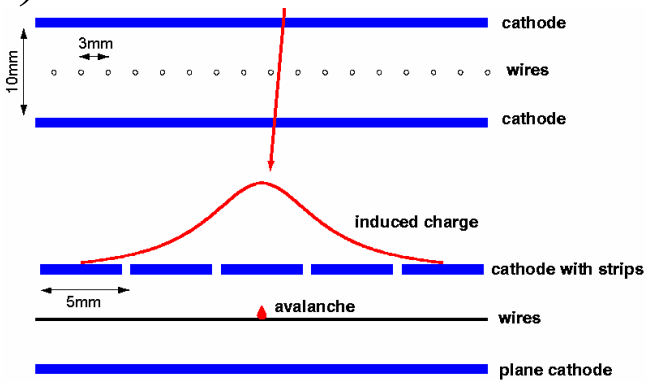
- T1 is composed by 2 arms
- Each arm contain 5 planes, each with 6 CSC trapezoidal chambers
- Each chamber is realized by 1 anode and 2 cathode planes
- For mechanical reasons, each arm is divided into two halves : each half is considered independent to the other also from electrical/logical point of view
- In total, each halve include 15 chambers

Handling signals

- In each chamber there are (maximum numbers):
  - 220 anode wires
  - 192 x 2 = 384 cathode strips
  - In total for the 2 arms there are

    220 x 30 x 2 = 13200 wires

    384 x 30 x 2 = 23040 strips



- Each wire (anode) and strip (cathode) generate a digital information:
  - 1 bit for each wire and 2 bits for each strip, assuming the half strip resolution for the cathode signals.
  - In total, the maximum number of bits managed by the electronic readout system is approximately 60000 (~1000 per chamber).
- Data taking and triggering are indipendent for each T1 halve: trigger can be combined together at higher hierarchical level.

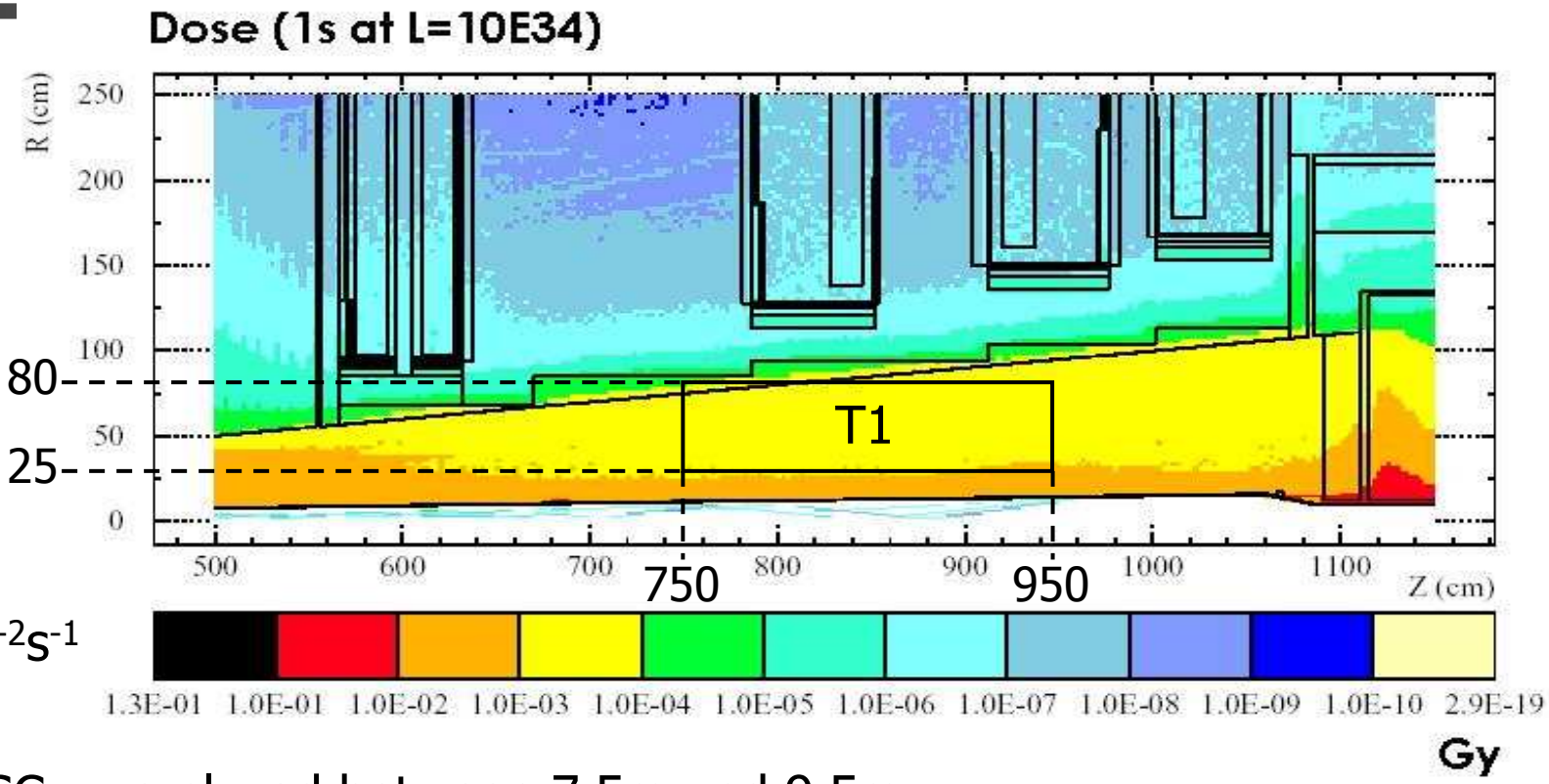
Anode/Cathode static measurements

- Impedance measured with TDR method.
- Capacitance measured with 4 wires LCR instrument.
- Anode wires:
  - Z = 330 ÷ 390 Ω
  - cap. 7 – 16.5 pF (others to gnd)
  - Anode wires length 20 – 100 cm
- Cathode Strips:
  - Z = 120 ÷ 150 Ω
  - cap. 7 – 88 pF (others to gnd)
  - Cathode Strips length 6 – 80 cm

T1 Radiation Environment

Mika's data

- Assuming:
  - 10^7s/year
  - L=10^{32}cm^{-2}s^{-1}



- T1 CSCs are placed between 7.5m and 9.5m
- Anode worst position R = 25 cm → $10^7*10^{-3}*10^2/10^2$ = 10krad/year
- Cathode position R = 63÷80 cm → $10^7*10^{-4}*10^2/10^2$ = 1krad/year

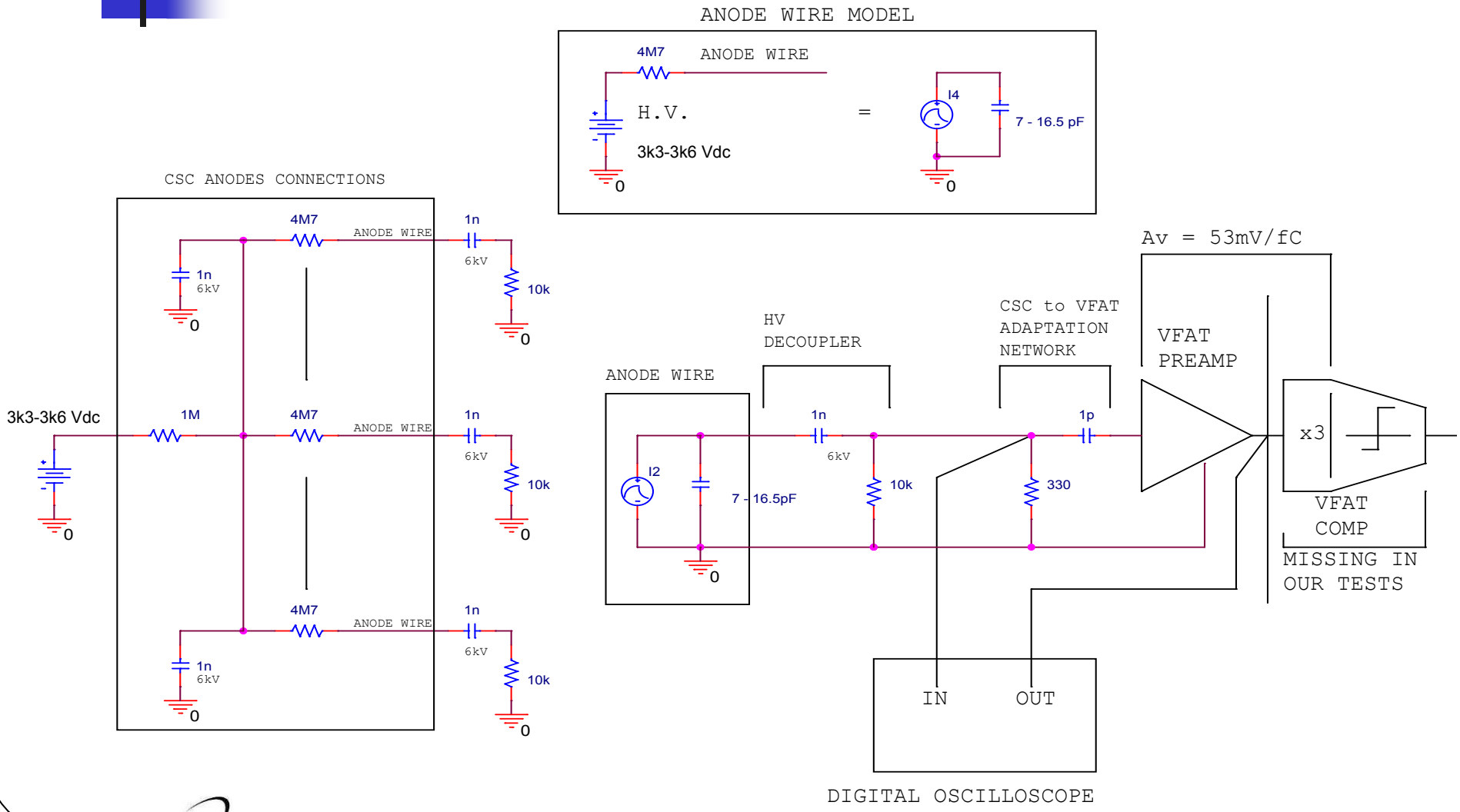
CSC FE Electronics

- The T1 chambers have been tested on beam, 2002-2003-2004.
- Due to the compatibility with the CMS-EMU CSC chambers, the same FE electronics have been used.
- Anode FE based on AFEB 16 – (validated by EMU people up to 65-70 krad; http://www hep.phys.cmu.edu/cms/RAD_HARD/2000/rad_test_p_63_1.html)
- Cathode FE based on:
  - BUCKEYE - (tested by EMU people up to 300 krad; no meaningful variation up to 60 krad http://www.physics.ohio-state.edu/~cms/raddaq2/results.html)
  - LCT-COMP - (validated by UCLA people up to 50 krad; http://www-collider.physics.ucla.edu/cms/trigger/proto99/comp_radiation_test.html)
- Concerning the Anodes FE electronic, due to the different environment, power consumption and mechanical constraints, an alternative solution have been evaluated:
  - We are investigating an testing the compatibility of the analog section of the VFAT2 with the anodes CSC wires.

CSC Anode FE Electronics → VFAT2

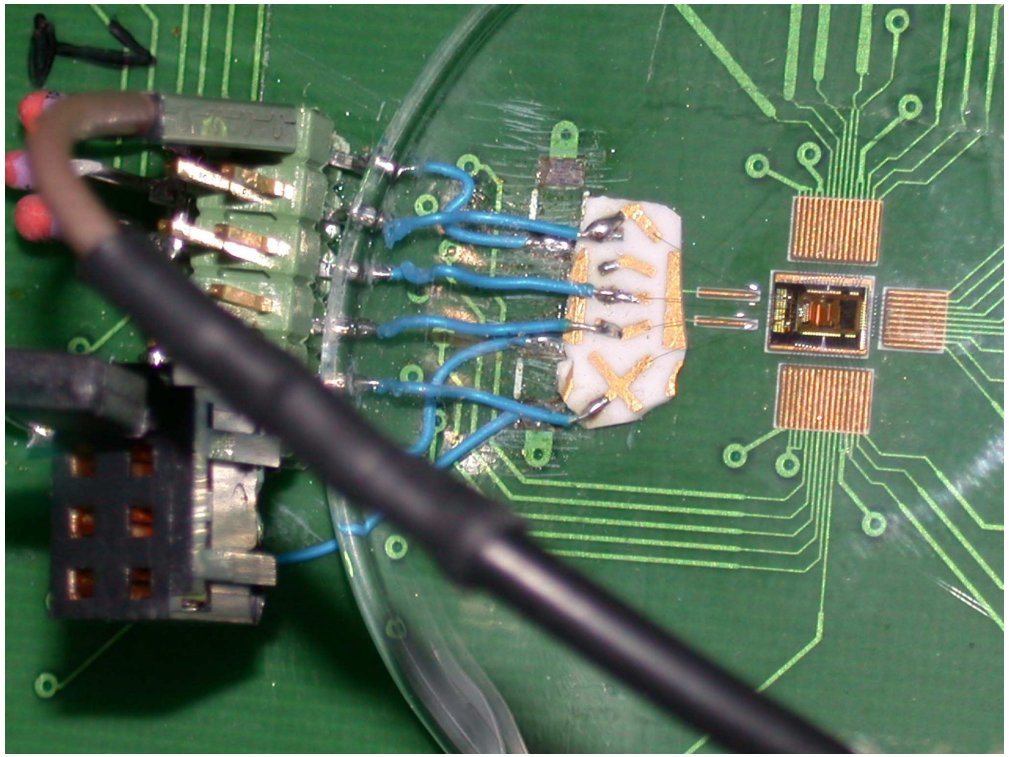
- VFAT2 was already planned to use for digital buffer, data storage and serializer.
- Now, for the anode FE, we will try to use also its analog section.
- Possible problems:
  - Anode capacitance
  - Signal Polarity
  - Shaping time, the CSC signals are not faster
  - VFAT analog, don't have any baseline restoring and tail cancellation
  - Signal amplitude, a CSC can produce hundred of fC
  - Jitter, our CSC have ~100ns

Anode FE channel adapter network scheme

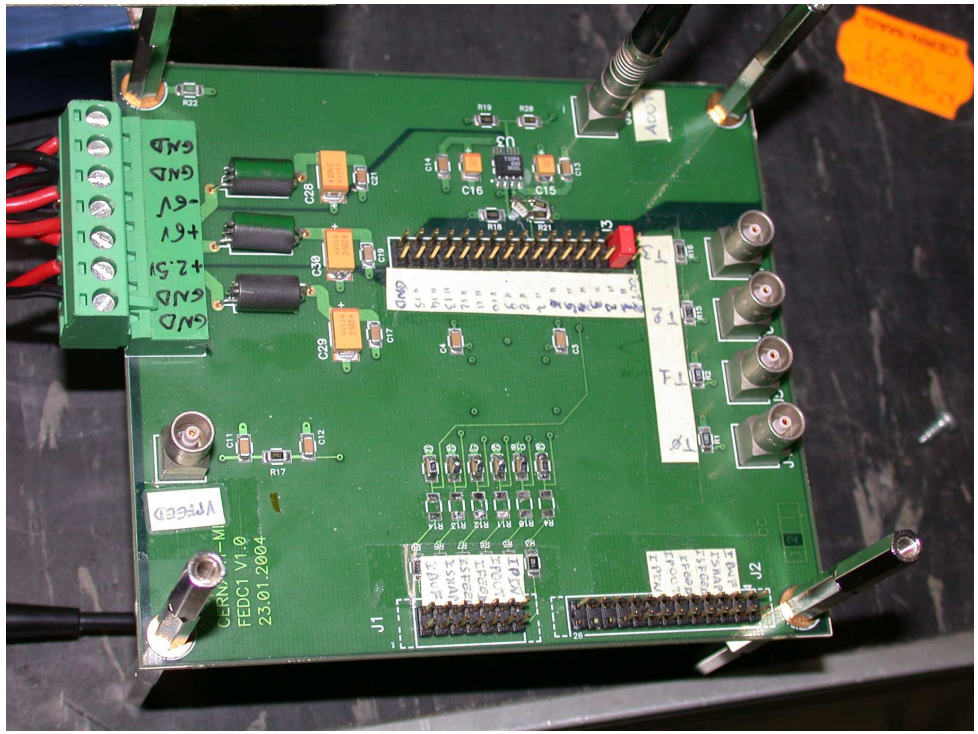


VFAT analog on the test bench

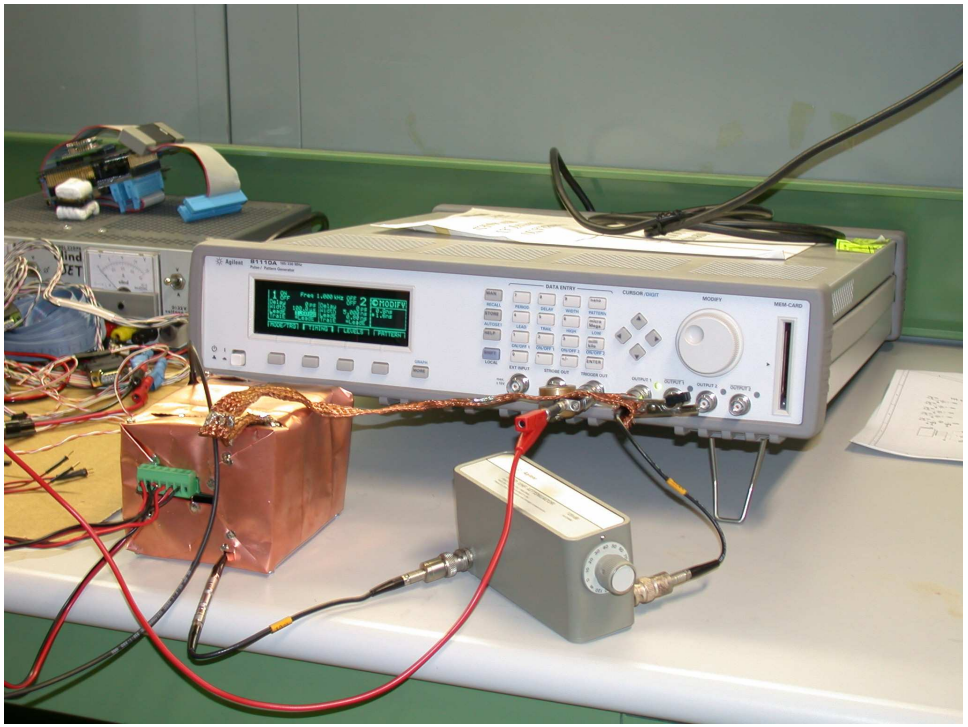
The VFAT preamplifier tested isn't the final version. The DUT, FEDC1 V1.0, is DC coupled, the preamp and the shaper stages are identical to the final version, the comparator stage and amplifier (gain x 3) are missing, as the digital parts and spikes protection networks. The test board in the pictures have been produced by the MIC group with the only intent to measure the noise due to the detector capacitance. The Genoa group has bonded few analog channels (6), coupling the passive network as near as possible to the die, but only once is possible to select in output.



VFAT analog on the test bench



VFAT preamp. test board



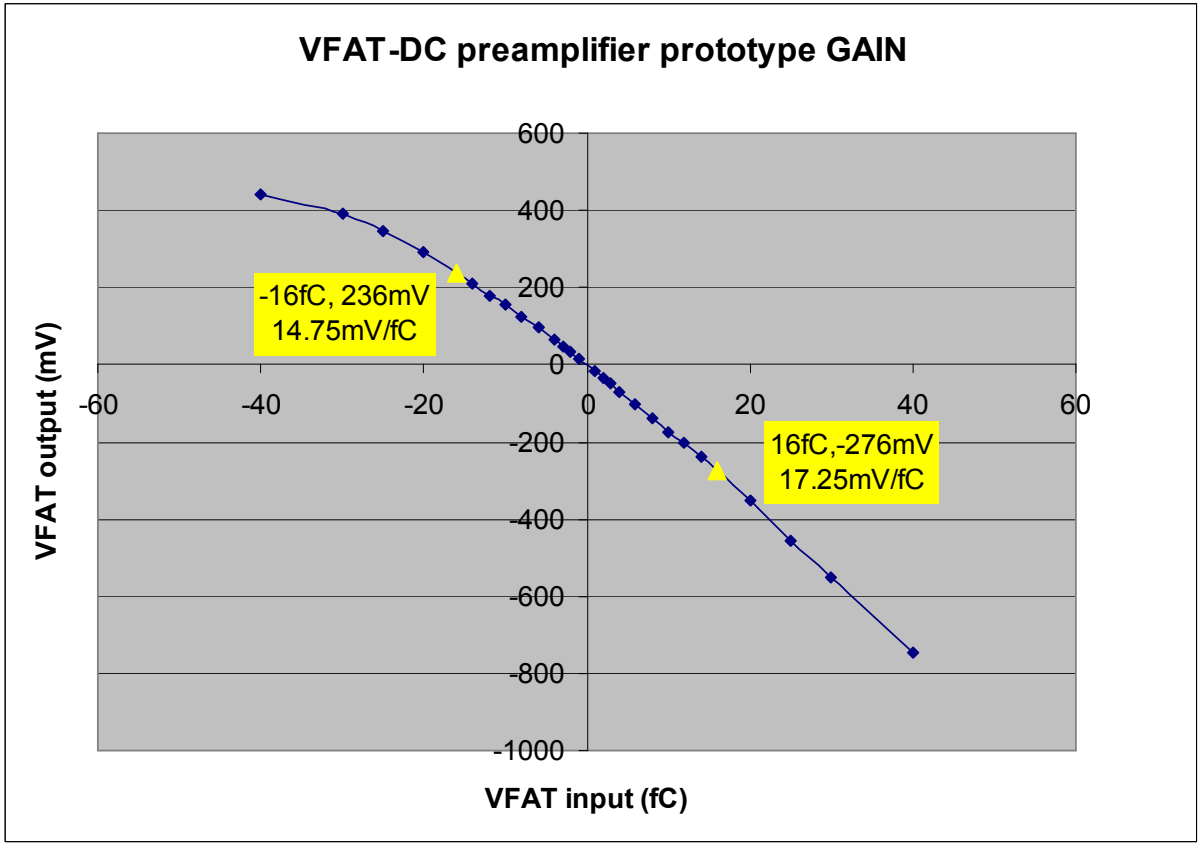
Gain and BW test bench

VFAT analog channel on the test bench

- External pulser, no chamber connected
- Pulse 100µs – 1kHz
- Pulse Gain expected value

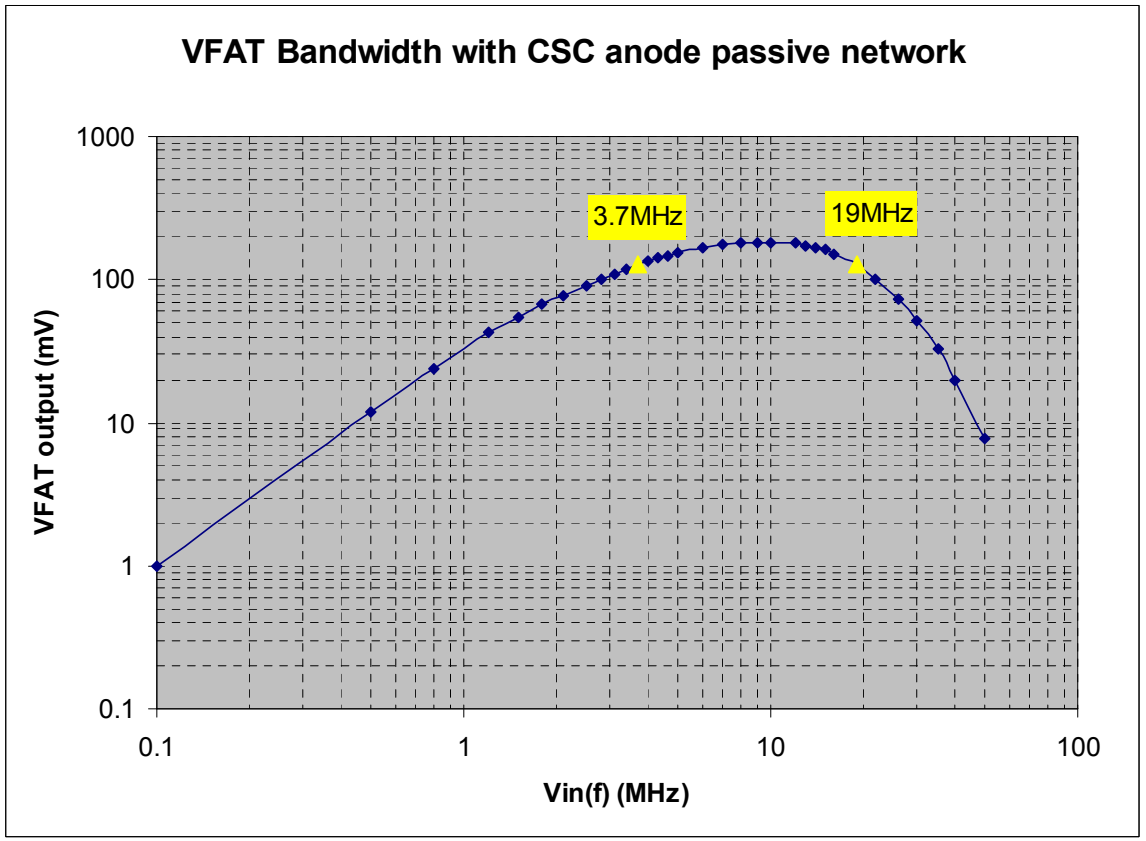
53/3=17.65mV/fC

- The anode signal could be much large, we risk to work in the bent region, where the stage saturate.



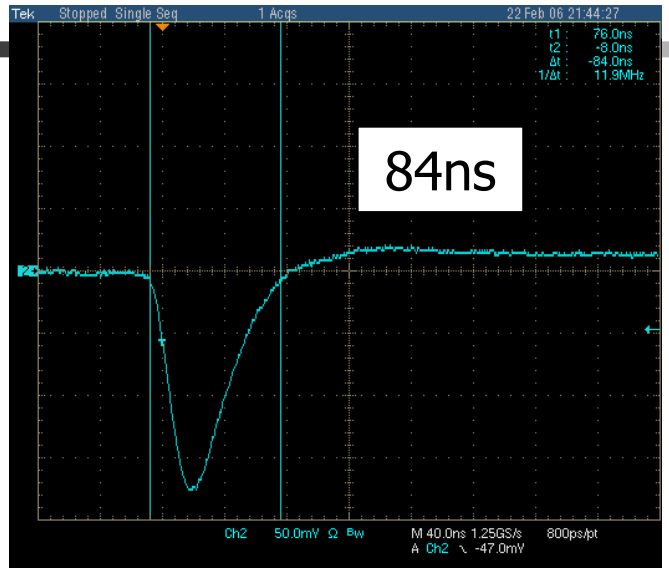
VFAT analog on the test bench

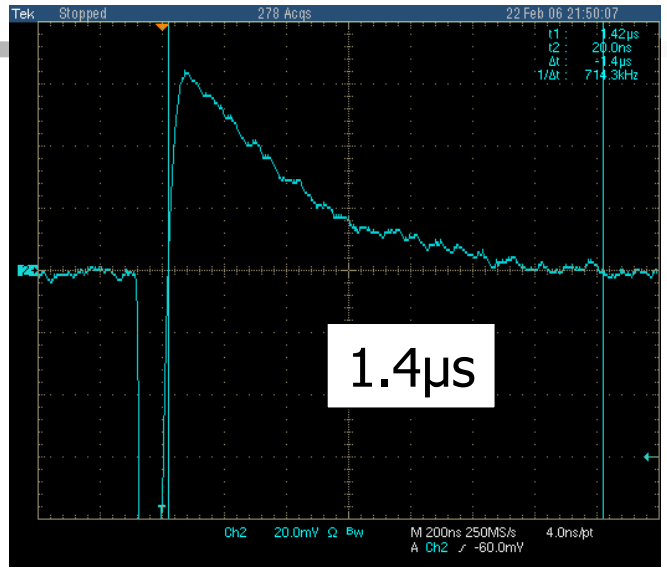
- External pulser, no chamber connected
- Sinus Input signal
- Constant Vin=~10fC
- Considering the CSC peaking time 40-50ns, our working position on the graph is around 4MHz



VFAT analog on the test bench

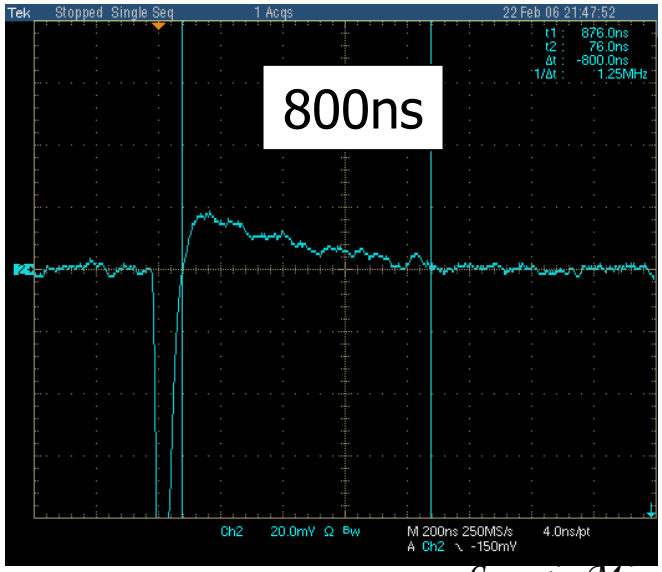
VFAT output width with 10fC Input

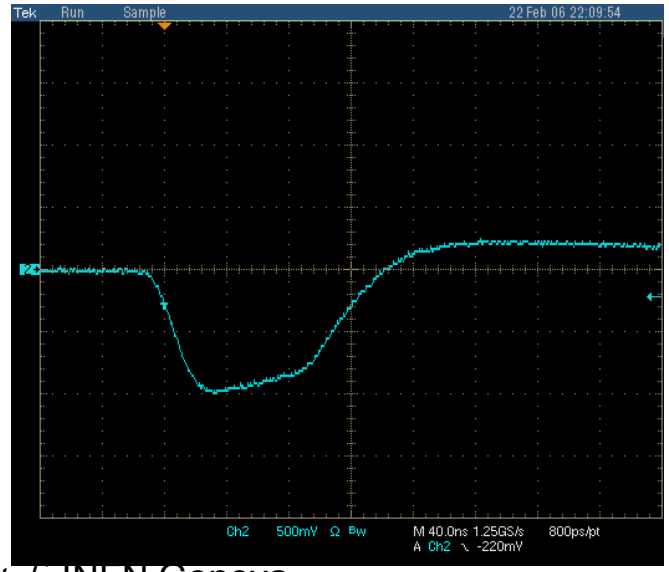




VFAT output tail with 30fC Input

VFAT output tail with 10fC Input

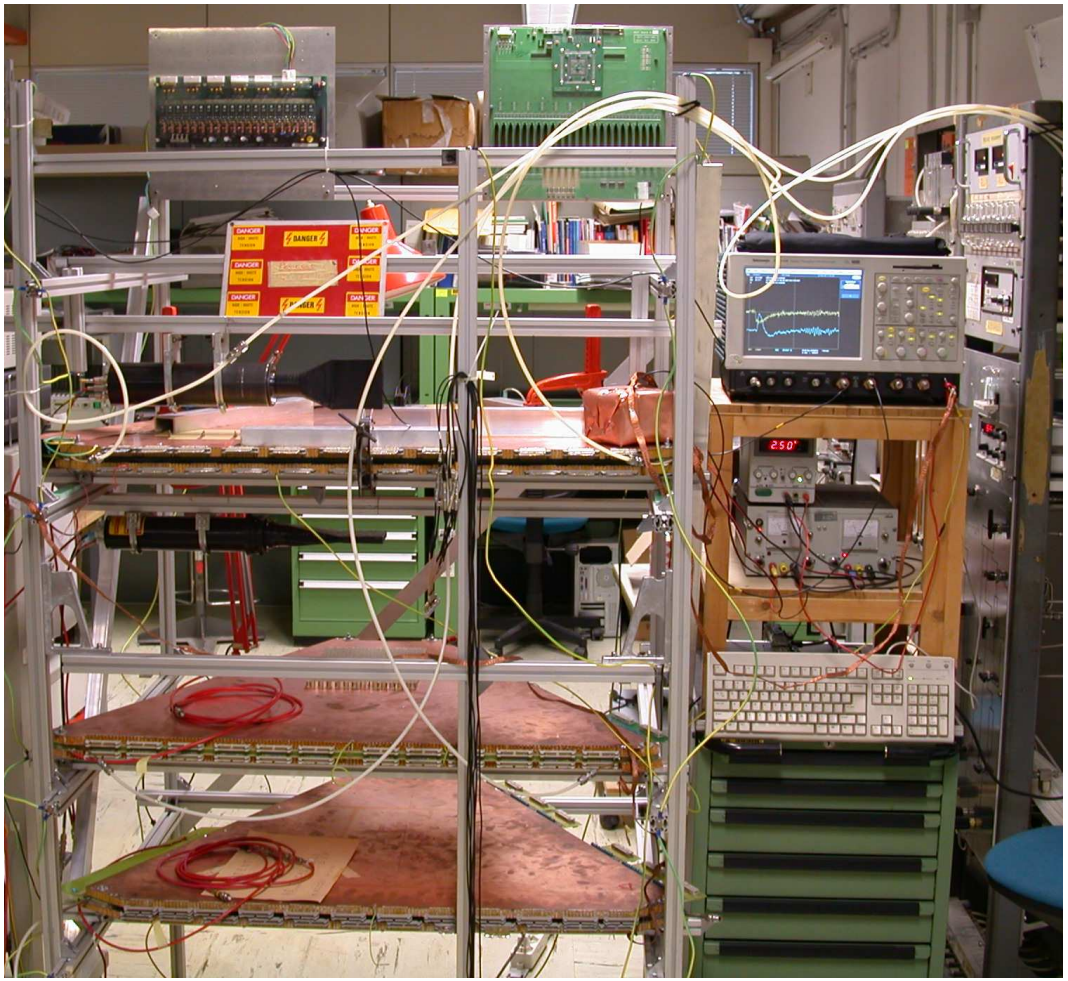




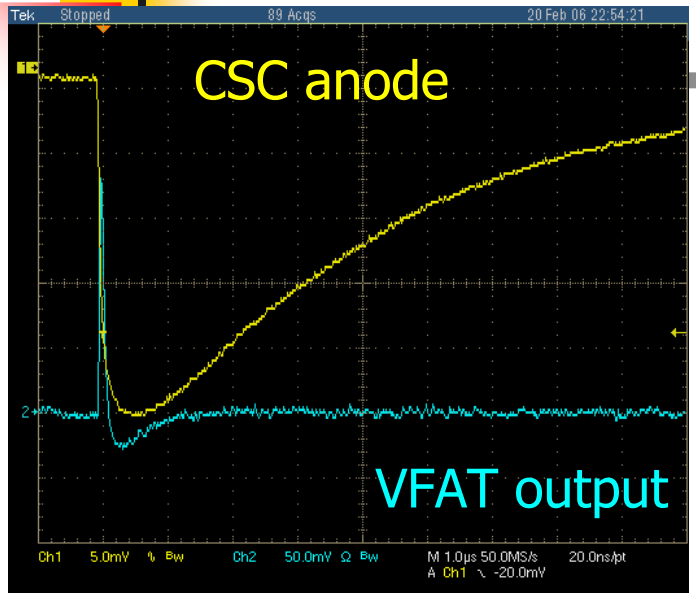
VFAT output saturation with 100fC Input

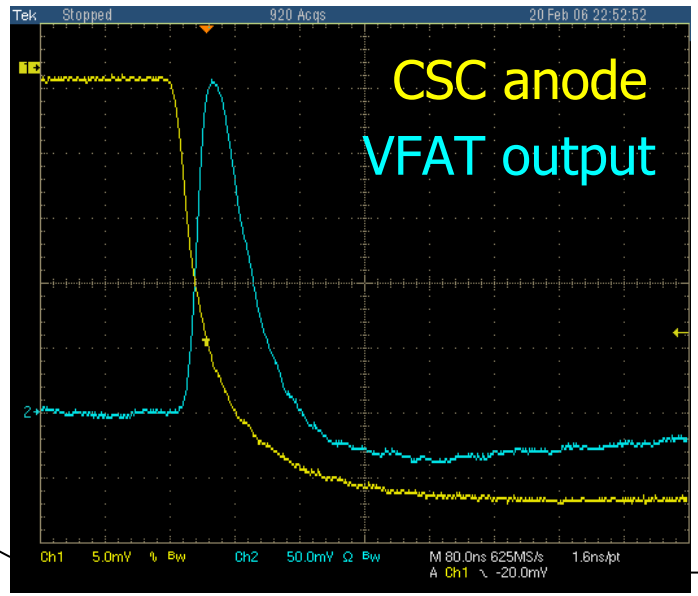
CSC Anode vs analog VFAT tests

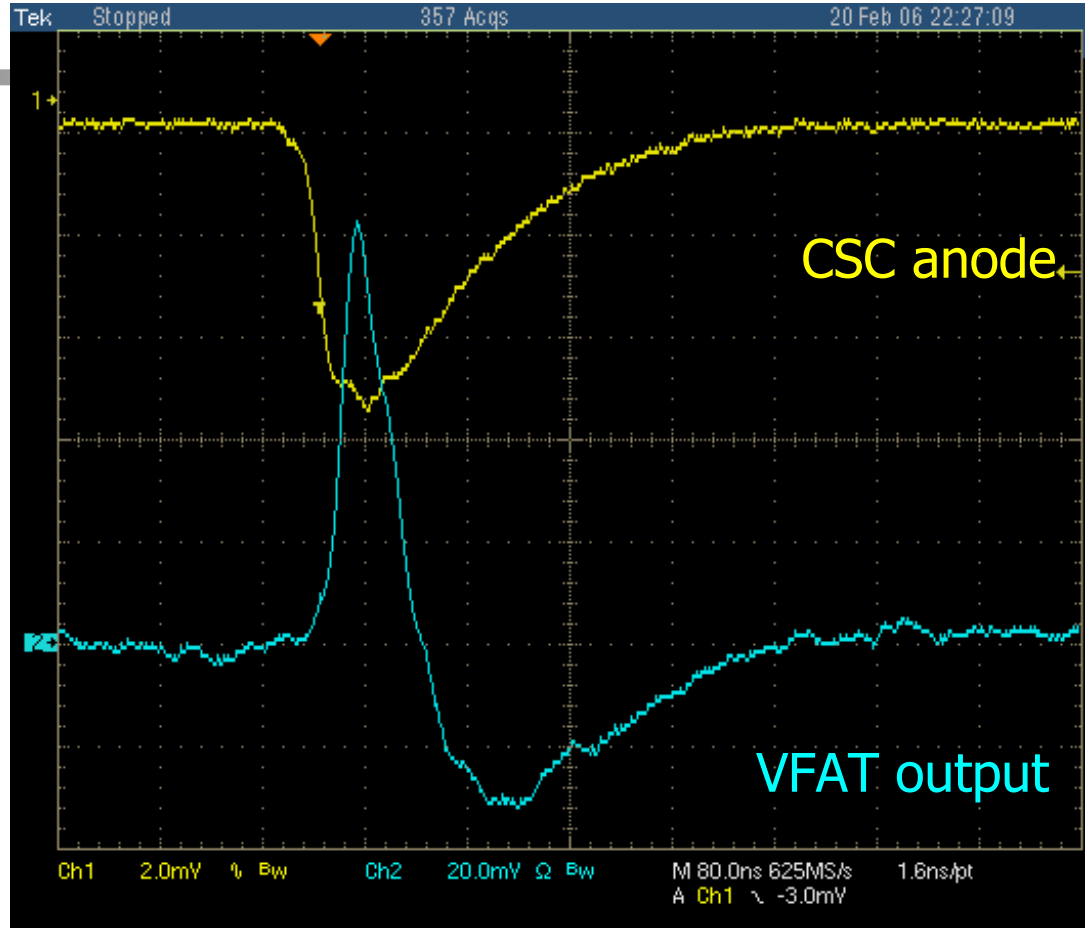
- CSC test conditions:
  - HV CSC chamber, 3250-3300 Vdc
  - Gas mixture 55% CO_2 – 45% Ar
  - Can be triggered with Cosmic rays



CSC Anode vs analog VFAT tests





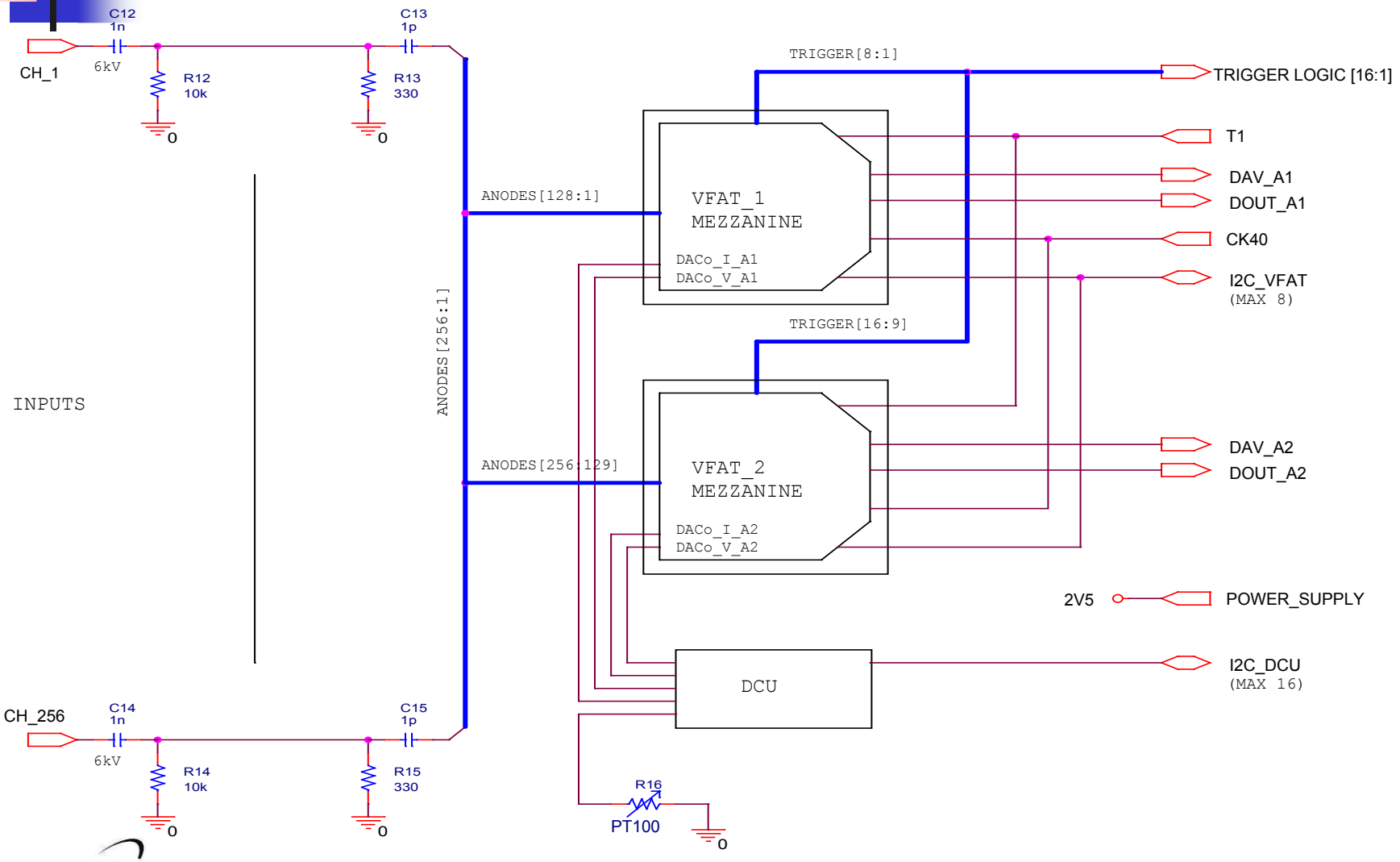


Anode with Z_L=10kΩ, tail too long,
with Z_L=330Ω seems ok.

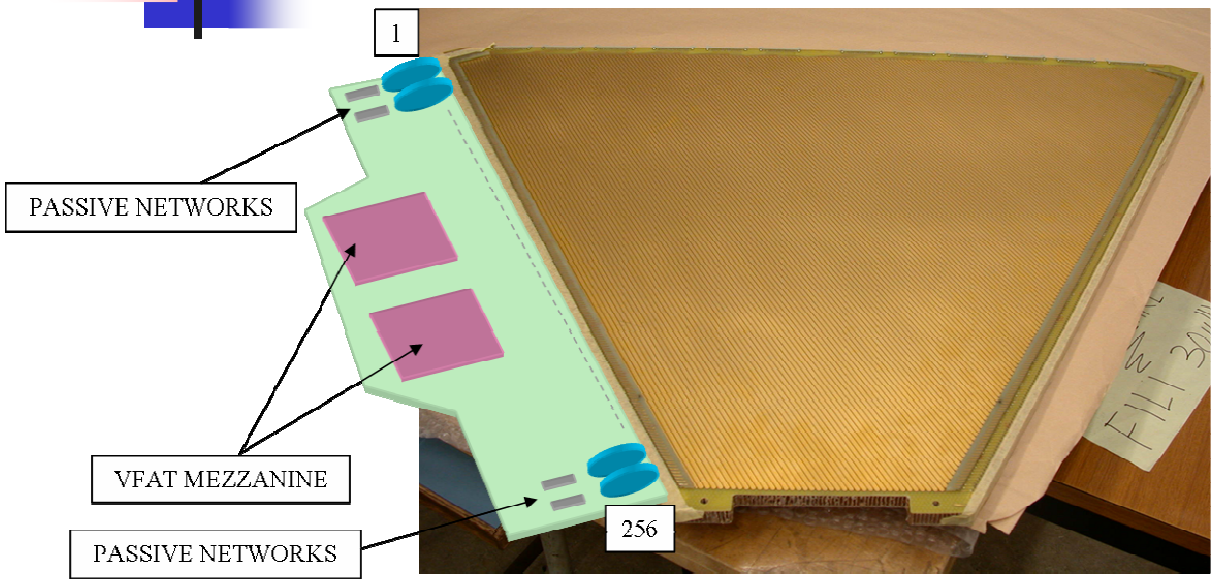
Anodes Considerations

- The VFAT2 analog section, can be adopted for the CSC anode wires, using the adapter passive network shown.
- Due to the shorter shaping time, we loose some signal, but we can accept it. With big signals we have a long recovery time due to missing tail cancellation circuits.
- CSC jitter has been solved with the digital programmable (up to 150ns) stretcher already included in the VFAT2 design.

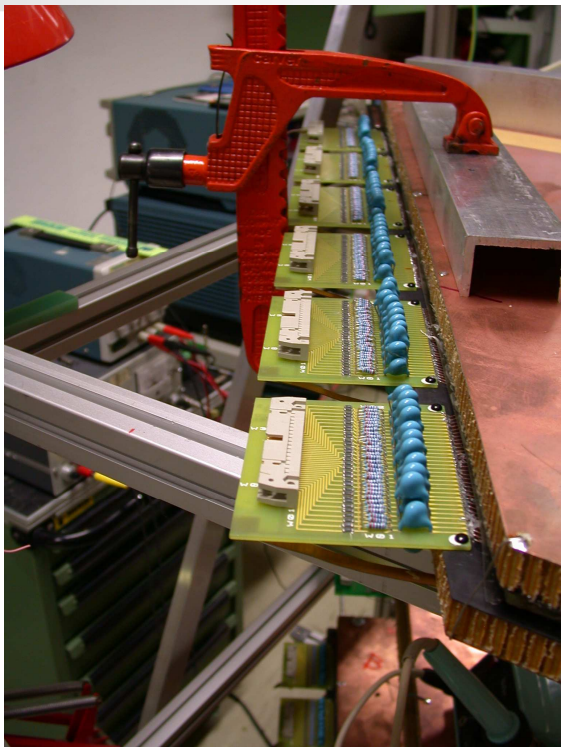
Anode FE Card block diagram



Anode FE Card integration



Sketch of the new Anode FE Card (AFEC).



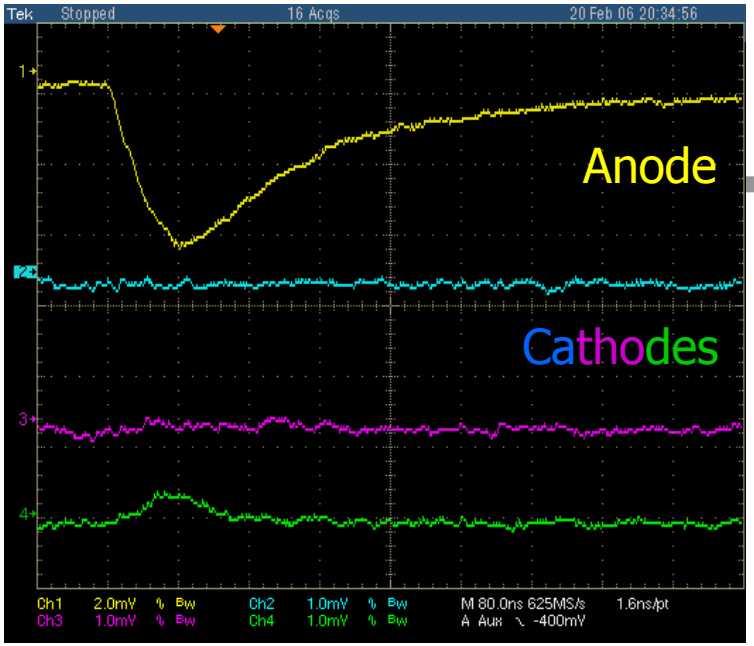
Old HV network board (digital part not shown)

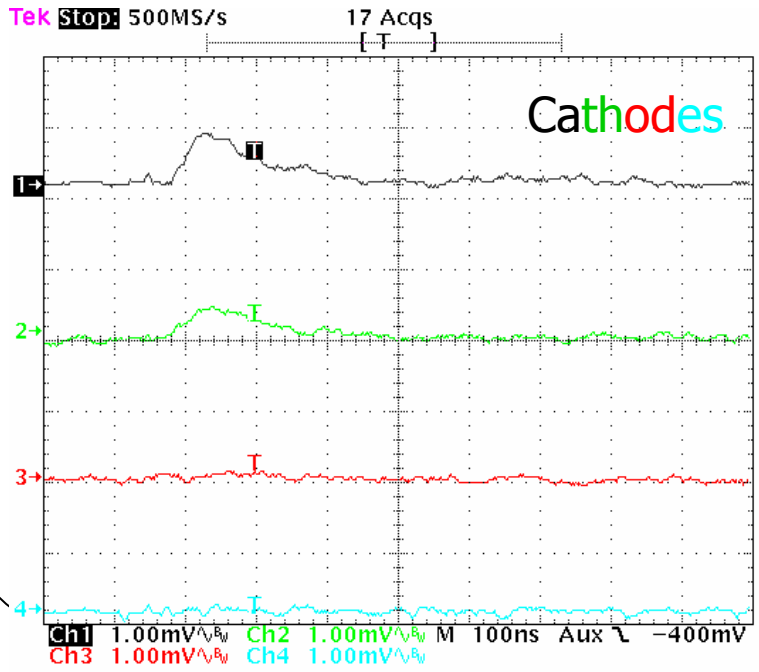
- The Anode FE Cards are 10 types, one for each kind of CSC chamber
- The VFAT mezzanine could be the same used for T2-GEM

Cathodes FE electronics

- The cathodes FE electronic components implemented in our design, are the same as used in the CMS-EMU detector.
- These devices can be well integrated in our CSC chambers system.
- Buckeye and LCT-COMP are available from CMS.
- Due to the LCT-COMP device, the cathodes spatial resolution will be increased of a factor two (half strip resolution) and a unique peak identification is also possible. This is usefull in the events where the charge distribution on the cathodes involve more than 3 strips.
- The structure foreseen is realized with 6 eurocard boards (bigger chamber) per chamber, managing 64 channels each.
- Each board allocate a VFAT mezzanine (2 bit/channel).

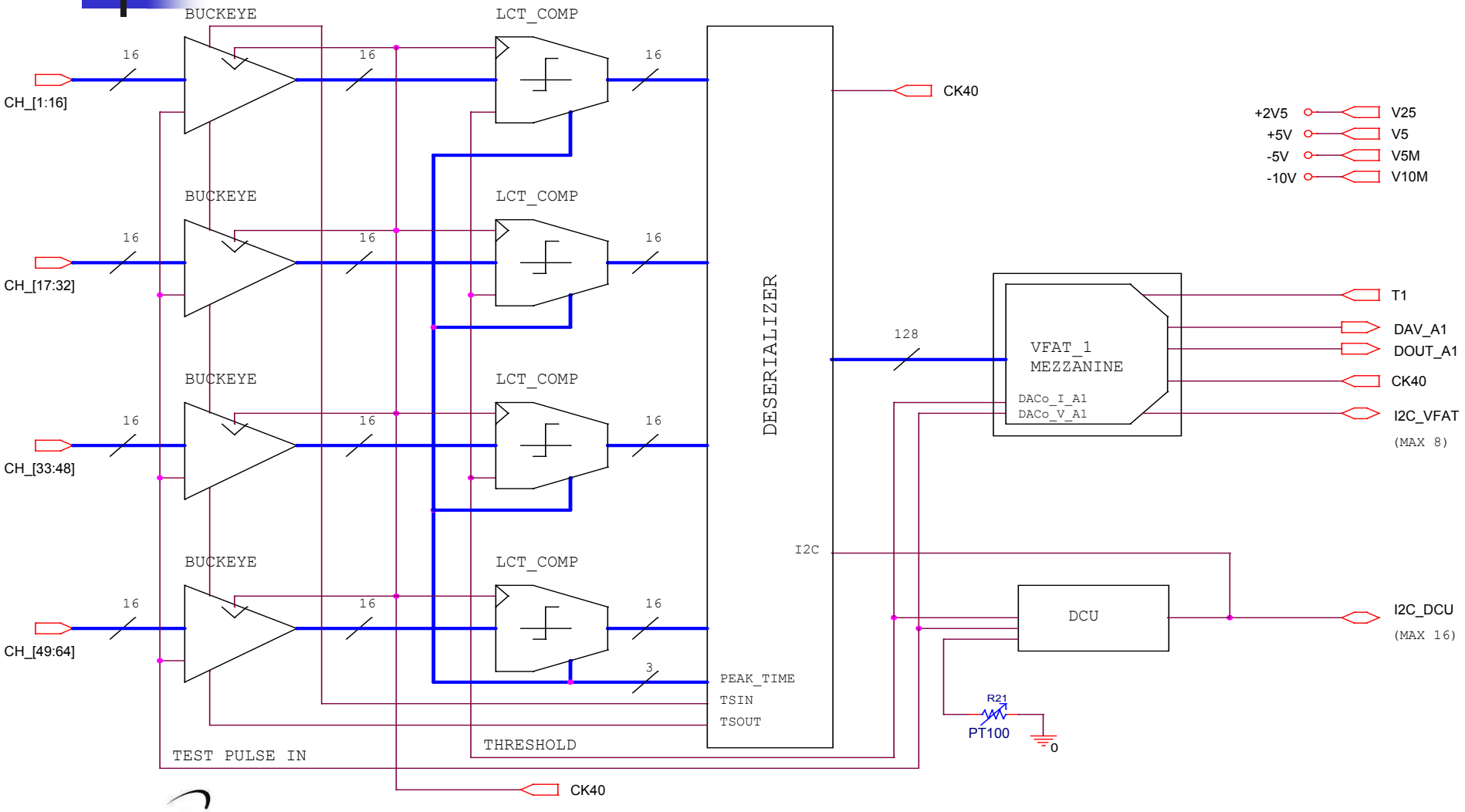
CSC Anode and Cathodes



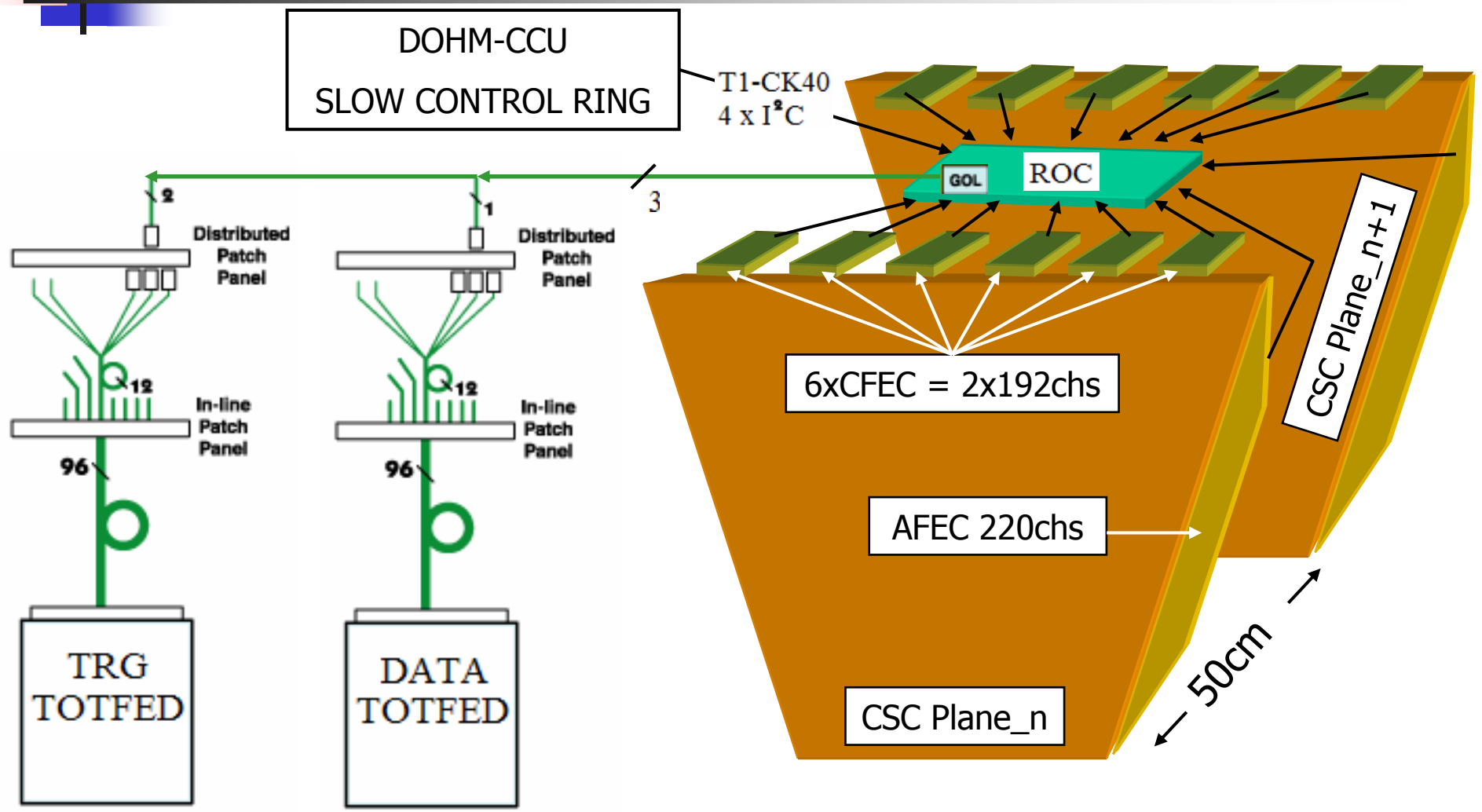


- Event with 3 cathodes hit underneath an anode.
- Cosmic triggering
- Anode Wire length 90cm
  - Z_L=330Ω (impedance line matching)
- Cathode strips length 80cm
  - Z_L=150Ω (impedance line matching)

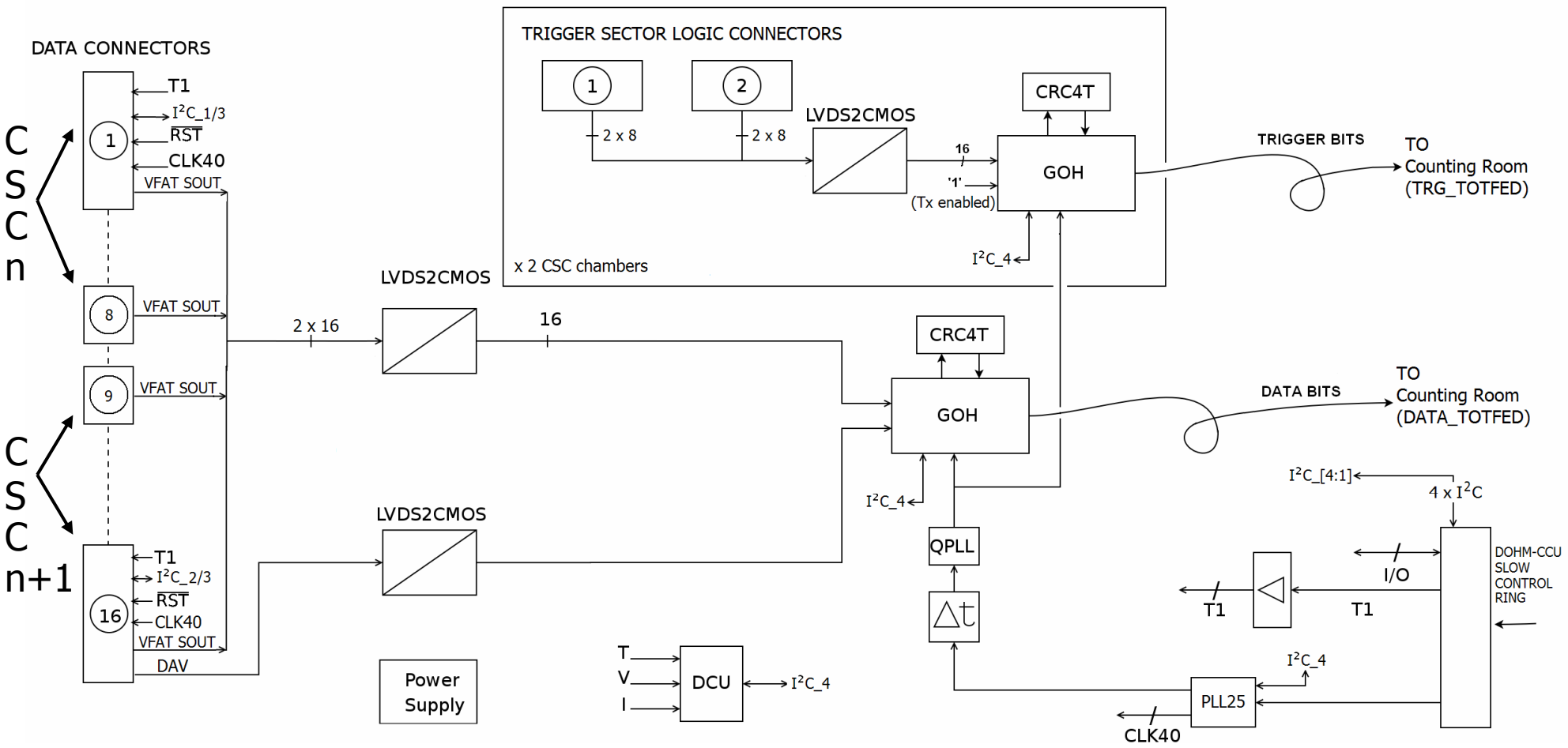
Cathode FE Card block diagram



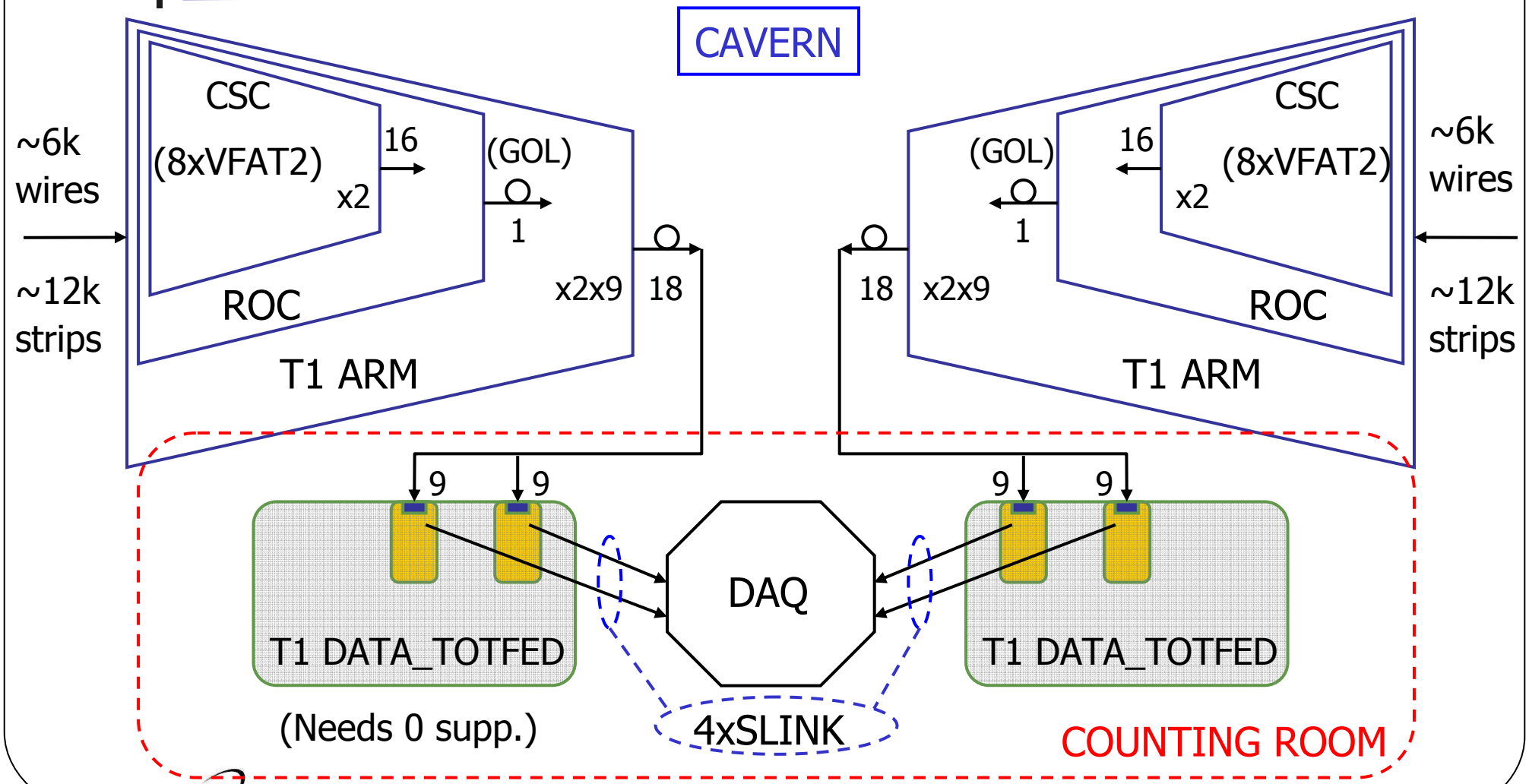
FE sub-system overview



FE Read-Out Card block diagram



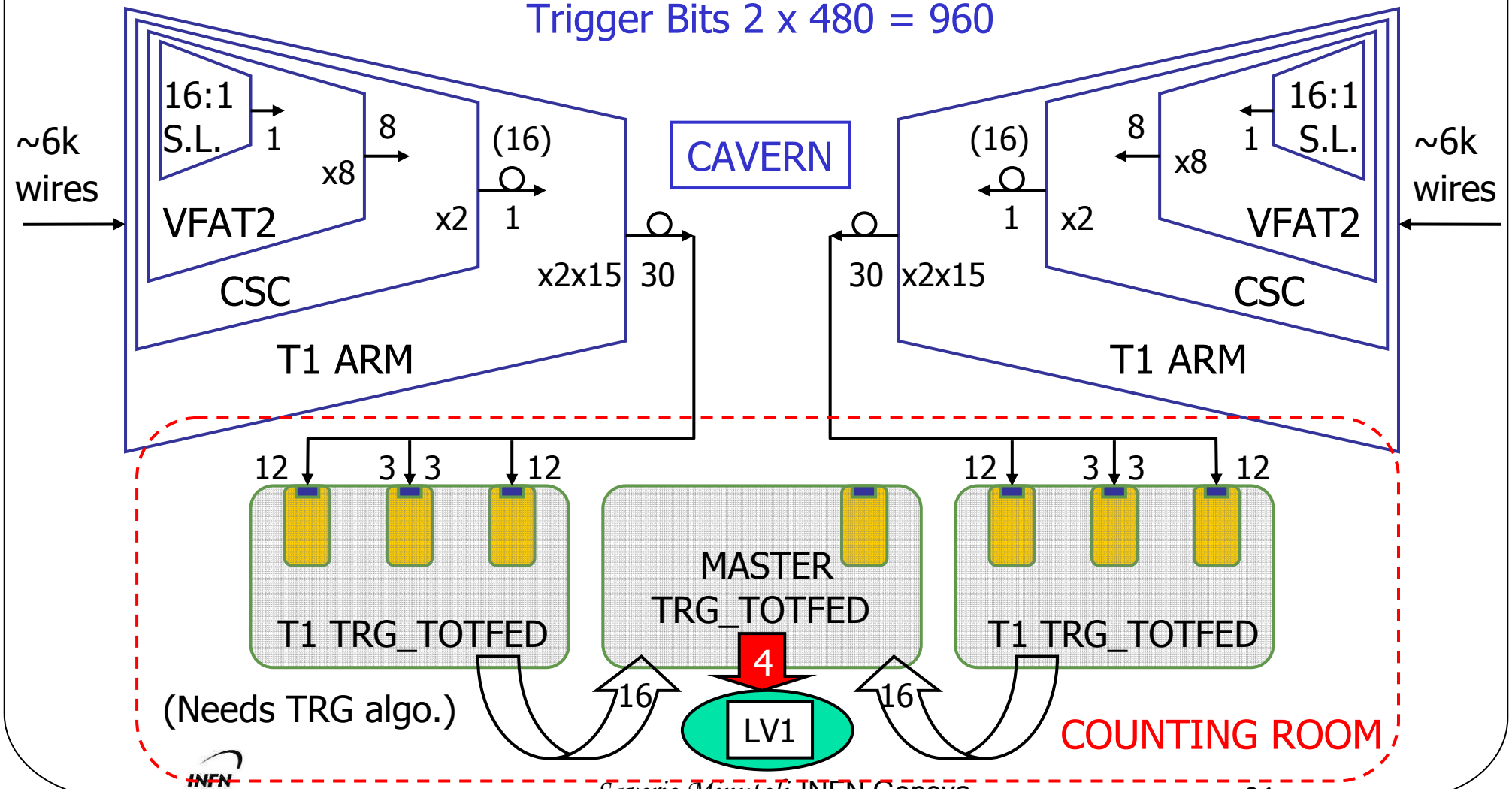
T1 Data architecture



T1 Trigger segmentation

- Only the anodes wires are used to generate trigger informations.
- T1 chambers will use the basic functions included in VFAT2.
- VFAT2 provide fast regional hit information to be included within the CMS First Level Trigger (LV1).
- Anode wires channels are grouped together to form sectors. A hit channel in a given sector will set an LVDS output assigned to that sector to a logic "1".
- The assigment of channels to sectors is programmable.
- There are 8 LVDS sector outputs available.
- T1 trigger set-up use all of them, conseguently, the 128 channels are divided into eight equal regions.
- Sector 1 (S1) will contain channels 1 to 16, sector 2 (S2) will contain channels 17 to 32 etc.

T1 Trigger architecture



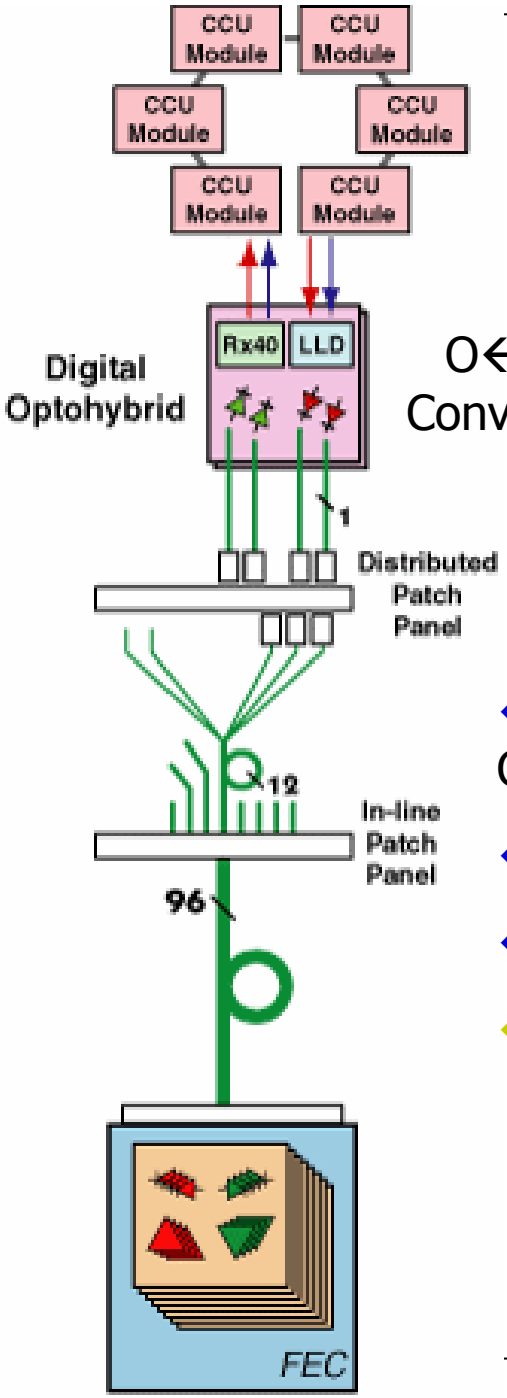
Data rates

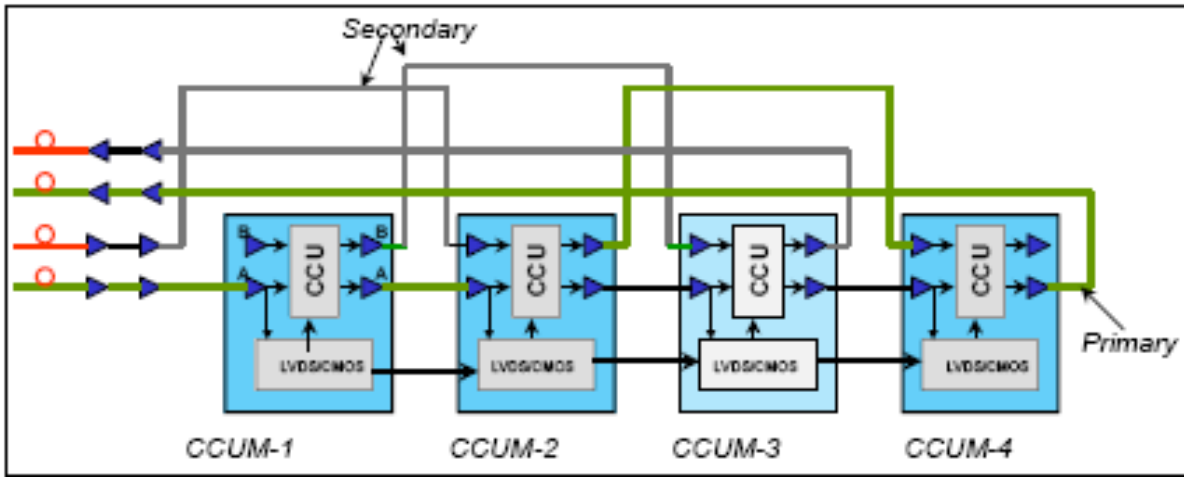
Assuming the highest LV1 rate of 100 KHz.

A single FRL can sustain up to 1.6 Gb/s with event size ≤ 2 kB.

- 8 ROC for each half (half T1 arm):
  - 9 data GOL, but only 7.5 are full
  - Need a zero suppression on DATA_TOTFED
  - 15 trigger GOL
- FRL data size= 128(chs)*16(VFAT)*7.5/8=1920B < 2kB
- Boards needed:
  - 2 data TOTFED with 2 mezzanines each
  - 2 trigger TOTFED with 3 mezzanines each

Slow Control Ring architecture

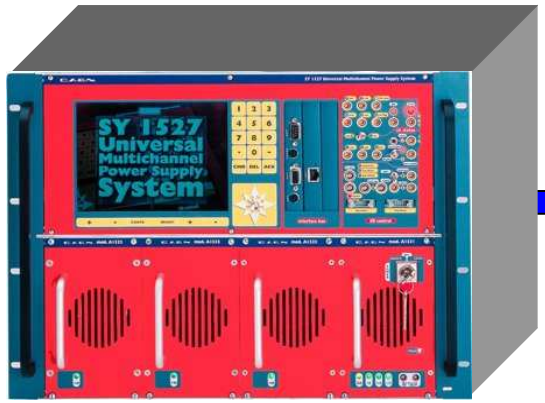




Fault repair configuration example.

- T1 will use the same CMS control ring components (DOHM-CCUM_TOB_TEC) and configuration.
- The modules shall be connected to guaranty the system redundancy
- T1 need a DOHM and a loop of 6 CCUM for each arm.
- Limitations due to the short ring length:
  - Max distance between CCUM modules 50-60cm
  - Total max ring length 2-3m
  - I^2C line max length ???

H.V. architecture



SCADA
OPC
Server

DCS

Patch -Panel

3 x R.M.

2

2

Patch -Panel

R.M.

15
SHV

Patch -Panel

15
SHV

R.M.

R.M.

15
SHV

Patch -Panel

15
SHV

R.M.

Patch -Panel

R.M.= 52 Radiall Multipin

A1733B
28 Channels
3 kV/3 mA or
4 kV/2 mA

Low Voltages

- Voltages:
  - -10V, -5V, +5V, +2.5V
- Current (1/4 T1):
  - CFEC: 4A@-10V; 4A@-5V; 70A@5V; 30A@2.5V
  - AFEC: 7A@2.5V
- Power Supply:
  - Need to have a local solution.
  - WIENER

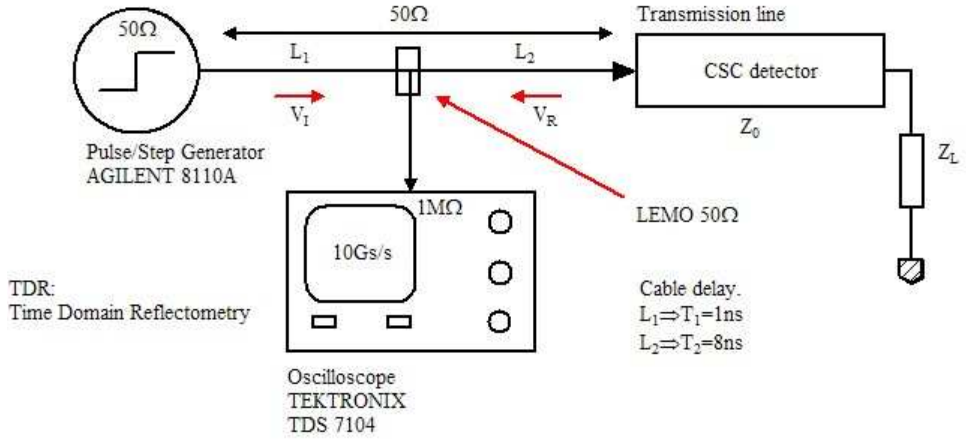
Summary

- The CSC parameters are well known
- We are ready to start with the FE electronic prototypes design.
- VFAT2 can be adopted how complete FE for the CSC anodes wires (only one channel tested):
  - Need an external passive circuit to reduce and adapt the detector signal amplitude.
  - Tests will continue in Genoa, now we are ready to use a new gas mix $Ar/CO_2/CF_4$ → 40/50/10.
- The AFEC are rad. hard., CFEC can operate up to $L=10^{33}cm^{-2}s^{-1}$
- The VFAT digital is of course used in the cathodes FE electronic chain.
- The anodes will be used to generate the trigger bits pattern, the VFAT trigger sector logic function is involved.
- Possible to use the same VFAT mezzanine as T2:
  - We have to check the connectors and the dimensions.
- Needs to check the Control Ring configuration, in particular the maximum electrical cable connections length.
- We agree to use the same low voltages power supplies as CMS.

- Extra slides

CSC transmission line impedance measure

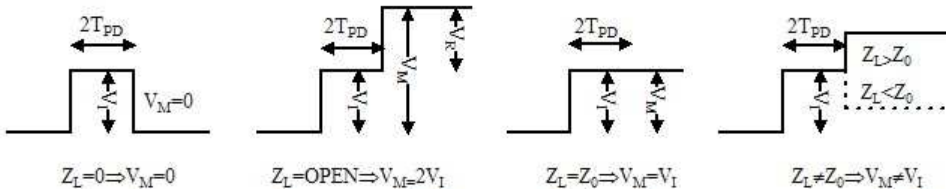
CSC Impedance Test_Bench Set-Up



FORMULARIO:

$$Z_0 = Z_L * \frac{1+\rho}{1-\rho} \qquad \rho = \frac{V_R}{V_I} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

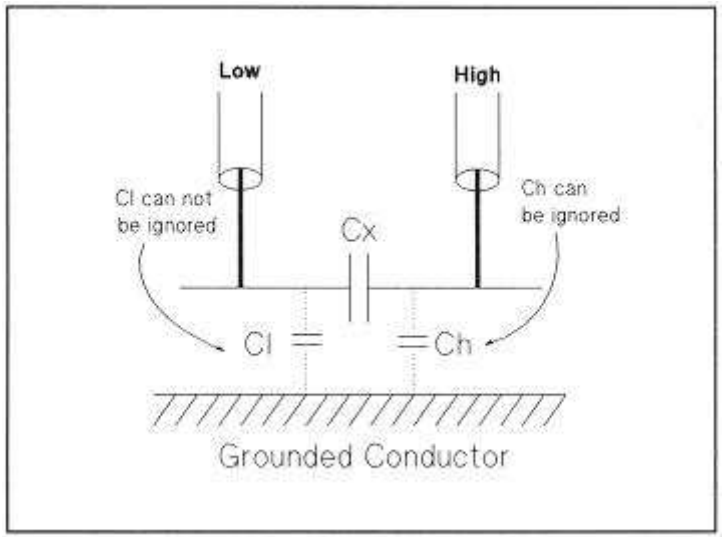
$$Z_L = Z_0 * \frac{V_M}{2V_I - V_M} \qquad V_M = V_I + V_R$$



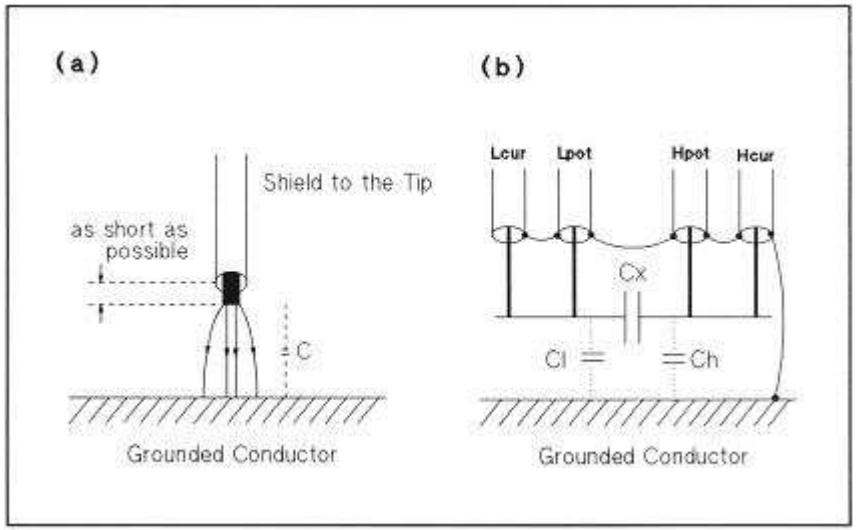
- Pulse 1V@10 ns
- Z_anode=330-390 Ω
  - [R = 115 Ω/m]
- Z_cathode=120-150 Ω

CSC capacitance test-bench

Two and four terminals LCR methods

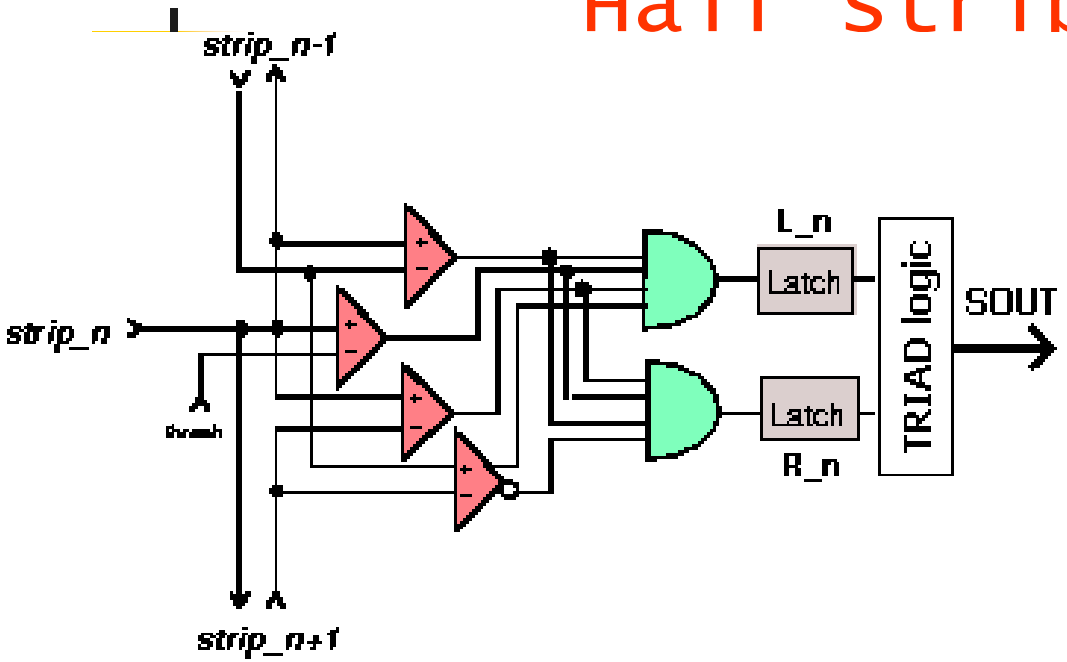


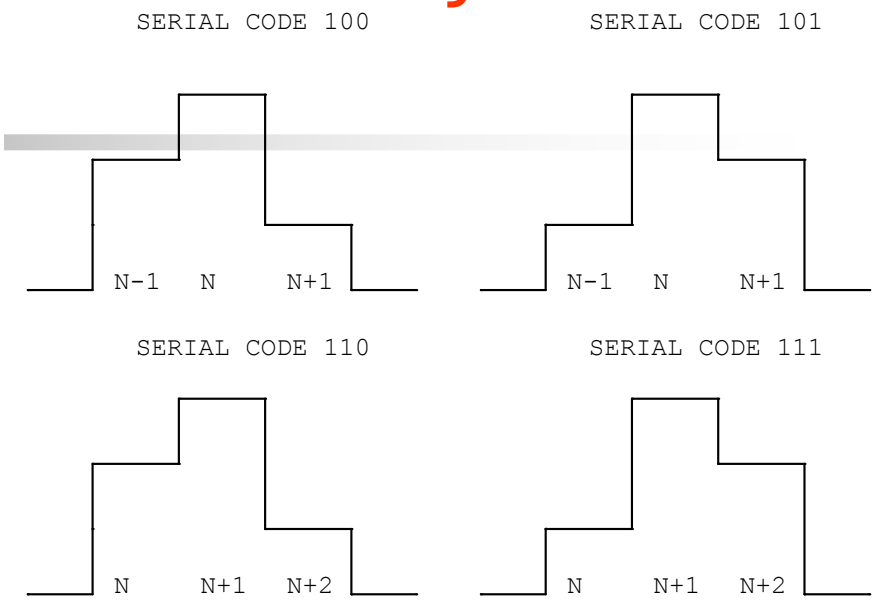
Stray and various parasite cap.



Use of a guard plate and shielding, to minimize test leads stray cap. and noise pick-up

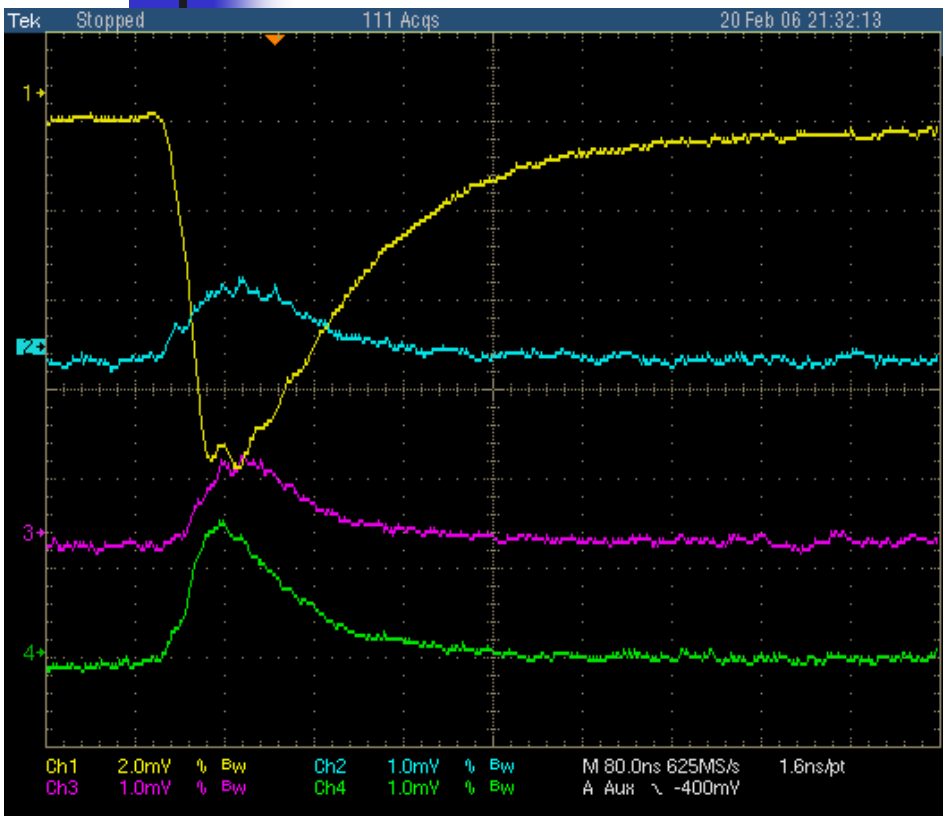
Half strip accuracy

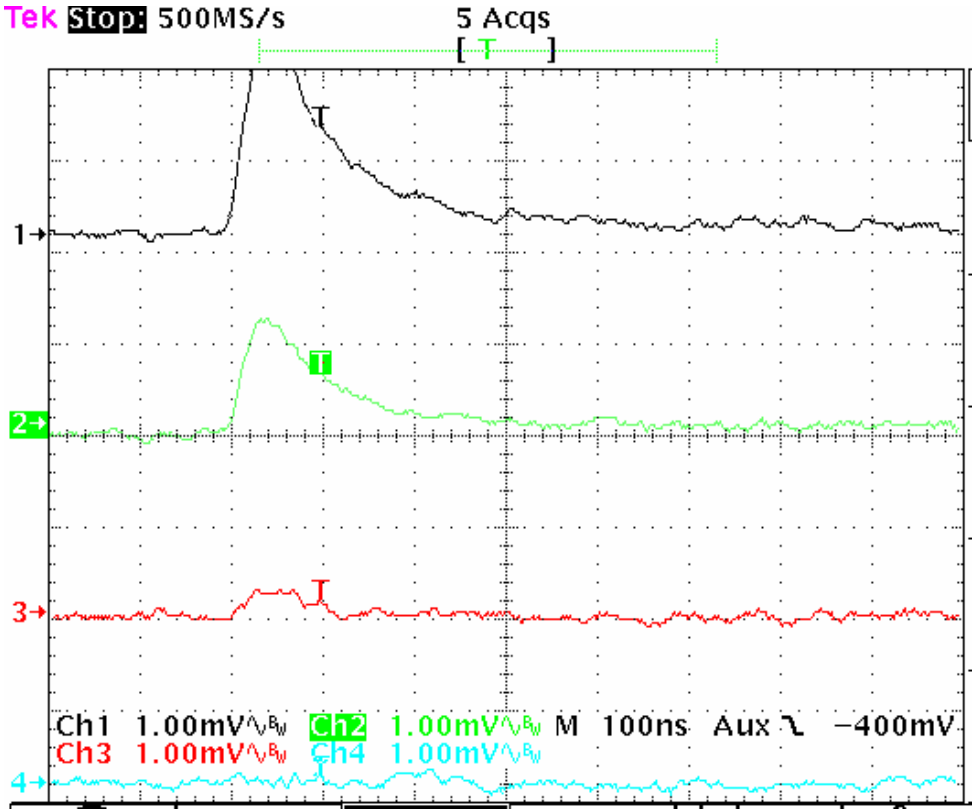




- The LCT-COMP allows to identify the charge distribution on CSC to a half strip accuracy. It permits to give the right or left position of an event within a strip.
- The LCT-COMP logic digitize the position of an event within 2 consecutive strips with a 3 serial bits word. Peaking time adjustable within 25÷200ns.
- The serial data stream are unusable in our system, we need a deserializer.
- The choise could be the ACTEL antifuse programmable devices A54SX32A, tested and qualified up to ~50krad by the INFN-BO group.

CSC Anode and Cathodes





Asymmetric and large distribution charge on cathodes

Side view of a T1 quarter