Commissioning of the Jet/Energy-sum and Cluster Processors for the ATLAS Level-1 Calorimeter Trigger System

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Abstract

The ATLAS first-level calorimeter trigger is a hardware-based system designed to identify high-p_T jets, electron/photon and tau candidates, and to measure total and missing E_T. The trigger consists of a Preprocessor system which digitises 7200 analogue inputs, and two digital multi-crate processor systems which find jets, measure energy sums, and identify localised energy deposits (electron/photon and tau candidates). In order to provide a trigger quickly enough, the hardware is parallel and pipelined.

Experience so far of the Jet/Energy-sum and Cluster Processor system production, commissioning, and integration into ATLAS will be described.

I. THE ATLAS LEVEL-1 CALORIMETER TRIGGER ARCHITECTURE

The ATLAS Level-1 Trigger is the first part of the three stage triggering system designed to select interesting events from the raw rate of 1 GHz of proton-proton interactions. The target for the Level-1 Trigger system is to reduce the event rate down to a maximum of 75 kHz before passing region-of-interest (RoI) event information on to Level-2 Trigger [1].

The Level-1 Trigger system consists of three parts: the Calorimeter Trigger, the Muon Trigger and the Central Trigger (CTP) as shown in figure 1.

The Level-1 Trigger works on reduced-granularity data from the calorimeter and muon systems. The Calorimeter Trigger is based on trigger towers, covering calorimeter cells of 0.1×0.1 in $\eta \times \phi$. Potentially interesting events are selected by identifying electron/photon candidates, jets, single-hadron/tau candidates, missing transverse energy, and total transverse energy.

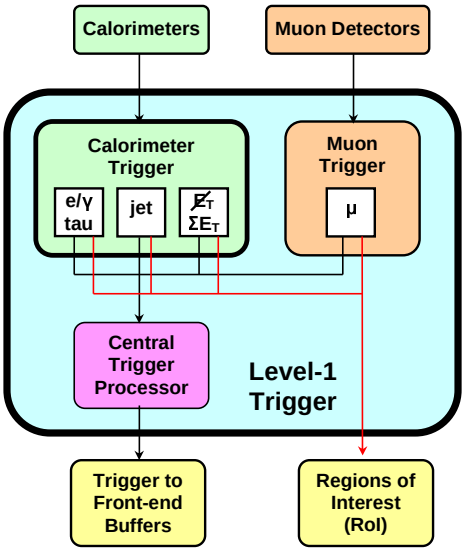

Figure 1: ATLAS Level-1 Trigger

Within the Level-1 Calorimeter Trigger there are four main subsystems as shown in figure 2 [2]: the Preprocessor, which performs signal digitisation; the e/gamma/tau Cluster Processor and Jet/Energy-Sum Processor, which contain the trigger algorithms; and the Readout Drivers, which collect DAQ and RoI information. Real-time results from the calorimeter trigger are sent to the Central Trigger Processor where the final Level-1 trigger decision is made.

The Preprocessor subsystem consists of 124 9U Preprocessor modules (PPM) spread over 8 crates. The Preprocessor digitises each trigger tower signal at the beam-crossing rate of 40 MHz, and feeds these data over high-speed LVDS links to the two algorithmic processors. This subsystem is described in detail elsewhere in these proceedings [3].

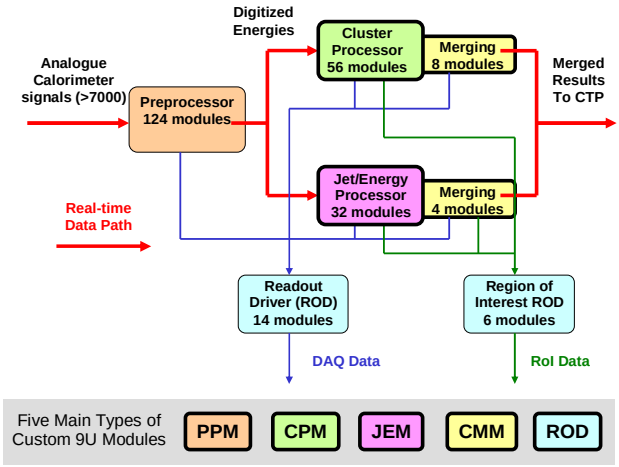

Figure 2: Level-1 Calorimeter Trigger

The trigger electronics is partitioned into azimuthal quadrants of the calorimeters. The e/gamma/tau trigger occupies 4 crates, one per quadrant, and the jet/energy-sum trigger occupies 2 crates with 2 quadrants per crate. The algorithm of event selection of the ATLAS Level-1 Calorimeter Trigger system is implemented in hardware, with the use of FPGAs to allow flexibility.

To process each trigger tower, the physics algorithms must examine their nearby environment of trigger towers. In the case of the Cluster Processor this is a 4×4 grid of trigger towers from both the electromagnetic and hadronic calorimeters. These 4×4 windows slide in both eta and phi directions, and overlap each other. Thus a very large amount of data has to be duplicated and shared between processing units (FPGAs, modules and crates). The fanout scheme adopted is that for data coming from a quadrant boundary (fanout in phi) the duplication is done using extra LVDS links from the Preprocessor. Duplication in the other axis (fanout in eta) is done at the crate backplane between adjacent modules. This duplication on the backplane requires use of high-density connectors with a large number of pins.

There are several outputs from the Level-1 Calorimeter Trigger: the merged real-time hit multiplicity information to the CTP which has a fixed latency, the DAQ data for the Event Builder, and the Region of Interest (RoI) data for Level-2.

II. IMPLEMENTATION

Each e/gamma/tau trigger crate contains 14 Cluster Processor modules (CPM). A CPM processes a grid of 4×16 trigger towers in $\eta \times \phi$ from both calorimeters. Similarly the jet/energy-sum trigger crate uses 16 Jet/Energy modules (JEM), each of which processes a 4×8 grid of summed trigger towers. Both of these modules are physically 9U in size and are shown in the photographs of figure 3 and figure 4 below.

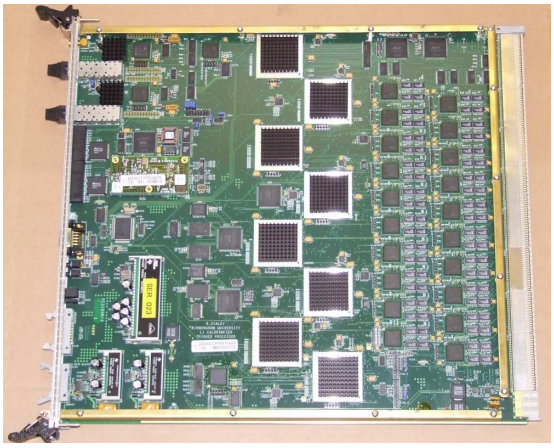

Figure 3: Example of a CPM processor module

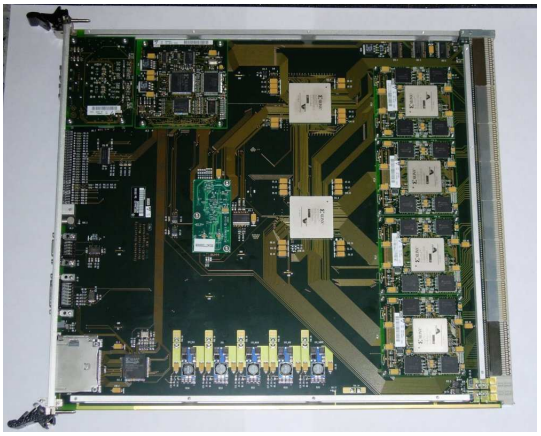

Figure 4: Example of a JEM processor module

Both modules have a common architecture: An Input stage to receive the LVDS serial links from Preprocessor and retime the data for transmission to the algorithm processor FPGA(s), a Merging stage that counts the trigger hits from the algorithm processor, and a Readout stage that transmits DAQ and RoI data over optical-fibre links to the Readout Drivers. On each module is a daughter-card mounted TTCrx chip that provides the real-time trigger, timing and control signals for the module.

All logic functions are contained within FPGAs. The serial links are implemented using commercially available chip-sets from National Semiconductor [4], and Agilent [5].

Some characteristics of both modules are shown in table 1 below:

	CPM	JEM
Backplane connector i/o	58 Gbit/s in 28 Gbit/s out	45 Gbit/s in 15 Gbit/s out
Input Stage	20 FPGAs	4 FPGAs
Processing Stage	8 FPGAs	2 FPGAs
Merging Stage	2 FPGAs	
Modules in system	56	32

Table 1: Characteristics of processor modules

Each processor module sends its real-time hit results over the backplane to a pair of Common Merger Modules (CMM) which merge the hit information from all processor modules in the crate. The CMMs send their sums over a cable link to a final pair of CMMs (so called System CMMs) where the results from all crates within the trigger subsystem are added and then transmitted to the Central Trigger Processor (CTP). The CMMs use FPGAs to sum the hit information. These are configured with different firmware that depends upon which crate they occupy. In a CP crate, e/gamma/tau clusters are counted, but in a JEP crate one CMM counts jets while the other sums missing and total E_T.

Within each processor crate there is also a Timing and Control Module (TCM) and a CPU module. The TCM receives the ATLAS TTC information from an optical-fibre and distributes this electrically over the backplane to the TTCrx chip on every module in the crate.

Prior to installation of the crates at CERN, there has been extensive testing of the manufacture and operation of all modules at the home institutes. The modules have been designed to make use of JTAG/Boundary Scan techniques to check the PCB assembly. The modules are then tested within subsystems, and then complete crates are built and tested, before being shipped to CERN. This testing has been described at a previous conference [6].

III. INSTALLATION IN USA15

The photographs in figure 5 show all crates of the e/gamma/tau trigger and the jet/energy-sum trigger installed in the underground cavern of USA15 at CERN.

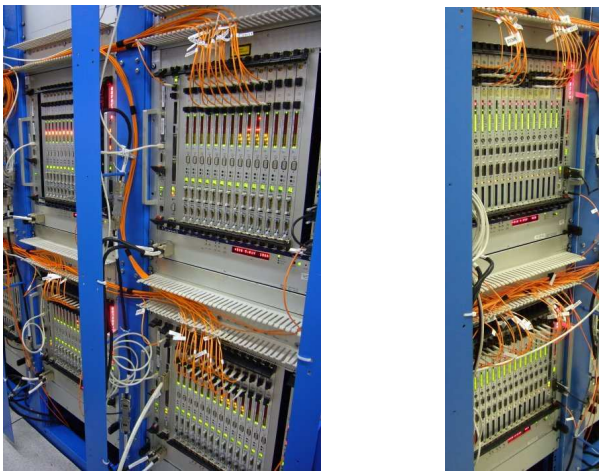

Figure 5: Photographs of the 4 CP Crates and the 2 JEP Crates

A. POWER SUPPLIES

The racks in USA15 at CERN use the commercial LHC remote water-cooled PSUs to supply the crate electronics. The power supplies are mounted on hinges behind the crates and have to use fairly long flexible cable to connect to busbars mounted on the crate backplane. These supplies showed instability in the form of a sinusoidal oscillation at a frequency of about 1 kHz, even when the crates are loaded with only a few modules. A current probe clipped over the power cable showed the oscillation to have an amplitude of ± 50% of the DC value.

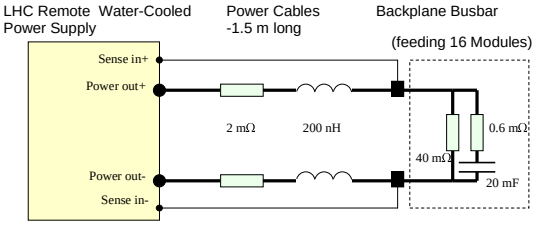

Figure 6: Equivalent circuit of power supply cable and load

The oscillation of the power supply was caused by reactances within the DC power distribution being sufficiently large to produce a phase shift between the PSU and backplane voltage. The inductance of the power cable and the large module decoupling capacitance together create a phase shift of greater than 120° at frequencies above a few kilohertz. The load voltage is sensed by the power supply to correct for changes in current, but with the large phase shift present in this case, the response of the PSU control circuit became unstable. An equivalent circuit of the power distribution circuit with remote sensing is shown in figure 6.

In some crates the instability of the power supply was cured by ensuring the power-ground pairs are tied together, and have any excess length removed, to reduce the loop inductance. The supply decoupling capacitance of the modules has been reduced where possible. However for some crates, the instability was still present, so the remote voltage sensing scheme had to be changed to a local one where the sensing is done back at the power supply. As the cable IR voltage drop is now outside the control of the power supply, this requires the use of extra-thick power cables to minimise the fluctuations in voltage due to load changes. The aim is to keep the load voltage to within 100mV of the operating value. The crates appear to be running without problems due to the change to local sensing.

B. BACKPLANE

The processor crates use a dense high-bandwidth backplane containing about 22,000 pins. After testing the production backplanes using pre-production modules, a few of the backplanes were found to have the odd pin with a defect, either a short to an adjacent pin, or with no connection to the backplane trace. X-ray photographs were taken to understand the cause of the defects, and then all backplanes were optically scanned, and with any defects noted, were sent back to the manufacturer for correction.

During installation, it was discovered by the test software that a pin on one of the CP backplanes had been damaged during module insertion (Figure 7). This is not a random event, but most likely caused by a previously bent pin catching on the module connector. With an estimated insertion force of 370N needed to push the module fully into the backplane, it is near impossible to feel any resistance from a misaligned pin.

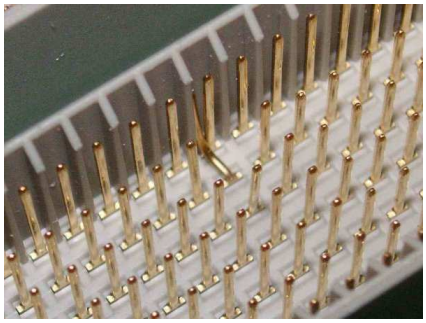

Figure 7: Photograph of damaged connector

The backplane had to be removed from the crate to replace the damaged pin. This has now been successfully repaired and re-assembled into the crate.

IV. COMMISSIONING

A. CABLES

The data into the processor crates comes over a large number of cables carrying high-speed LVDS signals. For example in each JEP crate there are 1368 serial LVDS data links giving an input bandwidth of 547 Gbit/s.

During connection of these cables, anti-static precautions were observed to prevent damage to the electronics at either end. At the end of August 2007 over 1/3 of cables had been checked by software, with only 1 cable pair found to be faulty. Spare cables have been laid alongside the normal cables and will be used if needed. Only very minor errors were found in the initial cable connections: these were straightforward to fix.

B. TIMING

Timing scans are performed throughout the trigger subsystem to set up optimal timing and to check the timing margins of signals transmitted between FPGAs, modules and crates. A few examples of these scans are described below.

The timing-margins of the de-serialised data coming over the LVDS links from the Preprocessor are checked in real-time by adjusting the phase of the capturing clock and then counting the parity errors seen on the data. Software uses the adjustable delay of the TTCrx on the module to step the delay in fine 104 ps increments over a period of 25 ns, and then count any errors received on each link.

A typical plot of a timing scan for the CPM is shown in figure 8, which shows the results of scanning all the LVDS links on a CPM, displayed as 20 groups of 4 LVDS links. Empty cells represent timing values with no errors. The error-free margin of 18 ns shown is more than adequate for these signals.

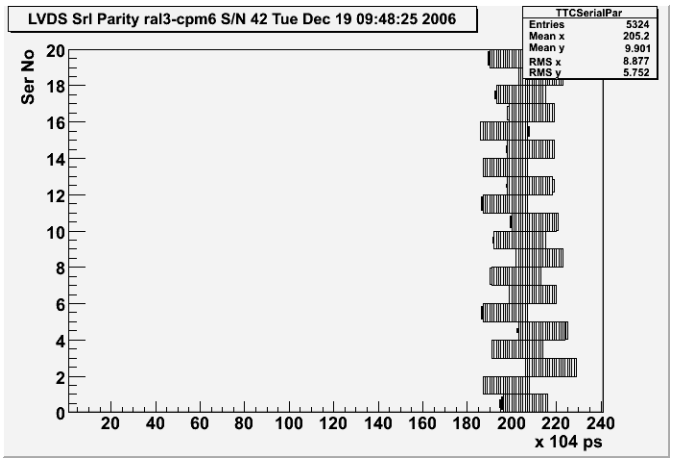

Figure 8: Parity error free timing window for incoming 80 LVDS links on a CPM.

Similarly figure 9 shows a timing scan of the intra- and inter-module 160 Mbit/s links. This shows the combined errors for all 108 inputs to each of the 8 processing FPGAs on a CPM. This scan spans the link bit-period of 6.25 ns. An error free window of at least 2 ns is seen on all signals, which is satisfactory for operation of these links.

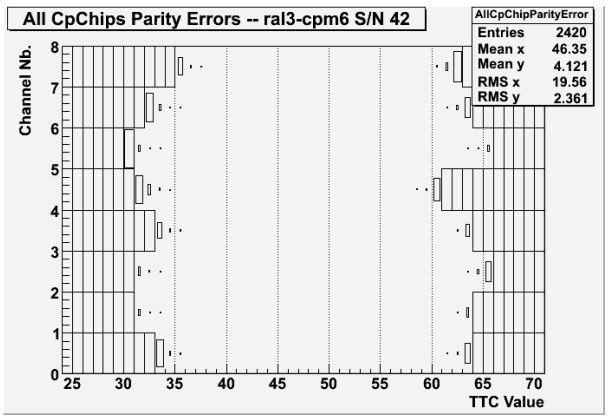

Figure 9: Error free timing window for inputs to the 8 FPGA chips on a CPM. 1 TTCrx step = 104 ps.

V. INTEGRATION INTO ATLAS

Tests of all downstream links have been performed. Data sent to the Readout System and Region of Interest Builder showed no corruption. The links to the Central Trigger Processor have been commissioned.

All crates within the Level-1 Calorimeter Trigger are now connected to the global Detector Control System (DCS). The crates may now be powered on and off from the ATLAS control room. Every module within these crates contains a CAN micro-controller that reports the various voltage, current and temperature readings within the module using the CANopen protocol over a separate CAN bus. Figure 10 shows a screen-shot of the status panel as seen from the ATLAS control room.

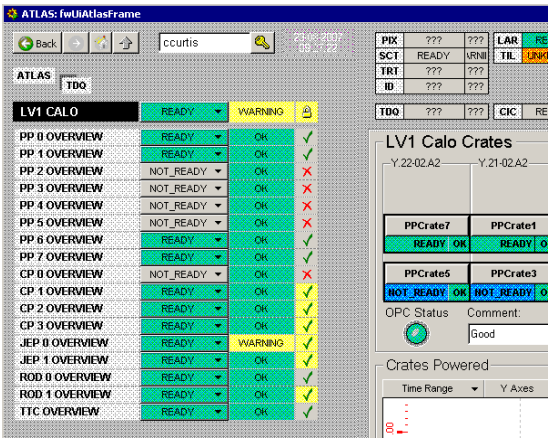

Figure 10: Part of L1Calorimeter DCS status panel.

At the time of writing most of the modules are visible to the global control station. This is work in progress.

VI. M4 COMMISSIONING RUN

The M4 commissioning run took place over a period of two weeks at the end of August 2007, using cosmic signals to provide the data. The hardware available for the run was as follows: 4 out of 8 Preprocessor crates; both JEP crates; 3 out of 4 CP crates.

2 ROD crates were partially filled with 9 ROD modules to provide the following readout: 4 RODs for Preprocessors, 1 DAQ plus 1 RoI for JEP, and 2 DAQ plus 1 RoI for CP crates.

The Level-1 Calorimeter Trigger was able to join the combined run a number of times during the period and ran continuously over the final weekend. Detector signals were aligned within the Preprocessor using calibration pulses, and cosmic data from the calorimeters was seen. Stable readout from more than 100 modules was performed. This is about half of the final system. Data was sent to the RoI Builder, recorded and verified correct.

VII. LESSONS LEARNT

Installation of the cables for the Level-1 Calorimeter Trigger was a major task. This involved three technicians going out to CERN for 1 week in every 3 over a period of 2 years.

The power supplies used at CERN are different from those initially used at the home institutes. Crates should be tested using the final power supplies as soon as they become available. This includes using identical wiring. Not only was instability present, but also the noise level and power-up time is different.

Cable support and strain relief for the cables entering and leaving crates required serious attention. Consulting a mechanical engineer early on in the design cycle would have benefited the manufacture and assembly of these parts.

The architecture and design of the trigger system had to be frozen several years ago. Since then, the performance of many components has advanced rapidly. The use of currently available models would have made the design and construction of the trigger much easier.

Newer FPGAs are larger and faster than those presently used. For the processor modules, especially the CPM, larger trigger tower coverage by each FPGA would benefit the PCB layout by needing fewer signals duplicated. These FPGAs have more higher-speed clock resources which would give improved timing margins. The I/O on these devices can run at a faster rate that would allow the LVDS links (with a modified clocking scheme) to run directly into the Processor FPGAs. This would remove the de-serialisation/re-serialisation stage and so reduce trigger latency.

Higher bandwidth connectors are now available with sufficient density to build very high speed backplanes with differential links operating at Gbit/s rates. These would reduce the backplane pin-count and give a lower insertion force.

VIII. SUMMARY

The installation of the first-level calorimeter trigger hardware is now more than half complete. The commissioning is progressing well, without finding any major problems. Completion of the system is foreseen before the end of 2007.

IX. REFERENCES

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