First Measurements with the ATLAS Level-1 Calorimeter Trigger PreProcessor System

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Abstract

The ATLAS level-1 calorimeter trigger is a hardware-based system with the goal of identifying high-p_T objects within an overall latency of 2.5 μs. It is composed of a PreProcessor system which digitises 7200 analogue channels, determines the bunch-crossing of the interaction and provides a fine timing and energy calibration; and two subsequent digital processors. The PreProcessor plays a central role during integration of the system as it provides digitisation and readout of calorimeter signals and serves as a digital signal source for the subsequent processors. In this presentation the system architecture, the board production testing, and cable installation are described. Results on commissioning efforts and signal integrity tests are presented.

I. Introduction

The enormous rate of proton-proton interactions provided by the LHC machine and the limited readout bandwidth pose strong requirements on the online event selection process. The ATLAS Trigger system is therefore composed of three levels with the first level being entirely realised in programmable hardware. The two subsequent levels are implemented as large computer farms with 500 and 1600 processing units.

The LHC machine collides bunches of protons every 25 ns with about 23 inelastic interactions per bunch crossing at the design luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The purpose of the first-level trigger is a rate reduction from the bunch crossing rate of 40 MHz to a maximum of 75 kHz using a strategy based on the search for high p_T objects measured in the calorimeters such as electrons, jets, etc. The calorimeter trigger combined with the muon trigger and the Central Trigger Processor form the first-level trigger of the ATLAS experiment [1]. The calorimeter trigger is itself composed of a PreProcessor system (PPr) which feeds data into two parallel digital processor systems. The PreProcessor system digitises about 7200 analogue calorimeter signals and determines the bunch crossing of the corresponding primary interaction. The Cluster Processor (CP) searches for electron, photon and tau candidates. The Jet/Energy-sum Processor (JEP) searches for jets and determines the missing transverse energy and the total transverse energy [2] (see figure 1). In addition to the main building blocks there are several additional components satisfying various infrastructural purposes which are used in the system for clock distribution, configuration and monitoring etc.

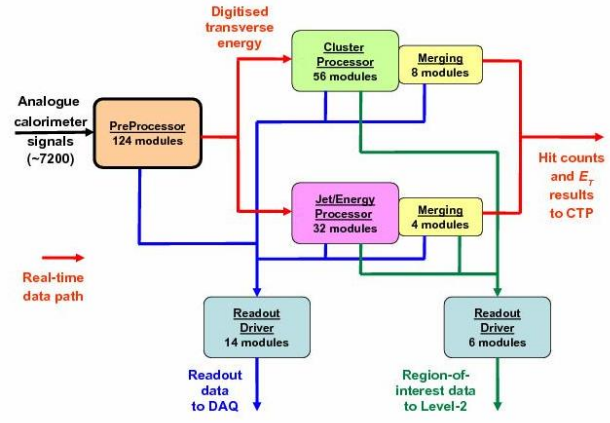

Figure 1: The different components of the level-1 calorimeter system as explained in the text. In addition to the hardware components also the real-time data path and the readout data path are indicated.

The dataflow consists of two parts: the real-time data path of information for the formation of the first-level trigger decision;

and the readout data path for asynchronous readout of event data on events which are triggered by ATLAS. The ATLAS first-level trigger decision is taken by the Central Trigger Processor, to which summary results are sent by the CP and JEP systems.

II. PreProcessor System

The main purposes of the PreProcessor system are the digitisation of the analogue input signals, the determination of the bunch crossing of the primary interaction and a precisely calibrated transverse energy measurement. These three logical steps as indicated in figure 2 are the basis for the hardware design of the PreProcessor system. The complete system consists of 124 9U VME boards in 8 crates which cover the full calorimeter area with about 7200 trigger channels. Each PreProcessor Module (PPM) processes 64 channels in parallel. It consists of a main board with a total of 23 daughter boards as can be seen in figure 3. The real-time signal processing is performed entirely on the daughter cards.

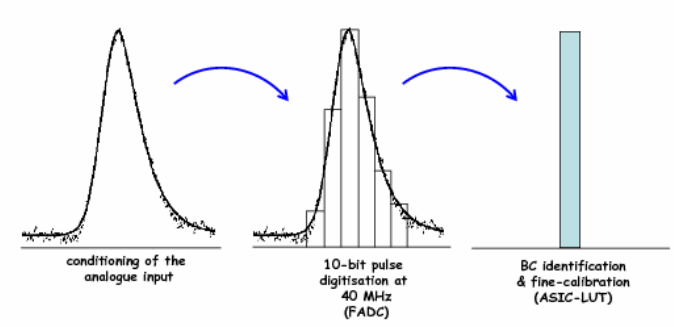

Figure 2: The signal processing chain consists of three steps: digitisation of the analogue signals, determination of the corresponding bunch crossing and finally a fine calibration of the transverse energy measurement.

Analogue trigger signals from the calorimeters are taken off the detector on $30 - 80\,\mathrm{m}$ long cables to a separate receiver system, situated next to the calorimeter trigger electronics, where they are conditioned. The trigger is designed to process transverse energies; e.m. calorimeter signals arrive in that form, but the gains of hadronic calorimeter signals must be adjusted. The receivers include variable-gain amplifiers that also provide precise gain calibration. A system of patch panels before and after the receiver system provides correct signal distribution to the corresponding PreProcessor Modules.

The differential signals are routed using stiff analogue cables with 16 channels each to the front panels of the PPMs. The signals are transformed to single-ended signals and shifted into the appropriate voltage window for the FADC. This processing takes place on Analog Input Cards (the four daughter boards seen on the left side of figure 3) which each process 16 channels.

The unipolar signals are then directed to 16 Multi Chip Modules (MCMs) which each process four channels. These MCMs form the core of the PPM processing. On the MCMs 10 bit FADCs perform the digitisation using a strobe adjustable in $1\,\mathrm{ns}$ steps under control of a special timing chip on the MCM. Subsequently, the bunch-crossing identification is done using a digital filter, and the fine calibration is performed using a look-up table. These are incorporated into a custom-designed application-specific integrated circuit (ASIC) that also includes other functionality as discussed later.

After some further processing (e.g. pre-summing of channels for the JEP system which work at lower granularity than the CP system) the information is serialised and sent using a further daughter card to the Processor systems as LVDS signals.

The board can be read out on receipt of a level-1 accept using a system of ReadOut Driver modules. Raw FADC data and final look-up table results are available. Since the processing in the CP and JEP systems as well as data transfer and the final decision by the Central Trigger need time, the digitised data (both after digitisation and calibration) are stored in pipeline memories situated in the PPr ASIC. In addition to this the ASICs provide the functionality of playback memories which can be used to test the digital part of the PPM and also serve as a signal source for testing the entire processor system. The playback memory can be used in the normal running mode for the storage of monitoring data. In addition to this the ASIC has built in temperature sensors which can be regularly read out to ensure safe operation of the system. In terms of temperature the MCM is certainly the most critical part of the system, since the density of signal processing is highest here.

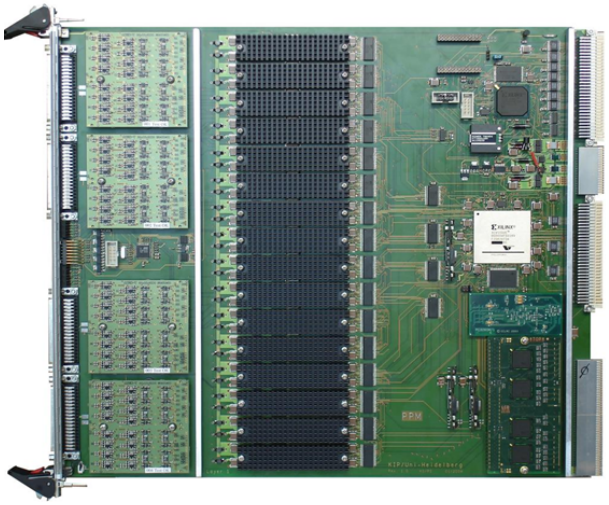

Figure 3: The PreProcessor Module consists of a main board which, apart from infrastructure, carries 23 daughter boards for signal processing, clock distribution, voltage and temperature control.

A so called TTCdec module decodes the clock information and several other time critical signals for use on the board.

The safe operation of the board is guaranteed by a daughter board which holds a digital signal processor using the CAN protocol to transmit temperature and voltage information continuously when the board is switched on independently of whether the other chips are configured.

The configuration and the control of the module is done via a Xilinx FPGA which is connected to all daughter cards and also to a memory chip for the storage of configuration parameters and monitoring information.

III. PPM Production Tests

The production of all components was finished by spring 2007. Some of the components (ASICS, MCMs) had been produced much earlier, and had undergone a thorough testing procedure [3]. In order to ensure the quality of the main boards and the fully equipped PPMs, an extensive test procedure has been developed with an increasing level of complexity. After each board is optically inspected using a microscope, power-up tests are performed, both before and after the daughtercards are mounted on the main board. The fully equipped boards are then operated in a test crate set-up and a series of functional tests are performed. First the input connectors of the PPMs are fed with analogue signals and the conditioning of the input signals is checked. Then the digitisation and processing of pulses from a signal generator is verified. The real-time output is checked by loading digital data in the playback memories and verifying both the signal processing as well as the transmission of the serialised data over $15\,\mathrm{m}$ long LVDS cables. The real-time and the readout data paths are tested with a dedicated VME based system (see figure 4).

The second step is performed in a similar crate set-up to the one installed in the final system with 16 PPMs and the necessary infrastructure. Similar tests as before are performed, however over much longer time periods (typically overnight).

No major problem was observed during the tests, only minor solder problems with the fine pitch MCM connectors which were fixed in the local lab. Rework at the production company was not needed for any of the boards.

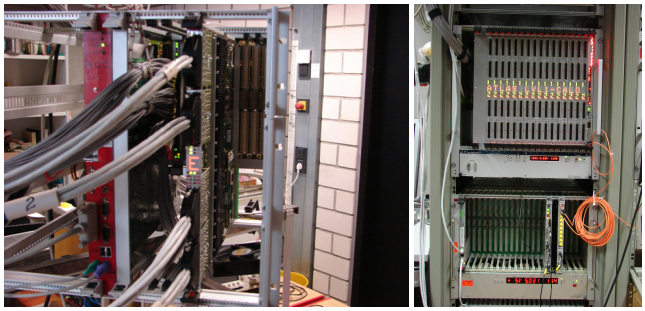

Figure 4: Photographs of the test system. Single board test (left) and full crate test (right).

IV. Installation Status

All eight PPM crates, and a total of 80 PPMs are installed in the electronics cavern at CERN. The cabling of the analogue input signals has been finished and 5 out of 8 crates are equipped with LVDS output cables. Due to the large number of channels and the high channel density on the backplane and the front panel, cabling turned out to be a time consuming and challenging task (see figure 5). In order to connect the LVDS cables in the back of the PreProcessor system a special procedure has been developed which also involves the usage of custom made support tools to hold backplane pieces during the installation. Of great help was the fact that the PPr backplane consists of four pieces which could be cabled up and put in place individually.

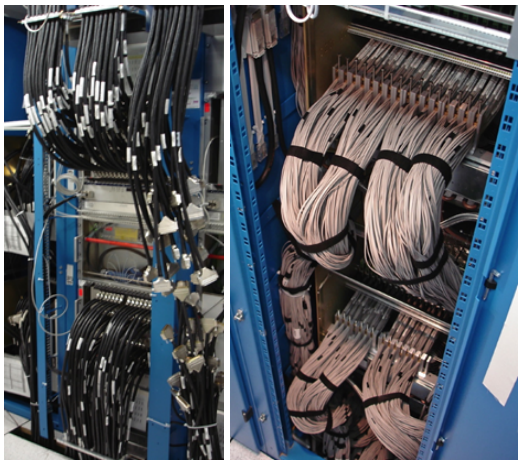

Figure 5: Photographs of the front panel cabling (left) and the backplane LVDS cabling (right).

V. Integration and System Tests

After the installation of the boards in the cavern, a series of tests is performed in order to check the safe and error free operation of the system.

A. Temperature Tests

Directly after switching on for the first time the temperatures are monitored and controlled for several hours. Figure 6 shows the temperature development for one particular channel. The maximum tempereture is reached after about 20 minutes. (The temperature curve starts at about $30^o\,\mathrm{C}$ since there was a setup time needed for the software.) The plateau which is reached is then very stable. Throughout the test the system is run in playback mode with special stress patterns which in the lab system have been found to produce a maximum of power consumption in the system. In the final system the temperature is therefore expected to be below these values.

The measured temperatures for all PreProcessor ASICs are found to be well below $60^o\,\mathrm{C}$ which is taken to be the limit for long term stable operation. Figure 7 shows a map of the maximum temperatures for all MCMs within one crate. The temperature profile shows rising values from bottom to top and some structure depending on the position of the module corresponding well to the configuration of the cooling system. The cold air flows from bottom to top, giving the rise in temperature upwards, and the position of the fans explains the variation in airflow and effective cooling as a function of the position in the crate.

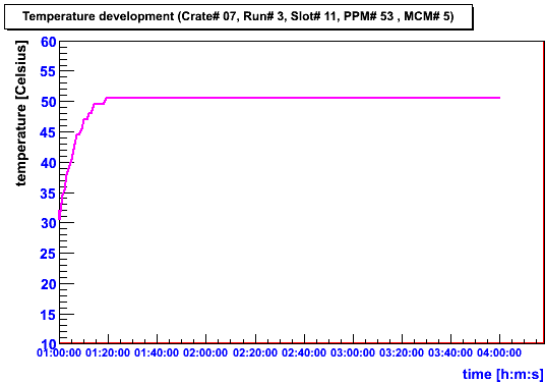

Figure 6: Temperature development as measured on one of the MCMs. The whole timescale is 3 hours.

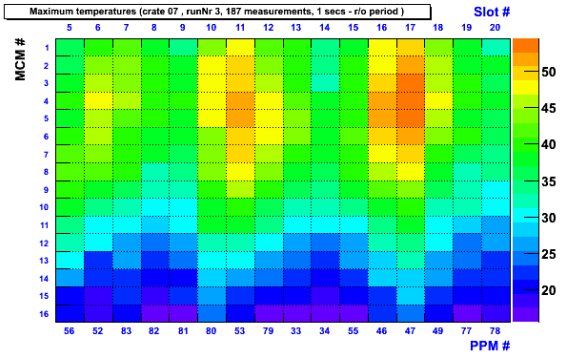

Figure 7: Measured temperatures for all MCMs in one crate fully equipped with PPMs. The observed structures are due to the geometry of the fans and the corresponding airflow profile.

B. *Connectivity Tests*

In order to test the validity of the connectivity of the analogue input channels a series of tests has been performed which use the ability of both the Liquid Argon and the Tile calorimeter to inject test pulses in their electronic chains or alternatively to produce signals using light sources. The signals are then digitised on the PreProcessor and read out using VME access to these boards. The maximum of the pulse is found using a simple algorithm. Figure 8 shows a two dimensional map of the η-ϕ space for some part of the system. The colour coded entries show the maximum of the pulses for the respective channels. The blue areas are parts where no signals were injected and therefore only a constant pedestal can be observed. The red and green areas are channels with signals injected. In the red area slightly higher values were chosen for technical reasons. It can be observed that all channels actually show a signal, however in the left (red) area two channels show a somewhat lower signal which might be a hint for potential problems. Further tests have shown that all channels in this example are actually connected correctly.

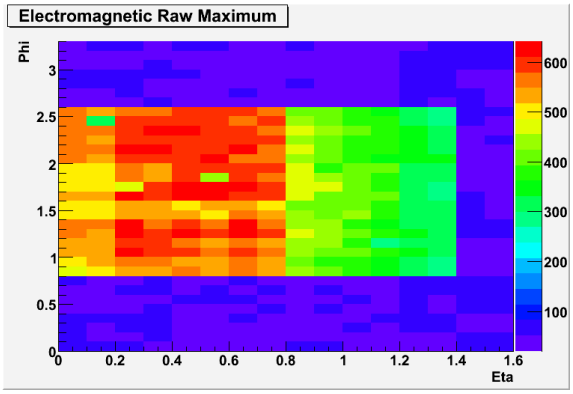

Figure 8: 2 dimensional channel map with the colour coded maximum of the corresponding pulses (see text for details).

In order to check all the channels using an efficient and automatic procedure, a method has been developed for connectivity tests which employs special patterns and therefore reduces the number of tests needed significantly (see figure 9).

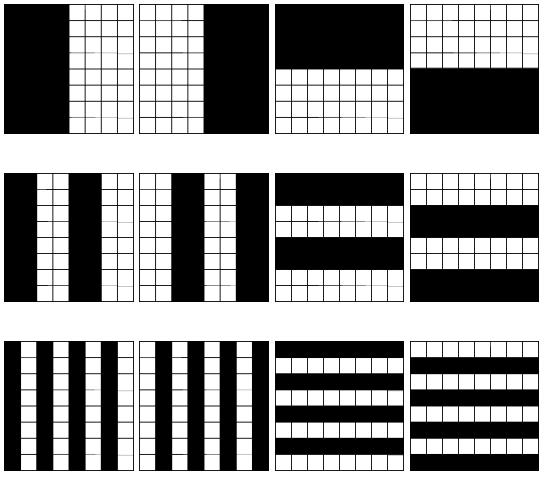

Figure 9: Example patterns which can be used to efficiently test unambigiously the connectivity of systems with a large number of channels. In this example with 64 channels the full connectivity can be tested with just 12 different patterns. This improves for even larger systems.

Figure 10 shows results from a test where several errors were found. The diagram shows again a η-ϕ map of channels with signals. In the middle a strip of channels in blue with no signal can be observed. However in the very left part this pattern is not continuous; this feature was traced back to two input connectors which were erroneously swapped. The red rectangles indicate the contribution from the 4 different input connectors into a PPM. With the exchange of the upper two connectors the problem was fixed.

Furthermore several single channels (in blue) in the red and green area can be observed which indicate no signal on these channels. The reason was found to be broken transformers in

the receiver system which were subsequently repaired. Apart from this also a few PPr channels were found to be malfunctioning.

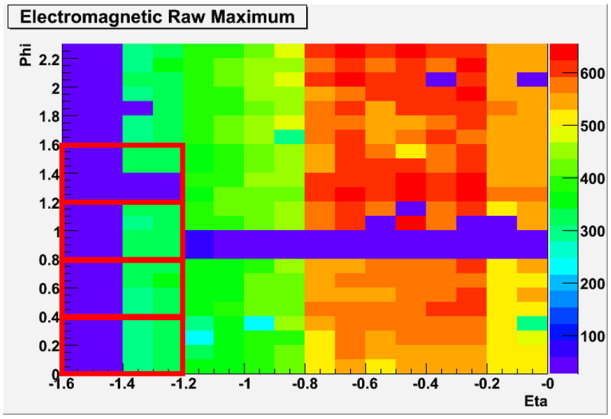

Figure 10: Test result which reveals several faults. Two wrongly connected cables lead to the discontinuity of the blue stripe (see text for details). Blue channels in the red area point to problems on single channels upstream of the PreProcessor system.

A significant percentage of the channels has now been tested for connectivity. However, this activity still has to be completed since at the time of testing, not all calorimeter inputs have yet been instrumented, and the input chain was not completed. Also there are still missing modules in the PreProcessor system itself leading to gaps in the coverage.

The next step in the testing procedure is the measurement of the signal shapes of all the channels. This activity has been started as can be seen in figure 11 where a digitised pulse is shown. The goal is to fit these pulse shapes and to determine defining parameters such as the height and the width of the pulses. Preparatory work on this has been started, however systematic tests have yet to be performed [4].

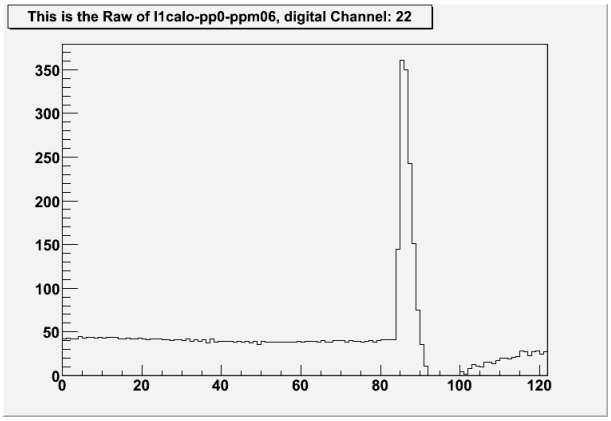

Figure 11: Typical example of a pulse from the LAr Calorimeter with a clear peak and a subsequent undershoot originating in the shaping electronics.

The output LVDS connectivity to the CP amd the JEP system has also been tested as far as this is momentarily possible. For this purpose special data have been loaded into the playback memories of the PPMs which encode the internal channel numbers. When running the system in playback mode these data have been captured in the processor systems and checked for validity. Up to now the LVDS cabling of 4 PPM crates has been tested; only one minor problem has been found which was corrected in situ.

The tests above concern the real-time data path. In addition to this the readout data has been tested using the Readout Driver Modules. For this purpose, the playback mode has been employed. The readout data was compared with the expectation from the loaded data. The system has been found to work well with only a few channels having problems.

VI. Summary

The PreProcessor system of the ATLAS Level-1 calorimeter trigger is currently being built and brought into operation. All components have been manufactured and an extensive test program has been set up in order to test the large configuration parameter space of the hard- and firmware. The yield is very high with only a few minor problems. More than half of the system has been tested and installed in the electronics cavern. The PPr system is used for regular connectivity tests with the calorimeters and as signal source for the digital processors. Up to now only minor problems have been found which were all fixed in place.

Acknowledgements

We wish to acknowledge the work of the ATLAS TDAQ community in providing the underlying online software and infrastructure for triggering, read-out and dataflow. We would also like to thank the ATLAS calorimeter communities, in particular those working on the trigger tower builders and receivers, for their efforts to provide genuine input signals to the trigger. Finally the successful installation of the infrastructure and cabling would have been impossible without the careful work of many technicians connected to the institutes involved.

References

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