Time-Based Circuits for Communication Systems in Advanced CMOS Technology

by

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Abstract

As device size scales down, there have been challenges to design conventional analog circuits, such as low voltage headroom and the low intrinsic gain of a device. Although ever-decreasing device channel length in CMOS technology has mainly negative effects on analog circuits, it increases device speed and reduces the power consumption of digital circuits. As a result, time-based signal processing has been attracting attention because time-based circuits take advantage of high speed and low power devices to deal with analog information in the time domain.

In this thesis, we focus on a ring oscillator as a core time-based circuit for communication systems. Ring oscillators are employed in analog-to-time conversion or time-to-digital conversion. In this work, we present A/D converters and an RF modulator based on ring oscillators in deep sub-micron CMOS processes.

We introduce a VCO-based $\Sigma\Delta$ A/D converter utilizing a *voltage-controlled ring oscillator* (ring VCO) as a continuous-time integrator. We propose to replace conventional integrators designed with analog circuits in a $\Sigma\Delta$ modulator with a ring VCO and a phase detector, thereby implementing an A/D converter without traditional analog circuits.

We also propose a single-slope A/D converter using time-to-digital conversion. By combining a few analog circuits and a ring oscillator based *Time-to-Digital Converter* (TDC), we achieve highly digital A/D conversion.

Finally, we demonstrate a VCO-based RF modulator. The proposed RF modulator generates an RF signal by simply switching transistors. As opposed to an RFDAC approach, the proposed RF modulator is not limited by quantization noise because it employs multiphase PWM signals. A VCO-based OP amp is also introduced as an alternative method of designing an OP amp in deep sub-micron CMOS. The proposed VCO-based OP amp is utilized to generate the multiphase PWM signals in the RF modulator.

This thesis also presents the fundamental limitations of a ring oscillator as a time-based circuit. Although the idea of time-based signal processing employing a ring oscillator has its own limitations such as non-linear tuning characteristics and phase

noise, the basic idea is worth investigating to solve the serious problems of analog circuits for future CMOS technology.

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Title: Visiting Associate Professor of Electrical Engineering

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I extend my thanks to my groupmates. I thank Scott Meninger and Ethan Crain for spending time to tell me of their experience. Charlotte Lau designed the ring VCO in my first chip. Belal Helal willingly discussed many things with me. Chun-Ming Hsu and Matt Park have been my good friends as much as they were great colleagues sharing the same pressure and depression as MIT graduate students.

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Chapter 1

Introduction

Designing analog building blocks in modern CMOS technology is getting more and more difficult as device size scales down. *International Technology Roadmap for Semiconductors* (ITRS) predicts that less than 1 V power supply voltage will be needed for smaller than 40 nm CMOS, which leaves a small voltage headroom for analog circuits. Intrinsic device gain is getting lower because of a short channel effect as the channel length of a transistor is getting shorter [1]. These are some of the examples of challenges for analog circuit design in deep sub-micron CMOS processes. It is meaningful to investigate analog circuit topology to solve these problems. However, there is an intriguing trend in using time-based signal processing in order to avoid using analog building blocks which are vulnerable to device scaling.

Time-based signal processing deals with time information rather than voltage or current information. *Pulsewidth Modulation* (PWM) and a phase signal from a *Voltage-Controlled Oscillator* (VCO) are two examples of time-based signals. Absolute voltage or current of those signals is unimportant because analog information is represented by the width of a pulse or the location of a signal edge in the time domain. Therefore, time-based signals do not suffer from the issues of device scaling. Moreover, the ever decreasing channel length of modern CMOS processes helps to improve the resolution of time-based signals because transistors are getting faster.

1.1 Time-Based Signal Processing and Circuits in Modern CMOS Technology

Since time-based signal processing has advantages over conventional voltage or current based signal processing in future deep sub-micron CMOS technology, time-based signal processing has recently been attracting attention from industry as well as researchers.

A digital *Phase-Locked Loop* (PLL) is a good example of the recent advances for the systems employing the time-based circuit concept [2, 3, 4, 5, 6]. One of the most important building blocks in [2, 3, 4, 5, 6] for time-based signal processing is a *Time-to-Digital Converter* (TDC). A TDC converts time information into a digital code. The digital PLLs use a TDC as a phase detector such that the phase difference between a reference clock and a VCO is converted into a digital value. Since the TDC output is a digital signal, a charge pump and a loop filter of the PLLs are replaced with reconfigurable digital filters. By employing a TDC, most of the building blocks of the PLLs are implemented with digital circuits which benefit from Moore's Law.

Time-based signal processing can also be employed to modulate the amplitude of an RF power amplifier [7, 8]. The approach presented in [7, 8] proposes to use pulse-width and pulse-position modulation for amplitude modulation of an RF power amplifier. Since pulse-width and pulse-position modulation is done by a simple switching of transistors, even an RF power amplifier could be integrated onto a single chip without dealing with all the issues related to analog circuits. The proposed approach in [7, 8] proves that the time-based signals such as pulse-width and pulse-position can be translated into the amplitude of an RF signal.

A/D converters employing time-based circuits have also been reported. The approaches in [9, 10] use a *voltage-controlled ring oscillator* (ring VCO) as a quantizer. A VCO converts voltage into frequency, and the output frequency of a VCO is easily digitized by a counter. Thus, the pairing of a ring VCO and a digital counter can replace a quantizer in a *Sigma-Delta* ($\Sigma\Delta$) A/D converter. A *VCO-based quantizer*, which is composed of a ring VCO and a digital counter, will be easily implemented

even in future CMOS processes. The resolution of a VCO-based quantizer is dependent on a device delay; this means that the quantizer's resolution improves by device scaling, and it is thus another example of the advantages of time-based circuits in modern CMOS technology. On the other hand, the A/D converter presented in [11] employs a time-to-digital conversion method for A/D conversion. Once an analog signal is converted into a time-based signal, digitization of the time-based signal can be done in an efficient way with modern CMOS processes because the time resolution of a TDC benefits from Moore's Law.

1.2 A Ring Oscillator as a Time-Based Circuit

In this thesis, we will focus on a ring oscillator as a time-based circuit. A ring oscillator is composed of cascaded delay stages which are readily implemented regardless of device channel length or power supply voltage, as long as digital circuits can be built. Therefore, it is guaranteed that a ring oscillator will be built in future deep submicron CMOS processes. The output signal of a ring oscillator is a time-based signal. We are interested only in the oscillator's frequency or phase information, not in its output voltage. In this work, the time information of a ring oscillator output will be utilized for two purposes: analog-to-time conversion and time-to-digital conversion.

A ring VCO converts an input analog voltage into phase or frequency information. A VCO-based quantizer utilizes the voltage-to-frequency conversion function of a ring VCO. We can also take advantage of the voltage-to-phase conversion function of a ring VCO where the VCO is modeled as a voltage-input phase-output integrator [12, 13].

Digitization of time information is also possible if one uses a ring oscillator by comparing input time information with a delay in a ring oscillator's delay stages [14, 15]. Accordingly, a ring oscillator can also be used for time-to-digital conversion.

In this work, we demonstrate A/D converters and an RF modulator which employ ring oscillators. By presenting the measured results of the prototype chips, we show that the use of time-based circuits, such as a ring oscillator, can serve as an alternative approach to implementing the basic building blocks of communication systems, which

traditionally require analog circuits.

In Chapter 2, we propose using a ring VCO as a continuous-time integrator in a $\Sigma\Delta$ A/D converter. The prototype chip of the proposed VCO-based A/D converter in 45 nm CMOS proves that an A/D converter can be implemented without traditional analog circuits in deep sub-micron CMOS by employing time-based circuits.

In Chapter 3, a single-slope A/D converter utilizing a ring oscillator based TDC is introduced. The proposed single-slope A/D converter is composed of two main building blocks: a voltage-to-time converter and a time-to-digital converter. The voltage-to-time converter requires two analog circuits: a sampler and a current source. Time-to-digital conversion is done in two steps: one through a low-resolution ring oscillator based TDC and the other through a high-resolution multi-path gated ring oscillator TDC which is introduced in [15]. Therefore, the single-slope A/D converter in Chapter 3 requires only two analog circuits, and all other building blocks are implemented by ring oscillators and digital circuits. The prototype chip of the A/D converter in 0.13 μm CMOS shows that the measured resolution and power consumption are mainly limited by the ring oscillator based TDCs. Therefore, better performance of the proposed single-slope A/D converter is expected for future CMOS technology by virtue of device scaling.

In Chapter 4, we introduce an alternative method to designing an OP amp in deep sub-micron CMOS. By using a ring VCO as a continuous-time integrator, we suggest the concept of a *VCO-based OP amp*. The VCO-based OP amp utilizes the analog-to-time conversion function of a ring VCO and requires some simple analog circuits such as an RC filter, thereby making it possible to build the OP amp even in 45 nm CMOS. In order to demonstrate the feasibility of the proposed VCO-based OP amp, we introduce an RF modulator driven by multiphase PWM signals which are generated by the VCO-based OP amp. The proposed RF modulator creates RF signals by simply switching transistors, and the baseband signal is generated by the PWM signals. The baseband PWM signals are generated by the VCO-based OP amp. Using ring oscillators, Chapter 4 demonstrates a novel RF modulator architecture which is compatible with deep sub-micron CMOS processes.

This thesis is concluded in Chapter 5. The presented A/D converters and an RF modulator employing time-based circuits are summarized. The fundamental limitations of a ring oscillator as a time-based circuit are also discussed based on the measured results of the three prototype ICs presented. Finally, the benefits and drawbacks of time-based signal processing of an analog signal utilizing a ring oscillator will be described.

1.3 Primary Contributions

In this thesis, three prototype chips are fabricated to demonstrate the feasibility and limitations of the systems employing time-based circuits, especially a ring oscillator, in deep sub-micron CMOS technology. A ring oscillator is the core circuit building block of this thesis for two important functions: analog-to-time conversion and time-to-digital conversion. This work proves the validity of the concept of the proposed system architecture using time-based circuits, and also presents the fundamental limitations of a ring oscillator by showing the measured results of the three prototype chips. With respect to time-based circuits for communication systems, the main contributions of this thesis are:

- The demonstration of a second order $\Sigma\Delta$ A/D converter utilizing a ring VCO as a continuous-time integrator in 45 nm CMOS process.
- The analysis of the proposed ring VCO-based $\Sigma\Delta$ A/D converter by applying a fractional-N frequency synthesizer modeling technique.
- The demonstration of a single-slope A/D converter employing ring oscillator based time-to-digital converter in 0.13 μm CMOS process.
- The introduction and analysis of the VCO-based OP amp employing a ring VCO as a continuous-time integrator.
- The demonstration of a VCO-based RF modulator driven by a multiphase PWM generator using the VCO-based OP amp in 45 nm CMOS process.

- The analysis and demonstration of the fundamental limitations of a ring oscillator for time-based signal processing.
- The demonstration of the advantages and disadvantages of time-based signal processing by the experimental results of various circuits.

Chapter 2

A VCO-Based Continuous-Time $\Sigma\Delta$ A/D Converter

2.1 Introduction

There has recently been increasing interest in developing highly digital *analog-to-digital converter* (ADC) structures for on-chip testing and ease of integration in future CMOS processes. An intriguing circuit to utilize in such cases is a ring VCO, which outputs a clock waveform whose frequency is a function of an input tuning voltage. By comparing the clock frequency to that of a separate clock reference using digital counters, one can create an ADC that can readily be utilized for on-chip monitoring of supply voltage variations and other on-chip waveforms [16]. Such VCO circuits have also been employed to realize multi-bit quantizers with first order noise shaping, which allow simplified implementation of high order $\Sigma\Delta$ ADCs [9, 17, 18]. A shortcoming of approach [16] is that the effective conversion rate must be quite low to achieve high resolution. Utilizing a multiphase ring VCO contributes to improvement of the resolution, but the conversion rate is still limited [19, 20]. The shortcoming of approaches in [9, 17, 18] is that the overall A/D implementation ends up being primarily analog in nature.

In this chapter, we propose a VCO-based ADC structure that allows second-order $\Sigma\Delta$ noise shaping to be achieved with a highly digital structure along with time-based

signal processing. The proposed VCO-based ADC is implemented in 45 nm CMOS for proof of concept. The proposed ADC can also be implemented in future CMOS technology without difficulty because the ADC is composed of digital circuits and a time-based circuit, which is a ring VCO in this case, and requires no traditional analog circuits. The topology presented here leverages a previously suggested structure for $\Sigma\Delta$ frequency discrimination described in [21]. Our contribution is in showing the utility of this structure for A/D conversion, applying fractional-N PLL modeling approaches [22] to quantify its behavior.

We begin by discussing the integrating characteristics of VCO structures and their application to $\Sigma\Delta$ A/D conversion in section 2.2. We then show the application of the structure in [21] to achieve a second-order $\Sigma\Delta$ ADC in Section 2.3. An analytical model of this ADC based on a fractional-N frequency synthesizer model is then presented in Section 2.4. Unique issues and benefits to the proposed structure are then discussed in Section 2.5 and 2.6. The prototype chip in 0.18 μm CMOS is briefly discussed in Section 2.7. Another prototype chip is fabricated in 45 nm CMOS process to address the issues revealed in the 0.18 μm CMOS prototype. The circuits for the 45 nm CMOS prototype are discussed in Section 2.8 followed by the simulated results of the proposed ADC in Section 2.9. The measured results will be presented in Section 2.10, and the chapter is concluded in Section 2.11.

2.2 Background

VCO-based ADCs typically utilize a VCO and a frequency counter as a quantizer. The approach [16] uses a VCO-counter pair for A/D conversion of supply voltage noise as illustrated in Figure 2-1 (a). The supply voltage noise is sampled and it controls a ring oscillator frequency. A frequency counter following the ring oscillator measures the frequency. As a result, the digital word from the counter is a digitized version of the input voltage. This technique is advantageous since it requires only digital circuits. The resolution improves by reducing the conversion rate. Employing a multiphase ring VCO also helps to improve the resolution, but the improvement is

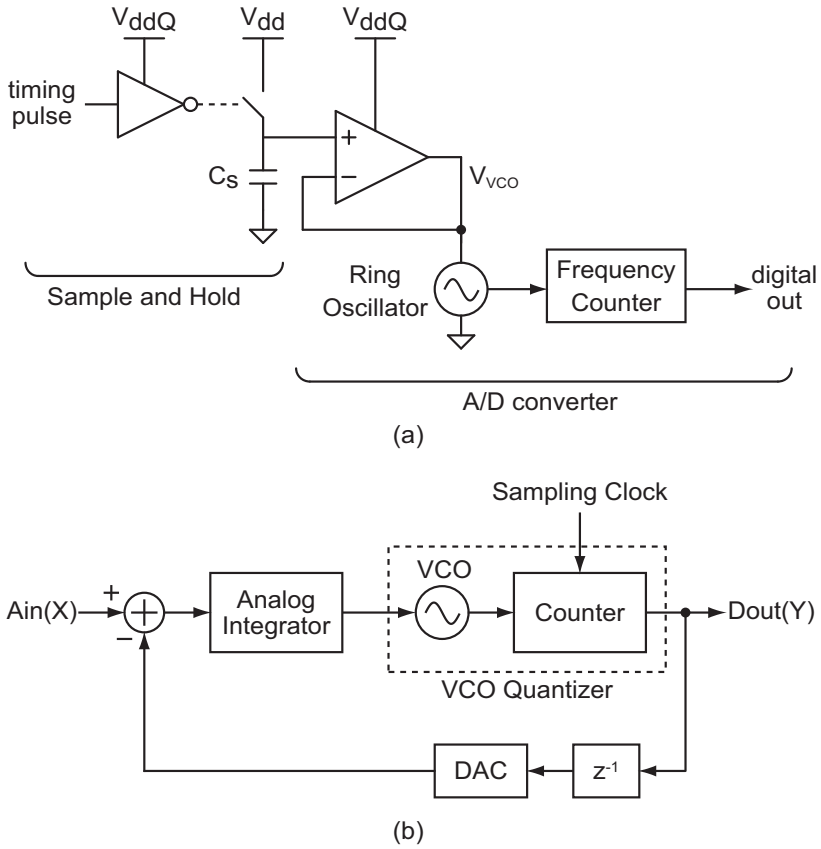

Figure 2-1: (a) Simplified block diagram of a VCO-based ADC of approach [16]. (b) Simplified block diagram of a VCO-based ADC of approach [17].

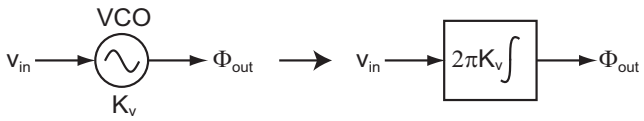

Figure 2-2: VCO as a voltage-to-phase integrator.

limited [19, 20]. On the other hand, the approach [17, 18] use a VCO-counter pair for a multi-bit quantizer of a $\Sigma\Delta$ ADC as shown in Figure 2-1 (b). The main advantage of the VCO-based quantizer over the conventional flash ADC is the inherent first-order noise shaping effect of the quantization noise [17]. As shown in Figure 2-1 (b), however, this approach requires analog circuits including an integrator and a DAC.

A VCO will be utilized as an integrator rather than a quantizer in the proposed VCO-based ADC in this chapter. Figure 2-2 illustrates the classical VCO model used for PLL modeling, which identifies its behavior as an ideal integrator with an input

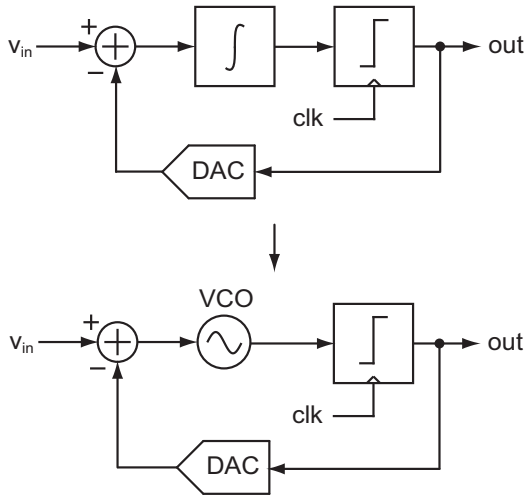

Figure 2-3: A first-order continuous-time ΣΔ ADC employing a VCO integrator.

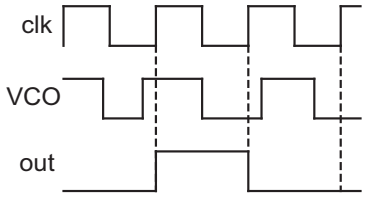

Figure 2-4: Timing diagram of a one-bit quantizer in a first-order continuous-time ΣΔ ADC employing a VCO.

signal in voltage and an output signal in phase. Note that a phase detector can be used to convert the output phase to voltage or current in order to use the VCO as a voltage-to-voltage or voltage-to-current integrator.

Figure 2-3 illustrates how a first-order continuous-time (CT) ΣΔ modulator can be implemented with a VCO. Instead of using a conventional integrator, we use a VCO for an integrator stage in a ΣΔ modulator. The advantage of using a VCO as an integrator is its infinite DC gain. Unlike a conventional integrator, a VCO does not have any leakage mechanism in its integral operation; hence, a ΣΔ modulator employing a VCO does not suffer from issues caused by finite DC gain of an integrator, such as signal-to-noise ratio (SNR) degradation [23] and a dead zone issue [24]. Here we assume that the VCO frequency is essentially locked to the reference clock frequency such that all phase deviations of the VCO are confined to one reference cycle interval. The VCO operates as a voltage-to-phase integrator, thus we need a phase detector to implement voltage-to-voltage or voltage-to-current integrator as

mentioned earlier. However, the phase detector is unnecessary in this case because the one-bit quantizer operates as a one-bit time-to-digital converter — the quantizer output goes to low if the VCO output signal lags behind the sampling clock, and it goes to high if the VCO output signal leads the sampling clock as shown in Figure 2-4. Thus, the output phase signal of the VCO, which is the integral of the VCO input voltage, is quantized and then fed back to the input of the VCO.

Note that a practical VCO requires a band-limited input control voltage to perform accurate voltage-to-phase integration, and a square waveform from the DAC in Figure 2-3 is not band-limited; hence, the integration of the VCO is not accurate in practice. A more practical A/D structure that solves this issue is proposed in the next section.

2.3 The Proposed VCO-Based A/D Converter

It is impractical to replace an integrator with a VCO integrator in traditional $\Sigma\Delta$ A/D architecture because the fast-varying analog signal from a feedback DAC causes inaccurate phase integration of the VCO integrator, as explained earlier. We propose an A/D architecture that solves this issue. The proposed architecture also employs second-order noise shaping for higher resolution. Figure 2-5 (a) and (b) shows the proposed second-order $\Sigma\Delta$ ADC architecture using a VCO as a first-stage integrator, and Figure 2-6 shows an ideal second-order continuous-time $\Sigma\Delta$ ADC as a point of comparison [24, 25, 26]. By using a dual-modulus divider, the quantizer output need not be fed back to the input of the VCO. Therefore, the VCO input is influenced only by a band-limited analog input signal, and accurate voltage-to-phase integration is achieved. Note that the analog integrator stage is implemented with a charge pump and a capacitor as shown in Figure 2-5 (a), and the analog integrator corresponds to the second stage integrator in Figure 2-6. The feedback DAC is also implemented with a charge pump. The charge pump currents and capacitance of the capacitor determines the integrator gain and the feedback coefficient. We use a one-bit quantizer for higher linearity of the quantizer as well as simplicity of its implementation. Note

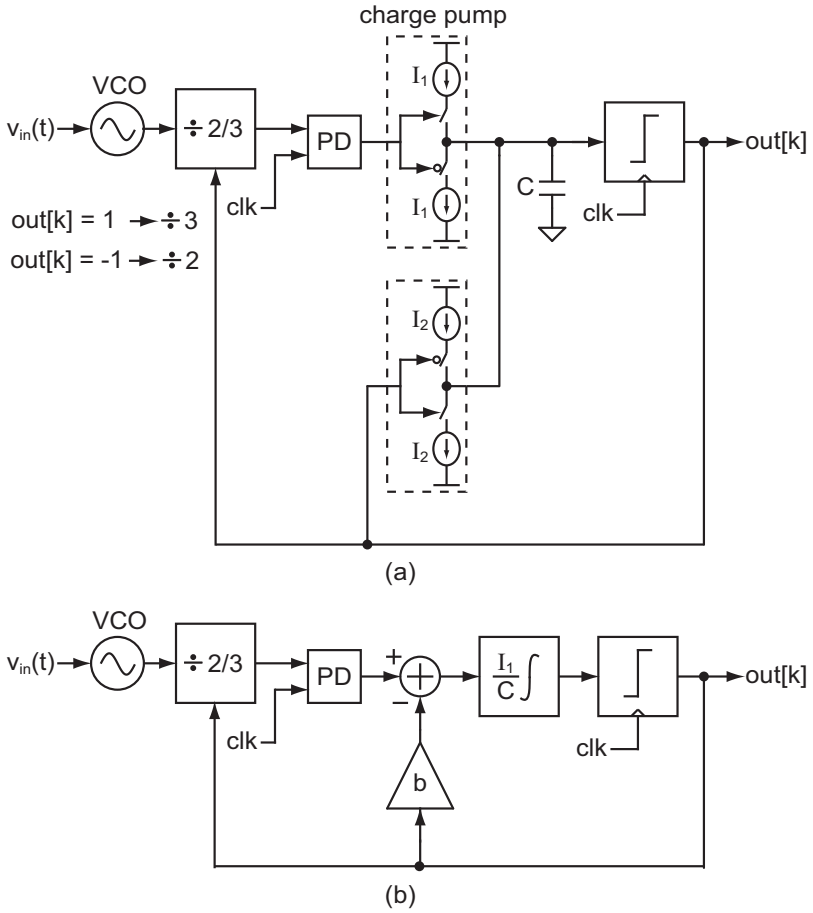

Figure 2-5: (a) Proposed second-order continuous-time ΣΔ ADC employing a VCO. (b) Simplified block diagram of the proposed continuous-time ΣΔ ADC employing a VCO.

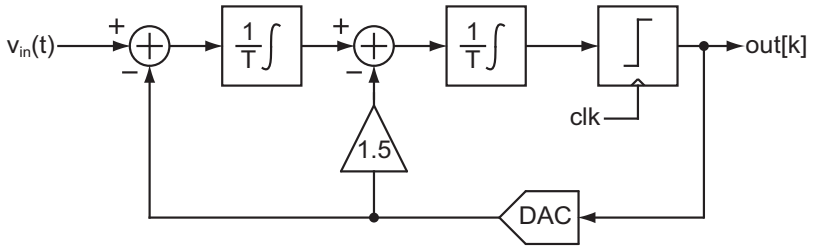

Figure 2-6: An ideal second-order ΣΔ ADC.

that the divide value of the divider is 3 when $out[k]$ is $+1$, and 2 when $out[k]$ is -1.

A similar structure to the one shown in Figure 2-5 has been previously suggested for use as a ΣΔ frequency discriminator [21], which converts the instantaneous frequency of an input signal to a digital sequence. Here we focus on converting the input tuning voltage of the VCO to a digital sequence, so that we are performing

voltage-to-digital conversion rather than frequency-to-digital conversion. The benefit of this structure for A/D conversion is that it performs second-order noise shaping with a highly digital implementation — the only analog elements are essentially the charge pump shown in Figure 2-5 (a).

2.4 Modeling

To understand the operation of the proposed ADC structure in Figure 2-5, consider the linearized analytical model shown in Figure 2-7 (a), which is a direct analogy of the fractional-N PLL model described in [22]. Here the VCO is modeled as an ideal integrator; the multi-modulus divider is modeled as a sampler, accumulator, and scaling factor of $\frac{1}{N_{nom}}$; and the phase detector is modeled as a subtractor and scaling factor of $\frac{\alpha T}{2\pi}$ [22]. Figure 2-7 (a) clearly shows how the quantizer output signal, which is not band-limited, is effectively fed back to the ADC input without impacting the actual VCO input. The signal paths from the VCO input and the quantizer output are physically separated, but the output phase of the divider is the difference between the integration of those two signals as shown in Figure 2-7 (a). Hence, the divider creates an all-digital negative feedback loop that allows the ADC architecture to operate as a second order $\Sigma\Delta$ modulator without the need for fast analog signals at the VCO input. Note that the gain of 0.5 is included in the feedback path so that the appropriate $n[k]$ value is set. In the proposed ADC architecture, a *divide-by-2/3* divider is used, and N_{nom} is 2.5 when the VCO center frequency is properly set [22]. $N[k]$ is 3 and 2, when $out[k]$ is 1 and –1, respectively, as shown in Figure 2-7 (a); hence $n[k]$ should be 0.5 and – 0.5, when $out[k]$ is 1 and –1, respectively [22]. The gain of 0.5 in Figure 2-7 (a) is used to convert the $out[k]$ values to the proper $n[k]$ values.

In the model, the accumulator in the feedback path can be replaced with an integrator as shown in Figure 2-8 because the frequency response of an integrator is approximately the same as that of an accumulator. By replacing the accumulator in the feedback path, the frequency-domain model in Figure 2-7 (a) can be simplified

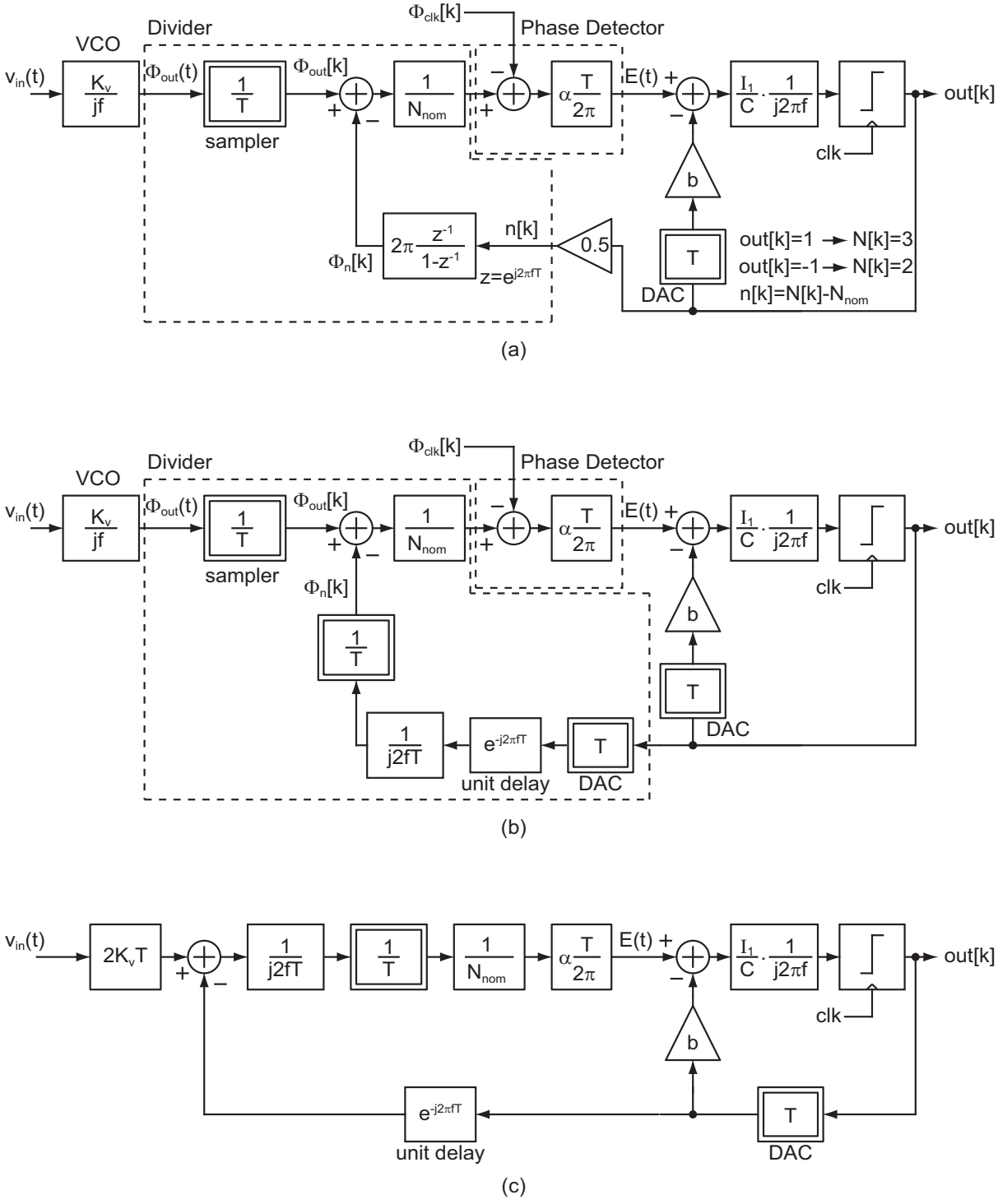

Figure 2-7: (a) Frequency-domain model of the proposed VCO-based ADC. (b) Simplification of frequency-domain model of the proposed VCO-based ADC by replacing the accumulator with an integrator. (c) Final simplification of the frequency-domain model of the proposed VCO-based ADC.

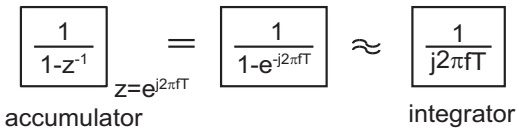

Figure 2-8: Replacement of an accumulator with an integrator.

as shown in Figure 2-7 (b) and finally Figure 2-7 (c). One can easily see the analogy of the model to an ideal ΣΔ ADC by comparing Figure 2-7 (c) and Figure 2-6. Note that $\Phi_{clk[k]}$ is always zero because it is the reference phase so that it is omitted in the model in Figure 2-7 (c).

Given the simplified model in Figure 2-7 (c), design of the ADC follows that of classical second-order ΣΔ ADC structures. In particular, the feedback gain in Figure 2-5 (a) should be appropriately set to realize second-order noise shaping in a stable manner.

Note that there is a unit delay in the feedback path of the simplified model in Figure 2-7 (c). The delay in the feedback path generally causes a stability issue in a high-order ΣΔ modulator. However, CppSim behavioral level simulation [27] shows that the proposed ΣΔ modulator is stable with the second-order configuration. Theoretically achievable SNR of the proposed VCO-based ADC may be lower than the ideal second-order ΣΔ modulator shown in Figure 2-6 because of the delay in the feedback path. However, in-band noise floor is dominated by the input referred noise such as device thermal noise of the conventional ΣΔ modulator and VCO phase noise of the proposed ADC rather than by the quantization noise. Hence, SNR degradation due to the delay is negligible in reality.

2.5 Phase Locking Range Issues

The proposed ADC structure introduces a unique constraint over that of a classical ΣΔ ADC, in that the VCO center frequency must be appropriately set. This constraint is imposed by the fact that the phase detector within the proposed VCO-based ADC must operate within its phase locking range (i.e., cycle slipping must be avoided) in order to achieve the desired ΣΔ noise shaping behavior. Therefore, the

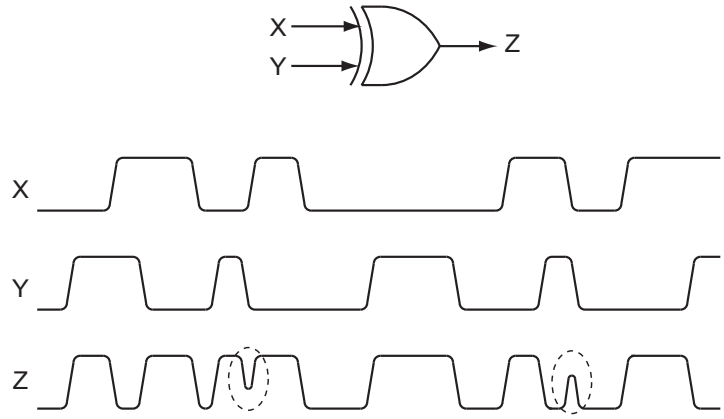

Figure 2-9: Failure of XOR operation due to finite rise and fall times of the input signals.

center frequency of the VCO should be set to be N_{nom} times the clock frequency, where N_{nom} corresponds to the nominal divide value [22]. As an example, in the simulation results presented in Figure 2-10, N_{nom} equals 2.5 and the reference clock frequency equals 800 MHz, so that the center frequency of the VCO should be set to 2 GHz.

The phase detector locking range also sets the achievable dynamic range of the proposed ADC. Since the output frequency of the VCO varies by the signal level of its input tuning voltage, a large input signal level causes a rapid phase change that can, in turn, cause the phase difference seen by the phase detector to go outside its locking range. The $\Sigma\Delta$ loop operation fails if the phase detector incurs cycle slips — this condition corresponds to a classical $\Sigma\Delta$ ADC becoming unstable due to the saturation of an internal integrator. In addition, the saturation of internal integrators can happen to the charge pump/capacitor integrator in the proposed ADC structure. However, CppSim behavioral simulation [27] of the proposed architecture shows the cycle slips occur before the saturation of the charge pump integrator. Therefore, the locking range of the phase detector in this architecture determines the upper limit of the input signal amplitude. In practice, the finite rise and fall times of the output voltage of the XOR further narrow the locking range because the XOR fails to operate when the edges of the two input signals are close to each other as shown in Figure 2-9.

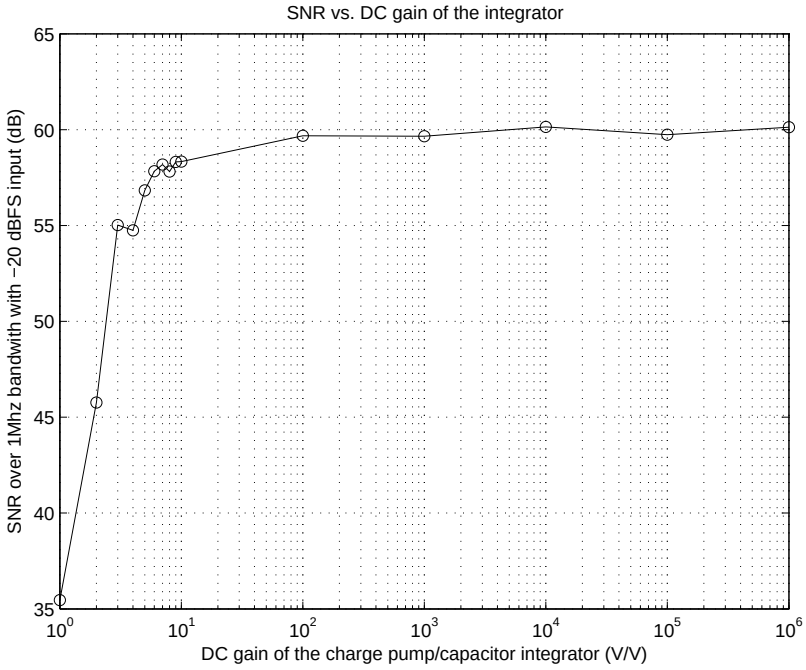

Figure 2-10: SNR vs. DC gain of the charge pump/capacitor integrator.

2.6 Benefits of the Proposed A/D Structure

The proposed ADC architecture is advantageous because the second-order noise shaping is possible in a highly digital manner. All the building blocks except for the second stage integrator can be implemented with digital circuitry as shown in Figure 2-5 (a). Even the second stage integrator can be implemented with simple inverters as will be presented in section 2.8.

Infinite DC gain of the first stage integrator, which is a VCO integrator, relaxes the design requirement of the second stage analog integrator in Figure 2-5 (a). Since the first stage integrator has infinite DC gain, low DC gain of the charge pump integrator in Figure 2-5 (a) does not degrade the overall performance much. The calculated SNR using CppSim behavioral simulations with different DC gains of the charge pump integrator is shown in Figure 2-10. In this simulation, the sampling rate is 800 MHz, and the VCO center frequency is 2 GHz. The behavioral simulation includes the VCO phase noise, and the signal bandwidth is 1 MHz. Figure 2-10 shows SNR drops less than 3 dB even if the DC gain of the charge pump/capacitor is as

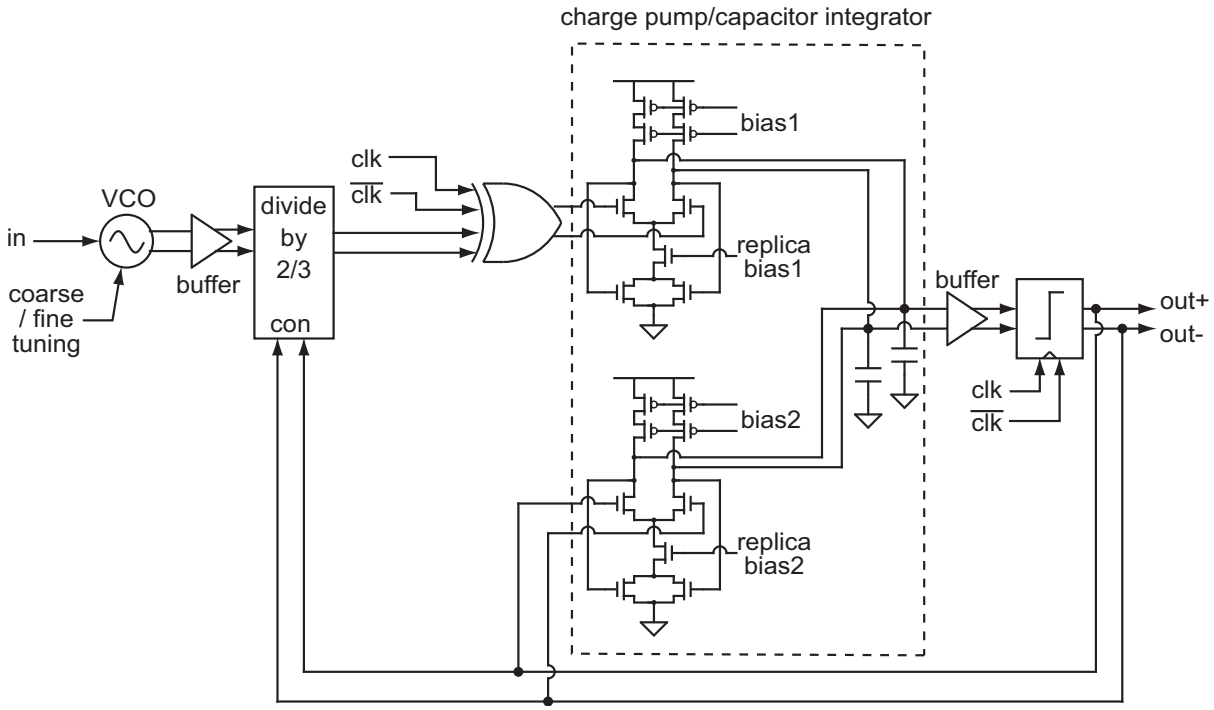

Figure 2-11: Simplified circuit block diagram of the prototype ADC in 0.18 μm CMOS.

low as 6, and it drops much less than 1 dB with the DC gain of 80. It is known that the performance degradation is on the order of 1 dB if the DC gain of the integrator is comparable to the oversampling ratio [23]. The simulation results in Figure 2-10 clearly show that this DC gain requirement for the charge pump integrator is significantly relaxed because of the infinite DC gain of the VCO integrator.

2.7 Prototype in 0.18 μm CMOS

The first prototype ADC was fabricated to prove the concept in 0.18 μm CMOS technology [28]. Figure 2-11 shows the simplified circuit block diagrams of the prototype VCO-based ADC in 0.18 μm CMOS. All digital circuits are implemented with *source-coupled logic* (SCL) for high-speed operation and common-mode noise rejection. SCLs are power hungry, and are not appropriate for low-power operation of an ADC. However, the SCL implementation has the benefit of decreasing the rise and fall times of the XOR phase detector, which improves its locking range. A 3-

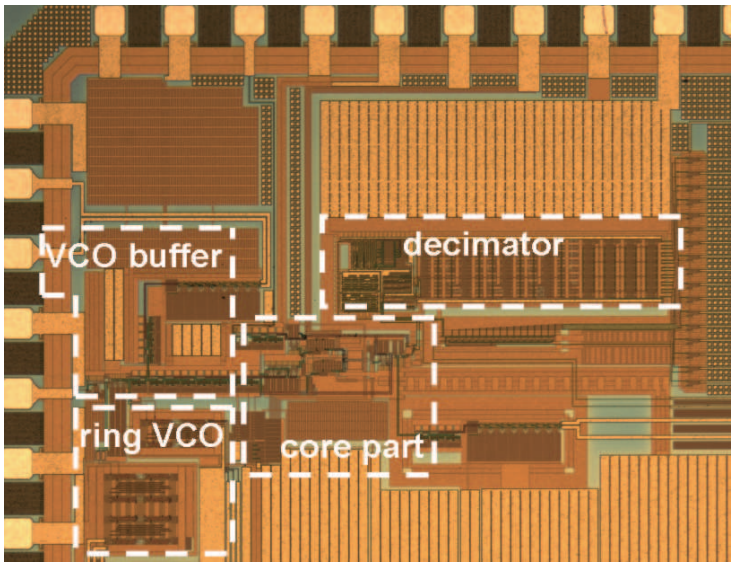

Figure 2-12: Die photograph of the prototype IC in 0.18 μm CMOS.

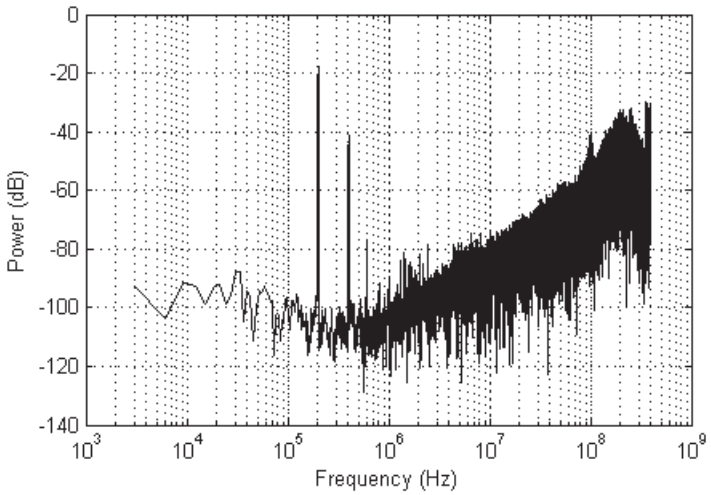

Figure 2-13: Measured output spectrum with –18 dBFS input of the prototype IC in 0.18 μm CMOS.

stage pseudo-differential ring VCO[1] is employed. Additional coarse and fine tuning inputs are included to adjust the center frequency of the VCO. The buffer is used as a preamplifier for the quantizer to reduce the occurrence of metastable behavior.

Figure 2-12 shows the die photograph of the first prototype IC in 0.18 μm CMOS. The total active area is about 0.5 mm^2. The total power consumption is 34 mW

[1]This VCO is designed by Charlotte Y. Lau, the former graduate student of MIT High-speed Circuit and System Group.

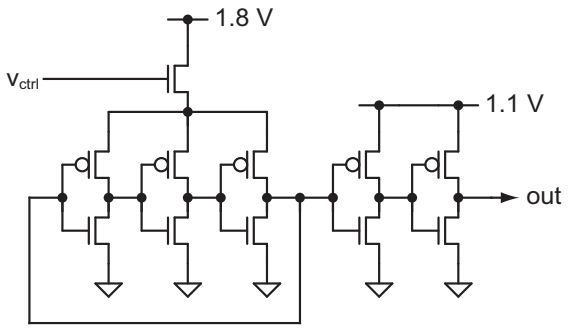

Figure 2-14: The ring VCO circuits employed for the proposed ADC in 45 nm CMOS.

excluding the VCO and its buffer stage. The VCO and the buffer consume 32 mW and 84 mW, respectively.

The measured output spectrum using a Hann window with –18 dBFS input signal is shown in Figure 2-13. The second harmonic components are about 22 dB lower than the desired input signal due to the non-linear voltage-frequency relation of the ring VCO.

The maximum SNR and SNDR measured are 60 dB and 39 dB over 1 MHz bandwidth, respectively. The SNDR is much lower than the SNR due to large harmonic components in band.

2.8 Circuit Design for the Prototype in 45 nm CMOS

Although the prototype in 0.18 μm CMOS proved the concept, there are several flaws. First, it wastes too much power in the high-speed digital circuits because it employed SCLs to maximize the speed. Second, non-linearity of the VCO leads to low SNDR [28]. Finally, it still uses analog circuits such as charge pumps. Another prototype IC in 45 nm CMOS is fabricated to address those problems.

The 45 nm CMOS prototype chip for the proposed VCO-based ADC employs single-ended full-swing CMOS logic circuits, thereby minimizing the power consumption of the digital circuits. The digital circuits in 45 nm CMOS are fast enough for higher than 5 GHz full-swing digital signals without difficulty. Figure 2-14 shows the ring VCO design for improved linearity of tuning characteristics. Using an NMOS

source follower, the control voltage changes the VDD voltage of the 3-stage ring oscillator, thereby changing the output frequency. The output voltage swing of the VCO core part depends on v_{ctrl}. The two cascaded inverter stage at the output of the ring VCO guarantees that the final output voltage swing of the ring VCO is VDD, 1.1 V in this case. The simulation results show the relationship between v_{ctrl} and the output frequency is more linear than the ring VCO in [28]. The prototype chip uses simple inverters for charge pumps as depicted in Figure 2-15. An inverter is similar to a charge pump in that the NMOS and PMOS of an inverter also sinks or sources a current to the output node. However, the amount of a current by a single NMOS and PMOS is highly dependent on the output voltage. Thus, the inverter-capacitor pair in Figure 2-15 makes a non-linear low-DC-gain integrator. The DC gain of the second stage integrator — $gm \cdot r_o$ of a single transistor is about 10 in this process — does not degrade the overall performance of a $\Sigma\Delta$ ADC if the first stage integrator has an infinite DC gain as discussed in Section 2.6; hence, a simple inverter can be employed as a charge pump without sacrificing the performance. Non-linearity of the ADC is dominated by the VCO's tuning characteristics; thus, the non-linearity of the second stage integrator is also tolerable.

2.9 CppSim Simulation Results for the Prototype in 45 nm CMOS

The proposed ADC is simulated with the CppSim behavioral simulation tool. In the simulation, the sampling rate is 1 GHz, and the VCO center frequency is 2.5 GHz. The DC gain of the charge pump is only 10. The noise profiles for the ring VCO and the charge pumps are from the Spectre RF simulations for the circuits described in Section 2.8. The phase noise of the ring VCO is about – 108 dBc at 20 MHz, and the flicker noise corner frequency is about 1 MHz. According to the Spectre RF simulations, the charge pump noise is dominated by the flicker noise because minimum channel length devices are used. In addition, the noise profiles for the NMOS transistors and the

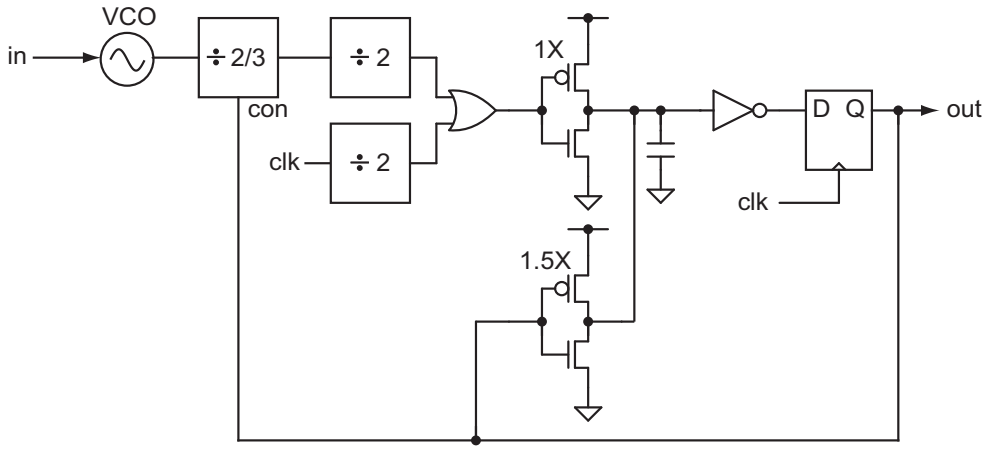

Figure 2-15: Circuit diagrams of the VCO-based continuous-time ΣΔ ADC in the 45 nm CMOS prototype IC.

PMOS transistors of the charge pumps are different. Thus, each noise source for the positive and the negative current are separately modeled in the CppSim simulations. The post-layout simulations of the ring VCO have created the look-up-table for the voltage-frequency relationship of the ring VCO. The non-linear tuning characteristics of the ring VCO are also modeled in the CppSim simulations based on the look-up-table.

Figure 2-16 shows the simulated output spectrum including the VCO phase noise. The charge pump noise is not included. The SNDR is 43.4 dB over 10 MHz. We can see the effect of the ring VCO's flicker noise whose corner frequency is around 1 MHz.

Figure 2-17 shows the simulated output spectrum including the charge pump noise. The VCO phase noise is not included. The SNDR is 44.1 dB over 10 MHz, and we can see only the quantization noise in Figure 2-17 because the noise from the charge pump is relatively smaller than the quantization noise. According to this simulation result, the in-band noise of the ADC will be dominated by the VCO phase noise.

Figure 2-18 shows the simulated output spectrum including both the VCO phase noise and the charge pump noise. Since the phase noise dominates the in-band noise, the SNDR is 43.4 dB over 10 MHz, which is the same as the result of the simulation including only the VCO phase noise.

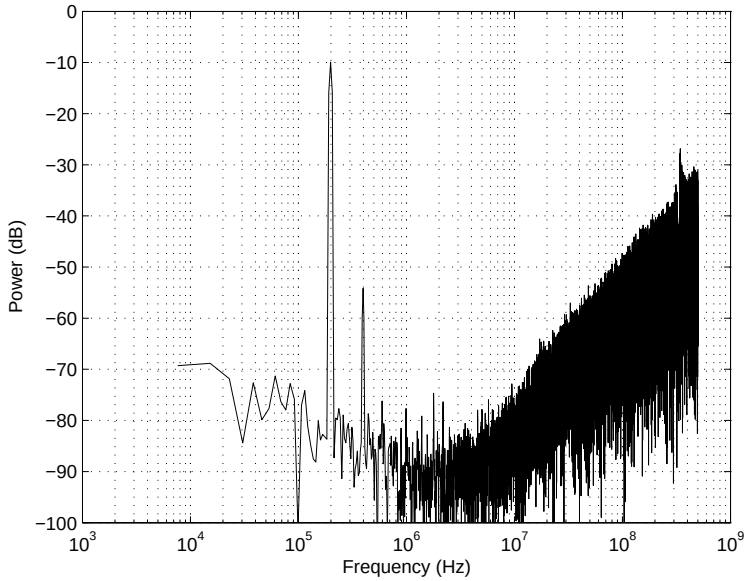

Figure 2-16: Output spectrum of the CppSim simulation including the VCO phase noise.

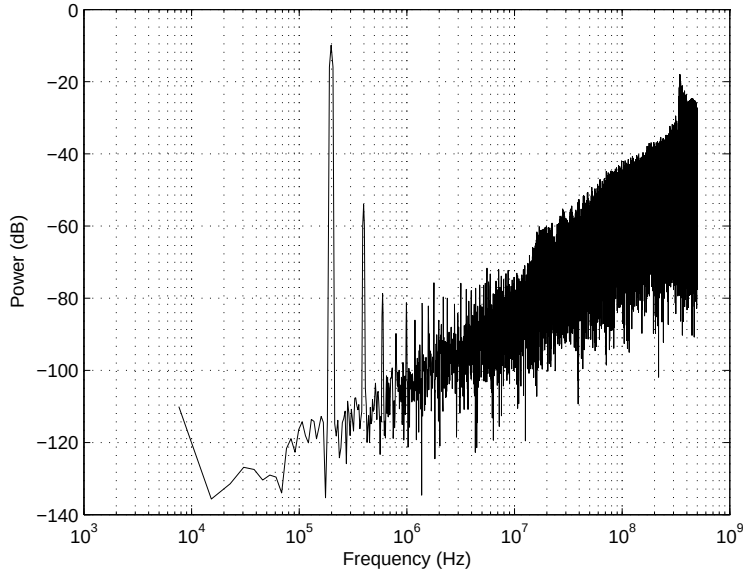

Figure 2-17: Output spectrum of the CppSim simulation including the charge pump noise.

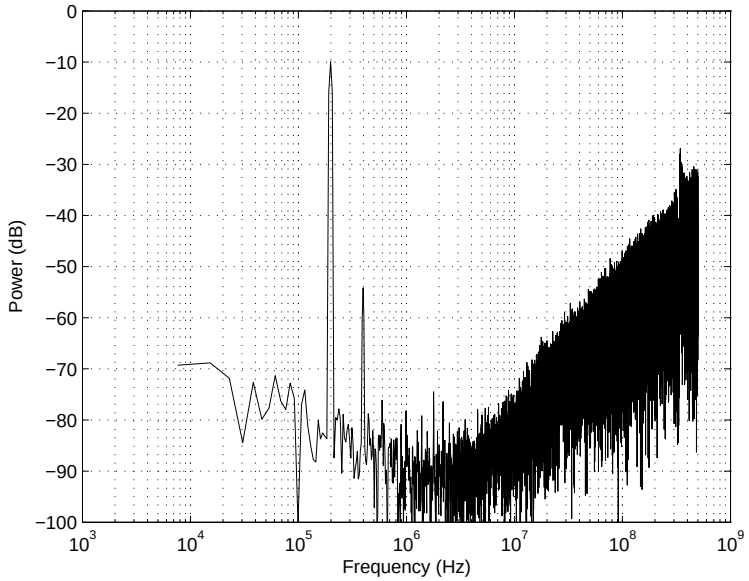

Figure 2-18: Output spectrum of the CppSim simulation including both the VCO phase noise and the charge pump noise.

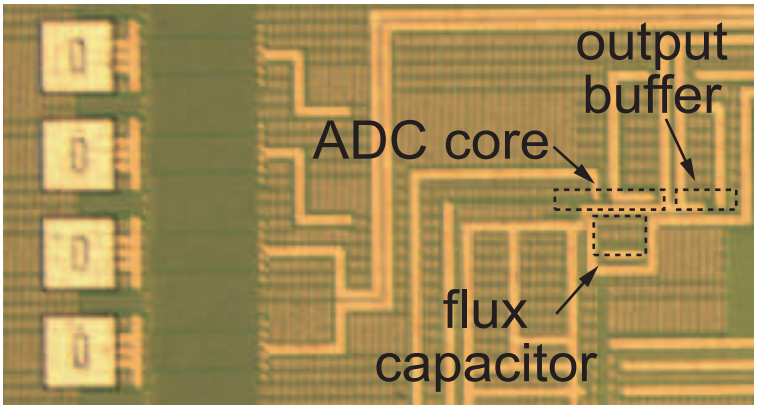

Figure 2-19: Die photograph of the prototype IC in 45 nm CMOS.

2.10 Measured Results

Figure 2-19 shows the die photograph of the prototype chip fabricated in 45 nm CMOS technology. The total active area including an interdigitated finger capacitor is about 1834 μm^2. The total power consumption is 1 mW. The VCO consumes 440 μW out of the total power.

As is described in Section 2.5, the center frequency of the VCO should be set to 2.5 times the sampling clock frequency. During the measurement, the center frequency of

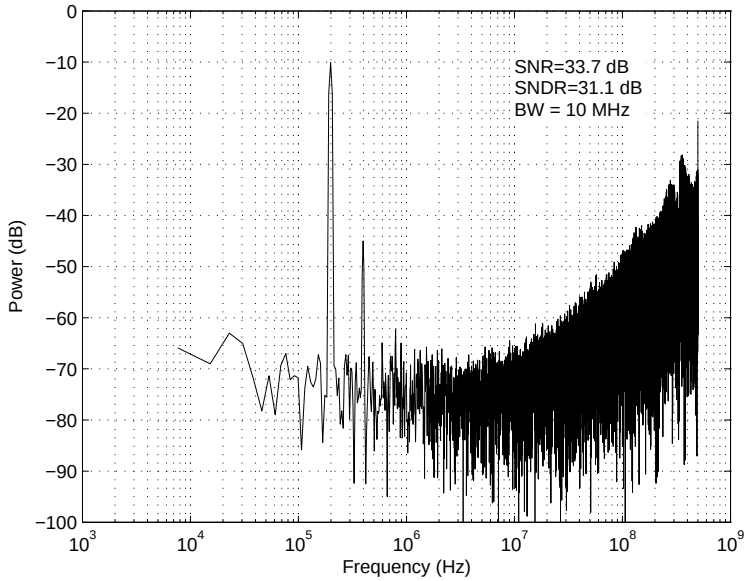

Figure 2-20: Measured output spectrum of the VCO-based ADC in 45 nm CMOS.

the VCO is controlled by the DC offset of the input signal. For the measurement, the sinusoidal input signal is AC-coupled to the A/D converter, and a separate, off-chip DC voltage source sets the offset of the input signal. The proper input DC offset is important to maximize the input dynamic range. If the input DC offset is inaccurate, the center frequency of the VCO is not 2.5 times the sampling frequency; thus, even a small input signal variation easily makes the input of the phase detector go outside the locking range and causes a cycle slipping.

The measured output spectrum using a Hann window is shown in Figure 2-20. The spectrum shows quantization noise shaping, as does the spectrum of the prototype in 0.18 μm CMOS. The second harmonic components are about 32 dB lower than the desired input signal due to the non-linear tuning characteristics of the ring VCO. The measured harmonics are bigger than those predicted in Figure 2-18. Compared with the prototype IC in 0.18 μm CMOS, however, the new prototype chip shows better linearity — the second harmonic of the 0.18 μm CMOS prototype is 22 dB lower than the main tone, whereas the second harmonic of the 45 nm CMOS prototype is 32 dB lower than the main tone. The maximum SNR measured is 33.7 dB over 10 MHz. The maximum SNDR is 31.1 dB due to the relatively large second harmonic.

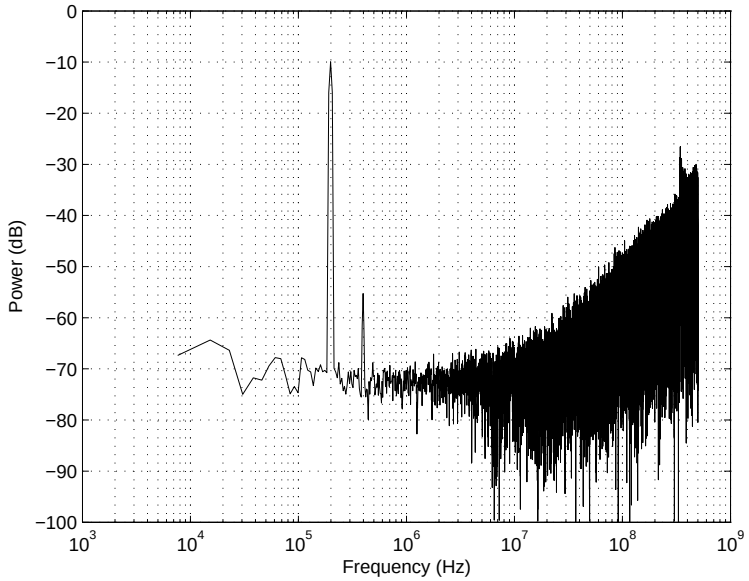

Figure 2-21: Output spectrum of the CppSim simulation with large charge pump noise.

The in-band noise floor shown in Figure 2-20 is higher than expected in the CppSim simulations. One possible reason of the higher in-band noise is an inaccurate charge pump noise model. Figure 2-21 shows the CppSim simulation results with large charge pump noise. The in-band noise in Figure 2-21 is similar to the measured results. Thus, the flicker noise model of the charge pumps for the Spectre RF simulations may not be accurate. If the flicker noise of the charge pumps is indeed the dominant in-band noise source, we can employ larger devices for the charge pumps instead of minimum length devices. However, we need to increase the power consumption to properly drive those large charge pumps. Adding degeneration resistors can be another solution since they decrease the flicker noise of the transistors. Note that the large thermal noise of the ring VCO or metastability of the quantizer can also be other possible causes of the large in-band noise.

Table 2.1 summarizes the performance comparison of the proposed VCO-based ADCs in 0.18 μm CMOS and 45 nm CMOS. The optimum signal bandwidth of the prototype in 45 nm CMOS has increased to 10 MHz due to the higher in-band noise, which is possibly caused by the large flicker noise from the charge pumps. However,

Table 2.1: The performance comparison of the proposed VCO-based ADCs in 0.18 μm CMOS and 45 nm CMOS

Prototype	0.18 μm CMOS	45 nm CMOS
Sampling Frequency	800 MHz	1 GHz
Signal Bandwidth	1 MHz	10 MHz
Peak SNR	60 dB (@ V_{in}=201 kHz)	33.7 dB (@ V_{in}=200 kHz)
Peak SNDR	39 dB (@ V_{in}=201 kHz)	31.1 dB (@ V_{in}=200 kHz)
ENOB	6.2-bit	4.9-bit
Total Power	150 mW (VCO : 32 mW)	1 mW (VCO : 440 μW)
Figure of Merit	1 nJ/level	1.7 pJ/level
Power supply	1.8 V (VCO : 1.8 V)	1.1 V (VCO : 1.8 V)
Acitve Area	0.5 mm^2	1834 μm^2

the total power consumption in the new prototype IC in 45 nm CMOS has improved greatly because of the low-power full-swing logic circuits employed in the new prototype; thus, the figure of merit of the ADC in 45 nm CMOS has improved by almost 600 times. The total active area has also reduced by almost 300 times in the 45 nm CMOS prototype IC.

2.11 Conclusions

A VCO-based ADC that achieves second order $\Sigma\Delta$ quantization noise shaping has been presented in this chapter. Fractional-N PLL modeling approaches have been applied to the proposed ADC to understand and quantify its behavior. The novel ADC architecture using time-based circuits makes it possible to realize an ADC in deep sub-micron CMOS with only digital circuits. The presented ADC is implemented in 45 nm digital CMOS process and achieves 33.7 dB SNR over 10 MHz bandwidth with 1 GHz of sampling rate.

The VCO phase noise is one of the bottlenecks of the proposed ADC. Although the phase noise of a ring oscillator improves by burning more power, there is a certain limitation on the phase noise unless new oscillator topology is employed, such as an

LC oscillator. The VCO non-linearity is another obstacle. We show that the linearity of the ring VCO can improve by using a different oscillator topology, but the linearity is not as good as that of an analog circuits. Therefore, the proposed ADC architecture is most suitable for the applications that require modest resolution and linearity in advanced digital CMOS technology, such as on-chip power supply monitoring.

Chapter 3

A Single-Slope A/D Converter Using Two-Step Time-to-Digital Conversion

3.1 Introduction

Single-slope conversion or integrating conversion is a classical means of implementing an ADC [29, 30, 31] and has the advantage of having a very simple implementation with minimal analog content. The key operating principle of such structures is to translate an input voltage to a ramp in time, and then measure the time duration it takes for the ramp to pass a given threshold voltage. Typically, the time measurement is performed with a digital counter, whose time resolution corresponds to the counter clock period. Since the clock frequencies of even the most modern CMOS processes are typically limited to less than 10 GHz, the time resolution offered by digital counter structures is constrained to be no better than hundreds of picoseconds. As a result, single-slope conversion is often constrained to very low sample rates even when only moderate resolution is desired of the ADC.

Recently, researchers have been investigating alternative approaches to using time-based quantization within an ADC in order to achieve a highly digital ADC imple-

mentation. One example of this trend is to tune the frequency of a VCO according to the input analog voltage, and then measure the period of the oscillator to determine the quantized output value [16]. Unfortunately, this approach yields limited conversion rates due to the limited frequency of the VCO and also introduces non-linearity into the ADC due to the non-linear frequency tuning characteristics of a practical VCO. The conversion rates can be increased by utilizing all phases of a multiphase VCO rather than just its overall output [19]. Still, the non-linear characteristics prevail as we could see from the measured results in Chapter 2. By surrounding the VCO-based quantizer with an analog feedback loop, the resulting ADC characteristic can be made much more linear [9, 10, 17], but the cost of such an approach is higher analog complexity in the system which will be difficult to apply in future CMOS technology.

In this chapter, we revisit the idea of using a single-slope conversion structure to leverage time-based quantization in the ADC. Rather than using a digital counter as the quantizer element, we instead draw off of recent advances in time-to-digital conversion (TDC) to perform this operation. The approach in [11] employs a similar concept for A/D conversion by utilizing a delay line based TDC. Instead of using a straightforward delay line for a TDC, in this work, we employ a ring oscillator to deal with a time-based signal. In particular, we leverage a recently published TDC based on a multipath gated ring oscillator (GRO) structure that achieves better than 10 ps of time resolution with a wide dynamic range [15]. To improve the power efficiency, we propose two-step conversion in which a low-frequency ring oscillator period is used to provide the initial coarse quantization, and the GRO TDC is used to provide fine quantization of the resulting residue. Measured results of the proposed architecture in 0.13 μm CMOS demonstrate 80 Ms/s conversion rate with an ENOB of 6.45 bits with a simple, compact ADC structure that has minimal analog complexity.

In contrast to the VCO approach in Chapter 2, the proposed A/D converter in this chapter is a hybrid approach that combines analog circuits and time-based circuits. By employing small analog circuits at the front-end, we can eliminate the issue of non-linearity in the VCO.

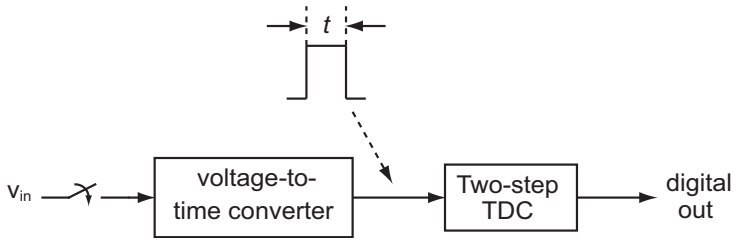

Figure 3-1: A/D conversion using a linear VTC and a two-step TDC.

In Section 3.2, we begin by showing the basic concept of the proposed ADC, which is composed of a linear voltage-to-time conversion (VTC) and a two-step TDC. We then show the circuit implementation of the linear VTC, followed by details of the two-step TDC. Following this discussion, we present a post-processing technique to mitigate the impact of mismatch in the two-step conversion process. Finally, measured results are shown for a custom IC prototype implementing the ADC in section 3.3. The chapter is concluded in section 3.4.

3.2 The Proposed Single-Slope A/D Converter

Figure 3-1 shows the basic concept of the proposed ADC architecture which utilizes a linear VTC and a two-step TDC. The VTC transforms a sampled input voltage to a pulse whose duration is linearly proportional to the input voltage. The duration of the pulse signal is measured by the two-step TDC, which yields a corresponding digital output. By using two-step architecture for the TDC, the power consumption is reduced while still achieving large range and fine resolution. The key idea is to first perform the time measurement with a coarse TDC that has low power consumption, and then use a fine TDC to measure the resulting residue. We will show that the two-step TDC implementation can be achieved with minimal analog complexity.

The key challenges of the ADC are to achieve a linear VTC structure along with an efficient circuit implementation of a two-step TDC.

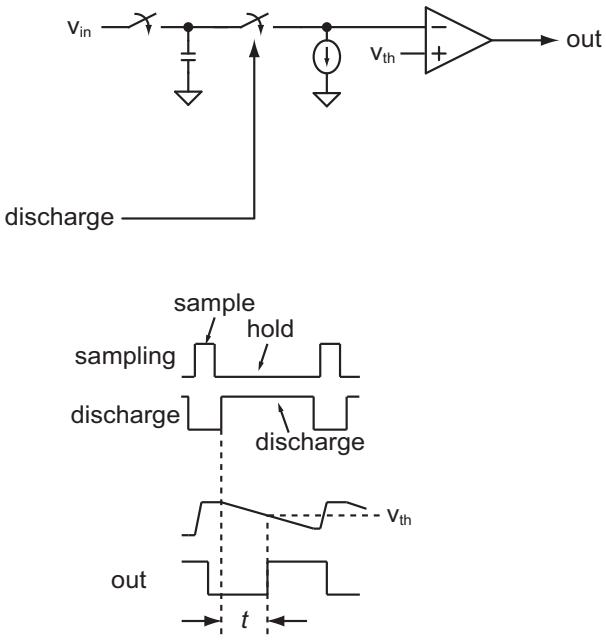

Figure 3-2: Block diagrams and timing diagrams of a linear VTC.

3.2.1 Linear Voltage-to-Time Conversion (VTC)

Figure 3-2 shows the block diagrams and timing diagrams of the suggested linear VTC. It is composed of a sample-and-hold circuit, a current source, and a comparator. The sample-and-hold circuit charges the sampling capacitor up to the input voltage while the current source is turned off. The current source is then turned on so that the voltage across the sampling capacitor decreases linearly as a function of time. When the voltage of the sampling capacitor crosses the threshold voltage of the comparator, the output of the comparator goes high. Assuming constant current drain on the capacitor, the resulting time duration between turning the current source on and having the comparator go high is linearly related to the input voltage, so that the desired VTC function is achieved.

By quantizing the time duration of the pulse output by the VTC with the two-step TDC, a digital representation of the input voltage is achieved. Therefore, the combination of the VTC and the TDC yields the desired ADC functionality.

A key issue in achieving good linearity in the proposed ADC is to maintain constant current drain on the capacitor within the VTC, which requires high output

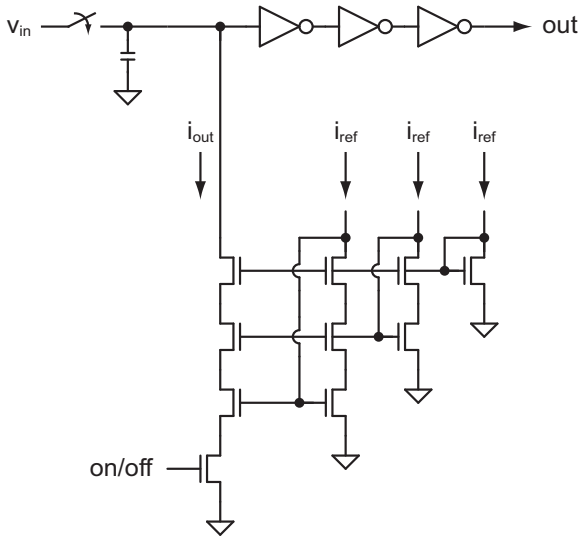

Figure 3-3: Simplified circuit diagrams of a linear VTC.

resistance of the current source. Figure 3-3 shows a simplified circuit diagram of the voltage-to-time converter which achieves a high output resistance current source through double cascode. The drawback of having two cascode devices is limited voltage swing at the output of the current source. However, high output resistance is only needed for voltages above the threshold voltage of the comparator since voltages below that value have no influence on the timing of the comparator decision. Therefore, the threshold voltage of the comparator is simply chosen to be large enough such that the cascode devices are in saturation above the threshold voltage.

Figure 3-3 also depicts the comparator implementation, which consists of a simple cascade of inverters. Although an inverter cannot be used as a general purpose comparator, it is suitable as a threshold-voltage-crossing detector if the input voltage is a constant slope ramp [32, 33, 34, 35]. Several stages of inverters achieve high enough sensitivity as a threshold-voltage-crossing detector, and inverters are easily implemented in advanced CMOS technology. The precise threshold voltage of the inverters cannot be controlled, but the threshold voltage affects only the offset of the voltage-to-time converter, which is easily subtracted out by post-processing in the digital domain.

3.2.2 Two-Step Time-to-Digital Conversion (TDC)

The fine resolution portion of the two-step TDC corresponds to a multipath GRO TDC which was first introduced in [14]. The GRO TDC performs time-to-digital conversion by counting transitions of a ring oscillator which is enabled only during the measurement interval. The raw resolution of this TDC corresponds to an inverter delay, but the structure interestingly achieves first order noise shaping of its quantization noise [14]. A further improvement in resolution is achieved by connecting the input for each delay stage to a *combination* of previous delay stages, which is referred to as a multipath GRO TDC as proposed in [15]. By doing so, the delay per stage can be dramatically reduced below that of an inverter. In $0.13\,\mu m$ CMOS, a multipath GRO TDC yields about 6 ps of raw time resolution [15], which is far less than the 35 ps inverter delay offered by this technology [14].

A critical issue related to a GRO TDC is that its power consumption increases as the duration of the input pulse signal increases due to the longer time duration that the ring oscillator and transition counting circuits must be active. In order to save power consumption, the proposed ADC utilizes a GRO TDC only to measure the residue of a quantization operation performed by a lower power, coarse TDC. The challenge in achieving this two-step conversion is that the time residue cannot be stored, so that the coarse/fine quantization must operate on the same pulse produced by the VTC.

To explain the two-step TDC structure, Figure 3-4 displays simplified block diagrams of the overall ADC, and Figure 3-5 shows its corresponding timing diagrams. The coarse TDC is composed of a ring oscillator and a counter. The oscillator's frequency is set to be relatively low so that low-power operation is obtained. The ring oscillator is enabled to start oscillating at the same moment that the current source is turned on to start discharging the sampling capacitor. A simple digital counter keeps track of the number of cycles that occur for the oscillator while the comparator is still low. At the point at which the comparator output goes high, a register stores the counter output so that coarse quantization of the pulse duration is achieved. The fine

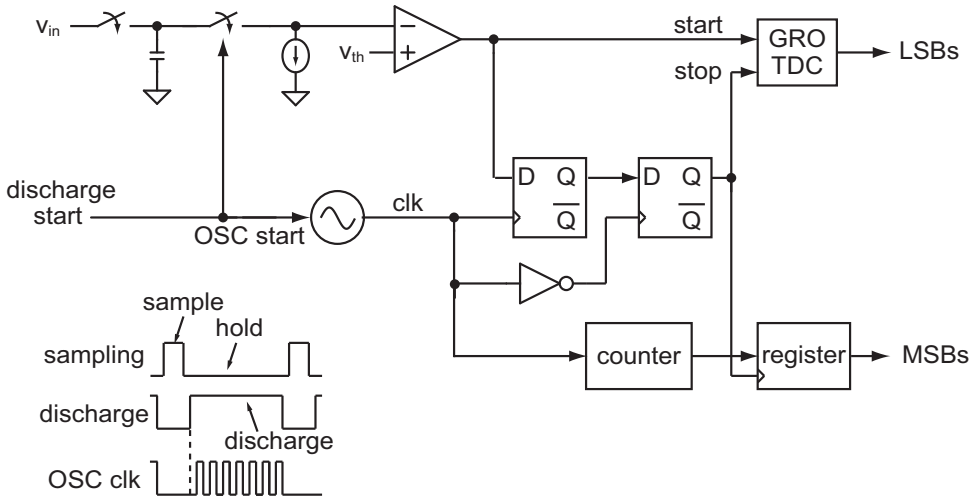

Figure 3-4: Simplified block diagrams of the proposed ADC.

quantization measurement is then performed by measuring the time duration from when the comparator went high to the next edge of the oscillator output, as depicted in Figure 3-5. By knowing the ring oscillator period, the resulting measurement by the GRO TDC can be easily utilized to compute the residual error of the coarse quantization performed by the ring oscillator. Since the GRO TDC is active for only the short time period, its power consumption is minimized.

One key issue of the GRO TDC is that it requires minimum input pulse duration to perform correctly since the internal ring oscillator of a GRO TDC requires a finite amount of time to turn on and off. As shown in Figure 3-4 and 3-5, two D flip-flops are utilized to add a half oscillator period to the GRO TDC pulse duration. As such, the minimum pulse duration will be half the coarse ring oscillator period and the maximum pulse duration will be one-and-a-half coarse ring oscillator periods.

Because of the addition of the half oscillator period, the final digital word from the GRO TDC includes a corresponding offset value. This offset must be considered during post-processing, as discussed in the next section.

3.2.3 Calibration and Post-Processing

The key issues in performing post-processing are to calibrate the relative scale factors between the coarse and fine TDC measurements, and to compensate for any

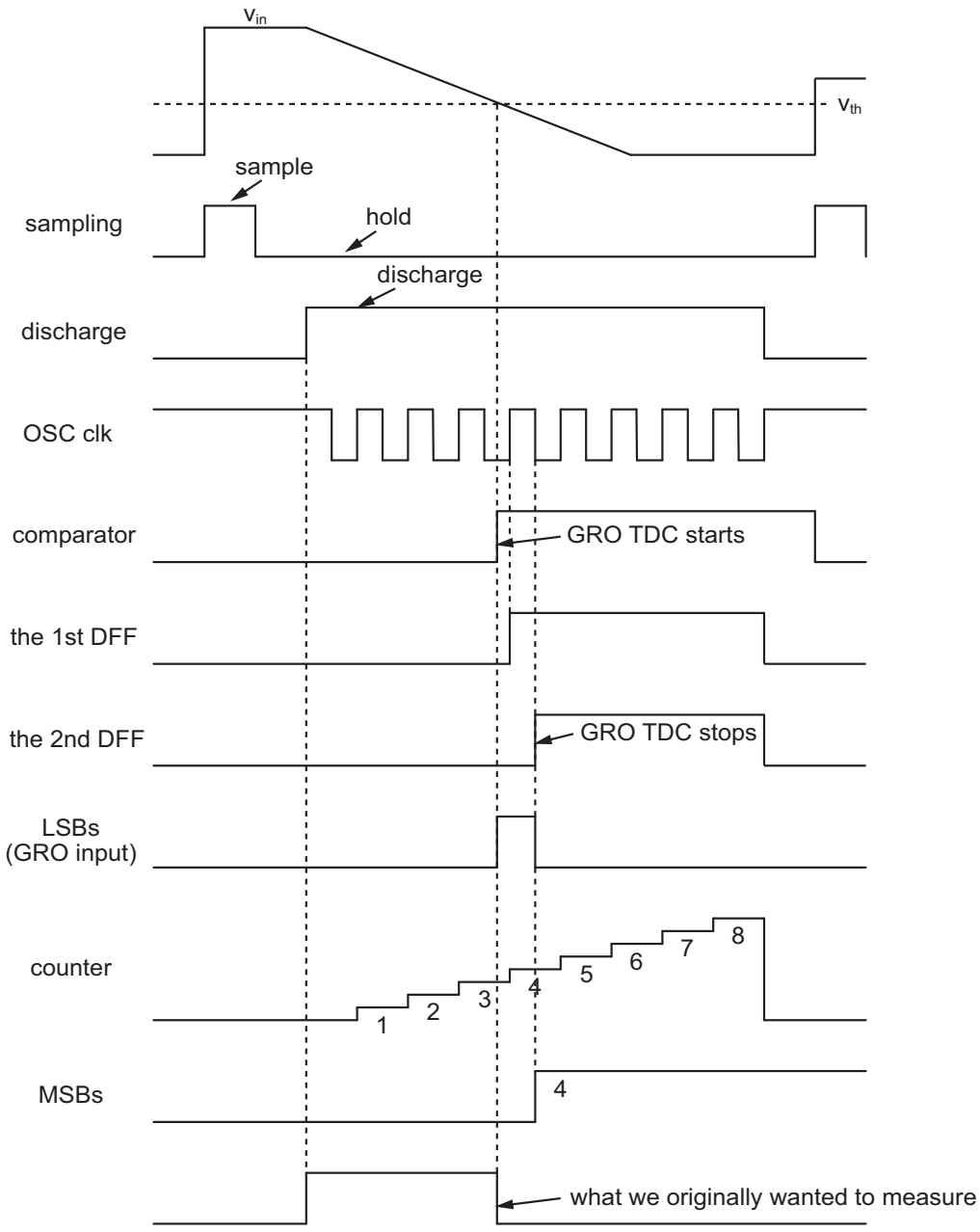

Figure 3-5: Timing diagrams of the proposed ADC.

systematic second order effects. The key second order effect that we will address is that the frequency of the ring oscillator used for coarse measurement takes some time to settle to its final frequency after being turned on. The resulting transient in frequency manifests itself as non-linearity in the coarse measurement. However, since the transient is entirely repeatable, it can be compensated by post-processing as will soon be discussed.

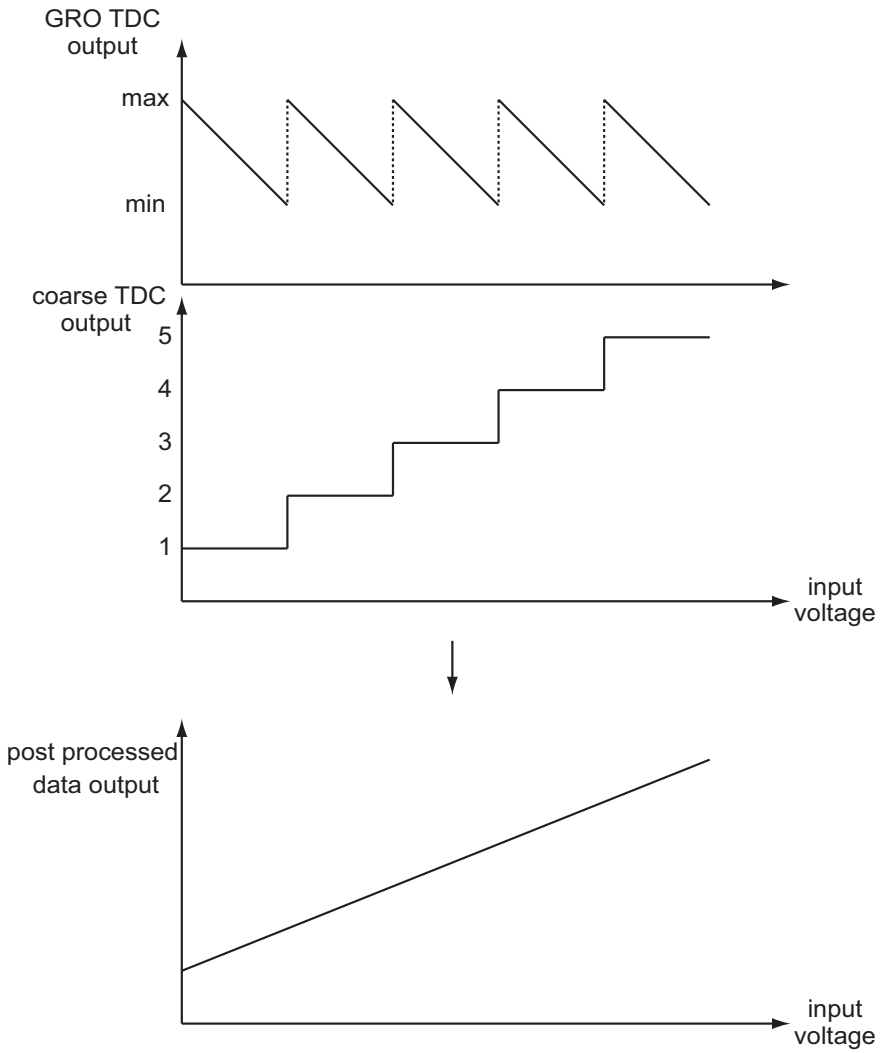

Figure 3-6: Input voltage vs. digital output code of the proposed ADC.

We first address the issue of calibrating the scale factors between coarse and fine TDC measurements. Figure 3-6 depicts an example of the GRO TDC and course TDC outputs as a function of input voltage, as well as the desired post-processed data output. As seen in the figure, the minimum and maximum values from the GRO TDC correspond to the half period and one-and-a-half period of the coarse TDC, respectively, as measured in increments of the GRO TDC unit step size. Therefore, to calibrate the relative scale factors between the coarse and fine TDC measurements, we simply need to measure the half period and one-and-a-half period of the coarse TDC oscillator with the GRO TDC. Once the minimum and maximum values of the

GRO TDC are obtained, the desired digital output is

$$out = out_{TDC_C} \cdot (max_{GRO} - min_{GRO}) + (max_{GRO} - out_{GRO}) \tag{3.1}$$

out_{TDC_C} is the output from a coarse TDC, out_{GRO} is the output from a GRO TDC, max_{GRO} is the maximum value from a GRO TDC, and min_{GRO} is the minimum value from a GRO TDC.

To deal with the issue of the transient in the coarse TDC ring oscillator frequency, more elaborate calibration is required which involves generating a known waveform at the input of the ADC that spans its full dynamic range, and performing a curve fitting operation to remove the observed non-linearity. However, one should note that only the coarse TDC need to be calibrated, which greatly simplifies the complexity of this operation. A more careful design of the coarse TDC ring oscillator should eliminate the need for this calibration in future designs. One could also eliminate this issue by keeping the coarse TDC ring oscillator on at all times, and then synchronizing the start time of the current source that drains the sample capacitor to the appropriate edges of the coarse TDC ring oscillator. However, such an approach would increase power consumption.

3.2.4 Noise Sources of the Proposed A/D Converter

Figure 3-7 illustrates three major noise sources in the proposed ADC. $\frac{kT}{C}$ noise of a sampling capacitor is omitted since choosing a large capacitor can make $\frac{kT}{C}$ noise negligible compared with other noise sources [36]. Thermal noise and flicker noise of the current source are integrated before influencing the comparator output, which influences the decision time of the comparator and, therefore, causes degradation in the ENOB of the ADC. Note that jitter of the coarse TDC ring oscillator has a similar effect on degrading the ENOB of the ADC.

In addition to the influence of the above noise sources, the quantization noise of the GRO TDC is another important noise source in the proposed ADC. The quantization noise of the GRO TDC is determined by its time resolution, which is set by the delay

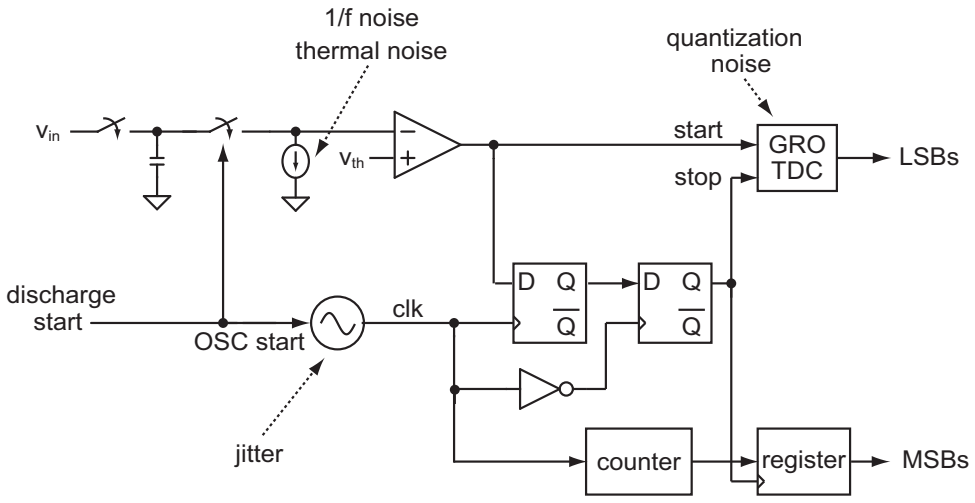

Figure 3-7: Noise sources of the proposed ADC.

per stage of its internal ring oscillator, as well as mismatch between the delays across the various stages. While the GRO TDC does offer noise shaping, this property is not of benefit in the Nyquist rate application considered here. However, due to the natural barrel-shifting action through the delay stages in the GRO TDC, the presence of mismatch does not impact the non-linearity of the ADC due to the noise shaping property of the barrel-shifting action [9, 15]. Therefore, while the GRO TDC does not provide noise shaping advantages in this application, it does provide linearity advantages in the presence of mismatch.

3.3 Measured Results

The prototype custom IC is implemented in 0.13 μm CMOS. A bootstrap circuit is employed for the sample-and-hold switches [37, 38], and a 20 pF sampling capacitor value is chosen. Digital circuits for calibration are included on the IC, though MATLAB is used to construct the final digital output sequence of the ADC.

During the calibration phase, a simple digital control circuit is used to measure the minimum and maximum values of the GRO TDC[1], and these values are retrieved by MATLAB through a USB interface for post-processing of the ADC output as

[1]This GRO TDC is designed by Matthew Z. Straayer, the former graduate student of MIT High-speed Circuit and System Group.

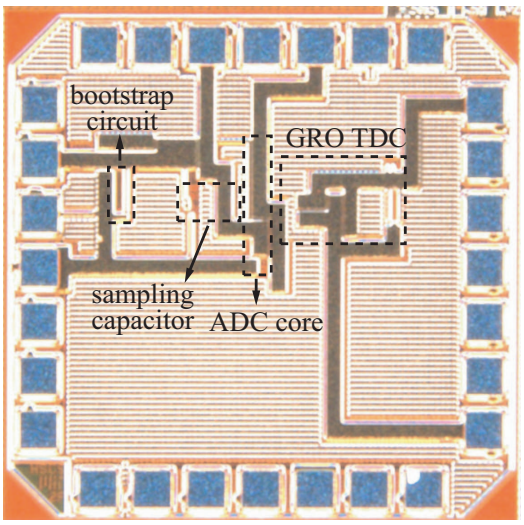

Figure 3-8: Die photograph of the prototype IC.

explained in the previous section. Non-linearity of the coarse TDC is measured by applying a full swing sinusoidal wave in the input of the ADC. By using a curve fitting method, the adjusted gains for the coarse TDC are calculated and stored for use by the MATLAB post-processing script.

Figure 3-8 shows the die photograph. The total active area is about 0.09 mm^2 including a sampling capacitor. Figure 3-9 shows the 4096 point FFT spectrum with 38 MHz input signal at 80 MS/s sampling rate without calibration of the coarse TDC non-linearity, and Figure 3-10 shows the spectrum with calibration. The maximum ENOB measured is 6.45 bit at 80 MS/s sample rate with calibration. The total power consumption is 6.4 mW, of which the GRO TDC consumes about 4 mW. The calculated *Figure Of Merit* (FOM) is 0.92 pJ/level. Table 3.1 summarizes the measured performance.

Note that most of power is consumed by the GRO TDC and the digital circuits. As we discussed in Chapter 1, both time-based circuits such as a ring oscillator and digital circuits benefit from Moore's Law. Therefore, the total power consumption of the proposed ADC is expected to decrease if it is fabricated in future CMOS technology. One of the analog circuits of the proposed ADC, a current source, will suffer from various issues if the channel length of the device shrinks; hence, it is unavoidable to use high supply voltage thick oxide devices for a current source. However, most of the

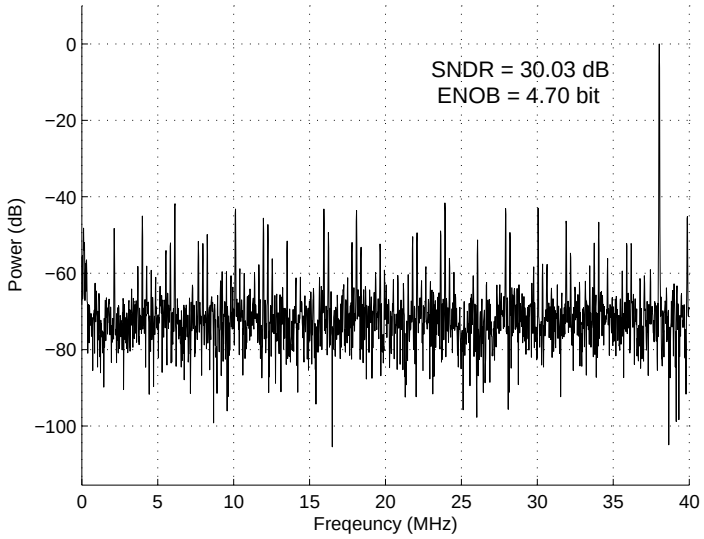

Figure 3-9: Output spectrum without calibration of coarse TDC non-linearity.

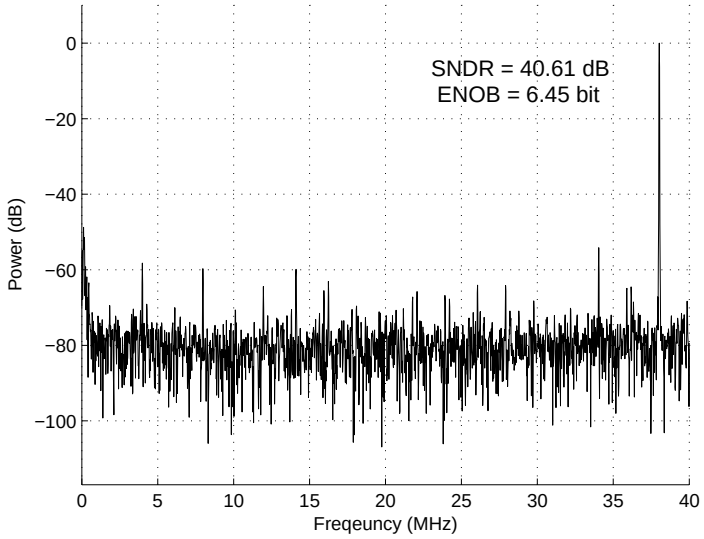

Figure 3-10: Output spectrum with calibration of coarse TDC non-linearity.

circuits of the proposed ADC are still scalable. The more advanced CMOS processes will make the performance and area of the proposed ADC improve.

Table 3.1: Performance summary of the proposed TDC-based single-slope ADC

Sampling frequency	80 MHz	
Peak SNDR	40.6 dB ($freq_{in}$=38 MHz)	
ENOB	6.45 bit	
Power consumption	GRO TDC	4 mW
	Digital Circuits	1.4 mW
	Analog Circuits	1 mW
	Total	6.4 mW
Process	0.13 μm CMOS	
Area	0.09 mm^2	
FOM	0.92 pJ/level	

3.4 Conclusions

A single-slope ADC which leverages two-step time-to-digital conversion along with post-processing was presented. The resulting structure is simple and compact, and the two-step conversion allows a power-efficient means of performing the time-to-digital conversion operation with wide range and high resolution. The overall ADC achieves 6.45 bit of ENOB at 80 MS/s with 6.4 mW of power dissipation.

The proposed hybrid approach that combines analog circuits and time-based circuits resolves the non-linearity issue, which was one of the bottlenecks of the VCO approach introduced in Chapter 2. However, we could see the flicker noise effect of the current source in the voltage-to-time converter. Accordingly, the proposed single-slope ADC may not be suitable for high-resolution low-speed A/D conversion due to the flicker noise dominance at the low frequency, unless very large devices are employed for the current source. If the proposed ADC is designed for a moderate sampling rate, however, the performance and power of the presented ADC will mainly be limited by digital circuits and a GRO TDC, as the measured results have shown in this chapter. Therefore, the performance of the proposed ADC is expected to improve when it is fabricated in future CMOS processes, in which time-based circuits and digital circuits perform better in terms of both the resolution and the power.

We believe that the proposed single-slope ADC would be suitable for a highly digital A/D conversion at a moderate sampling rate in deep sub-micron CMOS technology.

Chapter 4

A VCO-Based RF Modulator

4.1 Introduction

More and more wireless applications require sophisticated digital operations to perform many functions, such as camera, audio/video, and even a video game. A microprocessor, various memories, and a DSP are required to perform such complicated tasks. Therefore, digital circuits have dominated even wireless applications in terms of area and power. Ideally, integrating analog and RF circuits with those digital circuits is desired to lower the cost and power dissipation of chips.

For RF transmitters, some publications have suggested using an RFDAC for easier *System-on-Chip* (SoC) implementation [39, 40, 41]. An RFDAC generates an RF signal directly from a digital signal; hence, it eliminates a mixer and a DAC, of which analog characteristics are important for performance. An RFDAC requires fast switches for RF signal generation; on-going device scaling for modern CMOS technology helps to make the switches faster. Thus, an RFDAC is more suitable to integrate an RF transmitter with digital circuits in modern CMOS technology than a conventional RF transmitter architecture.

One of the challenges of RFDAC design is its resolution. The resolution is limited by lithography and device mismatch as is a conventional baseband DAC. The RF transmitter presented in [39] overcomes the resolution issue by $\Sigma\Delta$ modulation. However, it requires a well-tuned high-order LC filter in order to suppress the large

out-of-band noise generated by doing $\Sigma\Delta$ modulation. Such high quality LC filters require longer design time.

PMW is another way of generating an RF signal by simple switching [42, 43, 44]. However, PWM creates a strong ripple signal close to a carrier frequency although it does not suffer from a quantization noise issue. The ripple signal close to a carrier frequency requires a good filter. High PWM repetition rate relaxes the filter requirement, but it limits a dynamic range as will be discussed in Section 4.2.

We propose a multiphase PWM method to avoid aforementioned issues of a simple PWM RF transmitter. We also use a *VCO-based OP amp* to generate multiphase PWM signals in deep sub-micron CMOS processes. Our target bandwidth of the proposed RF modulator is 20 MHz. Compared with the bandwidth of the RF modulator in [39], our target bandwidth is narrower. It means that a passive LC filter with a higher Q is required for 20 MHz bandwidth in order to suppress the out-of-band quantization noise if the RF modulator architecture in [39] — RFDACs driven by $\Sigma\Delta$ modulation — is employed. However, we can eliminate such a high-Q filter by driving RFDACs using multiphase PWM signals.

We start with discussing a PWM-based RF transmitter in Section 4.2. The proposed VCO-based OP amp, which will be utilized for multiphase PWM signal generation in deep sub-micron CMOS, is introduced in section 4.3, followed by a proposed VCO-based RF modulator based on multiphase PWM scheme in Section 4.4. Circuit design of the proposed VCO-based RF modulator will be discussed in Section 4.5. Since the proposed RF modulator omits a poly phase filter for IQ clock generation in order to avoid using accurate passive components, the IQ LO clock signals are generated by high-speed flipflops as will be discussed in Section 4.5. Accordingly, IQ mismatch due to the delay of flipflops is inevitable. IQ mismatch compensation applying to the source baseband signal using digital filters will be mentioned in Section 4.6. The prototype chip was implemented in 45 nm CMOS. The measurement results are presented in Section 4.7, and the chapter is concluded in Section 4.8.

4.2 Background: An RF Modulator Based on PWM

Figure 4-1 illustrates a conventional direct-conversion RF modulator. It uses a baseband DAC to directly drive a Gilbert Cell mixer. Although a direct-conversion modulator is very popular topology for an RF modulator even targeting state-of-the-art wireless communication standards such as WiMax [45], it would be challenging to implement the Gilbert Cell in deep sub-micron CMOS technology mainly because of the analog operation of the transistors which the baseband DAC drives. One problem is a headroom issue. Limited voltage headroom in deep sub-micron CMOS may result in non-linearity of the transistors performing analog functions. High r_o of the transistors are also required for the linear voltage-to-current conversion. In addition, the input-offset of the analog transistors may cause a current imbalance of the differential signal paths — analog circuits are usually more sensitive to device mismatch than digital circuits. Therefore, it would be challenging to deal with analog circuits in the future CMOS processes, and the traditional RF modulator topology employing a mixer may not be the best candidate.

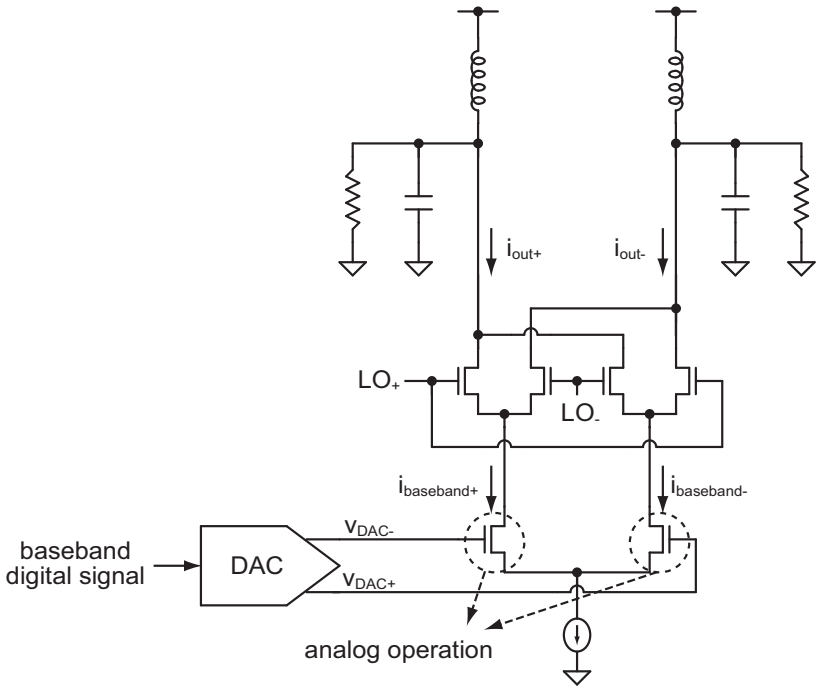

Figure 4-1: A conventional Gilbert Cell mixer based RF modulator.

An RFDAC eliminates the transistors that perform analog functions. However, the resolution of an RFDAC is limited by device mismatch. The approach in [39] employs $\Delta\Sigma$ modulation to increase in-band resolution, but it requires a precise on-chip reconstruction filter to remove the out-of-band quantization noise. Such a precise on-chip filter could lead to longer design cycles in order to properly tune the filter characteristics for a given application.

We propose to use PWM to solve the resolution issue. PWM uses simple switching waveforms rather than precise control of current or voltage, thereby making the resolution limited by the time resolution not by the current or voltage resolution. Time resolution, which is involved with a transistor switching time, scales as device size shrinks. Therefore, PWM could be a good solution for the resolution issue in advanced CMOS technology.

The simplest method to utilize PWM for higher resolution is to generate a baseband signal with PWM. Figure 4-2 depicts such an idea. As shown in Figure 4-2, the low frequency contents of the PWM signal represent the desired baseband signal, and ripples appear at the high frequency due to the periodic repetition of the pulses. The transistors in the Gilbert Cell mixer no longer perform an analog function because the PWM signal simply switches the transistors. Therefore, this topology will be easily implemented even in low cost digital CMOS processes with short channel length devices. A similar idea has been suggested for an all-digital RF signal generation in [44].

One drawback of a simple PWM approach for an RF modulator is that PWM generates an unwanted ripple frequency component in the output due to the repeated switching actions. The ripple component should be removed by filtering so that high ripple frequency is desirable for easy filtering. However, the high PWM frequency results in a dynamic range issue, as is shown in Figure 4-3. Because of the limited rise and fall times of switching devices, the maximum dynamic range of the output signal is also limited. In addition, the maximum dynamic range is proportional to the switching period, which is the inverse of the PWM frequency. Therefore, there is a trade-off between ripple frequency and dynamic range.

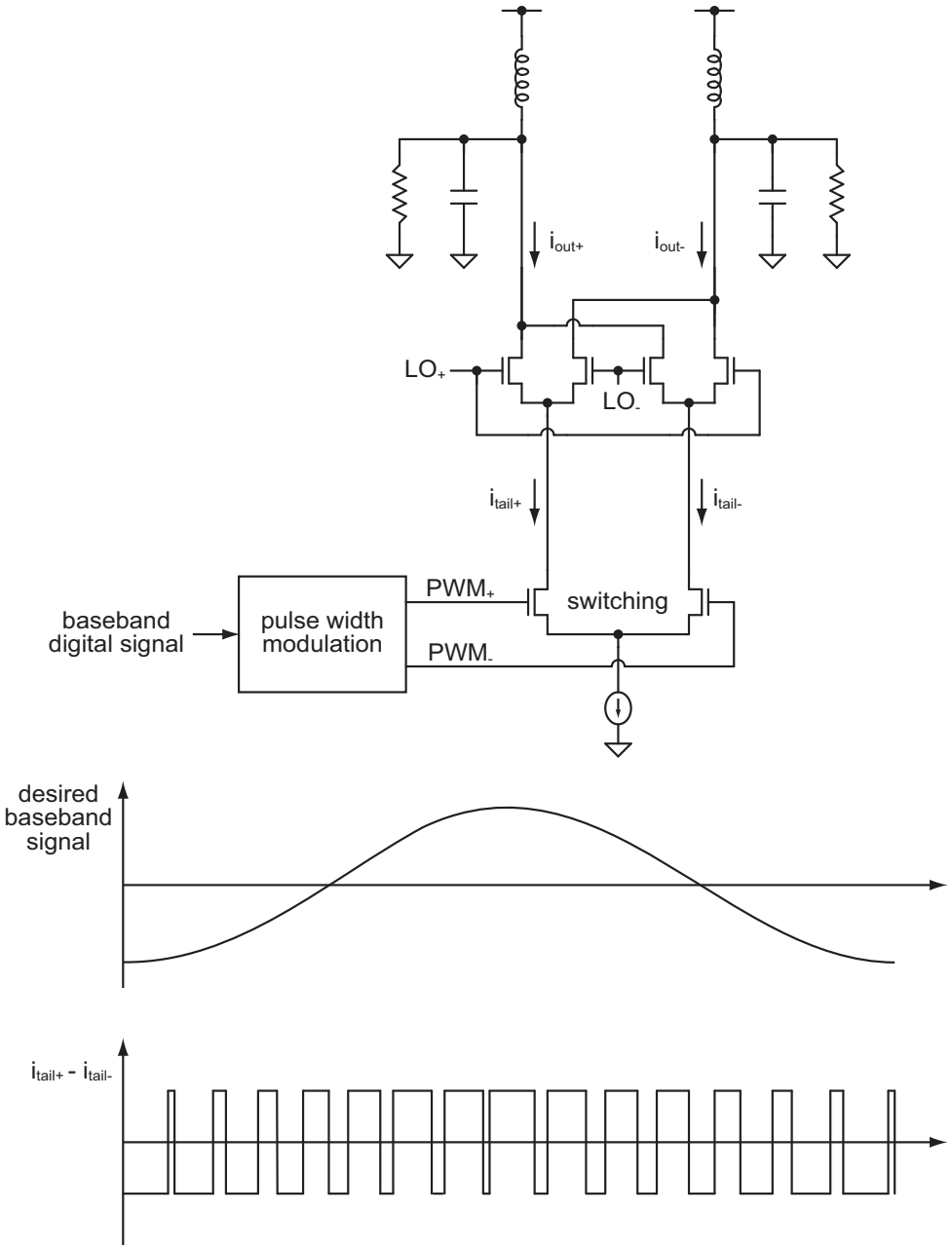

Figure 4-2: Generating a baseband signal by PWM.

The approach combining an RFDAC and PWM can address the dynamic range problem. Figure 4-4 depicts a Gilbert Cell driven by multiphase PWM signals. The topology shown in Figure 4-4 can be considered as a 3-level RFDAC driven by 3-phase PWM signals. The timing diagrams in Figure 4-5 present how the RFDAC driven by multiphase PWM signals works. Although the RFDAC in Figure 4-4 has only 3 current levels to generate the baseband signal, each switching element is driven by a

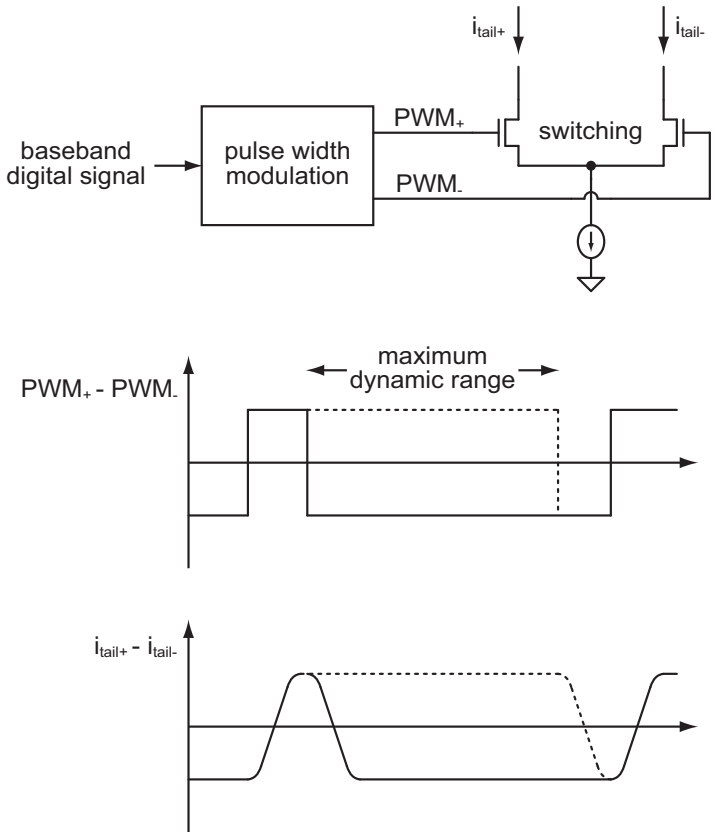

Figure 4-3: Dynamic range of a PWM signal.

separate PWM signal so that the combined signal of 3 current sources shows infinite resolution. In other words, a PWM signal does not create a quantization noise as long as the time resolution of the pulsewidth is infinite. In practice, the pulse edge contains timing jitter, which limits the resolution. Note that the individual PWM signal switches at a lower rate, but the ripple frequency of the combined PWM signal is higher, as is shown in Figure 4-5. Therefore, the ripple frequency of the combined PWM can be high enough to make filtering of the ripple signal easy. The dynamic range of the mixer in Figure 4-4 is higher than that of a single PWM RF modulator because the mixer driven by multiphase PWM signals can create more voltage or current levels. This multiphase PWM topology is introduced in [46]. For multiphase PWM generation, however, the approach presented in [46] employs triangular waveform generators and multilevel comparators that are analog circuits. These analog building blocks are inadequate since our goal for this RF modulator is to implement

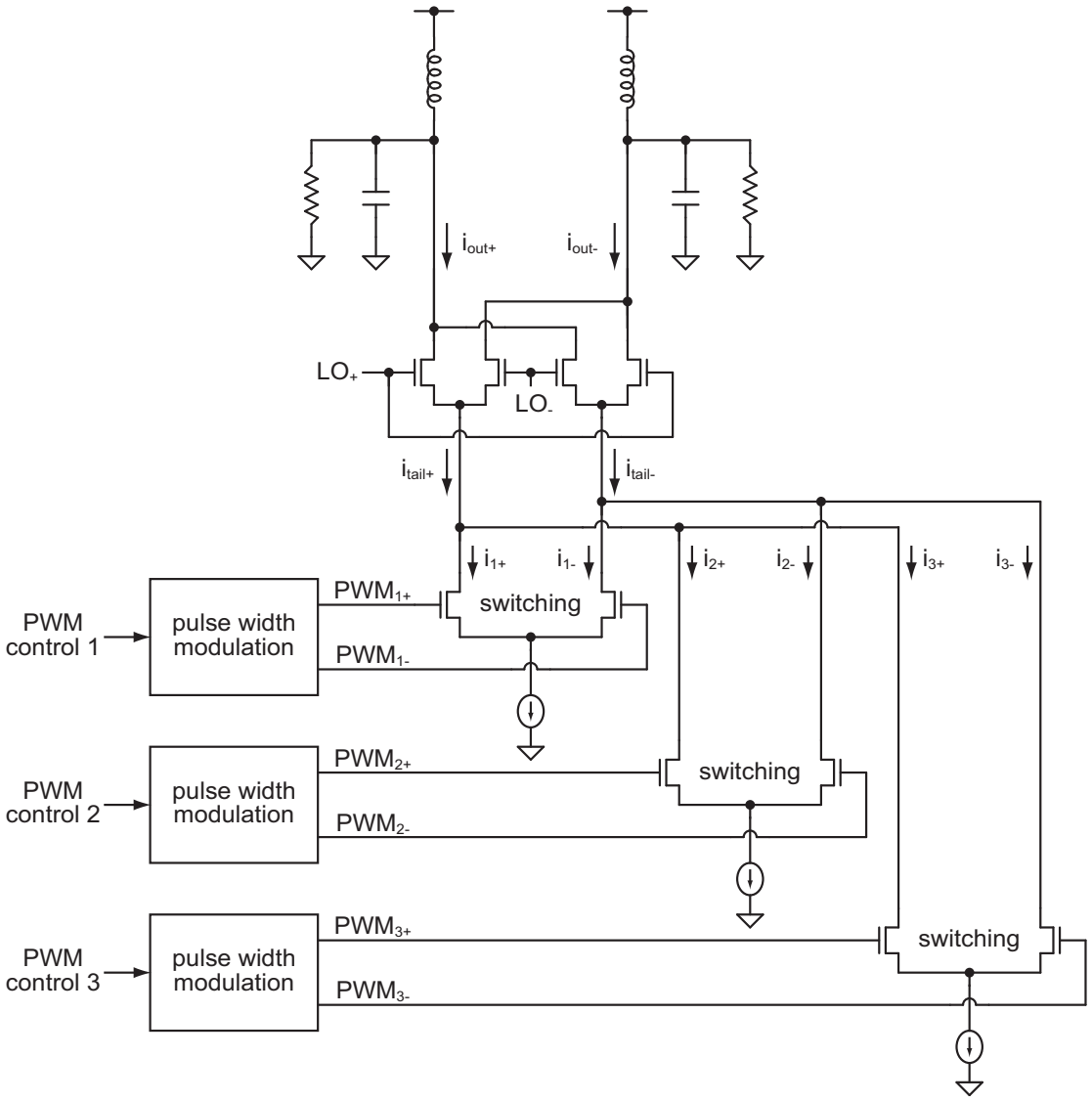

Figure 4-4: A mixer driven by multiphase PWM signals. 3-phase PWM signals are shown.

it in deep sub-micron CMOS.

We propose to use multiphase ring VCOs and phase detectors to generate the multiphase PWM signals. The behavior of the proposed architecture composed of multiphase ring VCOs and phase detectors is similar to the behavior of an OP amp. Thus, we will call the proposed architecture a *VCO-based OP amp*. The VCO-based OP amp is a core part of the VCO-based RF modulator.

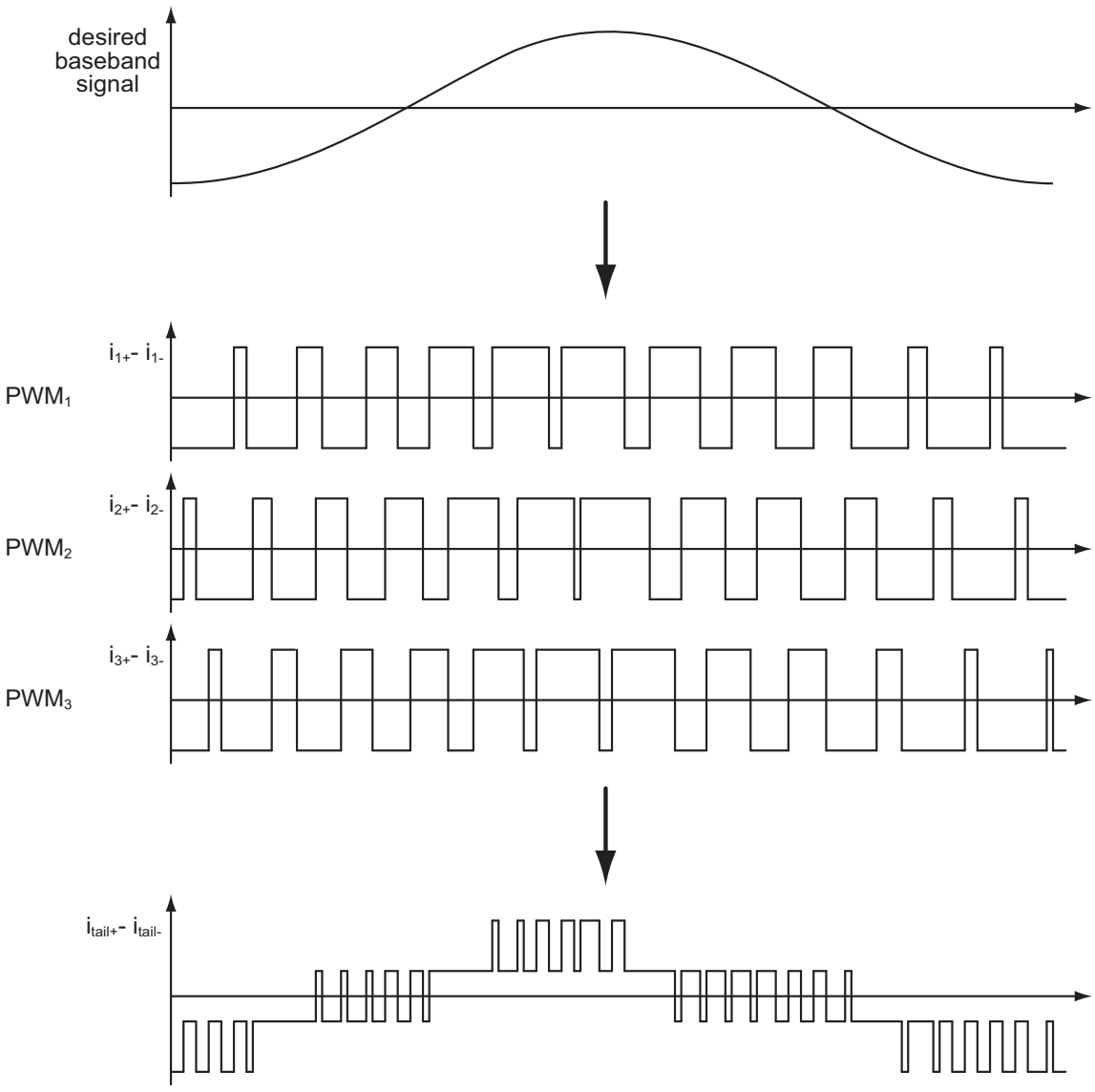

Figure 4-5: Generation of multiphase PWM signals.

4.3 The Proposed VCO-Based OP Amp

4.3.1 VCO-Based OP Amp Architecture

The main idea of the proposed VCO-based RF modulator is to drive multiple Gilbert Cell mixers with multiphase PWM signals using the VCO-based OP amp. Figure 4-6 illustrates a basic concept of the proposed VCO-based OP amp. The two VCOs work as integrators, and the phase detector converts the phase difference between the two integrators' outputs into a voltage or current signal. Because the phase detector

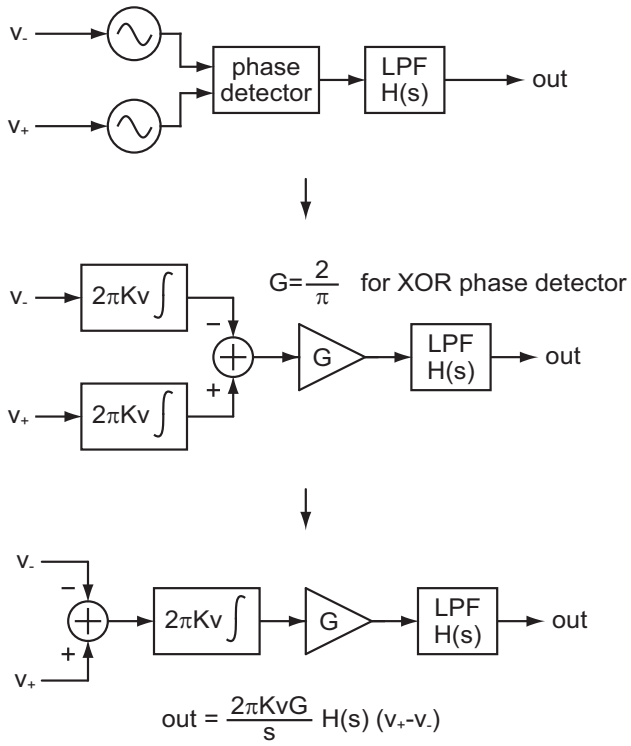

Figure 4-6: The proposed VCO-based OP amp.

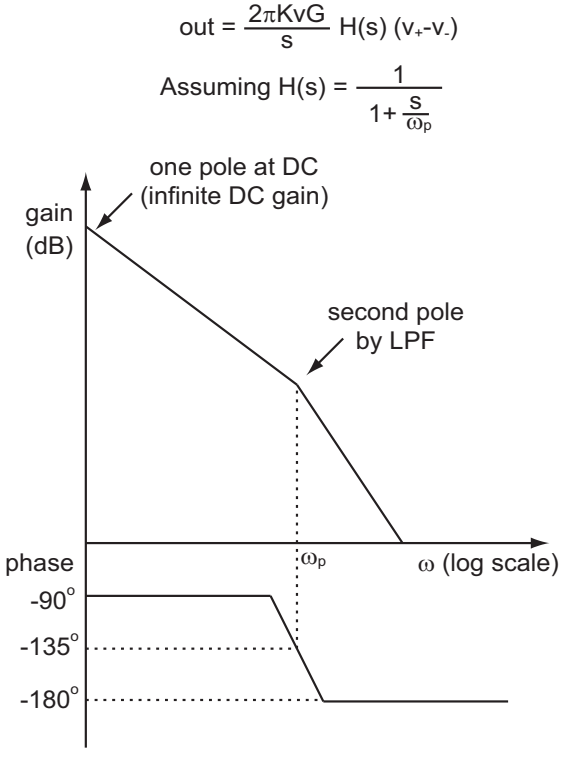

Figure 4-7: Bode plot of the suggested VCO-based OP amp.

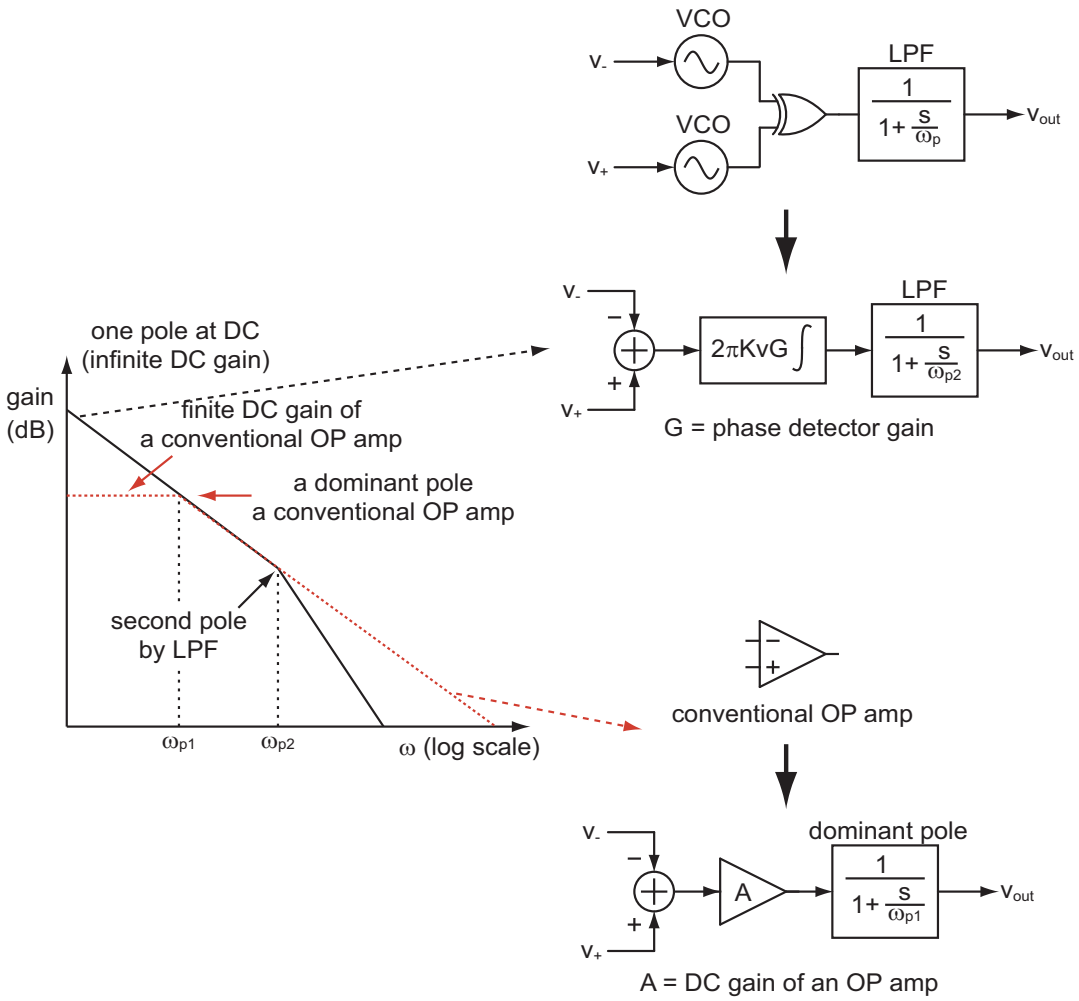

Figure 4-8: The proposed VCO-based OP amp vs. a conventional OP amp.

output has a ripple, a *low-pass filter* (LPF) is required for the output signal.

Figure 4-7 depicts the VCO-based OP amp's bode plot when the LPF is a simple one-pole filter, and Figure 4-8 compares the proposed VCO-based OP amp's bode plot with that of a conventional OP amp. As Figure 4-8 shows, the VCO-based OP amp has an infinite DC gain while the DC gain of the conventional one is limited by the finite gain of its gain stages. Achieving a high DC gain in conventional OP amps becomes more and more difficult as the device scales down, but the DC gain of the VCO-based OP amp is not limited by technology.

Note that the unity gain bandwidth of the VCO-based OP amp will generally need to be lower than that of a conventional OP amp due to the second pole frequency,

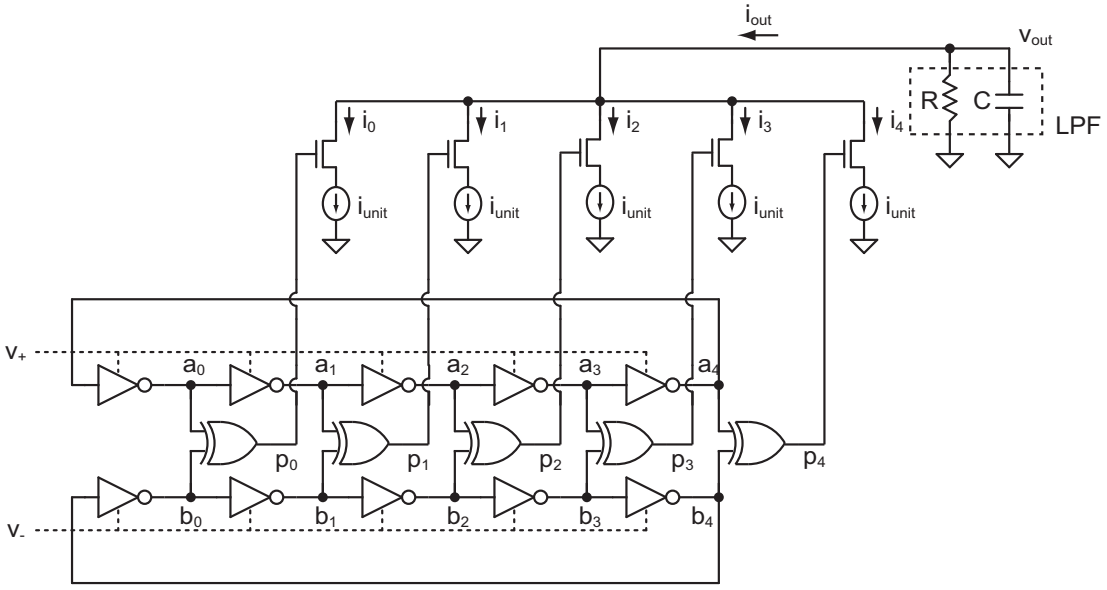

Figure 4-9: The proposed VCO-based OP amp with multiphase VCOs and phase detectors.

ω_p, required to filter the ripple. If the unity gain bandwidth is not low enough, the phase margin would be too small as we can see in Figure 4-7.

The major difference between the proposed VCO-based OP amp and a conventional OP amp is that a voltage ripple exists in the VCO-based OP amp due to the nature of the phase detector. We propose to employ multiphase ring VCOs and multiple phase detectors to reduce the ripples from phase detectors. In Figure 4-9, there are two ring VCOs and each output tap is connected to an XOR phase detector. Each XOR gate drives one element of a current DAC. The output current of the DAC will be the sum of the current of individual elements. The timing diagrams of the 5-phase ring VCO-based OP amp are shown in Figure 4-10 to Figure 4-14, and output ripple reduction by multiphase VCOs will be discussed later.

In Figure 4-10, an example of the timing diagrams of 5 XOR phase detectors is illustrated. Each XOR gate drives an element of a DAC as mentioned earlier; hence the output current of the DAC is proportional to the sum of the phase detector's output. If the phase difference between two ring VCOs is $\frac{\pi}{2}$, then the output current of the DAC will alternate between 2 and 3 unit-current at 50 % duty cycle, as is illustrated in Figure 4-10.

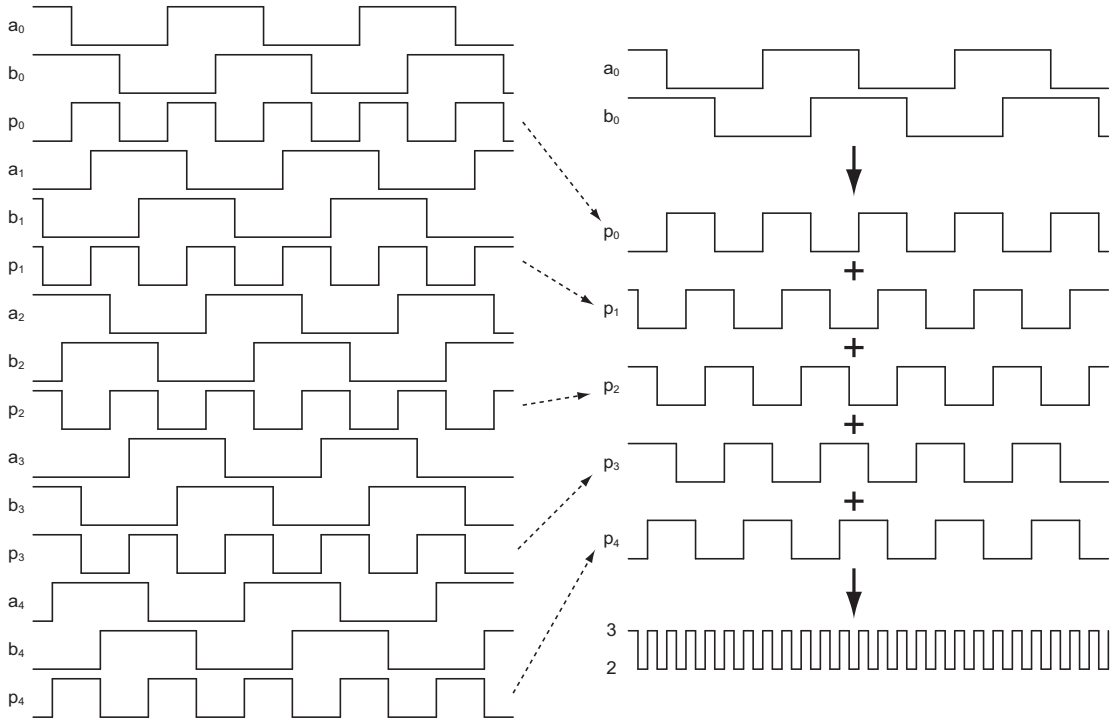

Figure 4-10: Timing diagrams of multiphase VCOs and phase detectors (1).

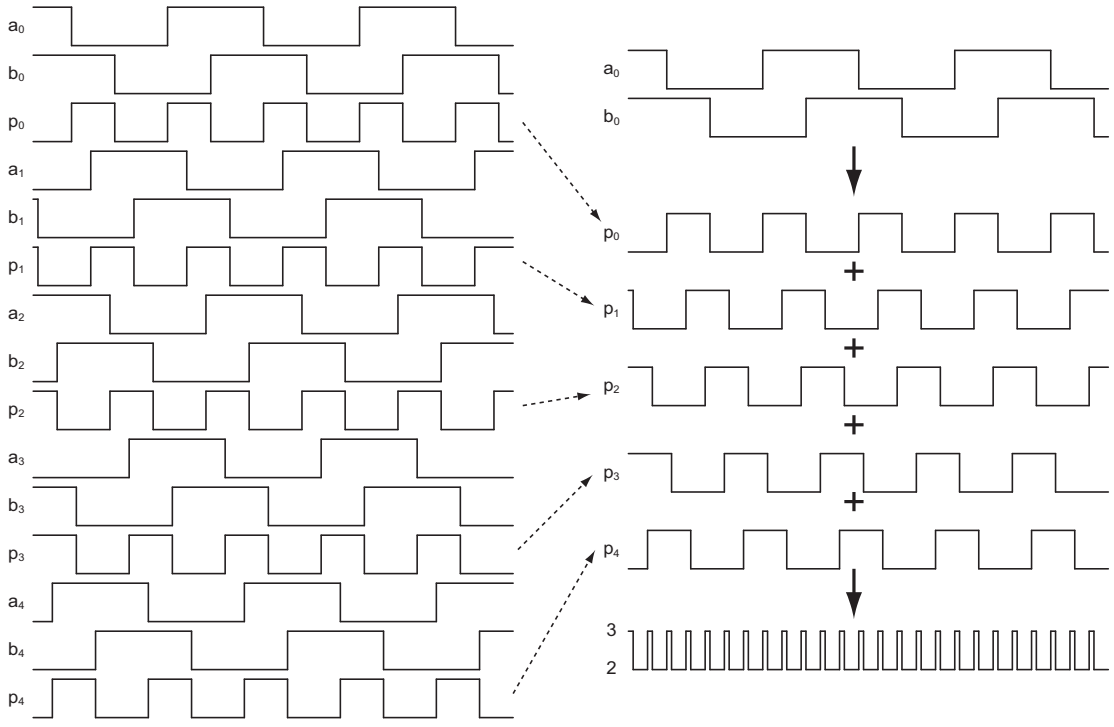

Figure 4-11: Timing diagrams of multiphase VCOs and phase detectors (2).

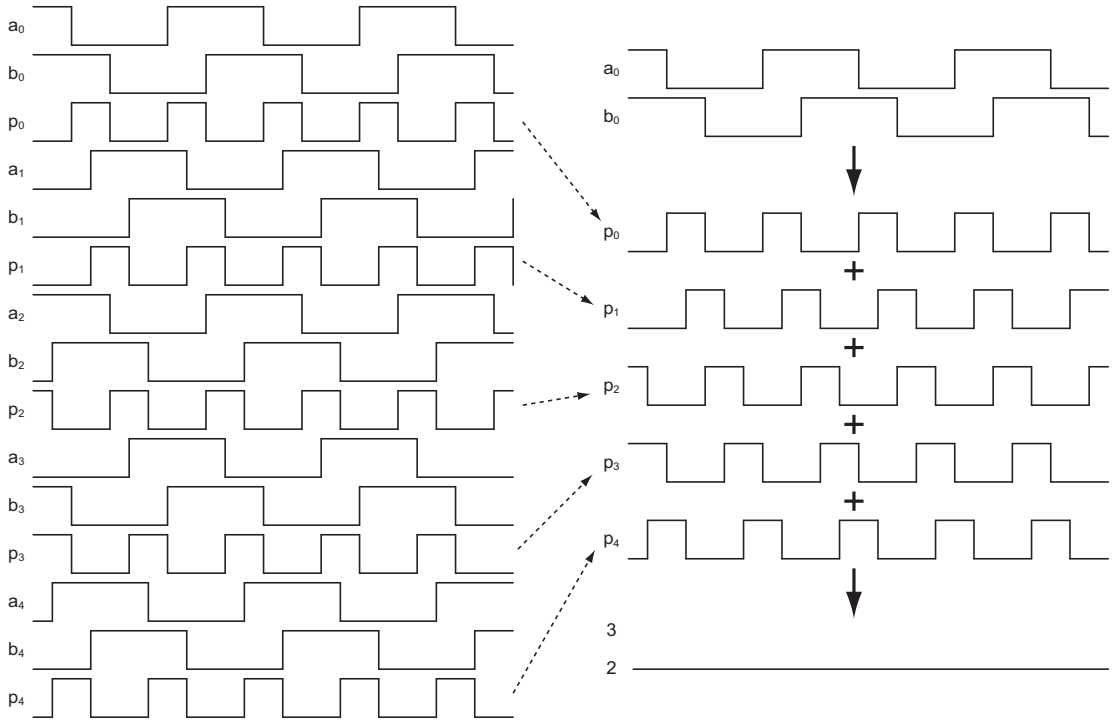

Figure 4-12: Timing diagrams of multiphase VCOs and phase detectors (3).

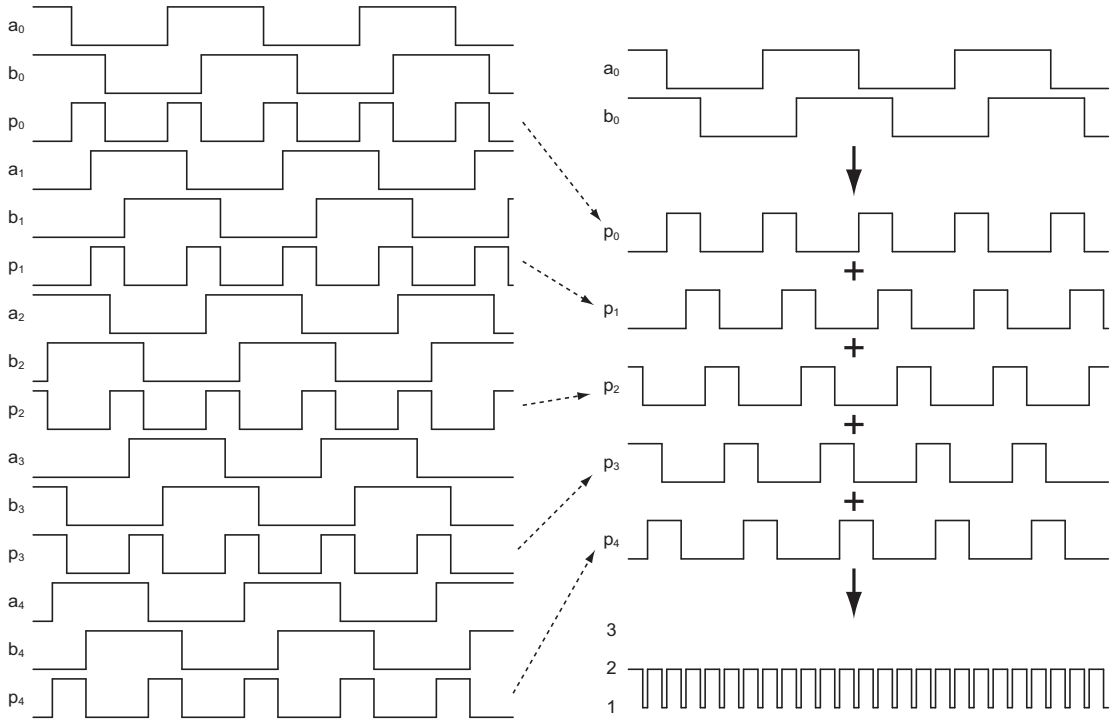

Figure 4-13: Timing diagrams of multiphase VCOs and phase detectors (4).

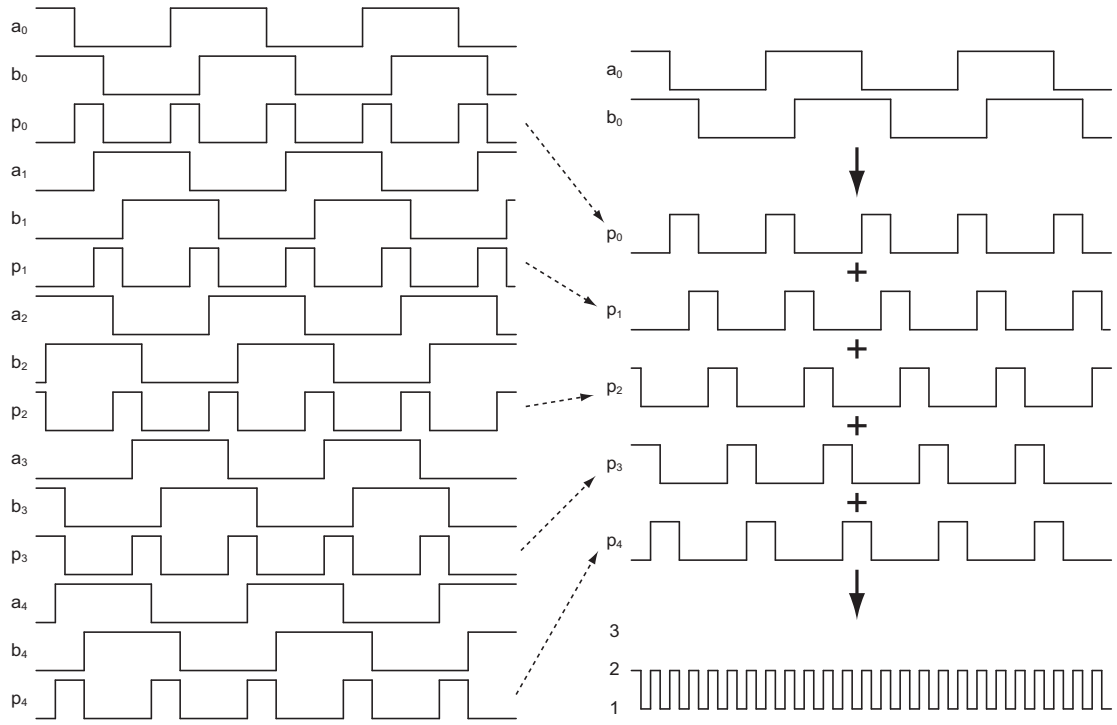

Figure 4-14: Timing diagrams of multiphase VCOs and phase detectors (5).

Figure 4-11 illustrates the timing diagrams when the phase difference is slightly less than $\frac{\pi}{2}$. The DAC output current also alternates between 2 and 3 unit-current, but at a lower duty cycle.

When the phase difference decreases further, the DAC output current will be just 2 unit-current, as is illustrated in Figure 4-12. As the phase difference continues to decrease, the DAC output current also keeps decreasing. Figure 4-13 and 4-14 illustrate how the DAC output current changes when the phase difference continues to reduce. It is obvious that the average DAC output current represents the phase difference, as shown in Figure 4-10 to Figure 4-14.

The peak-to-peak output ripple current can be as high as one unit-current. If only one phase detector is used, the ripple current can be as high as the maximum DAC output current. However, in the case of a multiphase ring VCO, the unit-current of a DAC is much smaller than the maximum DAC output current, and the DAC current becomes smaller as more ring VCO taps are employed. The frequency of the ripple is inversely proportional to the delay of the delay cells in the ring VCO. It is more

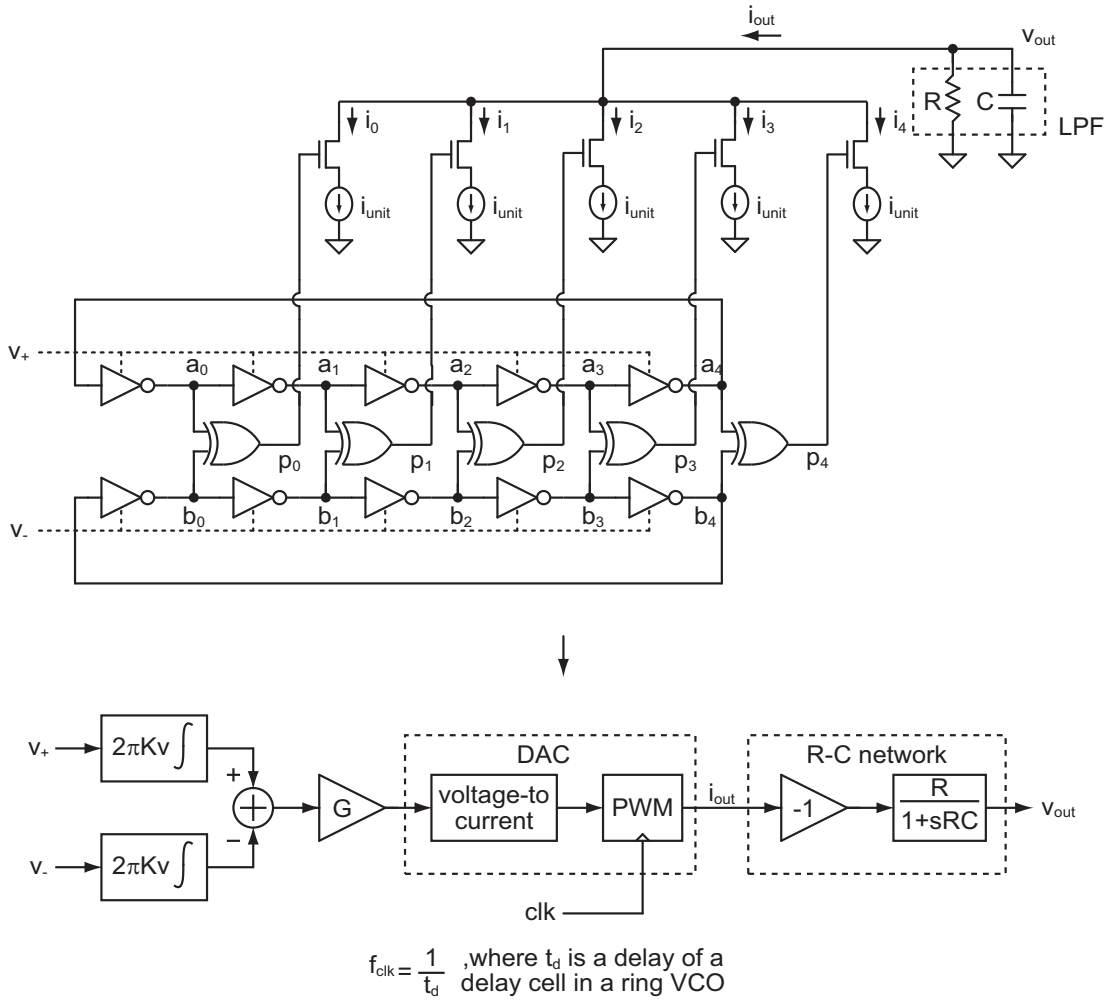

Figure 4-15: Modeling of the proposed VCO-based OP amp (1).

desirable to have a higher ripple frequency because removing a high frequency ripple is easy even by a simple filter. Accordingly, many taps and the short delay of the delay cells of ring VCOs are desired in order to reduce the output ripple.

4.3.2 Simplified Behavioral Model of the Proposed VCO-Based OP Amp

The full behavioral model of the VCO-based OP amp will be used in CppSim simulations for the analysis and verification of the system. However, the simplified behavioral model of the VCO-based OP amp will be useful in the initial design and analysis without also requiring long behavioral simulations because the closed form

equation can be easily derived from the model. If the simplified behavioral models include various design parameters such as the number of the stages of ring VCOs and a DAC unit current, the model will be especially helpful in optimizing the circuits for the VCO-based OP amp. The proposed VCO-based RF modulator's performance is determined by the characteristics of the included VCO-based OP amps for the most part. Therefore, it is important to develop the simplified behavioral model and the closed form equation of the VCO-based OP amp.

The proposed VCO-based OP amp is modeled with several functional building blocks in Figure 4-15. The ring VCOs are modeled as integrators whose gain is $2\pi K_V$. The XOR phase detectors are modeled as subtractors and gain stages. The DACs are modeled as PWM blocks that create a PWM signal. The DC component of the PWM signal corresponds to the output from the phase detectors, and the ripple frequency is $\frac{1}{t_d}$, where t_d is a delay of unit delay cells in a ring VCO. The current signal from the PWM block goes into an RC filter. $\frac{R}{1+sRC}$ is the transfer function of the RC filter with current as an input and voltage as an output.

Figure 4-16 and Figure 4-17 illustrate the DAC waveform from one DAC unit cell with different relative phases of two VCOs. When the phase difference is zero, the output current is zero. When the phase difference increases to $\frac{\pi}{4}$ and $\frac{\pi}{2}$, the average output current also grows to $\frac{i_{unit}}{4}$ and $\frac{i_{unit}}{2}$, respectively. In contrast, when the phase difference is higher than π, the average output current decreases as the phase grows. The sign of the XOR phase detector gain alternates periodically at every π of the relative phase difference. The total current from all the DAC cells will be the sum of the currents of each unit DAC cell, and the current will have the ripple whose frequency is $\frac{1}{t_d}$. In order to model the DAC current precisely, we need a behavioral building block that generates PWM signals, shown in Figure 4-10 to Figure 4-14. The ripple frequency of the PWM signals is also $\frac{1}{t_d}$, but their duty ratios are dependent on the relative phase difference between two ring VCOs. However, the ripple will eventually be filtered by the RC filter, and the effect of the ripple on the overall function of the VCO-based OP amp is trivial. Therefore, in the simplified behavioral models, only the average current of the DAC will be taken into account for calculation

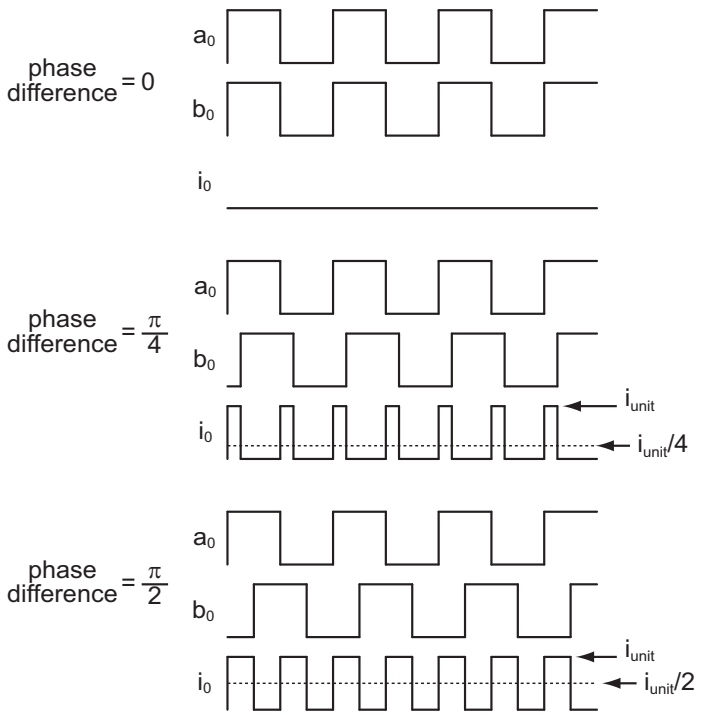

Figure 4-16: DAC output from one DAC unit cell with the phase difference larger than 0 and smaller than π.

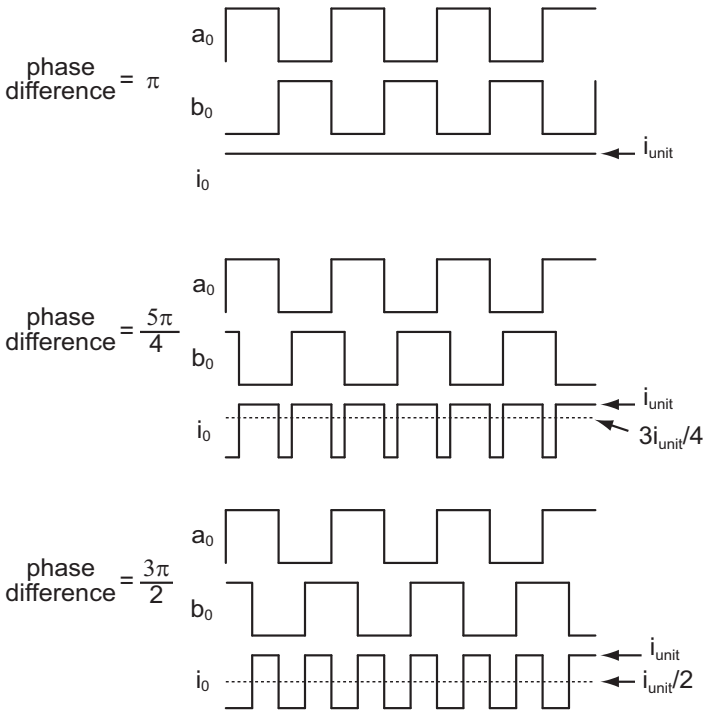

Figure 4-17: DAC output from one DAC unit cell with the phase difference larger than π and smaller than 2π.

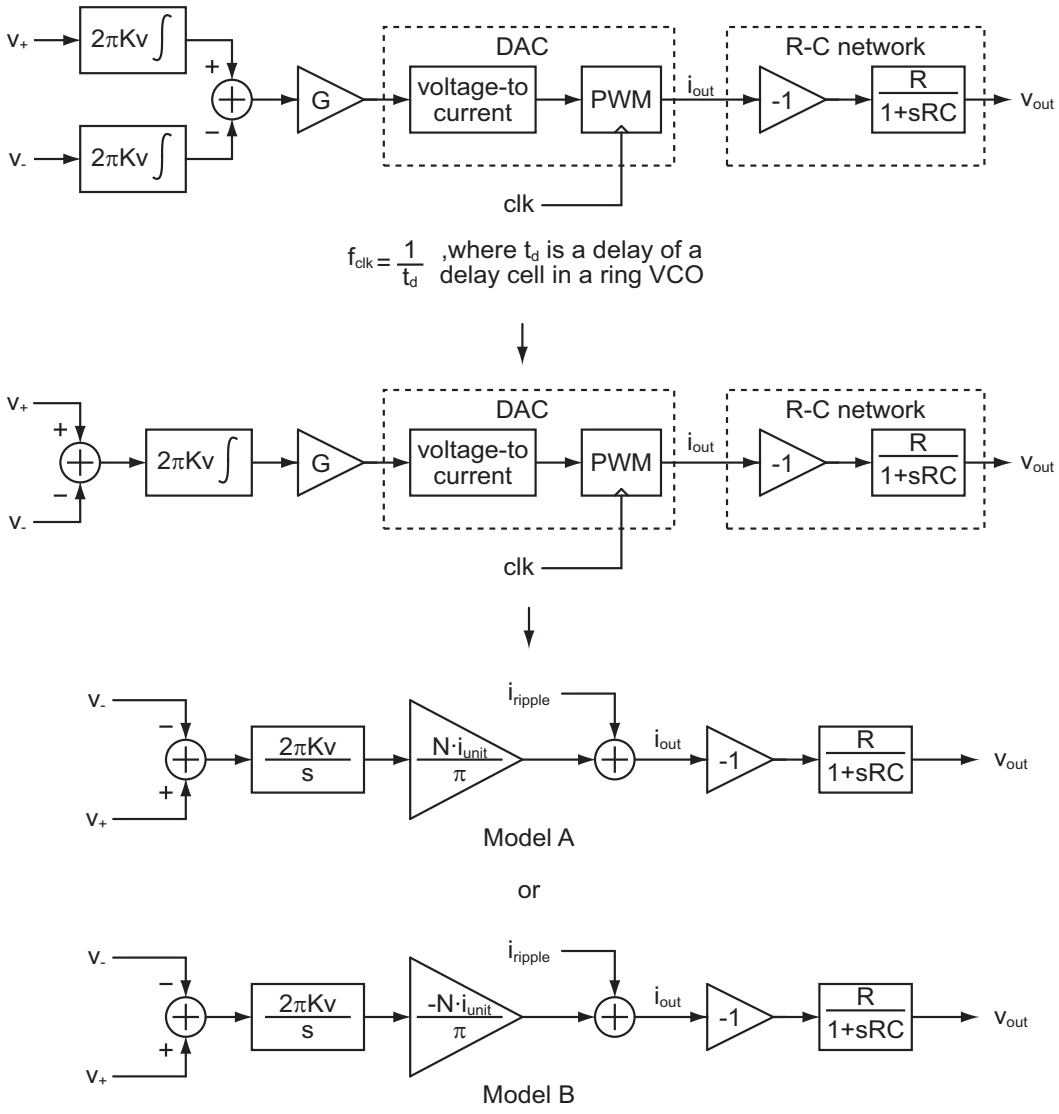

Figure 4-18: Modeling of the proposed VCO-based OP amp (2).

of the various transfer functions.

Figure 4-18 illustrates the final simplified behavioral model of the proposed VCO-based OP amp. The sign of the gain stage that models the phase detector and the DAC depends on the relative phase difference between the two ring VCOs. However, the gain from v_+ to v_{out} should be positive by convention. Accordingly, *Model B* in Figure 4-18 is the appropriate model of the VCO-based OP amp. In most cases, the VCO-based OP amp is used in feedback configuration, and the design will be based on Model B in Figure 4-18; this means that the transfer function of the feedback system based on Model A in Figure 4-18 will be unstable and that the system ends

up working based on Model B in Figure 4-18. A similar operation occurs during the frequency locking process in a PLL using an XOR phase detector. The ripple current from the DAC is not modeled mathematically, as is mentioned earlier. A fixed duty ratio square wave will be applied in the actual CppSim simulations to roughly model the ripple current as an option. The peak-to-peak amplitude of the square wave is i_{unit}, the unit current of a DAC, and the frequency of the square wave is $\frac{1}{t_d}$. This method is not a precise modeling of the ripple current from the VCO-based OP amp, but the modeling should be good enough for the initial design and optimization of the system.

In order to verify the developed simplified behavioral model, we simulate unity gain amplifiers using the VCO-based OP amp. Figure 4-19 compares a unity gain amplifier composed of the full behavioral model of the VCO-based OP amp with one composed of the simplified behavioral model of the VCO-based OP amp. DC current sources are added to set the appropriate output DC voltage. According to the simplified behavioral model shown in Figure 4-19, the transfer function is

$$
\begin{aligned}
v_{out} &= \frac{-R}{1+sRC} \cdot \frac{-2K_V \cdot N \cdot i_{unit}}{s}(v_{in} - v_{out}) + \frac{-R}{1+sRC} \cdot (i_{ripple} - i_{DC}) \\
v_{out} &= \frac{2RK_V N i_{unit}}{s^2RC + s + 2RK_V N i_{unit}} v_{in} \\
&\quad + \frac{-sR}{s^2RC + s + RK_V N i_{unit}} \cdot (i_{ripple} - i_{DC}) \qquad (Model\ B)
\end{aligned} \tag{4.1}
$$

$$
\begin{aligned}
v_{out} &= \frac{-R}{1+sRC} \cdot \frac{2K_V \cdot N \cdot i_{unit}}{s}(v_{in} - v_{out}) + \frac{-R}{1+sRC} \cdot (i_{ripple} - i_{DC}) \\
v_{out} &= \frac{-2RK_V N i_{unit}}{s^2RC + s - 2RK_V N i_{unit}} v_{in} \\
&\quad + \frac{-sR}{s^2RC + s - 2RK_V N i_{unit}} \cdot (i_{ripple} - i_{DC}) \qquad (Model\ A)
\end{aligned} \tag{4.2}
$$

As we mentioned earlier, with appropriate design parameters, only (4.1) based on Model B in Figure 4-18, which shows a desirable low-pass filtering as a unity gain amplifier, will be stable. Equation (4.1) reveals that all three signals, v_{in}, i_{ripple}, i_{DC}

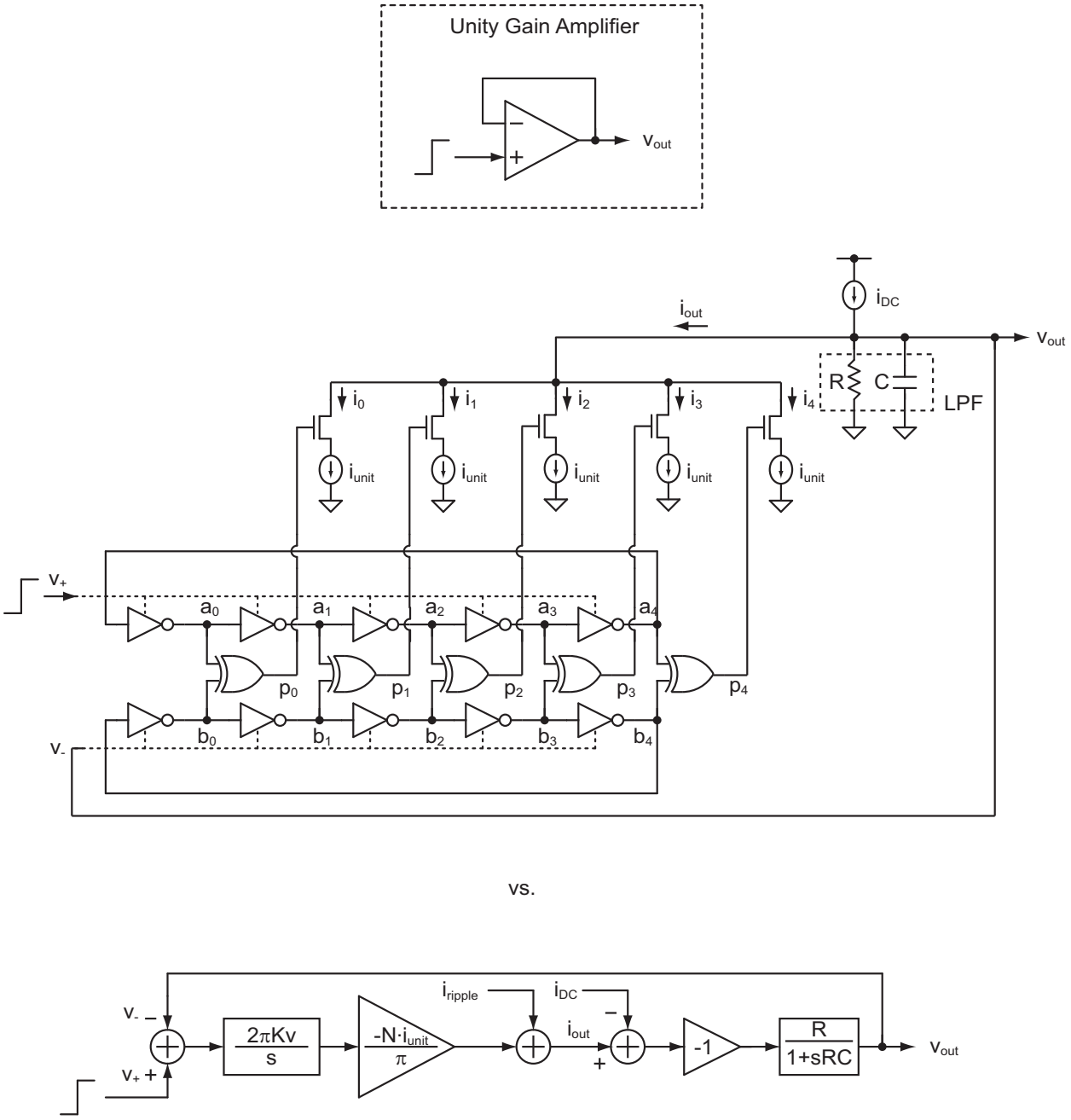

Figure 4-19: Full behavioral model vs. simplified behavioral model of a unity gain amplifier using VCO-based OP amp.

impact v_{out} through transfer functions that contain two poles. In the case of v_{in}, the transfer function is essentially a second order lowpass. In the case of i_{ripple} and i_{DC}, there is an additional zero at the origin which causes their transfer functions to become bandpass in nature.

Figure 4-20 displays the simulation results comparing the full, detailed behavioral model with the simplified behavioral model. In the simulation, 16-stage ring VCOs are used. K_V is around 220 MHz/V, i_{unit} is 125 μA, R is 550 Ω, and C is 3 pF. The full behavioral model and the simplified behavioral model reasonably agree with each other. Hence, the developed simplified behavioral model in Figure 4-18 is sufficient for predicting the characteristics of the VCO-based OP amp. This model will also be used to design the proposed VCO-based RF modulator.

4.3.3 Issues of the Proposed VCO-Based OP Amp

As described so far, an OP amp can be built with multiphase ring VCOs and multiple phase detectors. The VCO-based OP amp does not require any gain stages, and voltage headroom is no longer an issue because the OP amp can be implemented with full-swing logic circuits. The output ripple is the major drawback of this architecture. The ripple can be reduced by employing many taps of the VCOs and a short delay of the delay cells in ring VCOs. However, the VCO gain, K_V, decreases as the number of taps increases[1] so that the unity-gain bandwidth of the OP amp is limited. Moreover, the minimum delay of the delay cells is limited by technology. Therefore, it may not be possible to reduce the output ripple to the desired level in certain processes. Another problem is that the transfer function of the OP amp is a function of K_V, and K_V may vary with input common-mode voltages due to the non-linear tuning characteristics of a ring VCO. When the transfer function varies, the OP amp can be unstable.

[1]Let the delay of one voltage-controlled delay cell d_{unit}, then $d_{unit} = d_{nom} + G \cdot v$, where d_{nom} is a nominal delay, G is a delay gain, and v is a control voltage.

K_V of an N-stage ring VCO using the voltage-controlled delay cell is derived as follows:

$$
\begin{aligned}
f_{VCO} &= \frac{1}{2N \cdot d_{unit}} = \frac{1}{2N \cdot (d_{nom} + G \cdot v)} \\
K_V &= \frac{df_{VCO}}{dv} = \frac{-G}{\{2N \cdot (d_{nom} + G \cdot v)\}^2} \\
K_V\Big|_{v=0} &= \frac{-G}{\{2N d_{nom}\}^2}
\end{aligned}
\tag{4.3}
$$

Thus, K_V decreases when the number of stage increases if the delay gain of the voltage-controlled delay cell is fixed.

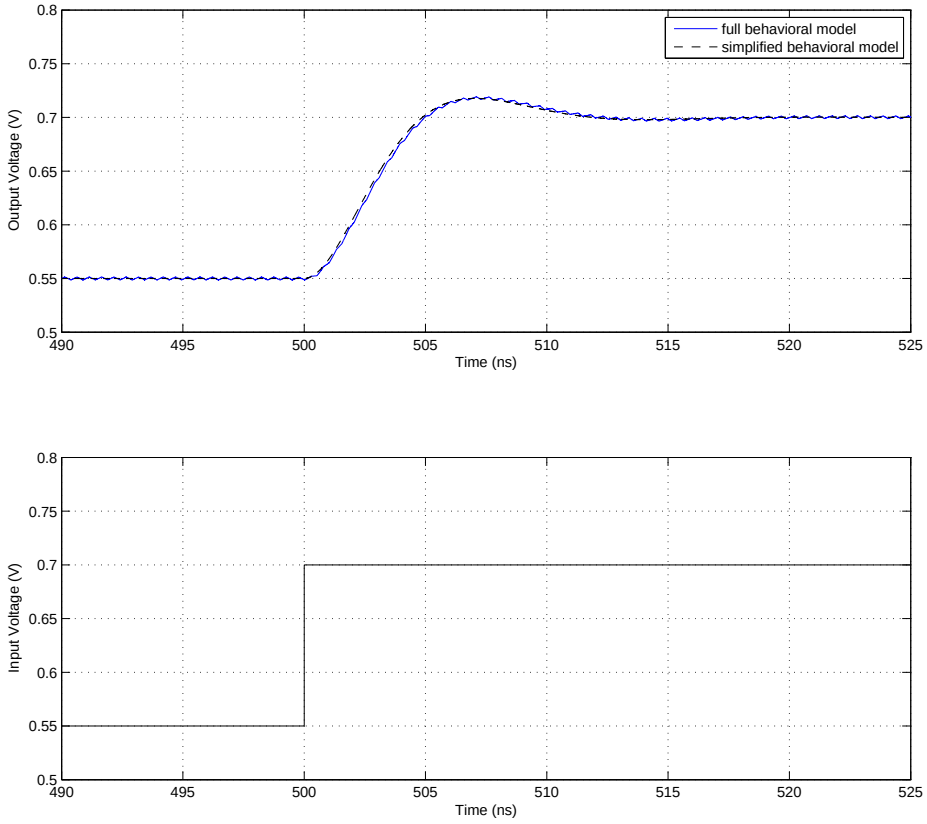

Figure 4-20: Simulation results. Full behavioral model vs. simplified behavioral model of a unity gain amplifier using the VCO-based OP amp.

Therefore, the input common-mode voltage should be limited in order to guarantee its stability. The phase locking range of a phase detector is also related to this issue. The maximum input phase variation of a phase detector is limited so that fast and large phase variation may cause a cycle slip of a phase detector. Hence, the phase locking range of a phase detector will limit the maximum input dynamic range. The other issue of the suggested OP amp architecture is the phase noise of the VCO. The phase noise in this OP amp is considered an input-referred voltage noise. Low phase noise of a ring VCO is challenging, especially in deep sub-micron technology, because of the large flicker noise of a small device.

While the above issues point to limitations in using the VCO-based OP amp for general applications, we will see that it is nicely suited for the multiphase PWM

generator presented here.

In this chapter, the VCO-based OP amp is utilized as a multiphase PWM generator that drives the proposed VCO-based RF modulator, and not as a substitution for a conventional OP amp. Therefore, most of the issues mentioned in this section can be addressed, especially the ripple and the VCO phase noise.

4.4 The Proposed VCO-Based RF Modulator

4.4.1 Proposed VCO-Based RF Modulator Architecture and Its Model

The basic idea of the proposed RF modulator is to employ the VCO-based OP amp to generate multiphase PWM signals that drive mixers, as introduced in Figure 4-4. In Figure 4-21, the multiphase PWM signals, $p_0 \sim p_4$, are generated from the phase detectors of the VCO-based OP amp. Each PWM signal drives additional DAC cells that generate $i_{replica}$. $i_{replica}$ is the baseband signal that will be up-converted by a mixer. In a Gilbert Cell mixer, the baseband current is differential, and the architecture in Figure 4-21 can be simply modified to generate a differential baseband current. i_{in} is the baseband input signal of the multiphase PWM signal generator, and $i_{replica}$ is the output signal. The negative feedback loop tries to keep i_{out} the same as i_{in}, and $i_{replica}$ is simply the replica current of i_{out} with a certain gain determined by the ratio of i_{unit} and i_{unit2}. The maximum amplitude of $i_{replica}$ is controlled by the unit current of the baseband DAC, i_{unit2}. The simplified behavioral model of the proposed architecture helps to derive its transfer function in closed form equations. According to the model shown in Figure 4-22, the transfer function is

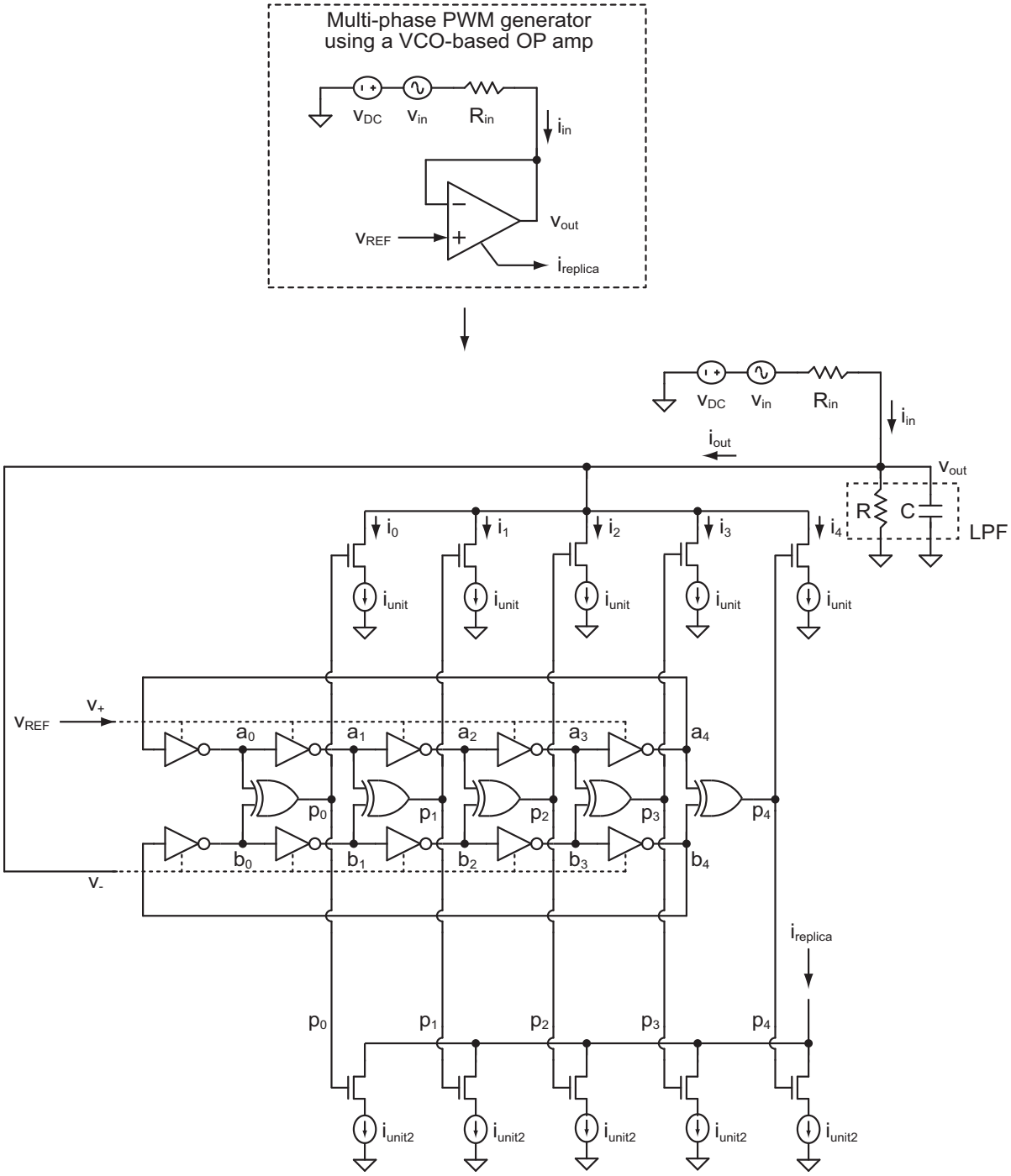

Figure 4-21: Multiphase PWM signal generation using the proposed VCO-based OP amp.

$$
\begin{aligned}
i_{out} &= i_{ripple} + \left(\frac{2\pi K_V}{s} \cdot \frac{-N \cdot i_{unit}}{\pi}\right)\left\{v_{REF} - \left(i_{out} - \frac{v_{DC}+v_{in}}{R_{in}}\right) \cdot \frac{-R \parallel R_{in}}{1+s(R \parallel R_{in})C}\right\} \\
&= i_{ripple} + \left(\frac{-2K_V N i_{unit}}{s}\right) v_{REF} \\
&\quad + \left(\frac{-2K_V N i_{unit}}{s}\right)\left(\frac{R \parallel R_{in}}{1+s(R \parallel R_{in})C}\right)\left(i_{out} - \frac{v_{DC}+v_{in}}{R_{in}}\right) \\
&= \frac{s\{1+s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})}\, i_{ripple} \\
&\quad - \frac{2K_V N i_{unit}\{1+s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})}\, v_{REF} \\
&\quad + \frac{2K_V N i_{unit}(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \cdot \frac{v_{DC}+v_{in}}{R_{in}}
\end{aligned}
$$

$$
i_{replica} = G \cdot i_{out} \qquad \text{, where } G = \frac{i_{unit2}}{i_{unit}}
$$

$$
\begin{aligned}
i_{replica} &= \frac{Gs\{1+s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})}\, i_{ripple} \\
&\quad - \frac{2GK_V N i_{unit}\{1+s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})}\, v_{REF} \\
&\quad + \frac{2GK_V N i_{unit}(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \cdot \frac{v_{DC}+v_{in}}{R_{in}}
\end{aligned} \tag{4.4}
$$

According to (4.4), v_{DC} and v_{in} are filtered by a two-pole low-pass filter. v_{REF} is filtered by a one-zero two-pole filter although v_{REF} will just be a DC voltage that controls the average voltage of the RC filter. The DC component of i_{ripple} will be suppressed according to (4.4). However, i_{ripple} has no DC component because it is a ripple current from the PWM generator. The transfer function for i_{ripple} has two zeros and two poles, and the zeros and the poles will eventually be canceled out at high frequency. Considering that the ripple frequency of the proposed VCO-based OP amp is meant to be high, i_{ripple} will appear at high frequency with almost no filtering. Figure 4-23 illustrates an example of the transfer functions for i_{ripple}, v_{REF},

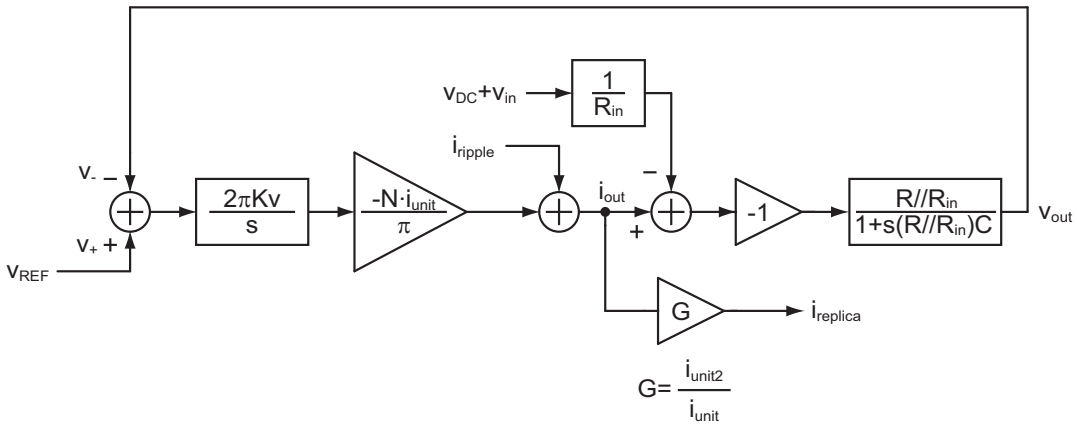

Figure 4-22: Simplified behavioral model of the multiphase PWM signal generator using the proposed VCO-based OP amp.

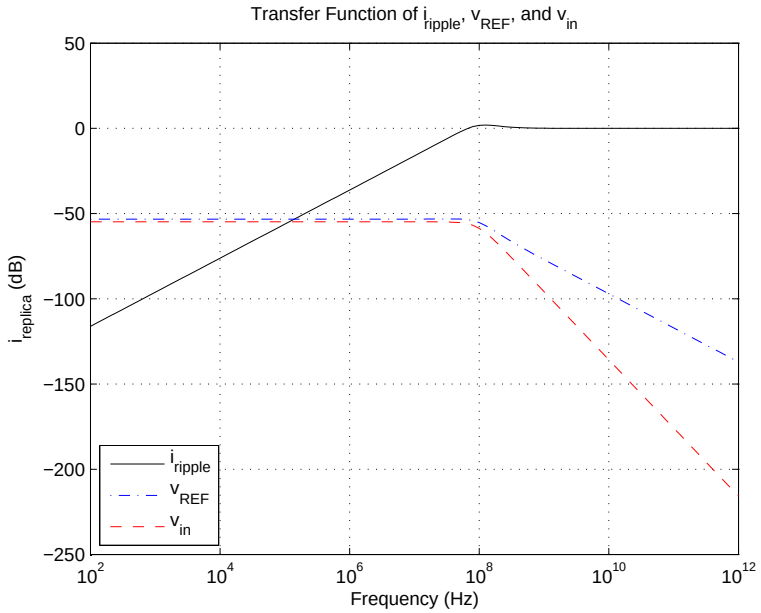

Figure 4-23: The transfer functions for i_{ripple}, v_{REF}, and v_{in}.

and v_{in}. We assume that 16-stage ring VCOs are used in Figure 4-23. K_V is around 220 MHz/V. i_{unit} and i_{unit2} are 125 μA, which means $G = 1$. R is 2.8 $k\Omega$, R_{in} is 550 Ω, and C is 2.5 pF. Note that the transfer function of v_{in} falls off at a rate of -40 dB/ decade while that of v_{REF} decreases at a rate of -20 dB/decade. The two-pole low-pass filter for v_{in}, as shown in Figure 4-23, makes the proposed architecture not only a multiphase PWM signal generator, but also a LPF for a baseband DAC whose output is represented by v_{in} in Figure 4-21. By choosing appropriate design

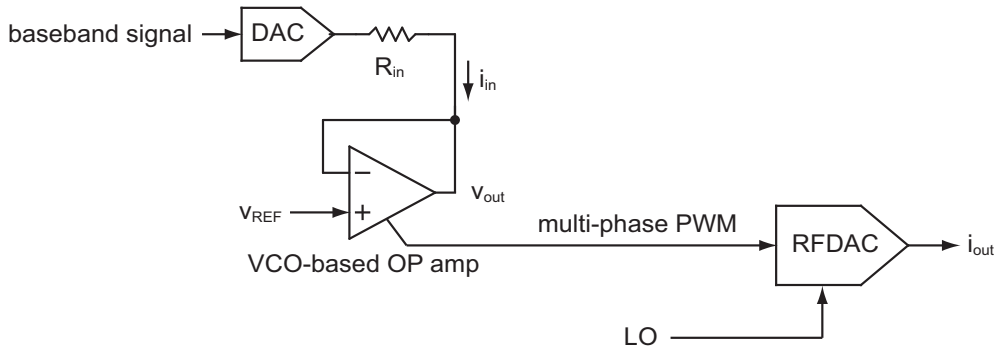

Figure 4-24: Simplified block diagrams of the proposed VCO-based RF modulator using RFDACs.

parameters, the two-pole low-pass filter for v_{in}, or a baseband DAC, can lead to large enough suppression at high frequency to relax the reconstruction filter requirement of the RF modulator. The resistor, R_{in}, gives us more freedom to choose appropriate pole locations of the low-pass filter for enough suppression.

The transfer function of i_{ripple} has two zeros and two poles as mentioned earlier. One zero is located at DC so that i_{ripple} is suppressed at the low frequency. The other zero is located near the two poles with the given parameters. Figure 4-23 shows that there is a little bump due to one zero and two poles which are all located at around 100 MHz. As a result, i_{ripple} is not filtered at high frequency. As was explained in the previous sections, the frequency of the ripple can be very high. For example, if the delay of a delay cell of the VCOs is 50 ps, the ripple frequency is theoretically 20 GHz. This frequency becomes even higher as more advanced technology is employed because device delay becomes shorter. Moreover, the magnitude of the ripple current can be lowered by employing more stages of VCOs and phase detectors, since the peak-to-peak amplitude of the ripple current is i_{unit}, which is inversely proportional to the number of stages with a given maximum output current. Accordingly, even a low-Q reconstruction filter at the output of the proposed RF modulator can suppress the high frequency ripple signals well enough even though the ripple is not filtered by the feedback operation of the proposed multiphase PWM generator. Thus, the ripple current is not a critical issue in this architecture.

Figure 4-24 and Figure 4-25 depict the block diagrams of the proposed VCO-

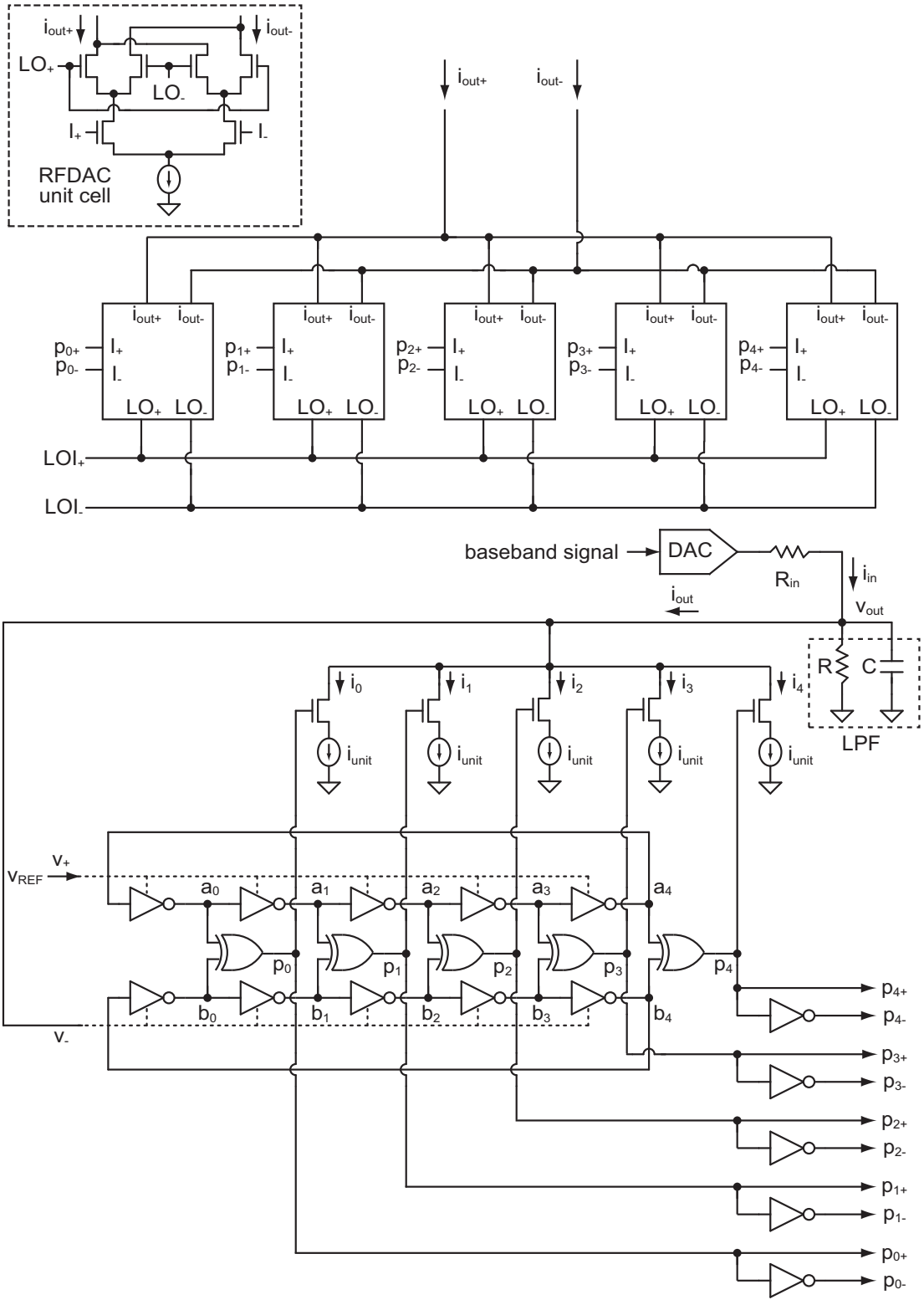

Figure 4-25: Detailed block diagrams of the proposed VCO-based RF modulator using 5-stage RFDACs.

based RF modulator employing RFDACs. Only an in-phase signal path is shown in Figure 4-24 and Figure 4-25, but a quadrature signal path will look exactly the same. The input baseband signal is created by an on-chip or off-chip baseband DAC.

If the baseband DAC is a $\Sigma\Delta$ DAC, the shaped out-of-band quantization noise will be filtered by the two-pole low-pass filter shown in Figure 4-23. Since the out-of-band noise from v_{in} will be suppressed at a rate of -40 dB/decade, the baseband $\Sigma\Delta$ DAC should be a first order or a second order. If a third or higher order baseband $\Sigma\Delta$ DAC is used, the output reconstruction filter should have high enough Q to suppress the excessive out-of-band quantization noise. Note that this RF modulator architecture is proposed in order to eliminate such a high Q LC filter. Therefore, the order of the baseband $\Sigma\Delta$ DAC should be up to 2.

If the baseband DAC is a Nyquist DAC, the image due to the DAC clock frequency will be suppressed by the two-pole low-pass filter. Therefore, the proposed architecture either eliminates the need of an additional reconstruction filter for the Nyquist DAC or lessens the filter requirement.

Another advantage of this architecture is that the ring VCOs and the phase detectors sequentially drive the RFDACs, such that *Dynamic Element Matching* (DEM) is achieved for free. A similar DEM effect in a VCO-based A/D converter is reported [9]. Accordingly, the matching requirement for the RFDACs in Figure 4-25 is more relaxed. The output voltage dependency of the RFDAC current also affects the linearity of the system. As is presented in [39], appropriate device sizing and additional cascode devices for the RFDACs can guarantee a reduction in output voltage dependency of the RFDAC current, such that good linearity of the RFDAC can be achieved.

In addition to the mismatch of the RFDACs and the output voltage dependency of the RFDAC current, the VCO's linearity also affects the overall linearity of the proposed RF modulator. The tuning characteristics of a practical VCO are non-linear. Therefore, the multiphase PWM signals generated by the architecture shown in Figure 4-21 are influenced by the VCO non-linearity. The non-linear relationship between the control voltage and the output frequency makes the VCO gain, K_V,

dependent on the control voltage, which results in a changing transfer function. In Figure 4-21, the voltage of v_- is determined by the loop dynamic while the voltage of v_+ is set to v_{REF}. Ideally, the two input voltages should be *virtually shorted* by a negative feedback operation. Thus, K_V will be constant because the control voltage is fixed, thereby suppressing the non-linearity of the VCOs. Similar non-linearity suppression is also achieved by a negative feedback system employing a traditional OP amp. However, with a large, fast-varying input signal coming in, the feedback cannot catch up with the input signal variation; thus, v_-, which is supposed to be virtually shorted to v_+, ends up being different from v_+. Therefore, K_V changes due to the varying v_-, and the non-linearity of the ring VCO cannot be suppressed sufficiently by the negative feedback loop. In reality, the non-linearity resulting from the non-linear VCO and loop dynamics is unavoidable. The harmonics caused by this non-linearity are dependent on the characteristics of the VCO, but it is possible to predict how much harmonic suppression is achieved by the negative feedback loop. The suppression will be determined by the error voltage of the virtually shorted two input nodes of the VCO-based OP amp, v_+ and v_-; the higher the error voltage, the less the non-linearity suppression. The error voltage, e, can be easily derived by the simplified behavioral model introduced in Figure 4-22.

$$e = v_+ - v_- = v_{REF} - v_{out}$$

$$\begin{aligned} v_{out} &= \frac{2K_V N i_{unit}(R \parallel R_{in})}{s\{1 + s(R \parallel R_{in})C\}}(v_{REF} - v_{out}) + \frac{R \parallel R_{in}}{1 + s(R \parallel R_{in})C} \cdot \frac{v_{DC} + v_{in}}{R_{in}} \\ &= \frac{2K_V N i_{unit}(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} v_{REF} \\ &\quad + \frac{s(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \cdot \frac{v_{DC} + v_{in}}{R_{in}} \end{aligned}$$

$$\begin{aligned} \therefore\ e &= \frac{s^2(R \parallel R_{in})C + s}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} v_{REF} \\ &\quad - \frac{s(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \cdot \frac{v_{DC} + v_{in}}{R_{in}} \end{aligned} \tag{4.5}$$

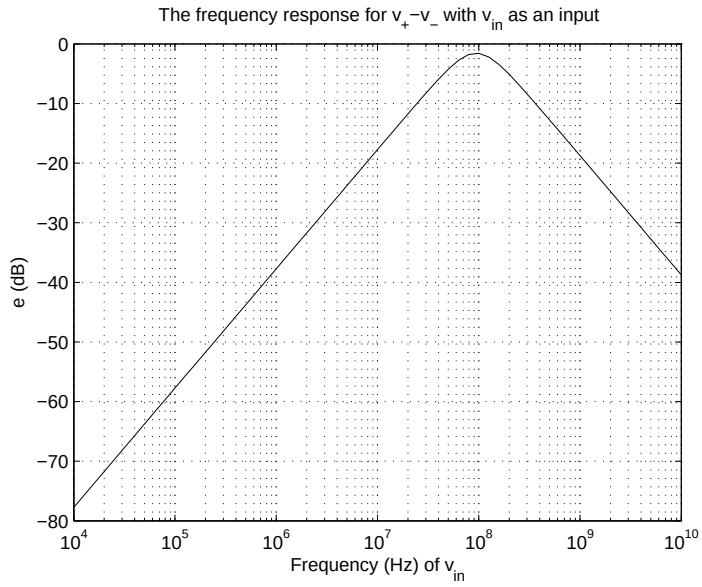

Figure 4-26: The frequency response for error voltage $(v_+ - v_-)$ with v_{in} as an input.

v_{REF} is a DC signal, and the DC term will be suppressed according to (4.5) due to the zero located at DC in the transfer function for v_{REF}. Hence, v_{REF} does not affect e. The baseband input signal, v_{in}, however, affects e. Figure 4-26 shows the frequency response for e with v_{in} as an input. For Figure 4-26, all the design parameters are the same as those for Figure 4-23. Obviously, the higher amplitude of the baseband input signal results in a higher error voltage, which means higher harmonics. Furthermore, Figure 4-26 implies that the non-linearity grows as the input frequency increases because the suppression decreases — if the input frequency is lower than 100 MHz, according to Figure 4-26. These changes can restrict the possible bandwidth of the proposed VCO-based RF modulator. The frequency dependency of the RF modulator's non-linearity will be verified by behavioral simulations.

4.4.2 Noise Analysis of the Proposed Multiphase PWM Generator

The noise analysis of the proposed multiphase PWM generator is performed based on the derived simplified behavioral model of the VCO-based OP amp. Two important noise sources of the proposed VCO-based OP amp are in the ring VCOs and the

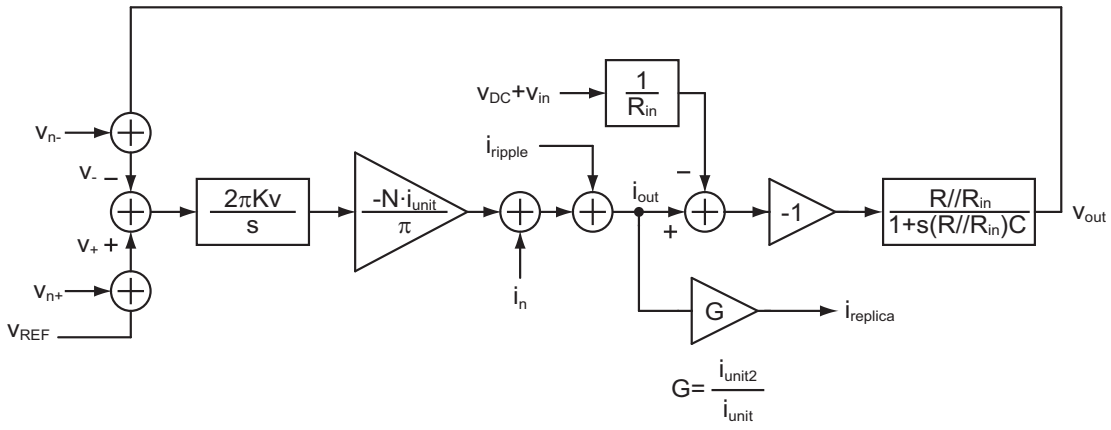

Figure 4-27: Model of the multiphase PWM signal generator using a VCO-based OP amp including noise sources.

DAC. They are easily modeled as input-referred noises or output-referred noises in the simplified behavioral models, as is shown in Figure 4-27, where v_{n+} and v_{n-} are the input-referred phase noise of the ring VCOs, and i_n is the output-referred current noise from the DAC. The input-referred VCO phase noise, v_{n+} and v_{n-}, has the same transfer function as v_{REF}, and the output-referred current noise from the DAC inside the VCO-based OP amp, i_n, has the same transfer function as i_{ripple}. The VCO phase noise will increase the in-band noise floor, but the phase noise will be filtered at high frequency since the transfer function for v_{REF} decreases by 20 dB/decade, as is shown in Figure 4-23. The proposed RF modulator is especially targeted for deep sub-micron CMOS, which usually exhibits large flicker noise. Therefore, the flicker noise from the VCO will appear at in-band without filtering. Conversely, the output-referred DAC noise will be suppressed in-band because of the high-pass filtering effect for i_{ripple}, as is shown in Figure 4-23. As a result, the VCO phase noise will dominate the in-band noise floor if the input baseband DAC has adequately low noise and high resolution.

4.4.3 Locking Range of the Proposed Multiphase PWM Generator

The proposed multiphase PWM generator is similar to a PLL in that the PWM generator consists of VCOs, phase detectors, and a loop filter. The proposed PWM

generator has a limited locking range as influenced by its phase detector, as does a PLL. The analysis method of a PLL can be also applied to the proposed multiphase PWM generator to find out the locking range of the phase detector.

Figure 4-28 shows the phase detector input signal in the simplified behavioral model of the proposed multiphase PWM signal generator. For the XOR phase detector, the locking range is known to be π. Therefore, the phase detector input, y, should also be within π to keep the feedback loop in lock.

$$\begin{aligned}
y = & \frac{2\pi K_V}{s}\left\{v_{REF} - \left(\frac{Ni_{unit}}{\pi}\right)\left(\frac{R \parallel R_{in}}{1+s(R \parallel R_{in})C}\right)y\right\} \\
& - \frac{2\pi K_V}{s}\left\{\frac{R \parallel R_{in}}{1+s(R \parallel R_{in})C}\left(i_{ripple} - \frac{v_{DC}+v_{in}}{R_{in}}\right)\right\} \\
= & \frac{2\pi K_V}{s}v_{REF} - \frac{2K_V N i_{unit}(R \parallel R_{in})}{s\{1+s(R \parallel R_{in})C\}}y \\
& - \frac{2\pi K_V(R \parallel R_{in})}{s\{1+s(R \parallel R_{in})C\{}\left(i_{ripple} - \frac{v_{DC}+v_{in}}{R_{in}}\right) \\
= & \frac{2\pi K_V\{1+s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})}v_{REF} \\
& - \frac{2\pi K_V(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})}\left(i_{ripple} - \frac{v_{DC}+v_{in}}{R_{in}}\right) \qquad (4.6)
\end{aligned}$$

Equation (4.6) shows that y is determined by v_{REF}, i_{ripple}, v_{DC}, and v_{in}. Note that v_{REF} is set to a DC voltage, and the negative feedback loop tries to keep v_{out} the same as v_{REF}. Because v_{out} changes with the varying input voltage, v_{in}, as is shown in (4.5) and Figure 4-26, it is best to set v_{REF} to $\frac{VDD}{2}$ so that v_{out} can have the maximum dynamic range. In addition, the purpose of v_{DC} is to set the offset voltage of the baseband signal such that the maximum voltage variation of v_{in} is guaranteed. For example, if the locking range of a phase detector is $(0,\ \pi)$, v_{DC} should be set such that y is $\frac{\pi}{2}$ when v_{in} is 0. Because v_{REF} and v_{DC} are static values, only the i_{ripple} and v_{in} terms from (4.6) affect the locking range. Interestingly enough, i_{ripple} term will be filtered out by the two-pole low-pass filter according to (4.6). Note that the frequency of i_{ripple} is $\frac{1}{t_d}$, where t_d is a unit delay of a ring VCO. Since the frequency of i_{ripple} is typically very high, the i_{ripple} term in (4.6) is negligible. Therefore, only v_{in}

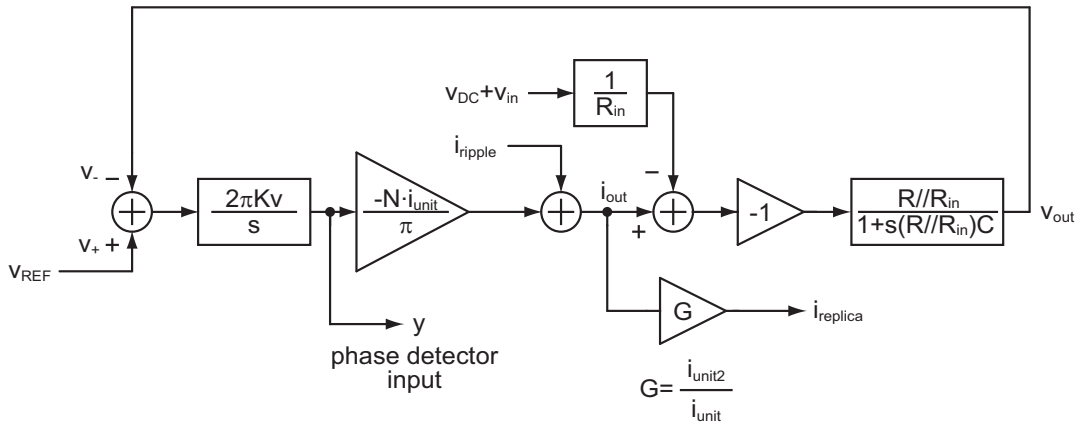

Figure 4-28: Phase detector input in the simplified behavioral model of the proposed multiphase PWM signal generator.

determines the locking range of the system. Assuming that the gain of the two-pole low-pass filter is flat over the in-band, the phase variation created by v_{in} is

$$\begin{aligned} y &= \frac{2\pi K_V (R \parallel R_{in})}{s^2 (R \parallel R_{in}) C + s + 2K_V N i_{unit} (R \parallel R_{in})} \cdot \frac{v_{in}}{R_{in}} \bigg|_{s=0, \text{ at DC}} \\ &= \frac{2\pi K_V (R \parallel R_{in})}{2K_V N i_{unit} (R \parallel R_{in})} \cdot \frac{v_{in}}{R_{in}} = \frac{\pi}{N i_{unit}} \cdot \frac{v_{in}}{R_{in}} \end{aligned} \tag{4.7}$$

where y is the phase detector input in Figure 4-28. (4.7) is an approximation. If there is a peak at a certain frequency in the transfer function, (4.7) is an underestimation of the phase variation created by v_{in} at that frequency. If the gain decreases at a certain frequency, (4.7) is an overestimation of the phase variation at that frequency. However, with appropriate filter design, (4.7) offers us reasonable guidance for the locking range. Assuming that v_{DC} is set properly and the locking range of an XOR phase detector is π, the value of y in (4.7) should be $(-\frac{\pi}{2},\ \frac{\pi}{2})$ for proper phase detector operation. Thus, the dynamic range of v_{in} keeping the system locked is

$$\begin{aligned} -\frac{\pi}{2} &< \frac{\pi}{N i_{unit}} \cdot \frac{v_{in}}{R_{in}} < \frac{\pi}{2} \\ -\frac{N i_{unit} R_{in}}{2} &< \quad v_{in} \quad < \frac{N i_{unit} R_{in}}{2} \end{aligned} \tag{4.8}$$

Therefore, with appropriate v_{DC}, the maximum dynamic range of v_{in} satisfying the

locking range of an XOR phase detector is $Ni_{unit}R_{in}$. In other words, the system will not work if v_{in} does not satisfy (4.8) due to the malfunction of the phase detector. Note that non-linearity of the proposed RF modulator worsens as the input amplitude and frequency grows. Accordingly, the maximum dynamic range of the input baseband signal is also determined by the non-linearity requirement and by the locking range of a phase detector.

4.4.4 Behavioral Level Simulations of the Proposed Multiphase PWM Generator

The proposed multiphase PWM generator employing the VCO-based OP amp is simulated with its behavioral model by CppSim. The output of the proposed VCO-based RF modulator will correspond to the upconversion of $i_{replica}$, so that the performance of the VCO-based RF modulator is predicted by the baseband spectrum of $i_{replica}$.

In the CppSim simulations, 16-stage ring VCOs are used. K_V and the nominal frequency of the ring VCO with $\frac{VDD}{2}$ of the control voltage are around 220 MHz/V and 985 MHz, respectively. Both i_{unit} and i_{unit2} are 125 μA. R is 2.8 $k\Omega$, R_{in} is 550 Ω, and C is 2.5 pF. The VCO phase noise is also included. The flicker noise component of the VCO phase noise is not modeled, for simplicity. The VCO phase noise is -115 dBc at 20 MHz offset from the center frequency. The current noise of the DAC is not modeled because the VCO phase noise is assumed to dominate the in-band noise floor. The delay mismatch between each delay cell of a ring VCO is modeled because delay mismatch is unavoidable in reality.

In the full behavioral model, the ring VCO consists of linear voltage-controlled delay cells, so the period of the ring VCO is linearly controlled by the voltage. This means that the relationship between the control voltage and the output frequency is non-linear. Therefore, the VCO non-linearity is roughly modeled in the CppSim simulations. Note that the non-linearity of a VCO in practical circuits will be different because the delay of a delay cell is not linearly controlled by the voltage. Thus, the non-linearity of the VCO in the prototype chip will be different from that in the

CppSim simulation results. Although the VCO non-linearity is not precisely modeled in the behavioral model, we can still verify the effect of the VCO's non-linearity on the system because the voltage-frequency relationship of the model is non-linear. For example, we can see that the harmonic tones due to the VCO non-linearity will grow as the input frequency increases, as is predicted in Figure 4-26.

Figure 4-29 shows the CppSim simulation results for the proposed multiphase PWM generator. The input baseband signal is a sinusoidal wave whose frequency is 9 MHz. The amplitude of the baseband signal is $\pm\, 522.5\, mV$, which is 95 % of the maximum dynamic range: $\pm\frac{16\times 125\mu A\times 550\Omega}{2} = \pm\, 550\, mV$, by (4.8). Figure 4-29 shows that the VCO phase noise is filtered by the two-pole, one-zero, low-pass filter, as is explained in section 4.4.2. The second harmonic of the baseband signal is created by the VCO non-linearity. The second harmonic is about 60 dB below the main tone, and this harmonic may not be appropriate when strict spectral requirements are imposed by applications such as cellular phone standards. However, it can be tolerable for less strict spectral requirement, such as the wireless LAN standards.

Figure 4-30 shows the voltages of two input nodes of the VCO-based OP amp used in the simulated multiphase PWM generator. v_+ is set to $\frac{VDD}{2}$, which is 0.55 V in this case. v_- is the output voltage of the VCO-based OP amp. v_- is supposed to be virtually shorted to v_+ by the negative feedback loop. However, the feedback loop is not fast enough to catch up with the 9 MHz input signal, so v_- swings from about 0.49 V to about 0.61 V, as is shown in Figure 4-30. Thus, the error voltage, e, is about $\pm\, 60\, mV$. According to Figure 4-26, the gain for e is about -18.5 dB at 9 MHz. Therefore, the expected error voltage from the simplified behavioral model is $e = \pm\, 522.5\, mV \times 10^{\frac{-18.5}{20}} = \pm\, 62.1\, mV$, where the amplitude of the baseband signal is $\pm\, 522.5\, mV$. The calculated value is close to the CppSim results. This voltage swing changes the effective K_V of one of the non-linear ring VCOs and results in the harmonics of the baseband input signal.

The nominal delay of the delay cells in the ring VCO is about 32 ps. Thus, the ripple from the phase detector causes the tone to be around 31 GHz and its harmonics, and the harmonics appear in Figure 4-29, as expected. A tone close to 1 GHz and

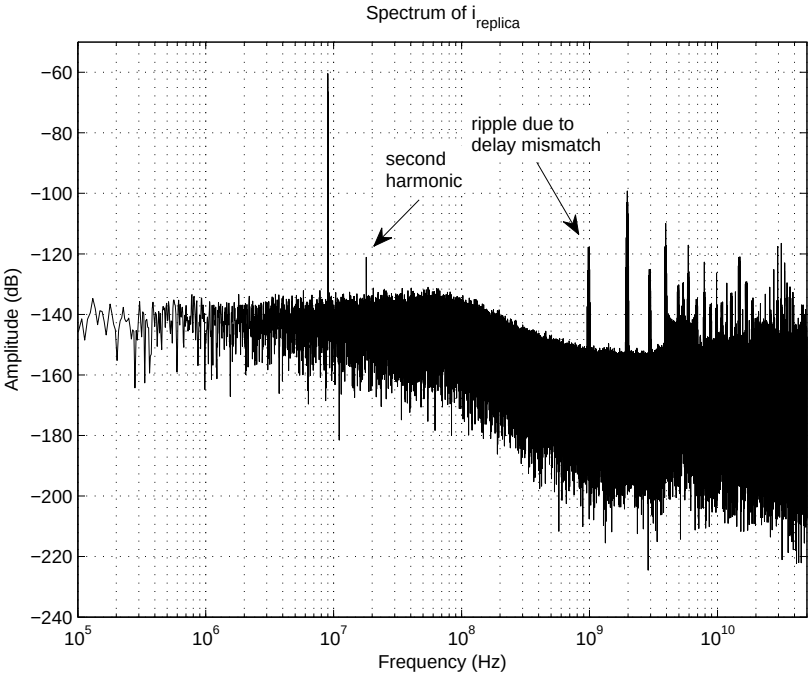

Figure 4-29: Spectrum of $i_{replica}$ from the proposed multiphase PWM generator using the VCO-based OP amp with its full, detailed behavioral model.

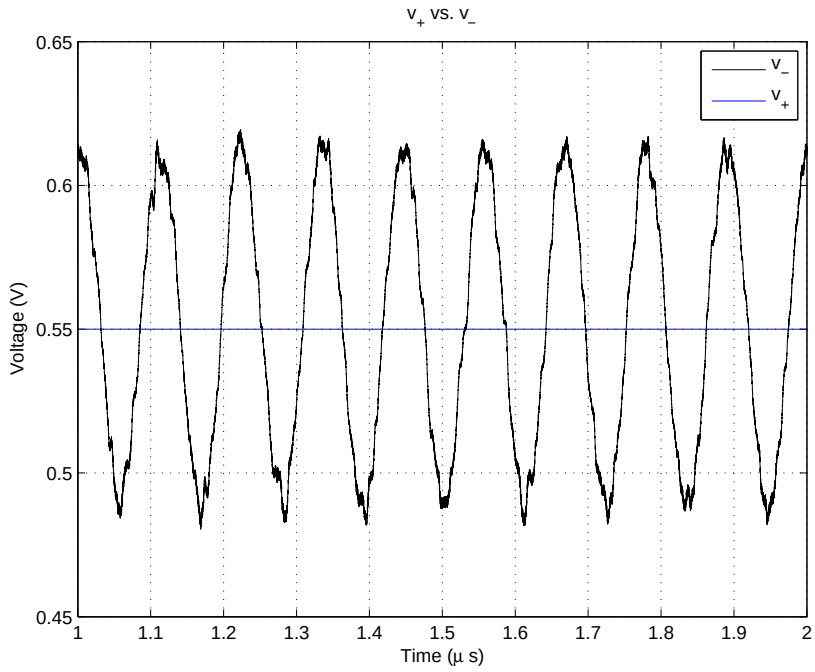

Figure 4-30: The voltages of two input nodes of the VCO-based OP amp.

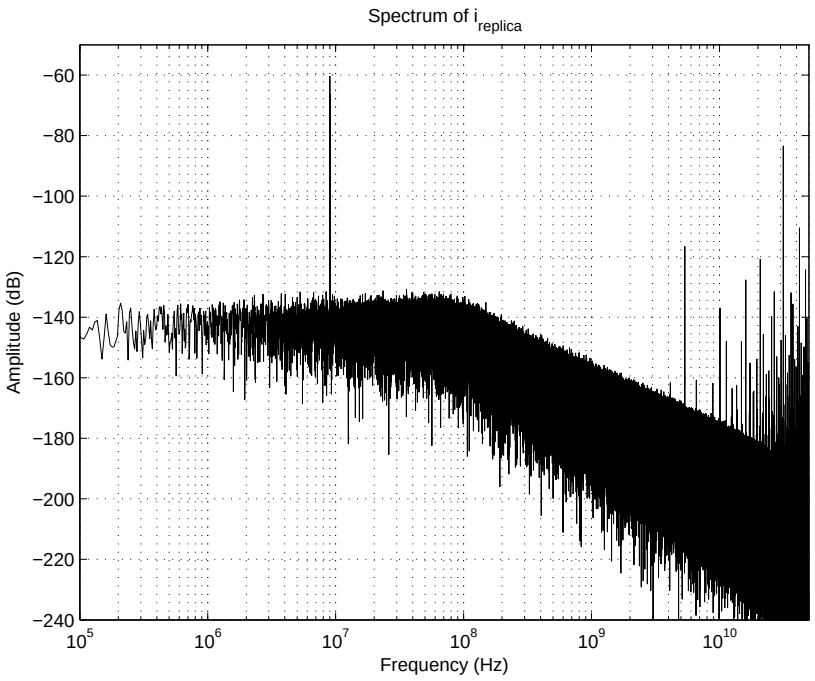

Figure 4-31: Spectrum of $i_{replica}$ from the proposed multiphase PWM generator using the VCO-based OP amp with its simplified behavioral model.

its harmonics are the results of the delay mismatch of the ring VCOs. The delay mismatch of two ring VCOs and an XOR phase detector generates the irregularity of an XOR output signal which repeats at every VCO cycle. Accordingly, at the VCO frequency, the repeated irregularity creates a tone that is about 985 MHz. Many harmonics of this tone also appear in Figure 4-29.

Figure 4-31 shows the spectrum of $i_{replica}$ from the proposed multiphase PWM generator simulated using the simplified behavioral model. The core part including the VCOs and the phase detectors are not modeled with the full, detailed behavioral models, but they are modeled based on the s-domain filter shown in Figure 4-27. The VCO phase noise is added to see the noise filtering characteristics of the system modeled with the simplified behavioral models. The ripple from the phase detector is simply modeled using a fixed duty ratio square wave. Since the VCO non-linearity and the delay mismatch between the delay stages of a ring VCO are not modeled in the simplified model shown in Figure 4-27, the spectrum shows only the ripple caused by PWM.

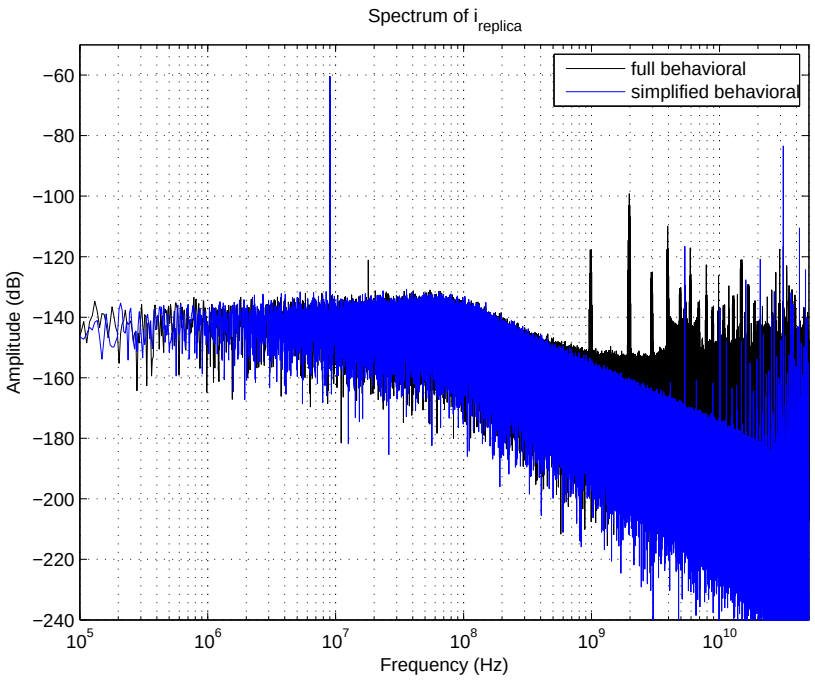

Figure 4-32: Comparison between the full behavioral model and the simplified behavioral model.

Figure 4-32 compares the full behavioral model and the simplified behavioral model. The full behavioral and simplified behavioral models agree with each other reasonably, except for the tones created by the VCO non-linearity and the delay mismatch. Both models show a similar low-pass filtering for the VCO phase noise. Therefore, we can verify that the core part modeled with the simplified behavioral model shown in Figure 4-27 is good enough for the initial design and analysis of the proposed VCO-based RF modulator.

Figure 4-33 shows the spectrum of $i_{replica}$ when the input baseband signal is a 2 MHz sinusoidal wave. The input amplitude is still $\pm$ 522.5 mV. The harmonics of the input signal disappear in Figure 4-33 since the non-linearity suppression is better for the slower input signal, as is predicted in Figure 4-26. Figure 4-34 shows the non-linearity suppression effect more clearly. The v_- swing is about $\pm$ 12.5 mV. Comparing with Figure 4-30, one can find out that the negative feedback loop can better track the slower input signal, even with the same input amplitude. Hence, the v_- swing in Figure 4-34 is suppressed more than the one in Figure 4-30. According to

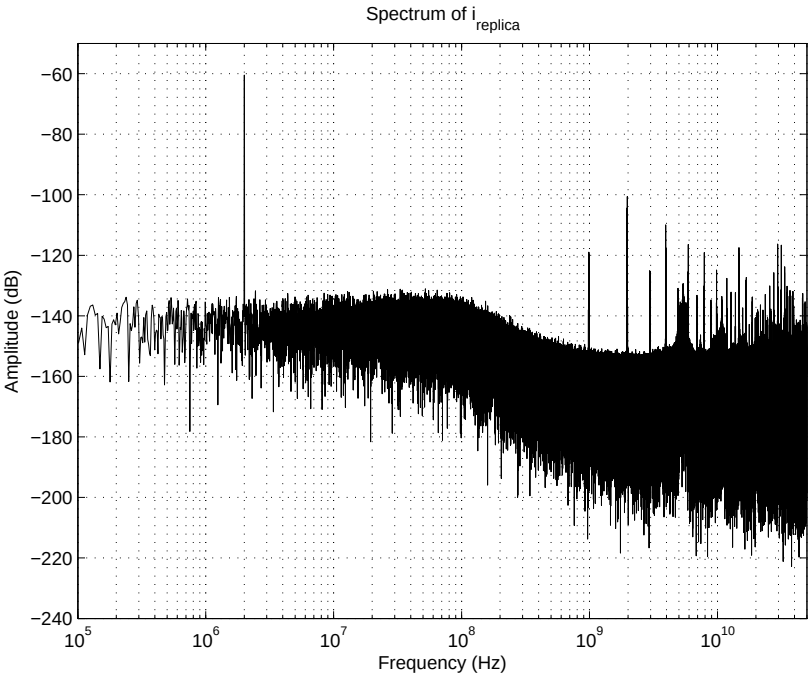

Figure 4-33: Spectrum of $i_{replica}$ from the proposed multiphase PWM generator using the VCO-based OP amp with its behavioral model when the input signal frequency is 2 MHz.

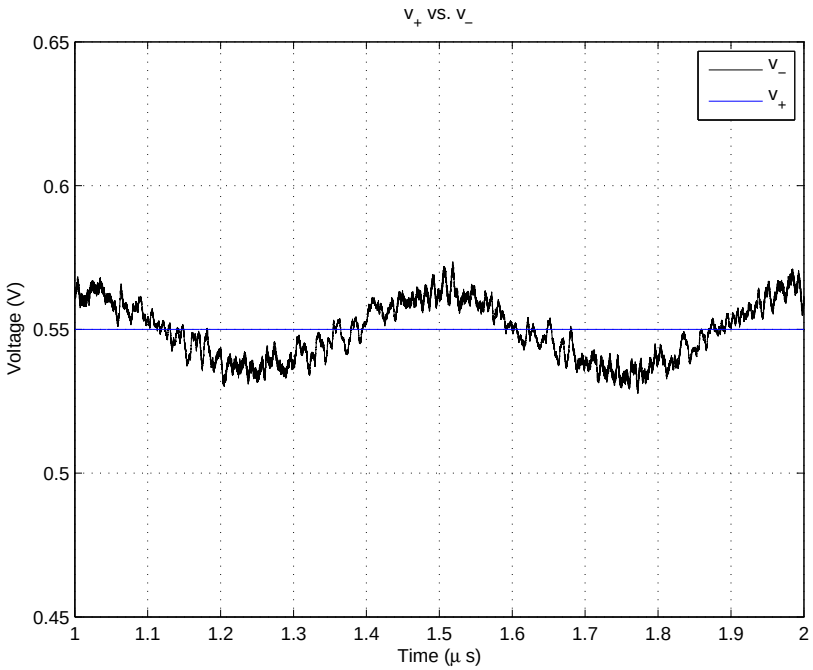

Figure 4-34: The voltages of two input nodes of the VCO-based OP amp when the input signal frequency is 2 MHz.

Figure 4-26, the gain for e is about -31.5 dB at 2 MHz. Therefore, the expected error voltage from the simplified behavioral model is $e = \pm 522.5mV \times 10^{\frac{-31.5}{20}} = \pm 13.9mV$. The calculated value agrees reasonably well with the CppSim results.

4.4.5 Behavioral Level Simulations of the Proposed VCO-Based RF Modulator

The proposed VCO-based RF modulator is simulated with its behavioral model by CppSim. Different filters are applied to the input baseband signal and the phase noise of the VCOs according to (4.4). In Section 4.4.2, we described that the phase noise has the same transfer function as v_{REF} in (4.4). As a result, the input baseband signal is filtered by a two-pole filter, and the phase noise is filtered by a one-zero two-pole filter, according to (4.4) and Section 4.4.2. The characteristics of those filters are determined by the RC filters of the VCO-based OP amps in the RF modulator. We have an on-chip resistor (R) and a capacitor (C), as well as an off-chip resistor (R_{in}). By selecting an appropriate R_{in} value, we obtain the optimized filtering for both the input signal and the phase noise.

By replacing v_{REF} with v_n, which is the input referred VCO phase noise, in (4.4), we can derive the transfer function of the phase noise. The DC gain of the VCO phase noise is

$$\left.\frac{i_{replica}}{v_n}\right|_{s=0,\text{ at DC}} = -\left.\frac{2GK_VNi_{unit}\{1+s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_VNi_{unit}(R \parallel R_{in})}\right|_{s=0} = \frac{G}{R \parallel R_{in}}$$

Thus, the bigger R_{in} value leads to the lower gain of the phase noise. However, too big an R_{in} value can make complex poles for both the input signal and the phase noise transfer functions, thereby resulting in peaking. Figure 4-35 illustrates the transfer function of the input baseband signal with different R_{in} values. Figure 4-35 shows that 1.1 kΩ of R_{in} causes a peaking and 50 Ω of R_{in} makes the bandwidth of the input signal too narrow. Figure 4-36 also depicts the transfer function of the VCO phase noise with different R_{in} values. Obviously, 50 Ω of R_{in} passes too much in-band noise. 1.1 kΩ of R_{in} leads to a peaking. Figure 4-35 and Figure 4-36 suggest that 550 Ω is

the optimum value for both input filtering and in-band noise.

Figure 4-37 is the CppSim simulation result, with $R_{in} = 50\,\Omega$. The baseband input signal is a 20 MHz OFDM signal. Figure 4-37 shows large in-band noise, as is predicted in Figure 4-36. Moreover, the input signal is filtered such that the modulated signal is not flat over in-band. The filtering of the input signal is also predicted in Figure 4-35.

Figure 4-38 is the CppSim simulation result, with $R_{in} = 550\,\Omega$. The figure shows the optimized spectrum for filtering of the input signal and for the phase noise.

Figure 4-39 is the CppSim results, with $R_{in} = 1.1\,k\Omega$. The figure shows a peaking of the phase noise, which can potentially violate the spectral mask. The peaking is also predicted in Figure 4-36.

4.5 Circuit Design

4.5.1 RFDAC

A Gilbert Cell is employed for the unit RFDAC in this work, as it is in [39]. Figure 4-40 illustrates the unit RFDAC cell. The Gilbert Cell is driven by full-swing pseudo-differential signals. Thus, all transistors except for a current source work as simple switches, and the mismatch of the RFDAC cells are dominated by the tail current source. For one to reduce mismatch, the tail transistor must be sufficiently large. Full-swing logic circuits do not draw static currents, but they are generally slower than SCLs. The full-swill logic speed is fast enough to drive the RFDAC cells at higher than 3 GHz in 45 nm CMOS. Moreover, full-swill logic circuits do not require resistors; hence, they are more digital-friendly. Thus, full-swing logic circuits are employed for the RFDAC in this work. The LO signals drive each RFDAC cell through a clock-tree that guarantees an equal distance between the clock load to the source. Therefore, a mismatch between LO_+ and LO_- nodes in Figure 4-40 should be minimal. However, the data signals are generated from a multiphase PWM generator, and it is almost impossible to route each phase of PWM signals to the RFDACs at an equal distance.

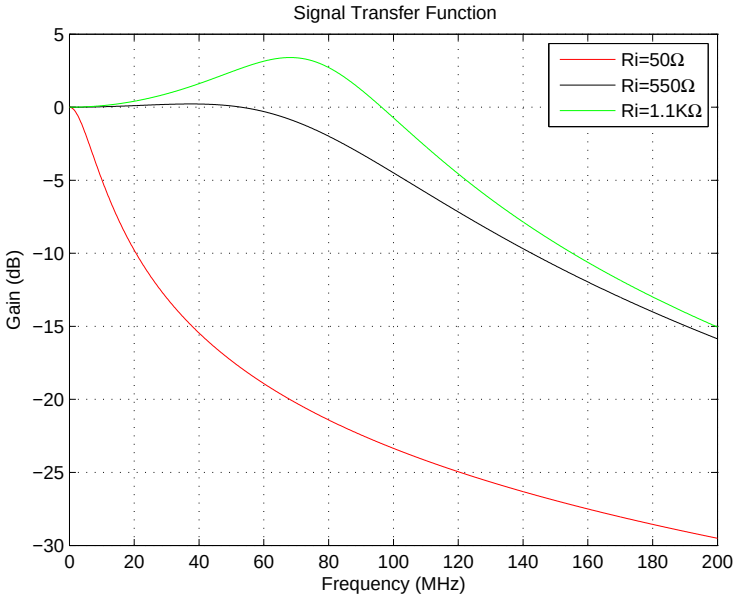

Figure 4-35: The transfer function of the input baseband signal with different R_{in} values.

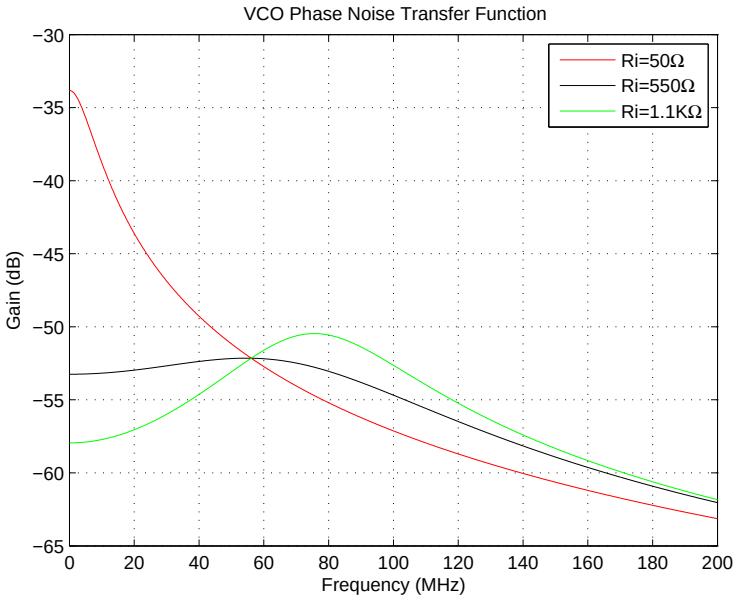

Figure 4-36: The transfer function of the VCO phase noise with different R_{in} values.

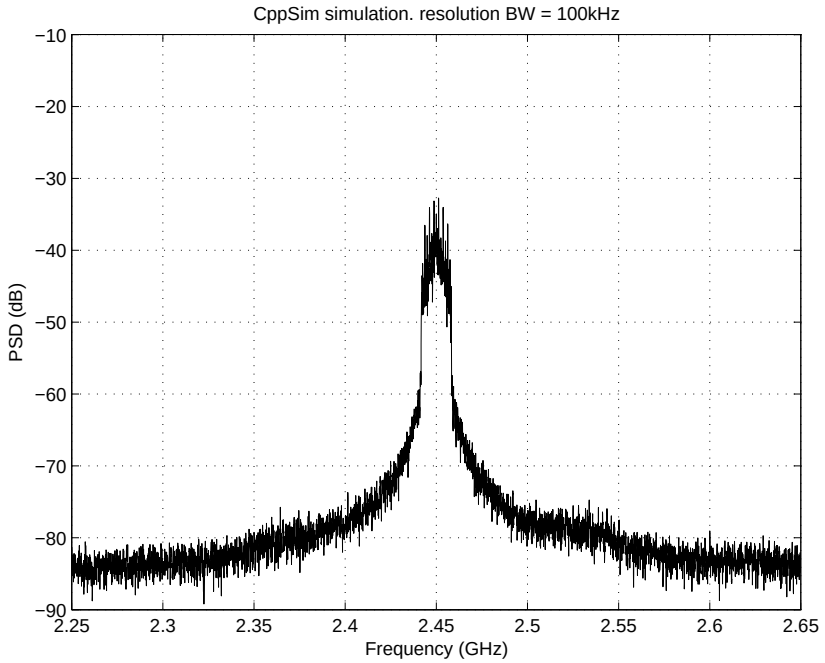

Figure 4-37: The CppSim simulation result with $R_{in} = 50\,\Omega$.

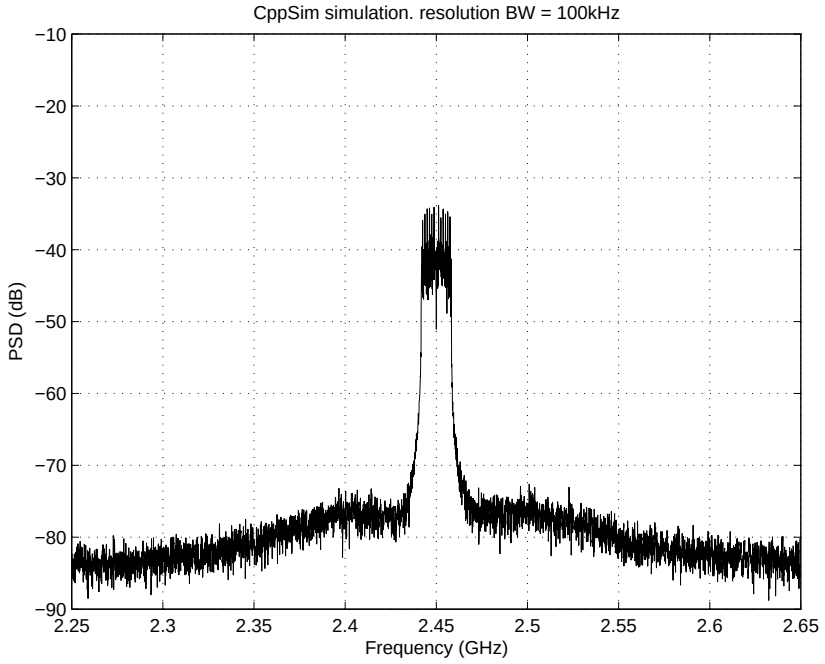

Figure 4-38: The CppSim simulation result with $R_{in} = 550\,\Omega$.

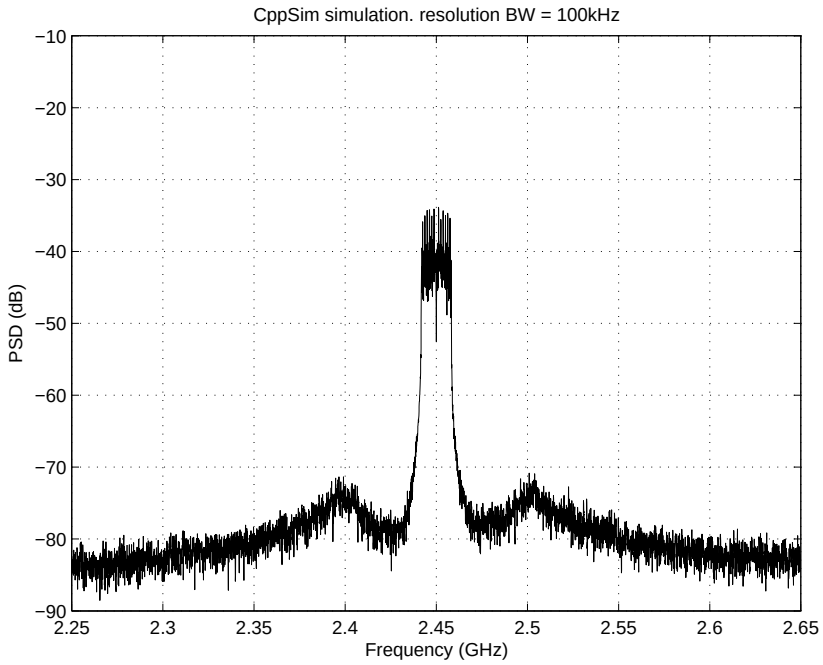

Figure 4-39: The CppSim simulation result with $R_{in} = 1.1\,k\Omega$.

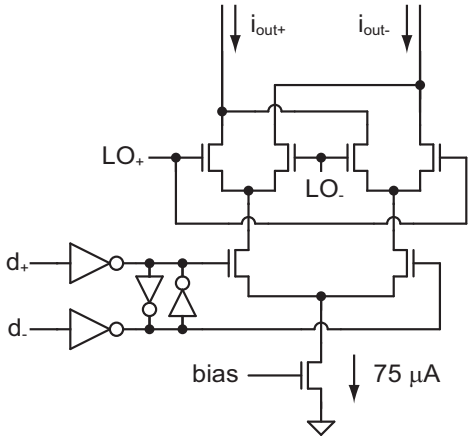

Figure 4-40: Unit RFDAC cell.

Thus, the delay mismatch due to different routing distances for the PWM signals are unavoidable. Local full-swing buffers for the PWM signals are included in each RFDAC cell to make the signal slope steep enough. The cross-coupled inverters in Figure 4-40 help to keep the pseudo-differential signal non-overlapping even with the timing-skew due to device and route mismatch.

A 16-stage RFDAC has been chosen after considering device mismatch and com-

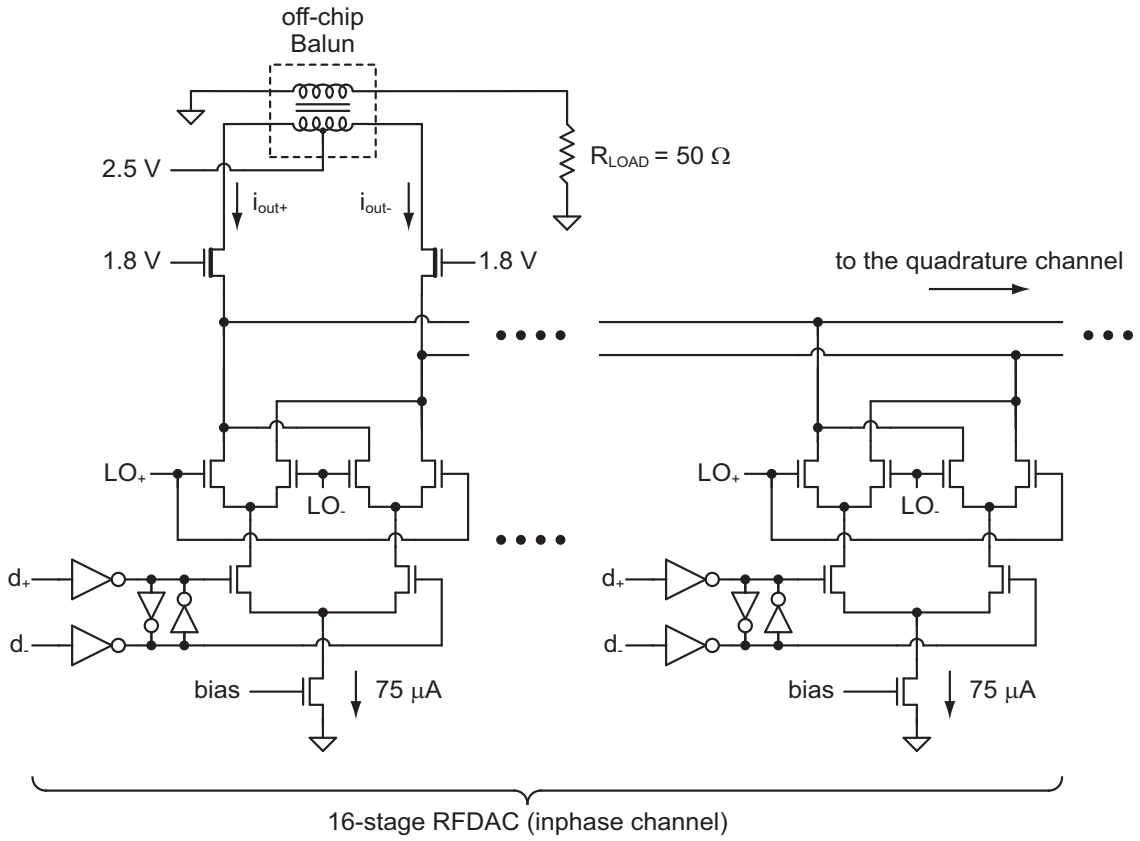

Figure 4-41: 16-stage RFDAC with cascode transistors.

plexity. 2^N stages for the RFDAC also allow equal distance clock-tree routing for each RFDAC cell. Since all the unit RFDAC cells have the same size, the designed RFDAC can be considered a 16-stage thermometer-code RFDAC. Cascode transistors with thick-oxide are connected to the output of the employed 16-stage RFDAC, as is shown in Figure 4-41, to reduce the voltage stress to the RFDACs, which are composed of fast, thin-oxide transistors. The drains of the cascode transistors will be connected to an off-chip balun. The supply voltage of the RFDAC output is 2.5 V, and the cascode devices are sized such that V_{DS} does not exceed 1.8 V, which is the recommended supply voltage for the thick-oxide transistors.

The current noise of the RFDAC is dominated by flicker noise, according to the Spectre simulations. The total integrated noise is about 3.04×10^{-13} A^2, from 100 Hz to 20 MHz, with about 1.1 mA of nominal current; this results in 65 dB of SNR over 20 MHz. The behavioral simulations, including the VCO phase noise, show a noise

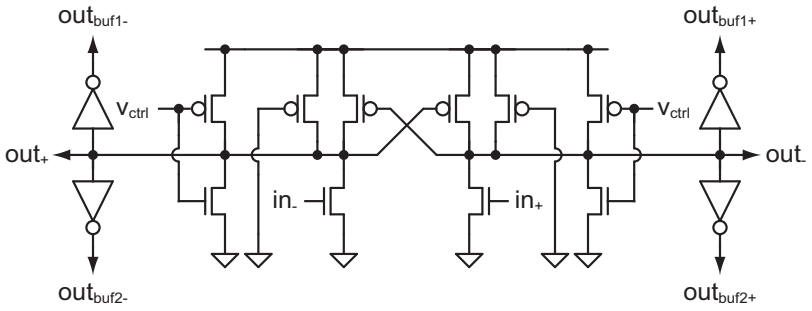

Figure 4-42: Voltage-controlled delay cell.

floor larger than the current noise floor of the RFDAC. Therefore, the noise from the RFDAC is insignificant compared with the VCO phase noise.

4.5.2 Ring VCO

The number of ring VCO stages should be the same as the number of RFDAC stages since each phase detector stage connected to the VCOs drives one RFDAC cell. Hence, a 16-stage ring VCO should be designed. Since the number of the stages is an even number, a differential delay cell is employed. A differential ring VCO is also a better choice because the RFDAC has differential data inputs.

Figure 4-42 shows the voltage-controlled delay cell: a cross-coupled, pseudo-differential delay cell [47]. A pseudo-differential ring oscillator is better than a differential one in terms of phase noise [48]. Each unit delay cell is cross-coupled in order to make a pair of input and output signals differential. v_{ctrl} weakly turns on the NMOS and PMOS depending on the voltage, and changes the current that flows into the output nodes, out_+ and out_-, which ends up changing the delay. The core part of the delay cell does not consume static current due to its pseudo-differential topology and rail-to-rail inputs. However, the NMOS and PMOS transistors controlling the delay draw static currents. The output nodes, out_+ and out_-, are connected to the input nodes, in_+ and in_-, of the next stage. The inverters in Figure 4-42 work as buffers driving XOR phase detectors.

The proposed VCO-based OP amp requires two ring VCOs and one of them generates reference multiphase clock signals. For IQ baseband PWM signal generation by

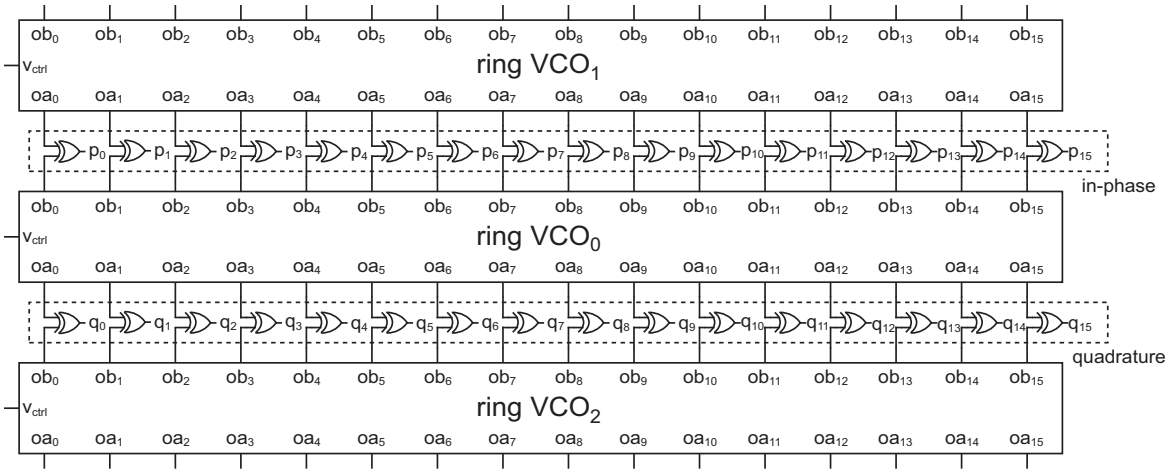

Figure 4-43: Ring VCOs and phase detectors for in-phase and quadrature VCO-based OP amps.

the VCO-based OP amp, two VCO-based OP amps are necessary, but one ring VCO that generates reference clock signals can be shared. In other words, three ring VCOs and two sets of phase detectors are required for IQ baseband PWM signal generation. In this case, the reference ring VCO drives two sets of XOR phase detectors. The delay cell in Figure 4-42 is designed for such a purpose. Two inverters at each node drive different XOR phase detectors. Other VCOs that create feedback paths in the VCO-based OP amp drive only one set of XOR phase detectors, so only one inverter per output node is required. However, the delay cell with two inverters per output node in Figure 4-42 is used for all three ring VCOs to guarantee the same loading at the output nodes, out_+ and out_-.

Figure 4-43 illustrates how the ring VCOs and phase detectors are connected for IQ channel VCO-based OP amps. The outputs and inputs of the ring VCOs and the XOR phase detectors are differential, but Figure 4-43 shows only single-ended signals, for simplicity. *Ring* VCO_0 generates multiphase reference clocks and drives both I-channel phase detectors and Q-channel phase detectors. One set of the output buffers in *ring* VCO_1 and *ring* VCO_2 is not used, as is shown in Figure 4-43, and the unused output buffers effectively work as dummy devices for better matching of the three ring VCOs.

As was discussed in Section 4.4.2, the VCO phase noise is a dominant in-band

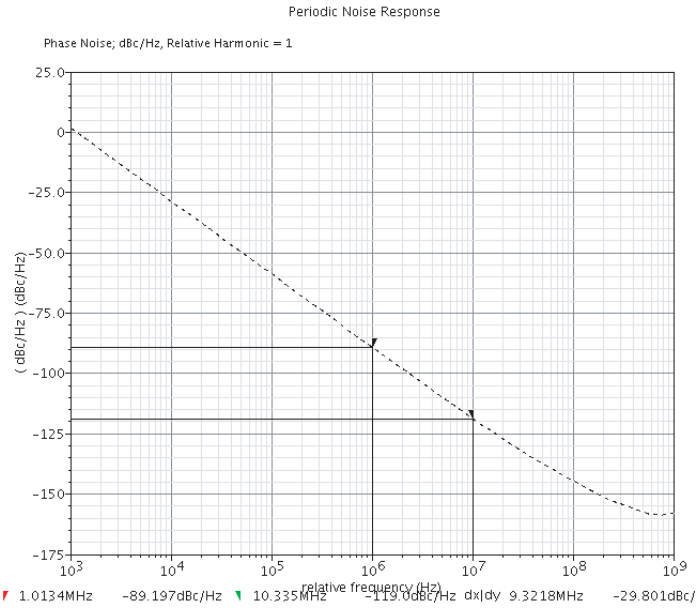

Figure 4-44: The post-layout simulation results for the phase noise of the ring VCO. The VCO frequency is about 985 MHz

noise source of the proposed multiphase PWM generator. One can calculate the in-band noise power caused by the phase noise of the ring VCOs. Post-layout simulations with the ring VCO based on the delay cell in Figure 4-42 shows the phase noise of –127 dBc/Hz at 20 MHz offset from the center frequency and about 185 MHz of K_V with 0.55 V of v_{ctrl}. As is shown in Figure 4-44, the phase noise grows up at a rate of 30 dB/decade below 10 MHz; this means that the flicker noise dominates the in-band VCO phase noise.

In order to quantify the in-band noise due to the VCO phase noise, we revisit the transfer function of the multiphase PWM generator.

$$\begin{aligned} i_{replica} = & \frac{Gs\{1+s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \, i_{ripple} \\ & - \frac{2GK_V N i_{unit}\{1+s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \, v_{REF} \\ & + \frac{2GK_V N i_{unit}(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \cdot \frac{v_{DC} + v_{in}}{R_{in}} \end{aligned}$$

As explained in Section 4.4.2, the input-referred phase noise has the same transfer

function as does v_{REF}, and the output-referred current noise from the DAC has the same transfer function as does i_{ripple}. Since we want to quantify the phase noise component by comparing it to the input signal v_{in}, the above equation can be rewritten as follows:

$$\begin{aligned} i_{replica} = & \frac{2GK_VNi_{unit}(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_VNi_{unit}(R \parallel R_{in})} \cdot \frac{v_{in}}{R_{in}} \\ & - \frac{2GK_VNi_{unit}\{1 + s(R \parallel R_{in})C\}}{s^2(R \parallel R_{in})C + s + 2K_VNi_{unit}(R \parallel R_{in})} (v_{n+} - v_{n-}) \end{aligned} \tag{4.9}$$

where v_{n+} and v_{n-} are the input-referred phase noise from the two ring VCOs of the multiphase PWM generator, as is shown in Figure 4-27. Note that since v_{n+} and v_{n-} are uncorrelated random noises, they are added together even with the *minus* symbol between them. The SNR is calculated via the ratio between the signal power and the noise power. The v_{in} term is the signal, and the $(v_{n+} - v_{n-})$ term is the noise in (4.9). Then, the SNR is

$$\begin{aligned} SNR &= \frac{(R \parallel R_{in})^2 \, v_{in,rms}^2}{\int_{in-band} R_{in}^2 \, \{1 + j\omega(R \parallel R_{in})C\}^2 \, (v_{n+}^2 + v_{n-}^2) \, \mathrm{d}\omega} \\ &= \frac{(R \parallel R_{in})^2 \, v_{in,rms}^2}{\int_{in-band} 2 \, R_{in}^2 \, \{1 + s(R \parallel R_{in})C\}^2 \, v_n^2 \, \mathrm{d}\omega} \end{aligned} \tag{4.10}$$

Equation (4.10) assumes that the two ring VCOs have the same noise power. R is $2.8\,k\Omega$, R_{in} is $550\,\Omega$, C is 2.5 pF, K_V is 185 MHz, N is 16, and i_{unit} is $125\,\mu A$. With these parameters, the 3-dB bandwidth of the denominator in (4.10) is about 70 MHz. Because the target signal bandwidth in this work is at most a few tens of MHz, the filtering effect of the two-pole, one-zero filter of $(v_{n+} - v_{n-})$ term in (4.9) can be neglected.

$$SNR \approx \frac{(R \parallel R_{in})^2 \, v_{in,rms}^2}{2 \, R_{in}^2 \, v_n^2} \tag{4.11}$$

The input-referred noise spectral density of a VCO phase noise is calculated with the following equation when the phase noise is caused by white noise such as device

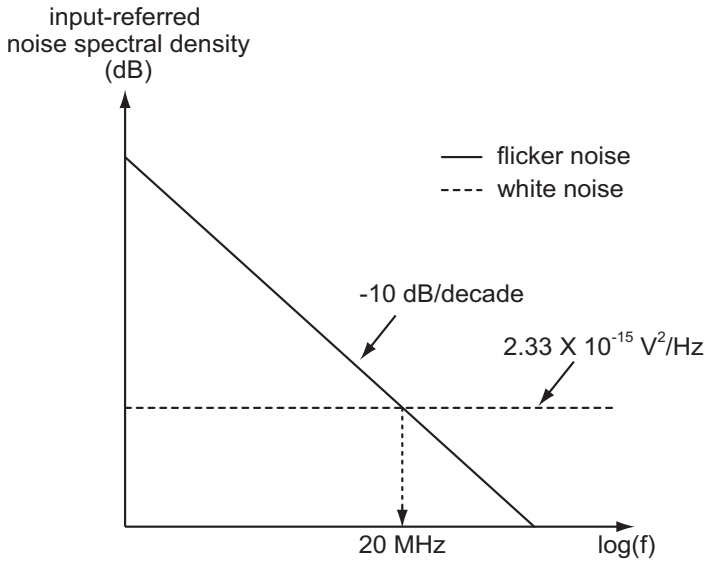

Figure 4-45: Input-referred noise spectral density for a VCO phase noise when flicker noise dominates and white noise dominates. The noise density number is from the post-layout simulations for the designed ring VCO in 45 nm CMOS technology.

thermal noise.

$$v_n^2(f) = \frac{f_{offset}^2}{K_V^2} \cdot 10^{\frac{phase\ noise}{10}} \quad \text{(for all the frequency)} \tag{4.12}$$

where f_{offset} is the offset frequency at which the phase noise is measured, K_V is the VCO gain, and *phase noise* is in dBc/Hz. The calculated input-referred noise spectral density is about 2.33×10^{-15} V^2/Hz for the designed ring VCO, whose phase noise is – 127 dBc at 20 MHz offset and K_V is 185 MHz. However, the input-referred voltage noise should be flicker noise rather than white noise, according to the simulation results. Therefore, the noise spectral density should go up at a rate of 10 dB/decade as the frequency decreases, as the solid line shows in Figure 4-45. The spectral density of the flicker noise is simply modeled as follows:

$$v_n^2(f) = \frac{2.33 \times 10^{-15}\ (V^2/Hz) \times 20 \times 10^6\ (Hz)}{f} \tag{4.13}$$

By integrating the noise spectral density in (4.13) over the in-band frequency range, we can calculate the total noise power of the ring VCO. Note that the flicker noise

diverges to infinity at DC. Since the output signal of the multiphase PWM generator will be directly up-converted to the carrier frequency by the RFDACs, we can expect the SNR of the OFDM signal at the frequency bins near the carrier frequency will be worse than those at other frequency bins. For the noise power estimation, the total noise power is calculated by integrating the spectral density in (4.13) from 100 Hz to 20 MHz, as was done in Section 4.5.1. This approximation underestimates the noise power around DC, but should still be a reasonable estimation. The total noise power from 100 Hz to 20 MHz is

$$\begin{aligned} v_n^2 &= \int_{100}^{20\times10^6} \frac{2.33\times10^{-15}\ (V^2/Hz)\times 20\times10^6\ (Hz)}{f}\, df \\ &= 2.33\times10^{-15}\times 20\times10^6 \cdot \Big[ln(f)\Big]_{100}^{20\times10^6} \approx 568.8\times10^{-9}\ V^2 \end{aligned}$$

The signal power of the proposed multiphase PWM generator is determined via the input signal swing, which is limited by the locking range of the XOR phase detector, as is discussed in Section 4.4.3. The maximum input signal swing with $N = 16$ and $i_{unit} = 125\,\mu A$ is $\pm 550\,mV$, according to (4.8). If the input signal is a sinusoidal wave with $\pm\,500\,mV$ peak amplitude for conservative estimation, then

$$v_{in,rms}^2 = \frac{\big(500\,mV\big)^2}{2} = 125\times10^{-3}\,V^2$$

With these numbers plugged in (4.11), the estimated SNR with the phase noise is

$$SNR \approx \frac{(R \parallel R_{in})^2\, v_{in,rms}^2}{2\,R_{in}^2\, v_n^2} = \frac{(2.8\,k\Omega \parallel 550\,\Omega)^2\times 125\times10^{-3}V^2}{2\times 550\,\Omega^2\times 568.8\times10^{-9}\ V^2} \approx 49\,\text{dB} \approx 7.8\text{-bit}$$

A comparison of this SNR with the SNR due to the current noise of the RFDAC (introduced in Section 4.5.1) reveals that the VCO phase noise dominates the in-band noise floor.

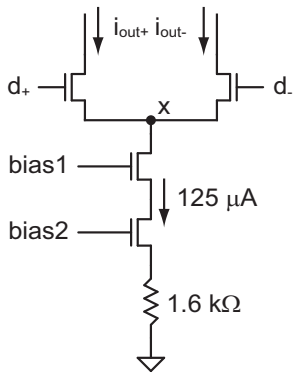

Figure 4-46: The unit DAC cell used for the proposed multiphase PWM generator.

4.5.3 DAC for the VCO-Based OP Amp

The proposed multiphase PWM generator requires a DAC, as was introduced in Figure 4-21. Since the RFDACs and the ring VCOs are differential, this DAC is also implemented differentially. The DAC is composed of 16 unit DAC cells, as were the RFDACs. Figure 4-46 shows the unit DAC cell circuit. If there were only one switching device in Figure 4-46, the voltage at the node X would drop to zero when the DAC is turned off. This leads to slow turn-on time and a large glitch at the output current when the DAC is turned on again, and can cause large *Inter Symbol Interference* (ISI). Since the DAC in Figure 4-46 has two differential switching devices, the voltage at the node X will remain relatively constant, even with one of the switching devices turned off in a differential DAC. Thus, a differential DAC has not only better common-mode noise rejection but also lower ISI at the cost of power.

Although the in-band DAC current noise is filtered by the zero located at DC in the transfer function of the proposed multiphase PMW generator (as explained in section 4.4.2), the filtered DAC noise could still be large if the flicker noise component of the DAC is large. The degeneration resistor in Figure 4-46 helps to reduce the noise of the DAC by suppressing the noise contribution, including the flicker noise, of the tail current transistor. The Spectre simulation results show that the DAC current noise is still dominated by a flicker noise. The total current noise of the 16-stage DAC is $2.58 \times 10^{-13}\,\mathrm{A}^2$ from 100 Hz to 20 MHz with 1.87 mA of a nominal current, and the resulting SNR over 20 MHz is 71 dB. With the filtering effect of the multiphase

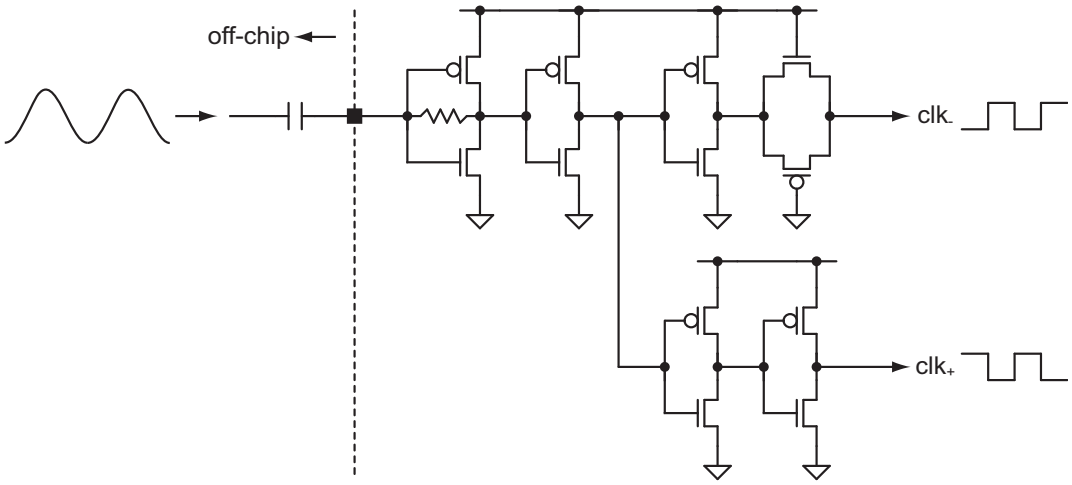

Figure 4-47: A single-to-differential clock converter.

PWM generator, the current noise of the DAC will be lower than this estimation.

4.5.4 Quadrature LO Generation

SCL, which is also called *Current-Mode Logic* (CML), is the fastest topology for high-speed digital circuit design, and it is frequently chosen for many high-speed digital applications. However, an SCL circuit requires static current and, therefore, larger power consumption. On the other hand, full-swing logic consumes less power but is slower in speed. Therefore, full-swing logic is the preferred implementation vehicle so long as the operation is sufficiently slow to support it. In this work, IQ LO clock signals are generated by full-swing logic circuits since 45 nm CMOS is fast enough to deal with 2.5 GHz IQ clock generation by employing full-swing logic. Figure 4-47 illustrates how to generate a pseudo-differential full-swing clock signal from an off-chip signal generator. The feedback resistor in the first stage inverter defines the input bias voltage such that a maximum output swing voltage is achieved. The absolute value of the resistance is unimportant, so a poly resistor with large process variation can be employed without a problem. There could be a timing skew between clk_+ and clk_- due to the mismatch of each clock signal path. However, the buffers with cross-coupled inverters are used after the single-to-differential converter stage, and these buffers reduce the timing skew.

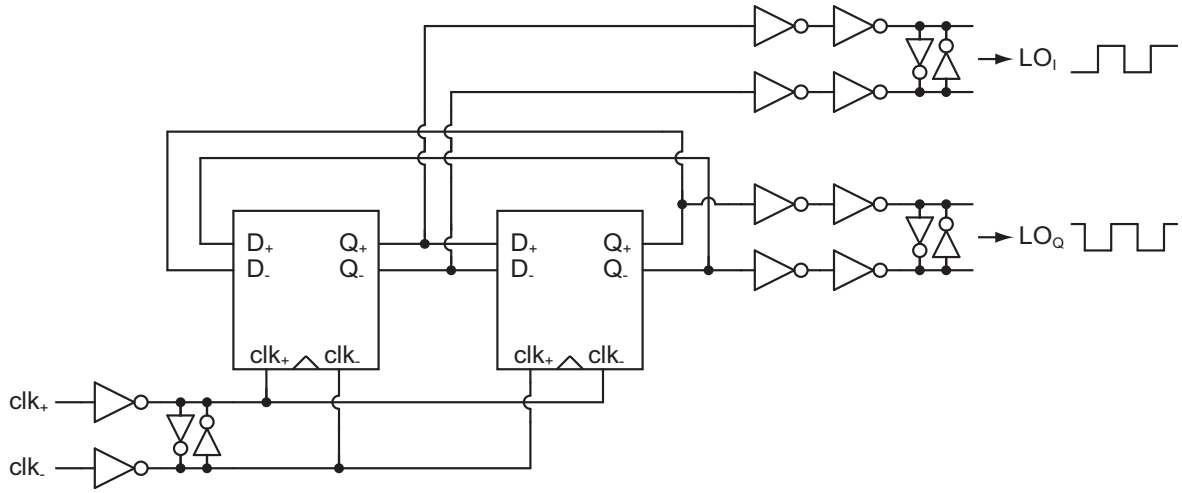

Figure 4-48: An IQ clock generator.

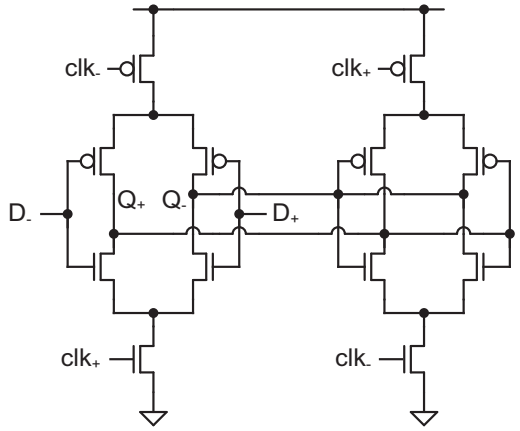

Figure 4-49: A pseudo-differential D flipflop.

The outputs from the single-to-differential clock converter drive an IQ clock generator, which is depicted in Figure 4-48. The IQ clock generator employs pseudo-differential D flipflops to create a 2.5 GHz IQ clock from a 5 GHz clock signal. Figure 4-48 shows the circuits for a pseudo-differential D flipflop. Because of the clock-to-Q delay of D flipflops, the phase difference between LO_I and LO_Q cannot be exactly 90 °, which will result in an imperfect image rejection. The image rejection will be improved by digital compensation when the baseband signal is generated. The digital compensation for the IQ mismatch will be discussed in Section 4.6.

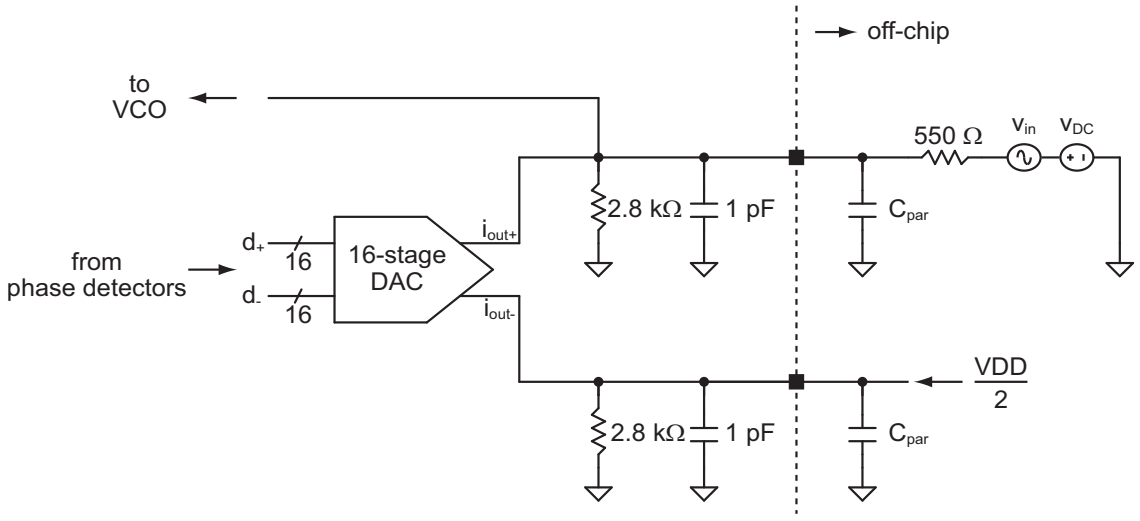

Figure 4-50: Off-chip RC filters for a multiphase PWM generator.

4.5.5 RC Filter

The proposed multiphase PWM generator requires RC filters as loop filters. The RC filter determines the transfer function and can also affect the stability of the negative feedback loop. On-chip *lateral flux capacitors*, which are also called *interdigitated finger capacitors*, are employed for the RC filters. The capacitance of a lateral flux capacitor is determined by the oxide's dielectric constant and the metal dimensions [49]. These are reasonably controlled, even in deep sub-micron CMOS; hence, the process variation of a lateral flux capacitor is tolerable. On-chip poly resistors are employed for the RC filters, but off-chip resistors are also employed for a flexible chip testing. The off-chip resistor is equivalent to R_{in} in Figure 4-25. Figure 4-50 illustrates the combination of on-chip and off-chip resistors. In Figure 4-50, the on-chip capacitance and resistance are 1 pF and 2.8 kΩ, respectively. The off-chip resistance is 550 Ω in Figure 4-50, as an example, but will be adjusted to find out the optimum filter characteristics during the measurement.

4.5.6 Overall Structure

Figure 4-51 depicts the overall architecture of the proposed VCO-based RF modulator. The IQ baseband signal is generated by an off-chip IQ signal generator. The

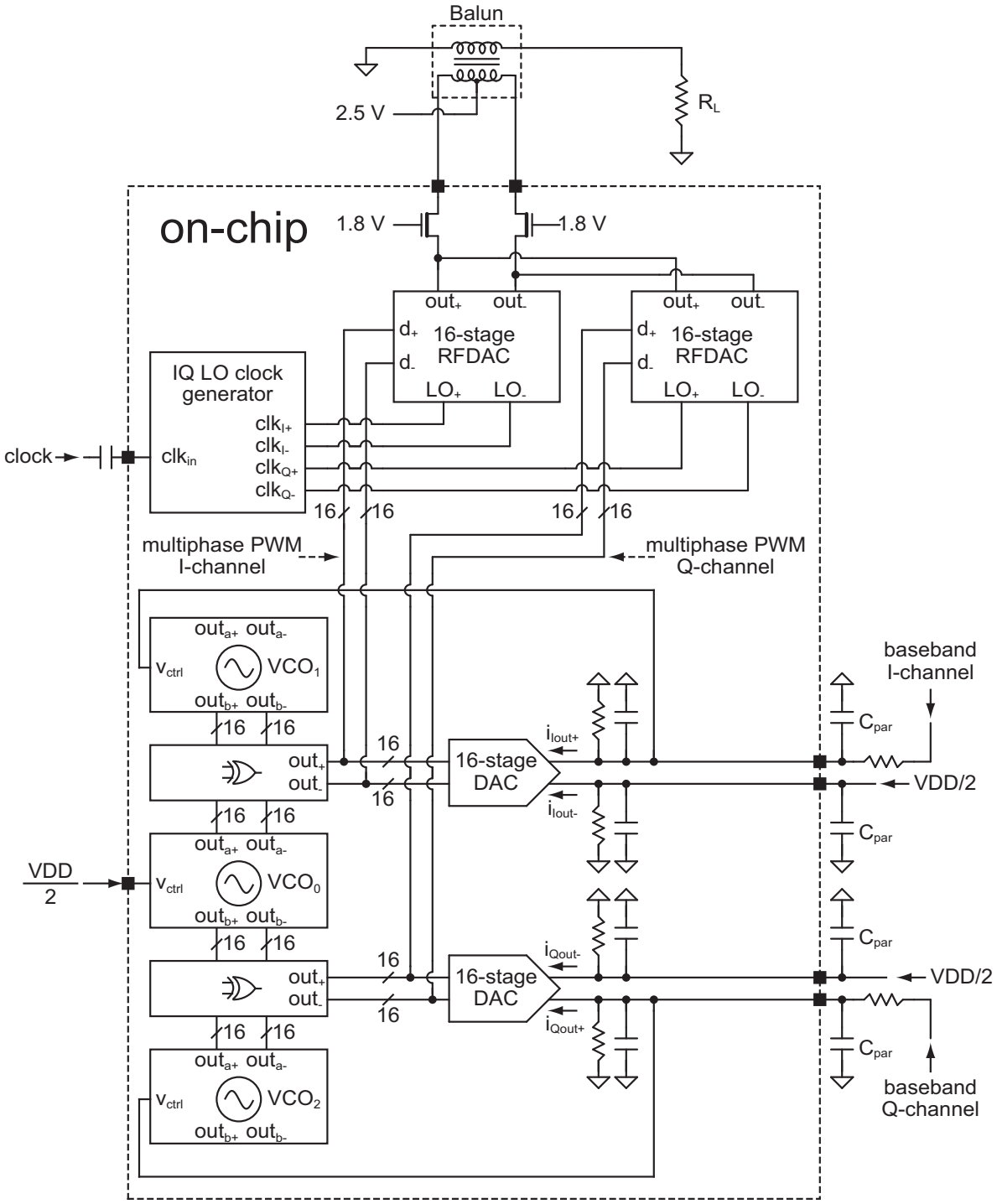

Figure 4-51: Overall architecture of the proposed VCO-based RF modulator.

off-chip resistors are utilized to set an appropriate filter characteristic of the on-chip multiphase PWM generator. A 5 GHz clock signal is applied to the IQ LO clock generator through an off-chip DC block capacitor. The current outputs from the RF-

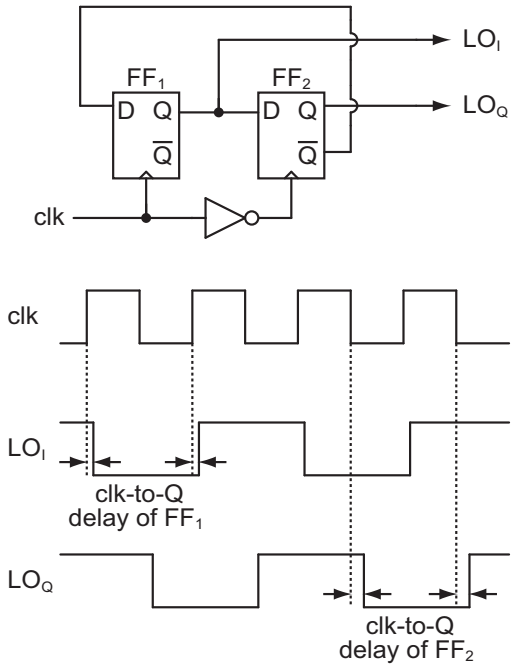

Figure 4-52: IQ mismatch due to clock-to-Q delay of flipflops.

DACs are connected to an off-chip balun for differential-to-single-ended conversion. Note that the bias generators for the DACs used in the VCO-based OP amps and the RFDACs are also included on the prototype IC, but are not shown in Figure 4-51 for simplicity.

4.6 IQ Mismatch Compensation

As presented in Section 4.5.4, the quadrature LO clock signals are created by pseudo-differential flipflops. IQ LO generation based on digital circuits achieves very high quadrature accuracy at a relatively low frequency [50]. However, there can be a phase imbalance when the input duty cycle is not exactly 50 % [51]. The delay of the flipflops may also cause IQ mismatch [52]. Figure 4-52 illustrates how the clock-to-Q delay of flipflops produces IQ inaccuracy in LO clock signals. Note that the IQ LO clock generator is implemented with pseudo-differential logic circuits, although all the signals are shown to be single-ended, for simplicity, in Figure 4-52. The inverter delay should be ignored because inverting a signal is implemented without a delay

by simple swapping of the pseudo-differential signal lines. As shown in Figure 4-52, the phase difference between LO_I and LO_Q is not exactly 90 ° when the mismatch of clock-to-Q delays exists. The delay mismatch is primarily dependent on device mismatch, which is unavoidable especially in deep sub-micron CMOS processes. The input duty cycle is also difficult to precisely control if a large device mismatch exists because the rise and fall time mismatch for clock buffers affects the duty cycle of the input clock. Therefore, IQ mismatch compensation is essential to compensating for the various phase mismatch sources.

The gain mismatch between the IQ baseband signal paths is another reason for the quadrature inaccuracy of an up-converted RF signal. The input baseband signal is converted to multiphase PWM signals by the VCO-based OP amp in the proposed RF modulator. According to (4.4), the transfer function from the input baseband signal to the output multiphase PWM signal is

$$i_{replica} = \frac{2GK_V N i_{unit}(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \cdot \frac{v_{in}}{R_{in}} \quad \text{where } G = \frac{i_{unit2}}{i_{unit}}$$

Many parameters determine the gain of the baseband signal path. Moreover, the gain is frequency dependent. However, the multiphase PWM generator will be designed such that the gain over the bandwidth of our interest is flat. Thus, it is safe to assume that the in-band gain is the same as the DC gain. The gain of the multiphase PWM generator at DC is

$$\begin{aligned} \left.\frac{i_{replica}}{v_{in}}\right|_{\text{at DC}} &= \left.\frac{2GK_V N i_{unit}(R \parallel R_{in})}{s^2(R \parallel R_{in})C + s + 2K_V N i_{unit}(R \parallel R_{in})} \cdot \frac{1}{R_{in}}\right|_{s=0,\text{ at DC}} \\ &= \frac{G}{R_{in}} = \frac{i_{unit2}}{i_{unit} \cdot R_{in}} \end{aligned} \tag{4.14}$$

Therefore, the DC gain of the baseband signal path is determined by i_{unit2}, i_{unit}, and R_{in}, which are the RFDAC's unit current, the VCO-based OP amp DAC's unit current, and the off-chip input resistor, respectively. The mismatch among those parameters for in-phase and quadrature baseband signal paths should be compensated, as should the phase mismatch of the IQ LO clock signals.

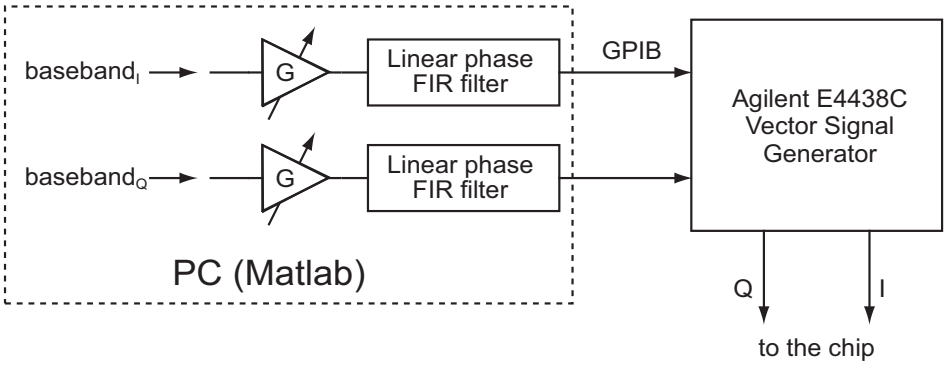

Figure 4-53: IQ mismatch compensation using FIR filters.

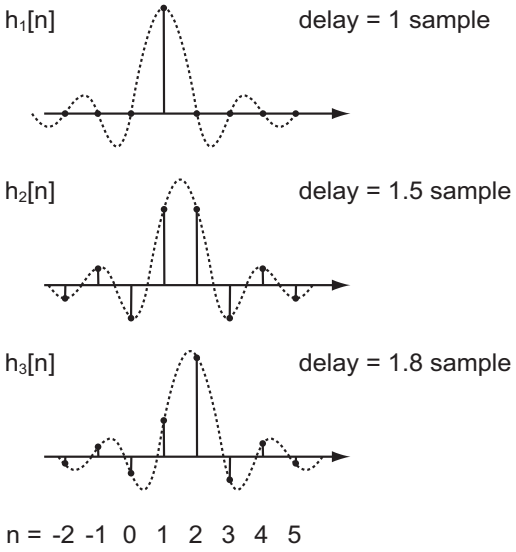

Figure 4-54: Examples of FIR filter coefficients for non-integer delay.

The gain and phase imbalance between IQ channel signal paths produces a *self-image* problem and can lower the SNR [53]. This is a serious problem especially for an OFDM signal because there exist many sub-channels in an OFDM signal and because the SNR of each sub-frequency bin is directly affected by the self-image signal. As a result, IQ mismatch compensation is essential for an OFDM baseband signal.

Many IQ mismatch detection and calibration techniques have been introduced [53], but they are beyond the scope of this thesis. In this work, we simply apply a pre-distortion digital filter to the baseband signal and manually adjust the filter coefficient until we get the proper results.

Figure 4-53 depicts how the IQ mismatch compensation is accomplished. All com-

pensation is done with Matlab, and the pre-distorted baseband signals are loaded into a vector signal generator via a GPIB cable. The gain compensation is implemented by simply adjusting the gain of the IQ signal. The phase compensation is achieved through linear phase *Finite-duration Impulse Response* (FIR) filters. The phase mismatch of IQ LO clock signals require linear phase compensation; this means that a constant group delay or a simple time delay is required for phase compensation.

One constraint of the digital compensation of phase mismatch is that a simple delay based digital filter cannot create an arbitrary phase or time delay because the minimum delay of a simple digital filter is one clock delay. For the testing of the prototype chip, we used an input OFDM signal at a rate of 40 MHz; hence, the minimum delay that can be generated by a simple digital filter is 25 ns. However, *non-integer* delay, such as 4.83 clock delay, can be created via a non-causal infinite-length digital filter [54]. Instead of using the infinite-length filter, we can choose only finite number of filter coefficients, thereby achieving a delay that is approximately close to the desired delay. Figure 4-54 illustrates how to choose FIR filter coefficients in order to get non-integer delay [54]. The impulse response of the filter is a sampled sinc function as shown in Figure 4-54. For practical implementation, we choose finite number of coefficients only. The accuracy of a delay achieved through the FIR filter improves if we use a greater number of coefficients. In this work, we use 3039-tap FIR filters for phase compensation.

4.7 Measured Results

The proposed VCO-based RF modulator is implemented in 45 nm CMOS process. Figure 4-55 shows the die photograph. The RF modulator occupies 0.126 mm^2. Figure 4-56 illustrates the test setup used for measuring the prototype chip. The IQ baseband signals are generated via an arbitrary function generator. The LO clock is generated via an AC coupled signal generator. The signal generator provides twice the LO frequency to the chip. The on-chip divide-by-2 frequency divider creates the quadrature LO clock signals. The output signal from the chip is amplified by two

15 dB amplifiers before the signal is measured by a spectrum analyzer.

4.7.1 Measured Spectrum with Sinusoidal Wave Inputs

Figure 4-57 shows the measured IQ performance with a 1.5 MHz sine wave. The figure depicts the spectrum over a 10 MHz frequency span, and the LO frequency is 2.45 GHz. The large LO leakage shown in Figure 4-57 is caused by the RFDACs. The power of the up-converted 1.5 MHz sine wave is about − 22 dBm, and the harmonic tones do not show in this case.

Figure 4-58 depicts harmonic tones when the power of the up-converted sine wave grows to − 10 dBm. Figure 4-59 shows the harmonic tones over a 50 MHz frequency span. As is predicted in Section 4.4.1, many harmonic tones are shown when the input signal increases because the non-linearity of the VCOs is not suppressed enough with the large amplitude of the input signal.

Note that phase adjustment of the input sinusoidal waves achieves IQ suppression only at the fundamental frequency. Harmonic tones in Figure 4-58 and Figure 4-59 are double-sided because IQ suppression is attained for only 1.5 MHz.

Figure 4-60 shows the measured IQ performance with an 8 MHz sine wave. The figure shows the spectrum over a 70 MHz frequency span. When the power of the up-converted 8 MHz sine wave is about − 22 dBm, the non-linearity of the VCOs does not appear. Figure 4-61 shows harmonic tones when the power of the up-converted sine wave grows up to − 10 dBm. Figure 4-62 shows the harmonic tones over a 200 MHz frequency span. Again, many harmonic tones are shown when the input signal increases. Note that a comparison of Figure 4-61 with Figure 4-58 reveals that harmonics tones with an 8 MHz input are larger than those with a 1.5 MHz input when the amplitudes of the two sine wave signals are the same. This difference confirms that the non-linearity worsens as an input frequency increases, as predicted in Figure 4-26.

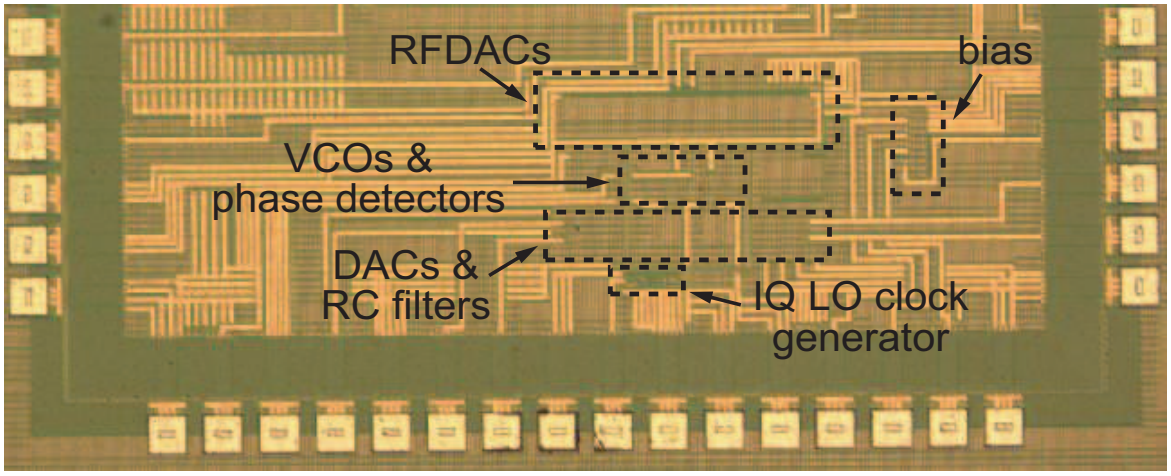

Figure 4-55: Die photograph of the implemented VCO-based RF modulator.

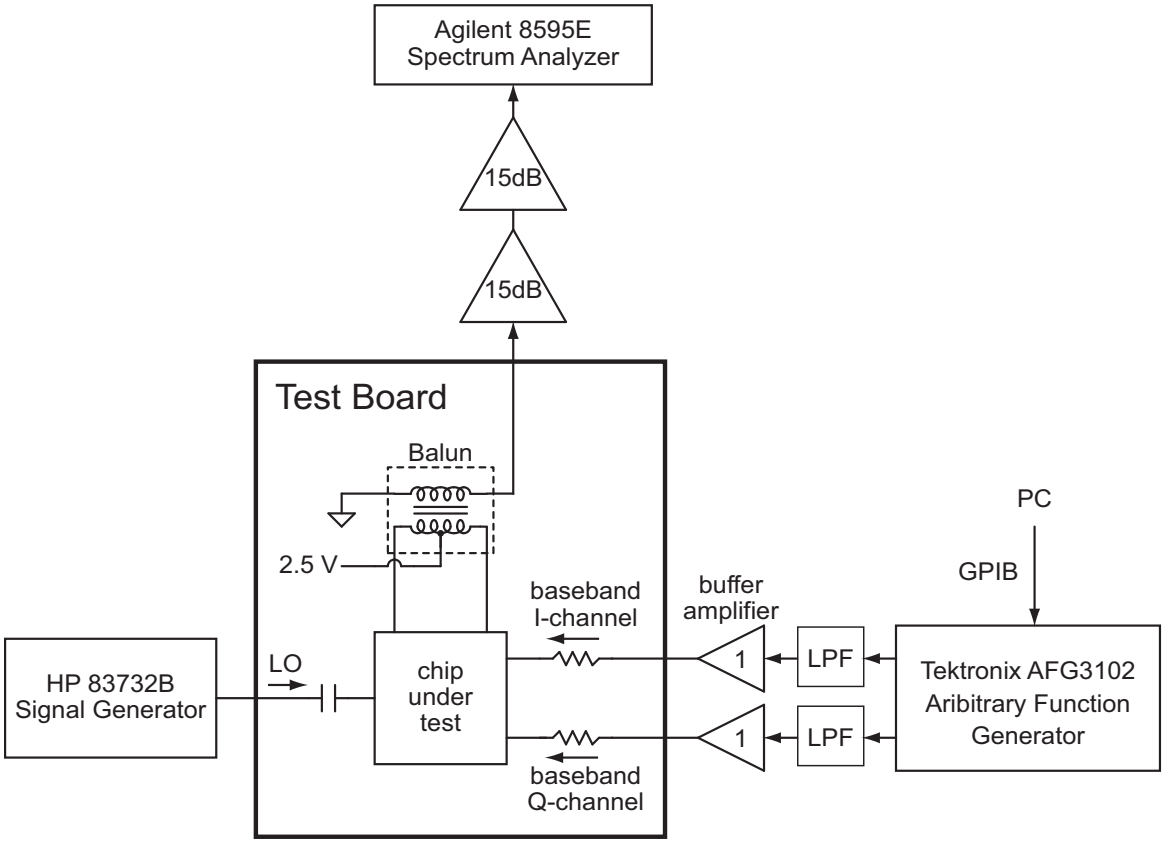

Figure 4-56: Test setup for the prototype chip.

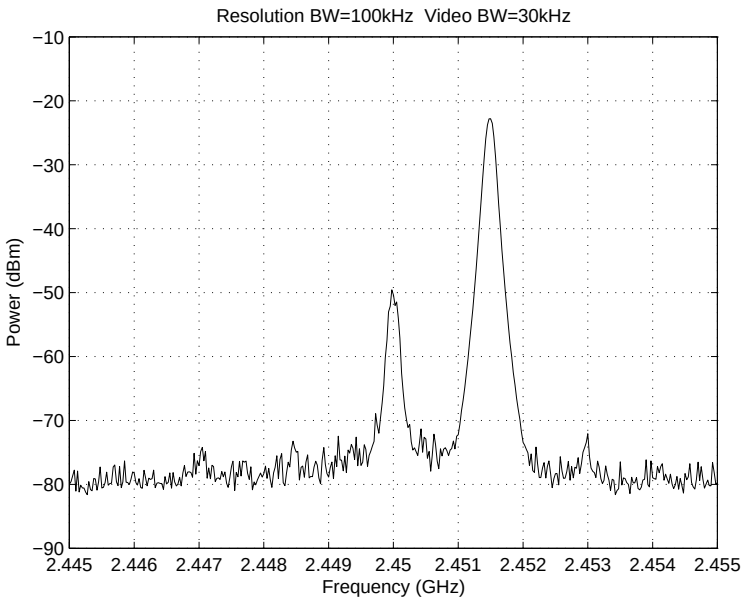

Figure 4-57: IQ performance with 1.5 MHz sine wave (1).

4.7.2 Measured Spectral Performance of the RF Modulator

The measured spectral performance of the RF modulator is shown in Figure 4-63. The input signal is a 20 MHz OFDM. The spectrum is compared with an 802.11g spectral mask as a reference. Figure 4-64 shows the spectrum with a 400 MHz frequency span.

As is mentioned in Section 4.4.5, different R_{in} values result in different filtering characteristics for both the baseband input signal and the VCO phase noise. Figure 4-65 to Figure 4-67 are the measured results, with $R_{in} = 50\,\Omega$, $R_{in} = 550\,\Omega$, and $R_{in} = 1.1\,k\Omega$, respectively. Comparing these figures with Figure 4-37 to Figure 4-39, one can find out that the measured results agree well with the CppSim simulation results in terms of the filtering characteristics. As is predicted in Section 4.4.5, the measurement results indicate that $550\,\Omega$ is the optimum R_{in} value.

4.7.3 Measured Error Vector Magnitude

Figure 4-68 illustrates the test setup for *Error Vector Magnitude* (EVM) measurement. A 10 MHz OFDM signal for an 802.11a wireless LAN is generated in a PC, and linear phase FIR filters are applied to the signal for IQ mismatch compensation,

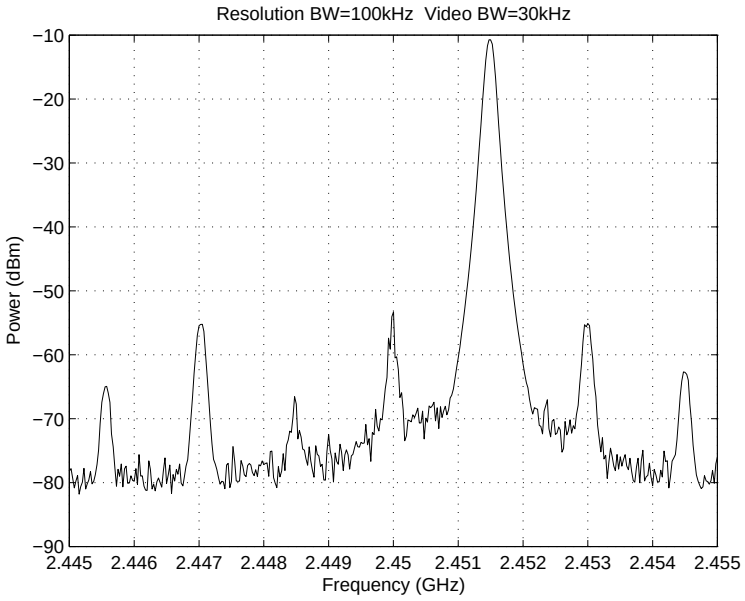

Figure 4-58: IQ performance with 1.5 MHz sine wave (2).

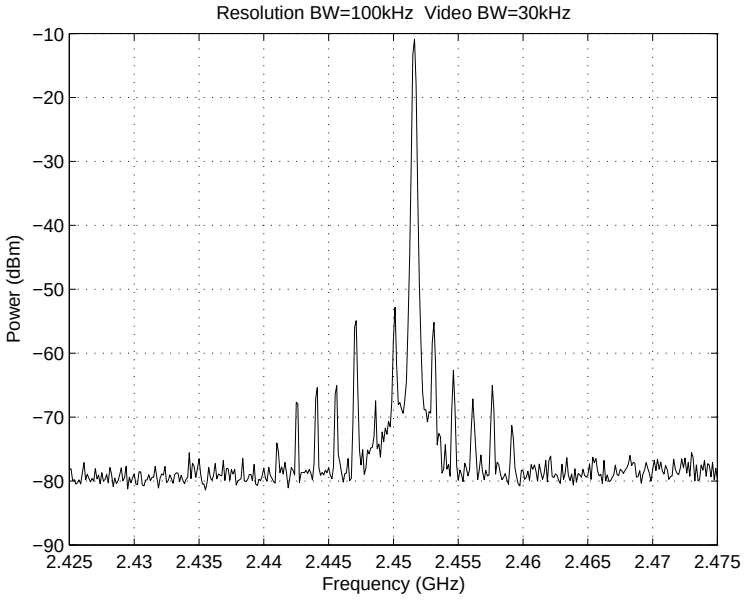

Figure 4-59: IQ performance with 1.5 MHz sine wave (3).

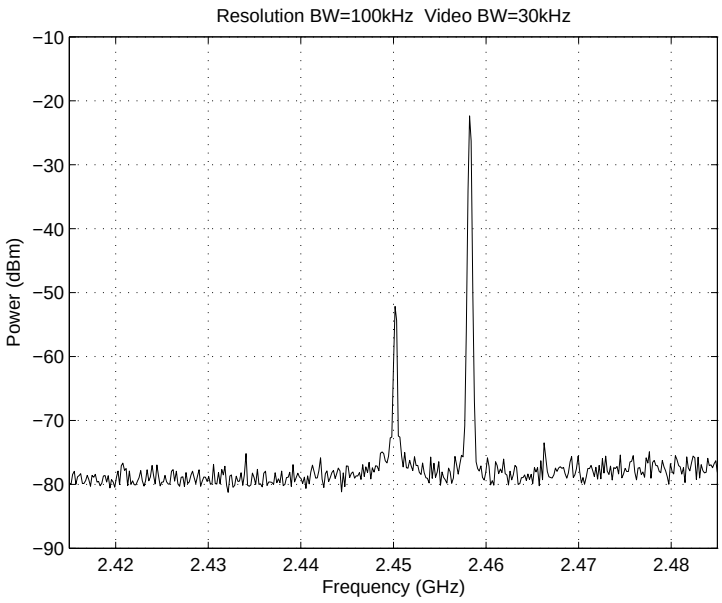

Figure 4-60: IQ performance with 8 MHz sine wave (1).

as is described in Section 4.6. The pre-distorted baseband signals are loaded into an Agilent E4483C vector signal generator, which creates baseband IQ signals. A separated RF signal is generated from the vector signal generator, and this signal is applied to the chip for LO signal generation. The carrier frequency is 2.45 GHz.

Figure 4-69 shows the measured EVM of the prototype chip with IQ compensation. The measured EVM is about 3 %rms, as is shown in the fourth quadrant of Figure 4-69. We believe the SNR of the RF modulator is limited by the VCO phase noise since the phase noise is the dominant in-band noise source. Thus, the VCO phase noise should be lowered to improve the EVM. The diagram in the first quadrant of Figure 4-69 shows the EVM at each frequency bin and reveals that the EVMs around the carrier frequency are higher than other EVMs. We believe that the up-converted flicker noise of the VCOs degrades the SNR of the frequency bins around the carrier frequency.

As a comparison, Figure 4-70 depicts the measured EVM results without IQ compensation. The measured EVM without compensation is 17.2 %rms.

Table 4.1 summarizes the measured power consumption of each building block of the RF modulator.

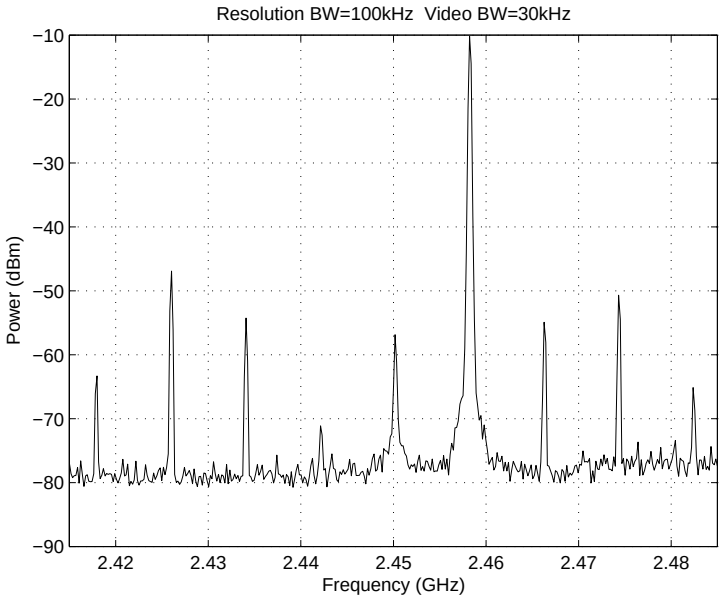

Figure 4-61: IQ performance with 8 MHz sine wave (2).

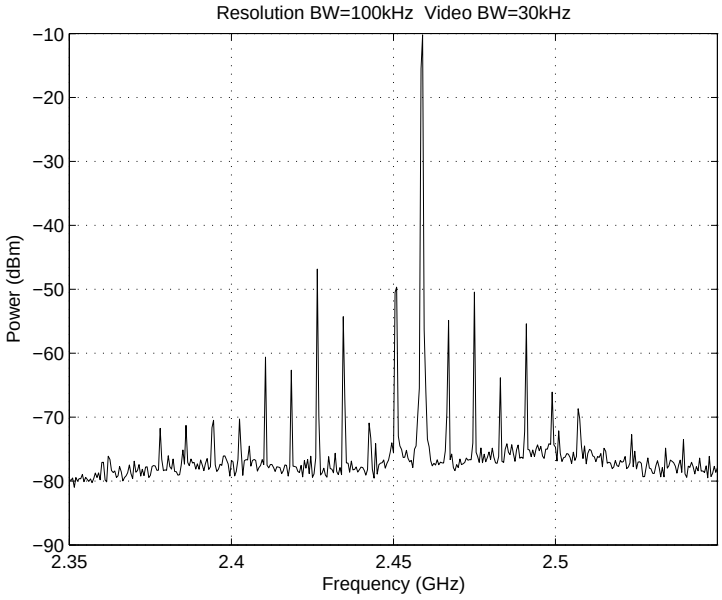

Figure 4-62: IQ performance with 8 MHz sine wave (3).

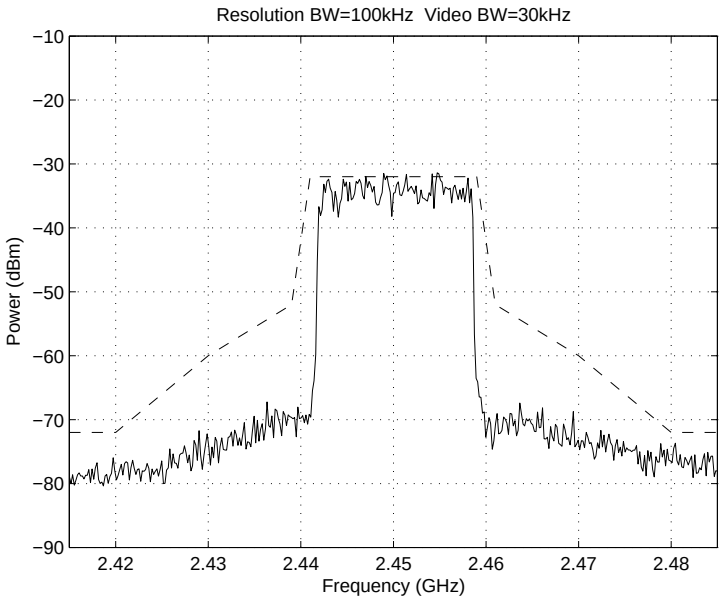

Figure 4-63: A 20 MHz OFDM signal with a spectral mask.

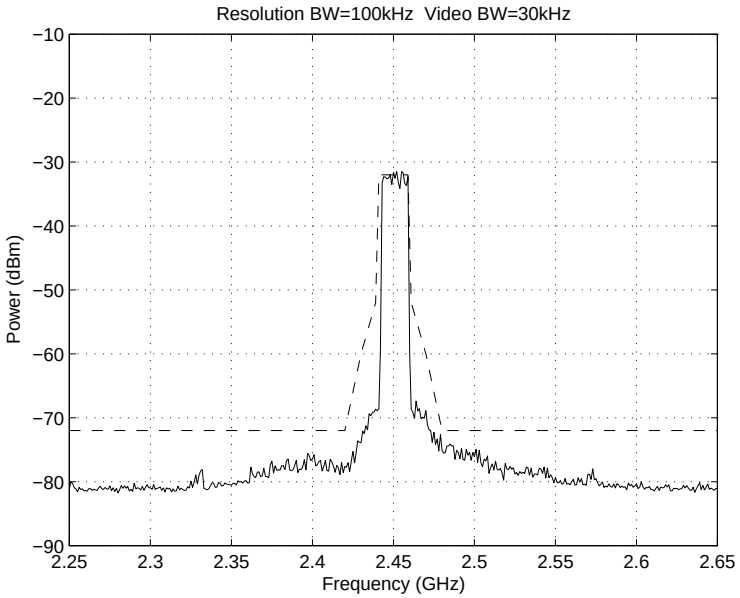

Figure 4-64: Spectrum of a 20 MHz OFDM signal with a 400 MHz frequency span.

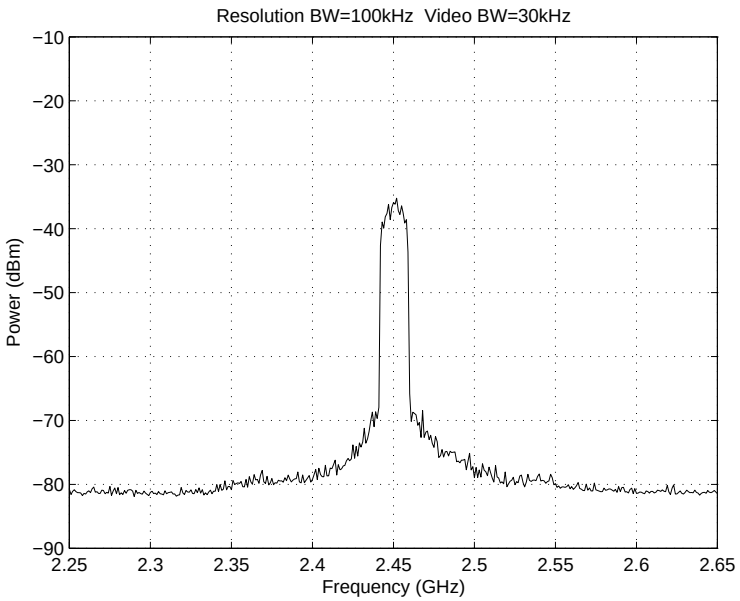

Figure 4-65: The measured spectrum with $R_{in} = 50\,\Omega$.

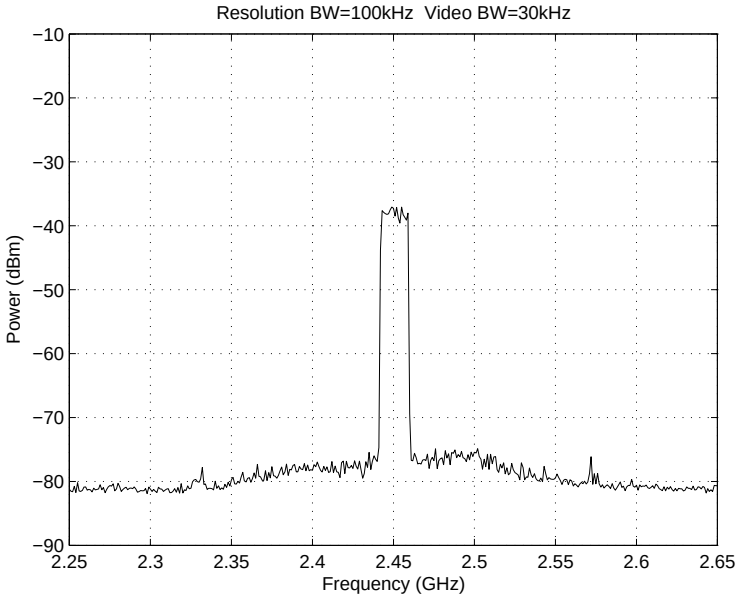

Figure 4-66: The measured spectrum with $R_{in} = 550\,\Omega$.

4.8 Conclusions

The VCO-based RF modulator implemented in 45 nm CMOS technology is presented in this chapter. The proposed RF modulator is driven by multiphase PWM signals such that up-conversion of a baseband signal is achieved by a simple switching of

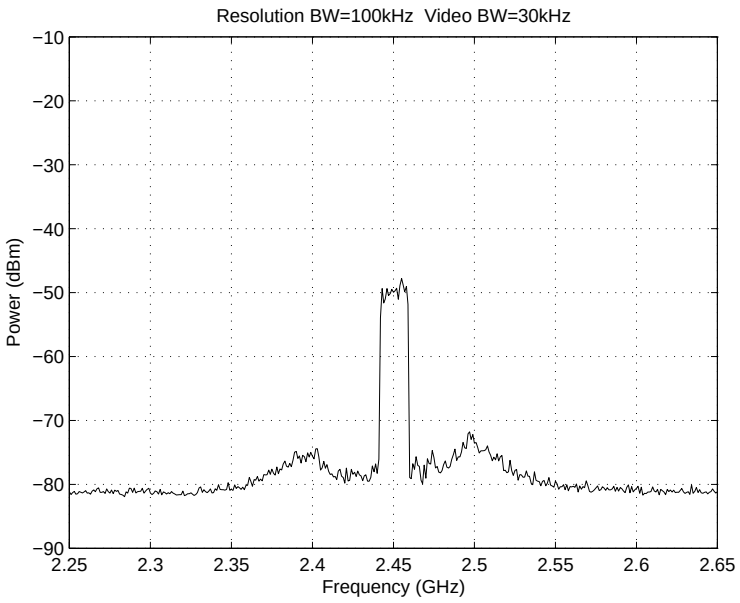

Figure 4-67: The measured spectrum with $R_{in} = 1.1\,k\Omega$.

Table 4.1: Measured power consumption of the proposed VCO-based RF modulator

Building Block	Supply Voltage	Measured Power
LO clock buffer	1.2 V	19.9 mW
RFDAC	2.5 V	5.5 mW
Bias current source	1.1 V	2.3 mW
3 VCOs	1.1 V	11.8 mW
Digital cirucits	1.1 V	14.8 mW
Total		54.3 mW

devices, thereby allowing integration of the modulator onto a single chip in deep sub-micron CMOS. The multiphase PWM signals are generated by the proposed VCO-based OP amp, which is composed of multiphase ring VCOs, phase detectors, simple DACs, and an RC filter.

The measured results of the prototype chip show that the in-band noise is dominated by the phase noise of the VCOs in the VCO-based OP amps. Because of the VCO phase noise, the proposed RF modulator may be inadequate for some wireless communication applications, such as cellular phones, which require high SNR. However, the proposed RF modulator could provide an attractive architecture for

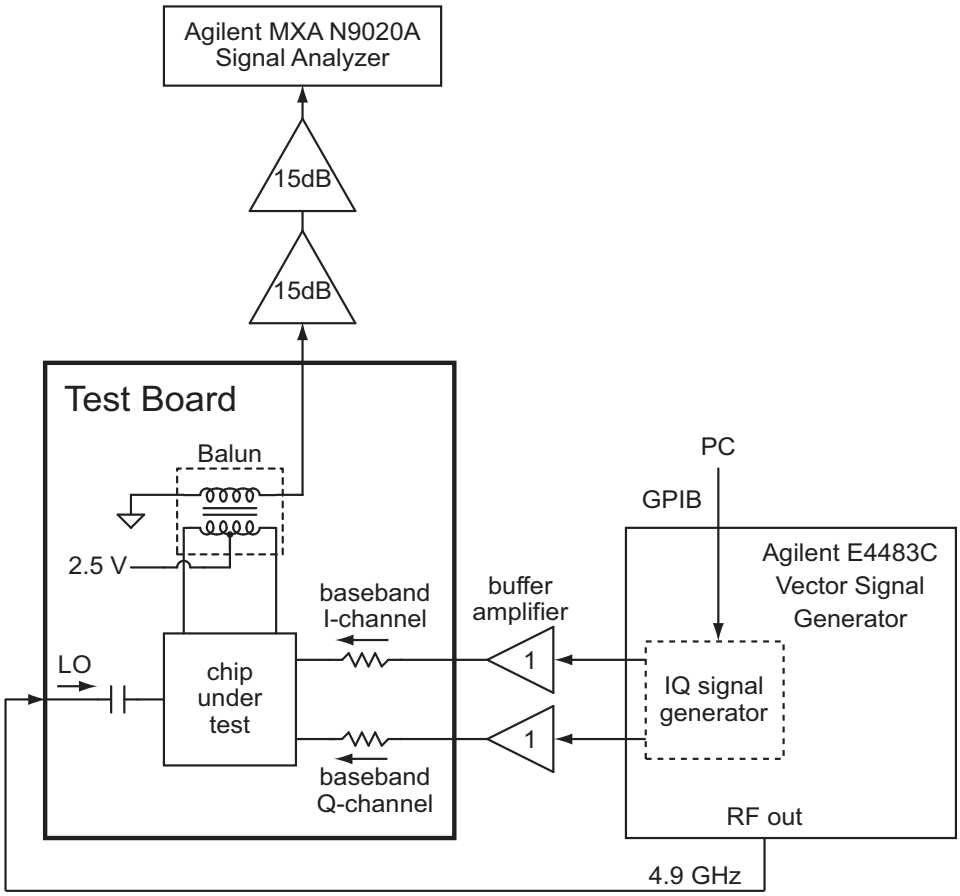

Figure 4-68: Test setup for the EVM measurement.

wideband wireless communications that require relatively low SNR, such as a wireless LAN. The measured spectrums show that extra filtering is unnecessary for the RF modulator with a 20 MHz OFDM input signal, and this is one advantage of the proposed RF modulator over the systems that employ RFDACs driven by $\Sigma\Delta$ modulation. However, the measurement results also indicate that the RF modulator becomes more non-linear as the input frequency increases; this implies that bandwidths wider than 20 MHz are inappropriate. Note that both drawbacks of the proposed RF modulator — phase noise and non-linearity — originate from the VCO-based OP amps. Therefore, we can verify two fundamental limitations of a ring oscillator as a time-based circuit in the application of RF signal generation.

Nonetheless, the function of the proposed VCO-based RF modulator mainly relies on time-based circuits such as ring VCOs and phase detectors, and should provide

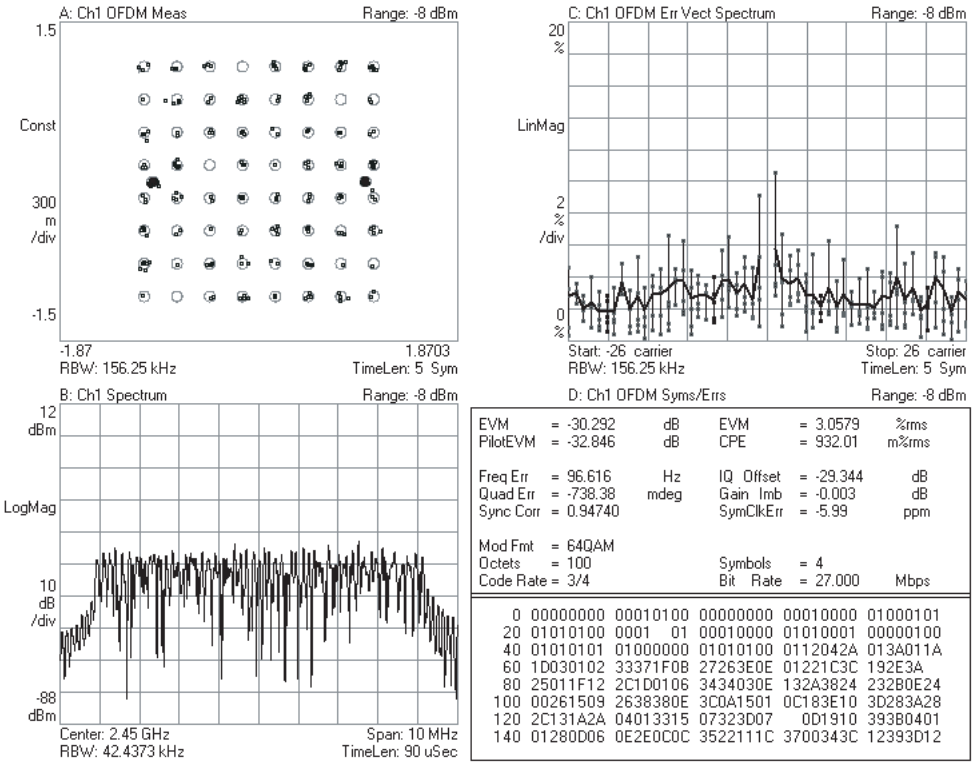

Figure 4-69: The measured EVM with IQ compensation.

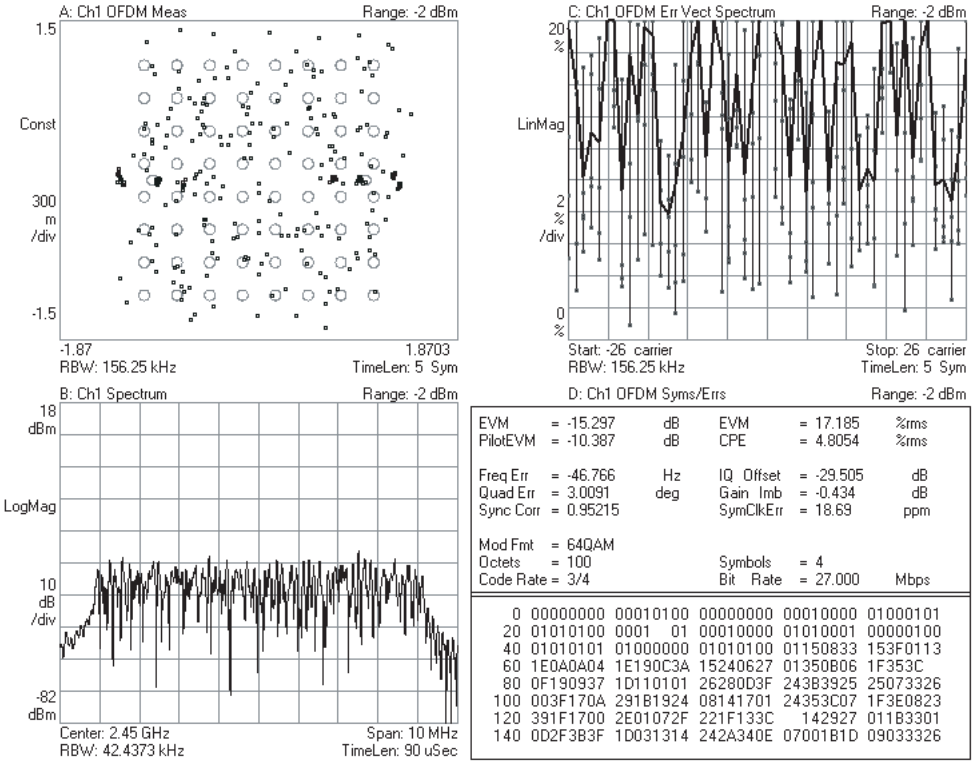

Figure 4-70: The measured EVM without IQ compensation.

an attractive implementation in future CMOS technology. Moreover, high quality reconstruction filters are not necessary in this architecture because there is no out-of-band quantization noise to be filtered. Thus, the proposed architecture may be the solution for the on-chip integration of an RF modulator.

Chapter 5

Conclusions

5.1 Summary

In this thesis, time-based circuits for communication systems in modern CMOS technology are introduced. Time-based signal processing relies on the time information of a signal rather than on voltage or current information. By dealing with an analog signal with time-based circuits instead of conventional analog circuits, we can avoid various issues relating to analog circuits in future CMOS technology. In this thesis, we have focused on a ring oscillator as an example of a time-based circuit and demonstrated that A/D converters and an RF modulator based on ring oscillators can reduce the need for traditional analog circuit content and still achieve moderate performance. In order to demonstrate the feasibility of the systems based on time-based circuits in future CMOS technology, we have fabricated the prototype chips in 0.13 μm and 45 nm CMOS processes.

For the VCO-based $\Sigma\Delta$ A/D converter, a ring VCO is employed as a continuous-time integrator replacing the first stage integrator of a second-order $\Sigma\Delta$ modulator. By taking advantage of the infinite DC gain of a VCO integrator, we can use a very simple low DC gain charge pump for the second stage integrator. The proposed VCO-based A/D converter was fabricated in a 45 nm CMOS process to prove our concept. We have successfully presented an A/D converter in deep sub-micron CMOS employing time-based circuits — a ring VCO and a phase detector, in this case. We

have also shown that the non-linear tuning characteristics and phase noise of the ring VCO are the fundamental limitations of using a ring oscillator as an analog-to-time converter.

The single-slope A/D converter using a TDC, on the other hand, has shown that a hybrid approach combining a few analog circuits and time-based circuits can serve as a path to improve linearity compared to the VCO-based $\Sigma\Delta$ A/D converter. The proposed single-slope A/D converter has achieved a highly digital A/D conversion by performing voltage-to-time and time-to-digital conversion. Time-to-digital conversion is achieved via a ring-oscillator-based TDC. Linear voltage-to-time conversion is achieved by employing a sampler and a current source, thereby solving the non-linearity issue of a ring-oscillator-based analog-to-time conversion. Although the proposed single-slope A/D converter utilizes some analog circuits, the majority of the A/D converter is composed of digital circuits and time-based circuits that are ring-oscillator-based TDCs. The measured performance of the A/D converter is mainly limited by the power and speed of digital circuits and ring oscillators; hence, we expect that the proposed single-slope A/D converter will improve as device size scales down.

The VCO-based RF modulator has demonstrated that time-based circuits are also useful in generating an RF signal in deep sub-micron CMOS processes. The proposed RF modulator up-converts a baseband signal by a simple switching of transistors. While an RF modulator using RFDACs also relies on device switching for signal generation, the RF modulator often suffers from high quantization noise since it deals with digitized signals. However, multiphase PWM signals are utilized for the proposed VCO-based RF modulator so that the baseband analog signal is represented by continuously adjustable multiphase PWM signals. Therefore, the proposed RF modulator has solved the resolution issue of an RFDAC, and the RF modulator still requires only switching devices which will be easily implemented even in future CMOS technology. A VCO-based OP amp is also introduced and analyzed as an alternative method to design an OP amp in deep sub-micron CMOS. The proposed VCO-based OP amp is employed to generate multiphase PWM signals, which drive

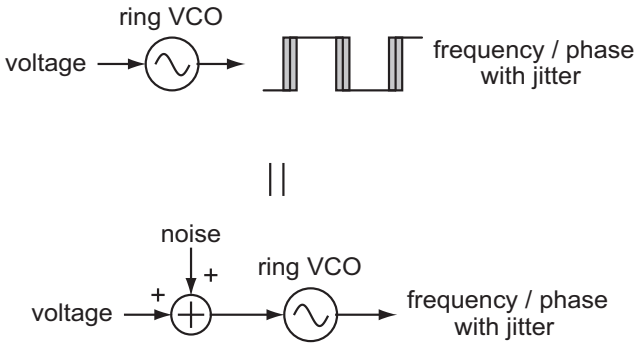

Figure 5-1: An input referred noise due to the timing jitter of a ring VCO as an analog-to-time converter

the RF modulator. The VCO-based RF modulator is fabricated in 45 nm CMOS, and the prototype IC has demonstrated up-conversion of a 20 MHz OFDM signal to a 2.5 GHz carrier frequency. Although the measured results of the proposed VCO-based RF modulator show the same issues as the VCO-based A/D converter — the phase noise and the non-linearity of VCOs affecting the SNR and the linearity of the system, the RF modulator achieves the moderate SNR and linearity, which are possibly adequate for wireless LAN applications.

5.2 Fundamental Limitations of a Ring Oscillator for Time-Based Signal Processing

In this work, we have focused on using a ring oscillator for communication systems. Two main functions of a ring oscillator we have relied on are analog-to-time conversion and time-to-digital conversion. A ring oscillator is a useful functional block for time-based signal processing, especially in future CMOS technology, in that it requires only delay elements which will be available regardless of device channel length and power supply voltage. However, there are fundamental limitations to a ring oscillator.

The first issue of a ring oscillator is its timing jitter or phase noise. The device's thermal and flicker noise create an unwanted timing jitter that generates noise in time-based signal processing. For analog-to-time conversion, the timing jitter acts as a noise source, as is shown in Figure 5-1. Accordingly, the timing jitter or the phase

noise of a ring oscillator limits the resolution of analog-to-time conversion. Even for time-to-digital conversion, the timing jitter could be a noise source. However, since the instantaneous timing jitter of one delay stage tends to be of an order of magnitude smaller than that of the delay of a delay stage with proper design, the dominant noise source of a TDC based on a ring oscillator will be the quantization noise of a TDC rather than the jitter. Nevertheless, the flicker noise of a TDC based on a ring oscillator dominates at low frequency because the slowly varying accumulated jitter due to a device flicker noise could be larger than the quantization noise [15], and the flicker noise effect will increase as the device size shrinks.

The timing jitter or the phase noise of a ring oscillator is somewhat analogous to the voltage or current noise of conventional analog circuits. For example, a transconductance amplifier has an output current noise that is also modeled as an input referred voltage noise. The solutions to noise reduction for a ring oscillator are also similar to those of conventional analog circuits. The timing jitter due to thermal noise is theoretically lowered by burning more power [55, 56], but the jitter improvement of a ring oscillator is limited to a certain level in practice. Large device size reduces the timing jitter caused by flicker noise [56]. However, flicker noise is especially difficult to contend with, considering that the device size is getting smaller for future CMOS processes. We can always deal with flicker noise by making the device size larger, but that would eliminate the benefits of Moore's Law, such as higher time resolution and lower power. It is worth mentioning that the symmetric rising and falling transitions of a single-ended ring oscillator help to lower the flicker noise effect [55]. However, symmetric transitions would be difficult to achieve because of device mismatch which is expected to get worse as channel length shrinks. Considering the decreasing size of transistors in modern CMOS technology, we can easily expect that the phase noise of a ring oscillator will be dominated by the flicker noise and gets worse as scaling continues. Therefore, the phase noise or the timing jitter would be one of the fundamental limitations of a ring oscillator for time-based signal processing in future CMOS technology. We have shown that the resolutions of both the VCO-based A/D converter and the VCO-based RF modulator are limited by the VCO phase noise in

Chapter 2 and 4.

The non-linear tuning characteristic of a ring VCO is another serious issue of a ring oscillator as an analog-to-time converter. Because of the non-linear relationship between the tuning voltage and the frequency of a ring VCO, voltage-to-phase or voltage-to-frequency conversion becomes non-linear. The tuning characteristics can be made more linear by careful design [57]. However, linearization of the tuning characteristic requires an accurate model of the transistors, which will be difficult to derive for the deep sub-micron CMOS devices. Therefore, the non-linearity of a ring VCO will be another fundamental limitation of a ring oscillator. We saw the performance degradation due to the non-linear tuning characteristics of a ring VCO in Chapters 2 and 4.

5.3 Conclusions

The three applications of time-based circuits presented have utilized ring oscillators as core building blocks for either analog-to-time conversion or time-to-digital conversion. This thesis has shown the fundamental limitations of ring oscillators in dealing with analog signals, while it has also demonstrated the feasibility of the usage of ring oscillators. A ring oscillator has its own advantage such as the infinite DC gain achievable even in the future deep sub-micron CMOS processes. In addition, a ring oscillator can be used as an efficient time-to-digital converter.

However, the demonstrated systems have shown the issues of the phase noise and the non-linearity of ring VCOs. The SNR and the linearity of both the VCO-based A/D converter and the VCO-based RF modulator were limited by the ring VCOs although the measured results have shown moderate performance. The phase noise of a VCO will worsen as transistor size shrinks, especially because of the flicker noise. The phase noise of a ring oscillator can improve either by burning more power or by using larger devices, as mentioned before. However, both of these solutions are undesirable because we can no longer get benefits from Moore's Law. The non-linear tuning characteristics are also not expected to improve by device scaling. Therefore,

a ring oscillator is the dominant performance limitation factor of the proposed system architectures.

We may be able to generalize the fundamental limitations of a ring oscillator to other time-based signal processing. A time-based signal always suffers from a timing jitter no matter what circuits deal with the signal. Because of the decreasing size of transistors, the jitter of a time-based signal is expected to be dominated by the flicker noise, and even a TDC is affected by the flicker noise [15]. We can also expect that there will always be the non-linear analog-to-time conversion issue unless analog circuits assist the conversion process for linearization.

As a result, there is a tradeoff between the conventional analog circuits and the time-based circuits. Time-based signal processing is better than conventional analog signal processing in deep sub-micron CMOS technology in terms of area, power, and the ease of implementation. Especially, a ring VCO achieves an infinite DC gain which conventional analog circuits cannot perform. However, in terms of the noise and the linearity, conventional analog circuits using thick-oxide transistors would be better than time-based circuits.

The above observations indicate that using a *combination* of time-based circuits and analog circuits will likely yield the best solution when seeking high performance with an efficient implementation. For moderate performance, employing more time-based circuits would be the better choice as we have presented in Chapter 2 and 4. A hybrid approach combining analog circuits and time-based circuits could solve some of the limitations of time-based signal processing. For example, the single-slope A/D converter in Chapter 3 has suggested that employment of a few analog circuits can avoid the non-linear analog-to-time conversion issue of a ring oscillator. For high performance, it would be better to utilize more conventional analog circuits. Both the high resolution and the high linearity have been achieved for the A/D converters in [9, 10] by keeping many conventional analog circuits but using ring VCOs only as quantizers.

This thesis has demonstrated that analog signals can efficiently be processed by leveraging time-based circuits in advanced CMOS technology. By specifying the fun-

damental limitations of a ring oscillator for time-based signal processing, we have shown that there is a tradeoff between time-based circuits and conventional analog circuits when seeking future circuit solutions. Specifically, time-based circuits utilizing ring oscillators provide an implementation path that can directly benefit from Moore's Law, but have disadvantages in terms of noise and linearity. Traditional analog circuits provide advantages in terms of noise and linearity, but suffer from degraded characteristics such as reduced intrinsic gain and headroom. Through proper combination of both time-based and analog circuits, we expect that high performance can be achieved with an efficient circuit implementation in future CMOS processes.

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