Overview of the ECAL Off-Detector Electronics of the CMS Experiment

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***Abstract*—Located between the on-detector front-end electronics and the global data acquisition system (DAQ), the off-detector electronics of the CMS electromagnetic calorimeter (ECAL) is involved in both detector readout and trigger system. Working at 40 MHz, the trigger part must, within ten clock cycles, receive and deserialize the data of the front-end electronics, encode the trigger primitives using a nonlinear scale, assure time alignment between channels using a histogramming technique and send the trigger primitives to the regional trigger. In addition, it must classify trigger towers in three classes of interest and send this classification to the readout part. The readout part must select the zero suppression level to be applied depending on the regions of interest determined from the trigger tower classification, deserialize front-end data coming from high-speed (800 Mb/s) serial links, check their integrity, apply zero suppression, build the event and send it to the DAQ, monitor the buffer occupancy and send back pressure to the trigger system when required, provide data spying and monitoring facilities for the local DAQ. The system, and especially the data link speed, the latency constraints and the bit-error rate requirements have been validated on prototypes. Part of the system is about to go to production.**

***Index Terms*—Calorimetry, data acquisition, triggering.**

I. Introduction

THE Compact Muon Solenoid (CMS) experiment, at the large hadron collider (LHC) in construction at CERN, will be equipped with a high resolution electromagnetic calorimeter (ECAL) made of 75848 crystals. The readout and trigger electronics of ECAL is divided into two parts: the on-detector electronics located inside the CMS detector and the off-detector electronics located outside the detector in the underground service cavern. The on-detector electronics is read through about 9000 high-speed (800 Mb/s) serial links by the off-detector electronics. These links and the corresponding opto-electronics must be resistant to the stringent radiation conditions of the detector area.

The information from the electromagnetic calorimeter is used by the level-one trigger (LV1) together with the hadronic calorimeter and the muon subdetector information. For the LV1 decision, the ECAL is read with a coarse granularity: 25 times coarser than the nominal one for the barrel and about 9 times coarser for the endcap. For this purpose, the ECAL is divided into $56 \times 72(\eta, \varphi)$-regions, 34×72 in the barrel and 11×72 in each endcap, called trigger towers. Here and in the following, φ denotes the azimuth (angle in the plan transverse to the beam) and η the pseudorapidity, $\eta = -\ln(\tan(\theta/2))$, where θ denotes the polar angle (angle with respect to the beam axis). In the barrel, a trigger tower corresponds to a 5×5 matrix of crystals. In the endcap, the number of crystals per trigger tower differs from tower to tower. The information used for the LV1 decision is called trigger primitives. A trigger primitive consists of the evaluated transverse energy deposited in a trigger tower and of a single bit qualifying the energy deposit expansion along η.

The CMS data acquisition (DAQ) system is designed to process events of 1-MB average size at a maximum average LV1 rate of 100 kHz, requiring an event builder bandwidth of 100 GB/s [1]. Ten percent of the 1–MB event size is allocated to the ECAL. The size of the whole ECAL data for a single event, $\sim$1.8 MB, exceeds the nominal full event size and a volume reduction of a factor $\sim$20 is required on the ECAL data to fit within the allocated size. This reduction is performed by the combination of zero suppression and of an algorithm, called "selective readout," selecting the regions of interest of the calorimeter. The selective readout algorithm, described in [2], selects the areas of the ECAL which must be read with a minimal zero suppression. Here and in the following, "minimal zero suppression" must be understood as no zero suppression at all or a zero suppression with a very low threshold (typically 0). The rest of the ECAL is read with a high zero suppression threshold or read only with the coarse granularity of the trigger primitives. In order to select the regions of interest, the trigger towers are classified in three classes of interest depending on the deposited transverse energy. The energy deposited in each trigger tower is compared to two thresholds; trigger towers

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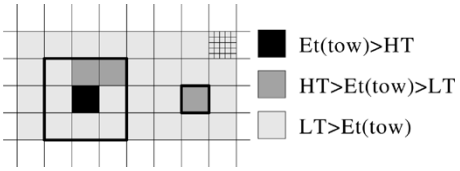

Fig. 1. Selective readout algorithm. See the text for the description of the algorithm. The figure illustrates the case of one trigger tower with a high transverse energy deposit (above the higher threshold HT, in black): the crystals of 3×3 trigger tower matrix around this trigger tower are read with a minimal zero suppression threshold. The crystals of the trigger tower with a medium transverse energy deposit (between the higher and lower thresholds, HT and LT, in dark gray) are also read with a minimal zero suppression threshold.

with an energy above the higher threshold are classified as high interest trigger towers, those with an energy between the two thresholds as medium interest ones and those with an energy below the lower threshold as low interest trigger towers. If a trigger tower belongs to the high-interest class then the crystals of this trigger tower and of its neighbor trigger towers (225 crystals in the barrel case) are read with a minimal zero suppression. If a trigger tower belongs to the medium interest class, then the crystals of this trigger tower (25 crystals in the barrel case) are read. If a trigger tower belongs to the low-interest class and it is not the neighbor of a high-interest trigger tower, then it is not read with the fine granularity or optionally it is read but with a severe zero suppression. This algorithm is illustrated in Fig. 1. In any case the full calorimeter is read with the coarse granularity of a trigger tower and this information (in principle, the trigger primitives themselves) is sent to the CMS DAQ and is always available offline, for instance for missing transverse energy calculation. For debugging purpose, the selective readout can be deactivated and either a global zero suppression (same threshold for every channel) or no-zero suppression is applied. If no zero suppression is applied the system will run with a lower rate because of the bandwidth constraints. Even when the selective readout is not applied on the data, the result of the algorithm (the selective readout flags) is inserted into the data stream and can be used offline for debugging purpose.

The general ECAL readout architecture is represented in Fig. 2. One very front-end card (VFE) reads five crystals and five of these cards are plugged into one front-end card (FE). The clock is distributed to the front-end through token rings controlled by the "Clock and Control System" cards (CCS). The FE cards compute trigger primitives and send them at 40 MHz to the trigger concentrator cards (TCC) through dedicated serial links. The TCCs finalize the trigger primitive calculation (for the endcap only), compress the trigger primitives using a nonlinear scale and, after synchronization and serialization done by the synchronization and link mezzanine board (SLB), send them to the level 1 trigger system.

The trigger is distributed to the front-end electronics, to the TCCs and to the data concentrator cards (DCC) by the CCS cards. On a level one accept, the FE cards send the data to the DCCs where they are delayed in input pipelines. During the latency introduced by these pipelines, the selective readout processor (SRP) receives trigger tower classification flags from the TCCs, determines the calorimeter regions of interest according to the selective readout algorithm previously described, produces the selective readout flags indicating the zero suppression level to apply for each readout unit (readout partition of 25 crystals) and sends them to the DCCs. The DCCs perform the actual zero suppression and send the resulting reduced data to the global DAQ. In addition the DCCs provide access to the data via the VME bus. This access is used by the local DAQ and the laser-based ECAL calibration system.

The architecture of the off-detector electronics which has been described highlights five main parts: the CCS cards, the TCC cards, the SLBs, the SRP, and the DCC boards.

II. Clock and Control System

The CCS cards have the following three main responsibilities:

- slow controls of the front-end electronics: configuration and status report;
- distribution of fast timing signals: e.g., clock, trigger;
- fan-in of the trigger throttle signals.

The slow control commands come from the VME bus. The front-end is accessed through mezzanine cards called mezzanine FE controllers (mFECs) [3]) and plugged on the CCS card (see Fig. 3). An interface between the VME and the local bus is implemented in a field programmable gate array (FPGA) chip, the Xilinx Spartan IIE. This VME interface FPGA, which is the master of the local bus, handles also the interrupts coming from the mFEC and translates them into VME interrupts.

The mFEC accesses to the front-end electronics through a control ring: each FE board has a communication and control unit (CCU) implemented in an application specific integrated circuit (ASIC). The CCUs together with the mFEC are connected in a ring as illustrated in Fig. 4. The protocol used to control the FE boards is similar to the IBM token ring protocol. The links between the CCUs, which are "on the detector" are electrical. The links to the CCS, which is "off-detector," are optical.

The fast timing signals arrive from the experiment trigger system by the timing and trigger control (TTC) [4] link. These signals are decoded by the LHC-standard TTCrx ASIC [5]. The TTCrx decodes the following two channels of the TCC signal:

- channel A providing the LV1 accept;
- channel B providing the fast control commands.

The following commands are used by the ECAL front-end electronics:

- "Bunch Crossing zero" (BC0), marks the beginning of an LHC orbit;
- "resync," resets all pointers, all the data are lost and the internal event ID is set to 0;
- "power-up reset;"
- "monitoring mode enabling," switches the crystal readout analog-to-digital converters to a secondary mode.

These commands are sent to the front-end electronics together with the clock: they are encoded by missing clock edges. The command translation and encoding is implemented in an FPGA chip of the Xilinx Spartan IIE family, denoted "Trigger FPGA" on the CCS block diagram represented in Fig. 5. Therefore, a single signal with the clock and the fast control commands goes from the Trigger controller to the mFECs (8 on a CCS board).

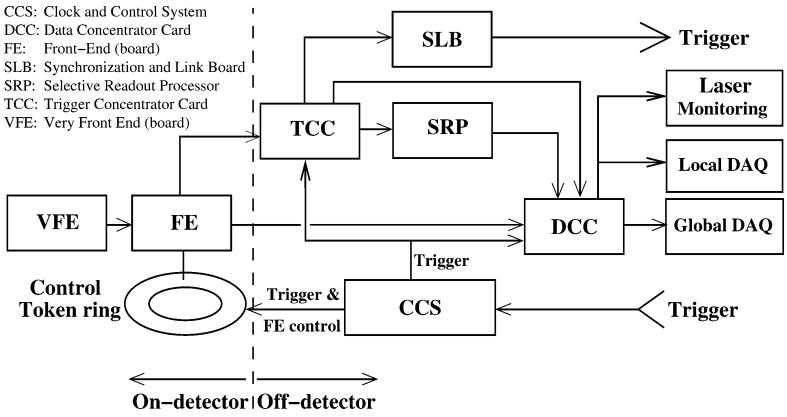

Fig. 2. ECAL readout and trigger architecture.

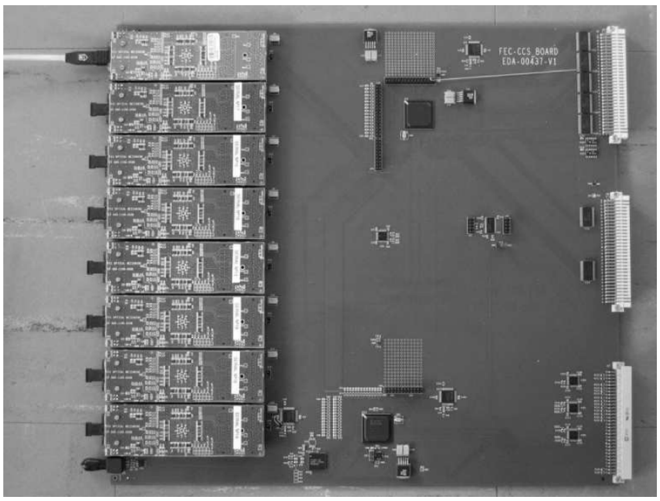

Fig. 3. CCS card prototype. The 8 mFEC mezzanine cards can be distinguished on the left part of the board.

This fast timing signal is then distributed to the FE boards of the control ring as illustrated in Fig. 4. On each FE board an ASIC, called tracker phase–locked loop (TPLL) chip extracts the commands and the clock from the fast timing signal, recovered with the help of a PLL. The TPLL contains also a phase shifter in order to synchronize the clocks arriving in each FE boards. A PLL with a crystal, called QPLL [6], is used to reduce the clock jitter.

One CCS card has 8 mFECs, each mFEC controlling one control ring of up to 10 FE boards. 54 CCSs are required in total for the control of the ECAL front-end electronics.

The trigger controller has another functionality: it merges the "Timing Throttle System" (TTS) signals from the TCC and DCC cards of the ECAL off-detector system, and sends the resulting TTS signal to the TTS link. The TTS signal is a feedback from the readout electronics (or its emulation) to control the trigger rate. Each DCC, TCC, and SRP card monitors its data buffers. It can send three types of TTS messages: a warning message will lower the trigger rate; an "almost full" signal will inhibit the trigger and empty events will be sent in order to keep the synchronization; a "full" signal will result in a resynchronization of the DAQ (the readout buffers will be reset). DCC, TCC, and SRP cards can also send "out-of-sync" signal to the TTS. Such a signal will also result in a resynchronization of the DAQ. The resynchronization procedure is described in [7].

Finally the CCS cards fan out the signal from the TTC link to the DCC and TCC cards. TTC and TTS signals transmitted between the ECAL off-detector cards travel on the TTS/TCC bus located on a back plane in the VME crate. Fast control commands can be inserted into the TTC signals sent to the TCC and DCC via the Trigger FPGA. A CCS card is already used to control the front-end in test beam.

III. Trigger Concentrator Cards

The TCC cards are responsible for sending the trigger primitives to the trigger system. A trigger primitive consists of the following:

- the measurement of the transverse energy deposited in a trigger tower coupled with the bunch crossing assignment;
- a bit, called "fine grain veto bit," qualifying the expansion along η of the energy deposit in the trigger tower.

To evaluate the energy deposited in a trigger tower it is required to sum the signals from each crystal (corresponding to a readout channel) of the trigger tower. In order to minimize the number of links between the detector and the TCC cards, this sum is done (only partially for the endcaps) in the on-detector electronics, more precisely on the FE boards.

First of all, sums of five crystals are computed: time samples are added one-to-one. In the barrel the sums are done on strips of five crystals along φ as represented in Fig. 6. Then, each strip signal passes through a finite impulse response (FIR) filter with 5 (optionally 6) taps and a peak-finder is used to extract the maximum value. This maximum value is proportional to the energy deposited in the strip. It is summed on the five strips of a trigger tower to obtain the transverse energy part of the trigger primitive.

The fine grain veto bit is calculated in the following way. All the possible sums of two consecutive strips of a trigger tower are computed and the one with the maximum value is considered. The ratio of this maximum to the sum of the energy of the five strips is compared to a threshold, typically 0.90. The fine grain veto bit is active if the threshold is passed. It is used to tag energy deposits not compatible with electrons and photons.

For the barrel, all of the above operations are done in the FE boards. Each FE board serializes the computed trigger primitive

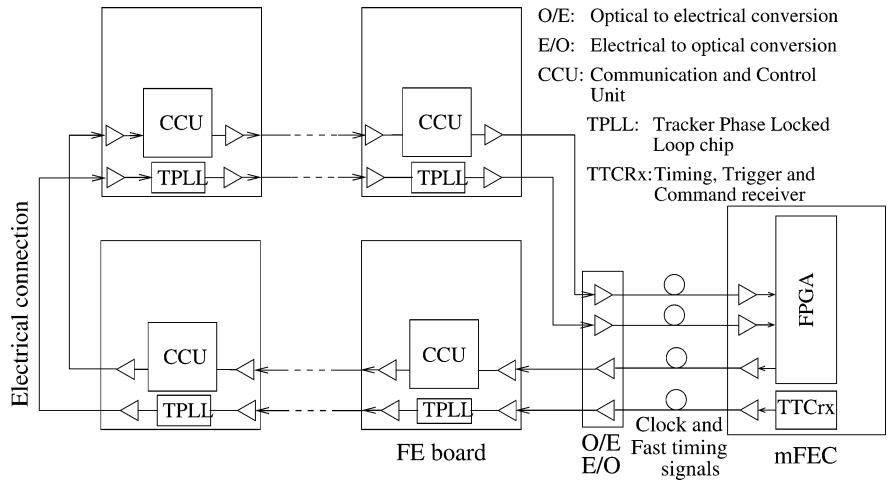

Fig. 4. Front-end electronics slow control and fast timing signal distribution.

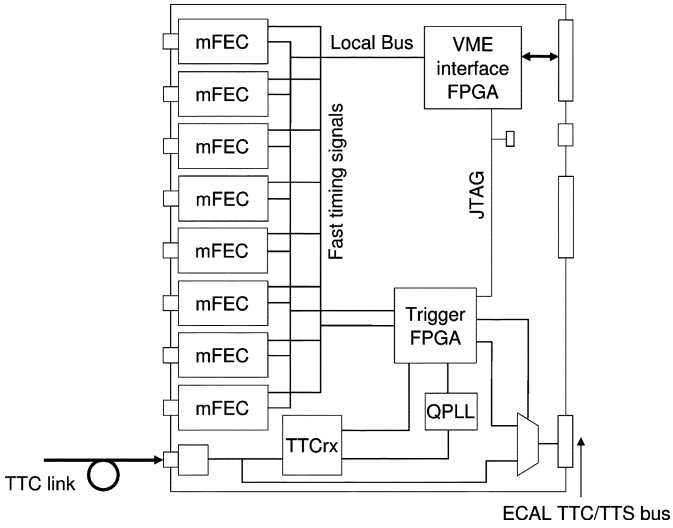

Fig. 5. Simplified CCS block diagram.

and sends it to a TCC via one optical link. The TCC must first deserialize the data coming from the FE boards. The energy sums are then compressed into an 8-bit word using a nonlinear scale. The result of this compression together with the fine grain veto bit go to the SLB. All of these operations must be done within a 7 clock cycle latency. The encoded trigger primitives are stored during the LV1 latency; in case of an LV1 accept, they will be sent to the DCC in order to be stored together with the data.

The complete trigger primitive calculation (except the compression part) can be precisely done in the FE boards for the barrel because a trigger tower, which contains all the information required for a trigger primitive, is read by a single FE board. This condition is not fulfilled for the endcap. Indeed, in the endcap, the crystals are organized in an (x, y)-grid. As for the barrel, an FE board reads an (x, y)-matrix of 5×5 crystals. On the other hand the trigger towers must be organized according to an (η, φ)- partitioning: a trigger tower should cover a region $\Delta\eta \times \Delta\varphi \simeq 0.138 \times 0.0873$. The crystals are grouped to form trigger towers approaching this $\Delta\eta \times \Delta\varphi$ region. This mapping is done in such a way that the crystals of a readout unit are assigned to trigger towers by multiples of 5. Thanks to this "multiple of 5" constraint, the five-crystal partial sums can still be calculated on the FE boards. The sets of five crystals used to make the partial sums do not form strips running along φ like in the barrel but have more complex shapes, which differ from tower to tower. These five-crystal sets are called pseudo-strips. The FIR filter and the peak finder of the FE board operate on the partial sums. The final sums are computed in the TCC cards. In this way a compromise is done between the number of optical links and the trigger efficiency, which requires an η, φ trigger tower partitioning.

Two types of TCC are required: one for the barrel and one for the endcap. The barrel TCCs have 72 inputs (68 are used), the endcap ones have 48 inputs. The endcaps have five FE board-TCC optical links (one for each partial sum) per FE board instead of one for the barrel. 36 TCCs are required to cover the barrel and 72 TCCs for the endcaps. The TCCs are also in charge of organizing the trigger towers in the classes of interest described in the introduction. These trigger tower flags, coded on two bits. The two bits plus one reserved bit are sent to the selective readout processor.

For testing the TCC, a VME64x card, the TCC tester card, is used to emulate the front-end interface. This card is a replica (with a modified firmware) of the DCC tester card that will be described in the DCC section. The TCC input patterns are generated with a simulation of the front-end written in SystemC [8] and loaded into the TCC tester card. The latency introduced by the TCC on the trigger primitive path and the bit-error rate (BER) of the data links were validated on a prototype implemented with one third of the nominal number of inputs. A picture of this TCC prototype is shown in Fig. 7. Direct measurements on a long-term run have shown that the BER at the output of the input deserializer is less than $3 \cdot 10^{-15}$. Measurements from eye diagram and jitter of the signal entering the input deserializer have shown that the BER is much lower than 10^{-15}. The measured jitter of this signal is low, 20 ps and is within the requirements (<80 ps). Finally the latency was measured between one input of the TCC and the output of its deserializer: the 3.13 clock cycles value was obtained. The latency introduced by the FPGA part is expected to be within two clock cycles and, therefore, the total latency should be below 6 clock cycles, the specified maximum value being 7 clock cycles.

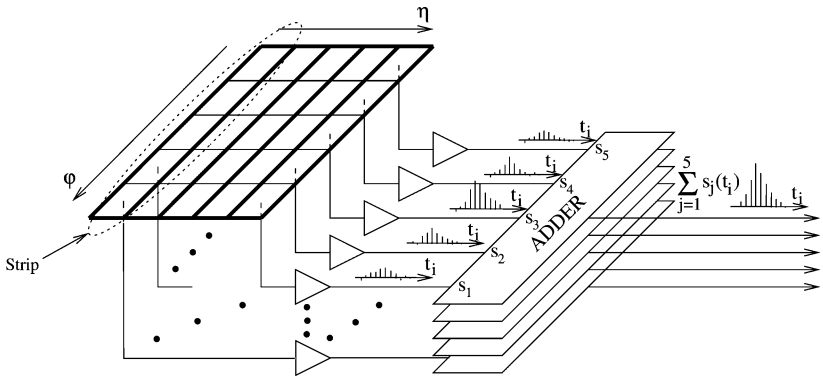

Fig. 6. Sums of the signals of five-crystal "strips," performed on the FE boards.

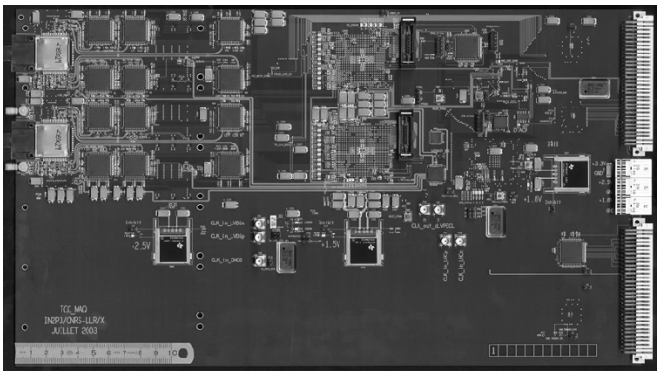

Fig. 7. TCC prototype with 24 inputs ("TCC24").

IV. Synchronisation and Link Mezzanine Boards

On a TCC card, nine SLB mezzanine cards are plugged. The SLB cards [9] are responsible for synchronizing the trigger primitives with respect to the bunch crossing time and sending them to the regional calorimeter trigger system. Histograms are used to rebuild the bunch structure of the LHC orbit. The bunch crossing time can be deduced from this structure and then used as a reference to synchronize data. A three clock unit budget is allocated for the SLB operation.

V. Selective Readout Processor

The SRP [2] must determine the calorimeter regions of interest to read with a minimal zero suppression threshold. The SRP time budget allocated to perform this operation is 6.4 μs. The SRP operates asynchronously at the 100 kHz LV1 accept rate. To perform the selective readout algorithm, the ECAL is partitioned in 12 regions. Each region is covered by one "Algorithm Board" (AB). The algorithm requires that each AB exchanges tower data with the 8 AB boards covering the adjacent regions: this makes 39 AB bidirectional interconnections. A commercial passive optical cross-connect is used for these interconnections. In addition to these AB-AB connections, there are 108 TCC to SRP and 54 SRP to DCC unidirectional connections. The AB board is built around the high integration FPGA Xilinx Virtex2Pro 2vp70. This FPGA contains 20 RocketIO multigigabit transceivers (MGT) operating at up to 3.125 Gbit/s transmission rate. Up to 12 of these MGTs are used for the unidirectional communications with the TCC and DCC boards

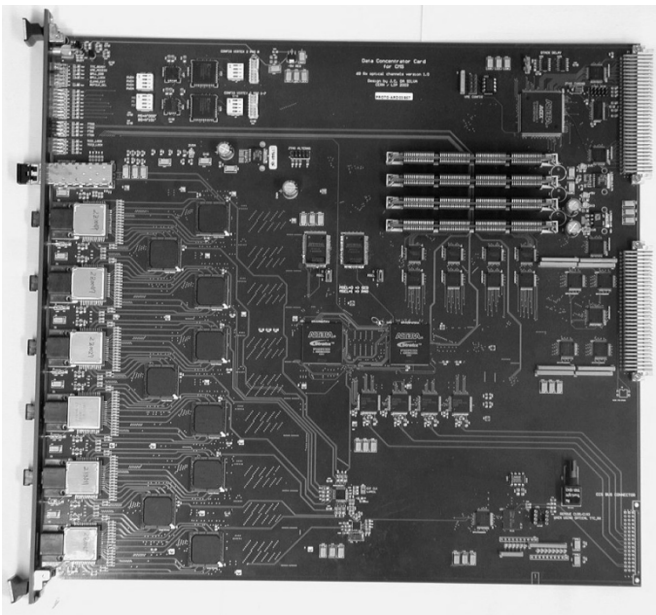

Fig. 8. DCC prototype.

and up to 8 are used for the communication with the adjacent ABs. The connection of the parallel optical links from TCCs and DCCs and the AB cross-connect is made with SNAP12 multisource agreement pluggable modules.

As for the TCC, the BER has been measured from long term run and from jitter and eye opening. The direct measurements on a long term run show that the BER is less than 10^{-15}, which is better than the requirements. The jitter and eye opening measurements show a BER much lower than 10^{-15}. The jitter budget and the optical power budget have also been validated from calculation.

The latency has been measured on a simplified AB model. The simplified AB exchanges trigger tower data to only two ABs and serves only one-sixth of the assigned barrel area. The measured value, 2 μs, is well below the 6.4 μs time budget. Because of the intrinsic parallelism of the AB firmware, the overall SRP latency is not expected to increase significantly.

VI. Data Concentrator Cards

The DCC [10], a VME64x 9U board (see Fig. 8), must deserialize the data coming from the 68 high-speed links (800

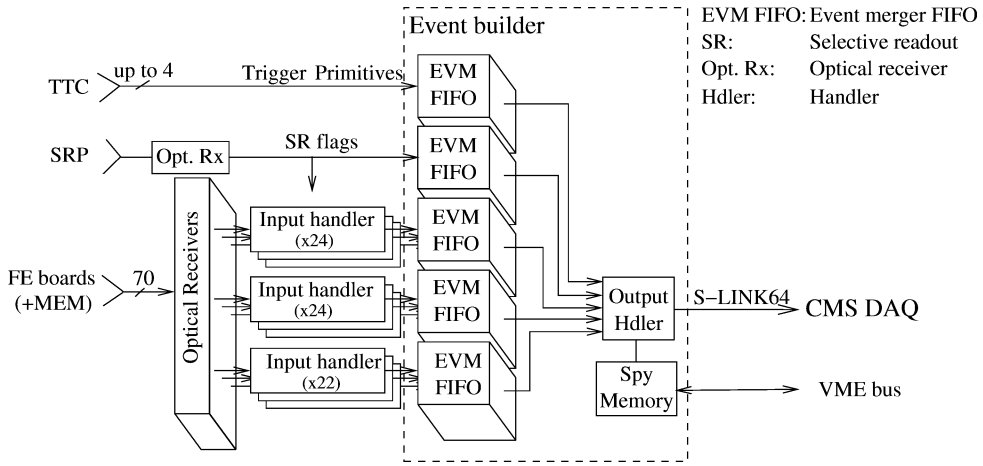

Fig. 9. Event building in the DCC.

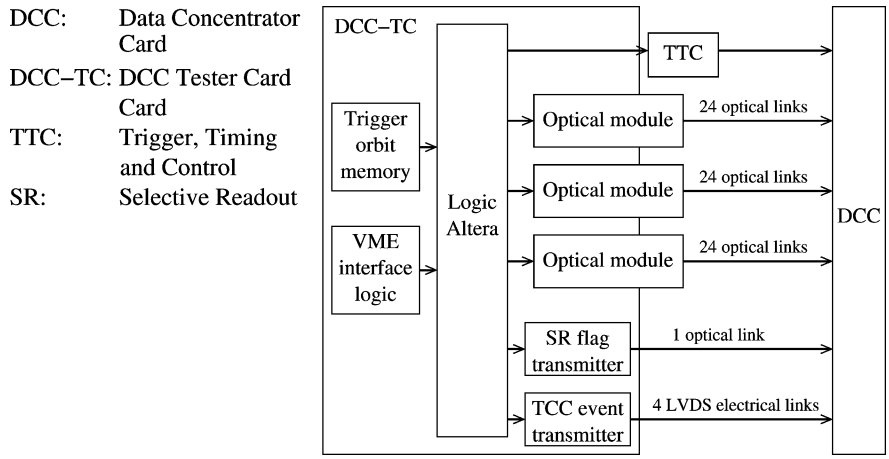

Fig. 10. DCC-TC design architecture.

Mb/s) of the FE boards (and two data links coming from the laser-based ECAL calibration system). After a data integrity check, it applies the zero suppression in order to reduce the data volume by a factor ∼20. The zero suppression threshold is chosen according to the area of the calorimeter that is read and the flags received from the SRP. The two possible threshold values are programmable per DCC basis. The DCC builds and formats the ECAL event fragments from the data received from the FE boards, the trigger primitives received from the TCC, and the selective readout flags received from the SRP. It serializes the event fragments and sends them to the global DAQ via an S-LINK 64 interface [11] at an average rate of 200 MB/s with a maximum link designed rate of 528 MB/s.

The event building is performed in two stages. Firstly five data blocks (channels 1 to 24, channels 25 to 48, channels 49 to 70, SRP block, and TTC block) are built in parallel. Then these blocks are merged by the output handler to form the final DCC event. This two-stage event building is represented in Fig. 9. The 70 input handlers represented on the figure perform the data integrity check and the zero suppression.

A dedicated VME64x-9U card was developed for the DCC test bench. This tester card emulates the interfaces with the FE boards, the TCC and the SRP. The architecture of this DCC Tester Card (DCC-TC) [10] is represented in Fig. 10. The optical modules emulate the FE board interfaces. The TCC and SRP interfaces are emulated by the TCC event and SRP flag transmitters. Raw data of physics events generated with the CMS detector response simulation software [12], [13] can be loaded into the DCC-TC. The final DCC prototype is already used in test beam.

VII. Crate Configuration

For the barrel, an ECAL DAQ unit is made of one DCC, one CCS and one TCC. There are 34 DAQ units for the barrel arranged in 12 9U VME64x crates. For the endcaps, a DAQ unit is made of one DCC, one CCS, and four TCCs. There are 18 endcap DAQ units arranged in six 9U VME64x crates. The nine AB cards of the SRP system are grouped in one 6U VME64x crate.

VIII. Conclusion

The designed off-detector electronics of the CMS electromagnetic calorimeter, presented in this paper, is able to provide to the trigger system the required information for level one accept decision in the short time budget and to reduce the event size by the required factor ∼20. The DCC and the CCS boards are already used for the ECAL test beams. Most of the other

components of the ECAL off-detector electronics were tested and validated, especially BER of the data links were carefully measured.

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