XXX. NETWORK SYNTHESIS

Prof. H. B. Lee
Prof. W. C. Schwab
J. Anderson
V. K. Prabu

RESEARCH OBJECTIVES

Our group aims to achieve an improved understanding of lumped, linear, finite, passive, bilateral networks. During the coming year we shall be concerned primarily with the following problems:

1. Determination of fundamental properties of transformerless networks.
2. Development of new methods for synthesizing lossless driving-point impedances.
3. Implications of time-domain power conservation.
4. Extension of known synthesis procedures to include new types of circuit elements.

Research is now under way on all four problems.

H. B. Lee

A. NON SERIES PARALLEL REALIZATION FOR LOSSLESS DRIVING-POINT IMPEDANCES

The purpose of this report is to call attention to a new method for realizing lossless driving-point impedances. The method enables one to realize impedances of the form

$$Z = \sum_{i=1}^{n} k_i \frac{s}{s^2 + \omega_i^2} \tag{1}$$

upon the network N shown in Fig. XXX-1. The final realization contains one more

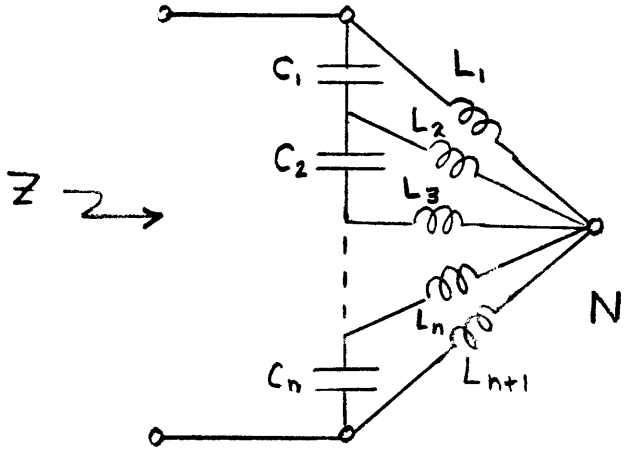

Fig. XXX-1.

than the minimum number of circuit elements; thus the realization procedure is not canonic. Because of the superfluous circuit element, the realization procedure involves one independently specifiable parameter.

The synthesis method can best be explained if one redraws the network N as shown in Fig. XXX-2. It is evident from this figure that N consists of a ladder network driven from an unconventional entry. In the synthesis procedure, one assumes that the network of Fig. XXX-2 realizes the impedance Z. One then determines the corresponding impedance z_{11} shown in Fig. XXX-2. Once z_{11} is known, one realizes Z by developing z_{11} into a ladder. The details of the determination of z_{11} are as follows.

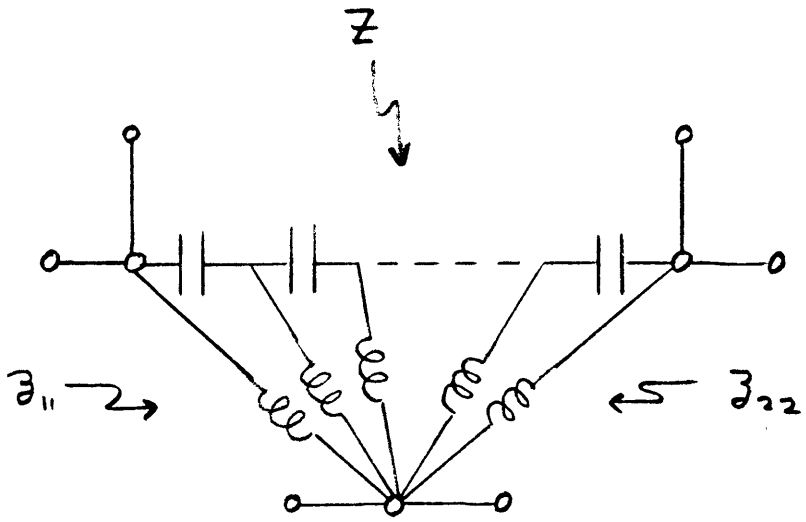

Fig. XXX-2.

If the network of Fig. XXX-2 is to realize the impedance (1), then the impedance z_{11} must have the form

$$z_{11} = As + \sum_{i=1}^{n} a_i \frac{s}{s^2 + \omega_i^2}. \tag{2}$$

Moreover, the transfer impedance of the ladder must take the form

$$z_{12} = A \frac{s^{2n+1}}{\prod_{i=1}^{n} \left(s^2 + \omega_i^2\right)}. \tag{3}$$

Because z_{12} is determined within the multiplier A, z_{12} can be rewritten as follows:

$$z_{12} = As + \sum_{i=1}^{n} A\rho_i \frac{s}{s^2 + \omega_i^2}; \tag{4}$$

the ρ_i in (4) are completely determined, and are given by

$$\rho_i = \lim_{\Omega \to \omega_i} \left[\frac{(s^2 + \Omega^2)\, s^{2n}}{\prod_{j=1}^{n} \left(s^2 + \omega_j^2\right)} \right]. \tag{5}$$

If one assumes that $\omega_1 < \omega_2 \ldots < \omega_n$, then it follows from (5) that the signs of successive ρ_i alternate, the sign of each ρ_i being the same as that of $(-1)^{n-i+1}$. The alternation of sign may be made explicit by rewriting (4) as follows:

$$z_{12} = As + \sum_{i=1}^{n} (-1)^{n-i+1} A|\rho_i| \frac{s}{s^2 + \omega_i^2}. \tag{6}$$

The expression for the impedance z_{22} of the ladder is a simple consequence of (2), (6), and the fact that the z_{ij} are compact.[1] The expression is

$$z_{22} = As + \sum_{i=1}^{n} \frac{A^2|\rho_i|^2}{a_i} \frac{s}{s^2 + \omega_i^2}. \tag{7}$$

Expressions (2), (6), and (7) enable one to express the (given) impedance Z in terms of the parameters of the (desired) impedance z_{11}. Reference to the Tee equivalent of the ladder shows that

$$Z = z_{11} + z_{22} - 2z_{12}. \tag{8}$$

Substitution of (2), (6), and (7) in (8) leads to the following expression for Z

$$Z = \sum_{i=1}^{n} \frac{1}{a_i} \left[a_i + (-1)^{n-i} A|\rho_i| \right]^2 \frac{s}{s^2 + \omega_i^2}. \tag{9}$$

If the impedance Z that results when z_{11} is developed into a ladder is to coincide with the (given) impedance (1), then (9) must coincide with (1). Thus the parameters of z_{11} must satisfy the equations

$$\frac{1}{a_i} \left[a_i + (-1)^{n-i} A|\rho_i| \right]^2 = k_i \qquad \text{for } i = 1, 2, \ldots n. \tag{10}$$

The requirement for Z to be realizable as shown in Fig. XXX-2 is that Eqs. 10 admit of positive real solutions for A and the a_i.

Equations 10 may explicitly be solved for the a_i in terms of the parameter A, through use of the quadratic formula. The resulting expressions are

$$a_i = \left[\frac{k_i}{2} + (-1)^{n-i+1} A|\rho_i|\right] \pm \sqrt{\frac{k_i^2}{4} + (-1)^{n-i+1} A|\rho_i| k_i} \qquad \text{for } i = 1, 2, \ldots n. \tag{11}$$

Examination of the expressions (11) reveals that all of the a_i are real and positive, provided

$$0 < A \leq \min. \left[\frac{k_n}{4|\rho_n|}, \frac{k_{n-2}}{4|\rho_{n-2}|}, \frac{k_{n-4}}{4|\rho_{n-4}|}, \text{ etc.}\right]. \tag{12}$$

Thus Eqs. 10 indeed admit of positive real solutions for the a_i and A, and, consequently, any impedance of the form (1) is realizable by N.

To realize a given impedance Z, one need only to

(i) select A in the interval (12),

(ii) determine the a_i from (11), and

(iii) develop (2) into a ladder.

Because (12) permits an infinite number of possible choices for A, the impedance Z always can be realized in an infinite number of ways. Further realization possibilities are introduced by the sign option in each of Eqs. 11.

To illustrate the procedure, we realize the impedance

$$Z = \frac{s}{s^2 + 1} + \frac{s}{s^2 + 2}. \tag{13}$$

Substitution of the values $k_1 = 1$, $k_2 = 1$, $\omega_1^2 = 1$, and $\omega_2^2 = 2$ in (5) leads to the values $\rho_1 = 1$ and $\rho_2 = -4$. Thus (12) amounts to the requirement

$$0 < A \leq \frac{1}{16}. \tag{14}$$

If A is chosen to be the maximum value allowed by (12), then (11) shows that

$$a_1 = \frac{9 \pm 4\sqrt{5}}{16} \quad \text{and} \quad a_2 = \frac{1}{4}. \tag{15}$$

If one elects the positive sign in the expression for a_1, and substitutes A, a_1, and a_2 in (2), the following expression results.

$$z_{11} = \frac{s^5 + [16 + 4\sqrt{5}]\, s^3 + [24 + 8\sqrt{5}]\, s}{16s^4 + 48s^2 + 32}. \tag{16}$$

When z_{11} is developed into a ladder, the realization of Z shown in Fig. XXX-3 is obtained.

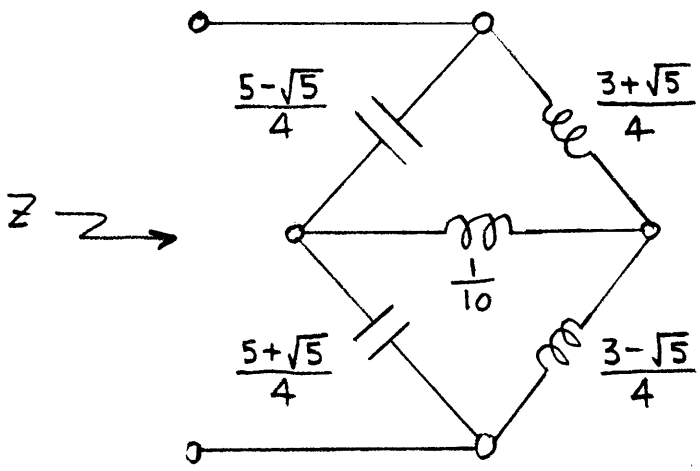

Fig. XXX-3.

By employing the same general approach that has just been described, and slightly varying the details, one can develop a number of related synthesis procedures. For example, one can develop synthesis procedures

(i) for the network that results when the inductors and capacitors of Fig. XXX-1 are interchanged;

(ii) for the dual of the network shown in Fig. XXX-1; and

(iii) for the dual of the network described in (i).

H. B. Lee

References

1. H. B. Lee, The physical meaning of compactness, IEEE Trans., Vol. CT-10, pp. 255-261, June 1963.