DIGITAL BEAM TRAJECTORY AND ORBIT SYSTEM, FOR THE CERN PROTON SYNCHROTRON

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Abstract

A new trajectory and orbit measurement system using fast signal sampling and digital signal processing in an FPGA is proposed for the CERN PS. The system uses a constant sampling frequency while the beam revolution frequency changes during acceleration. Synchronization with the beam is accomplished through a numerical PLL algorithm. This algorithm is also capable of treating RF gymnastics like bunch splitting or batch compression with the help of external timing signals. Baseline and position calculation are provided in the FPGA code as well. After having implemented the algorithms in C and MatLab and tested them with data from a test run at the PS, they have now been implemented in the FPGA for online use. Results of measurements on a single beam position monitor in the CERN PS and the SIS-18 at GSI will be presented.

INTRODUCTION

Even though over 50 years old, CERN's Proton Synchrotron (PS) plays a central role in the production of particle beams for all of CERN. Its extremely flexible RF accelerating system manipulates the beam in many different and complicated ways. Several types of beam (see Figure 1) are produced for various users. The PS is equipped with a trajectory measurement system, based on 40 electrostatic pick-ups (PUs), which measures the beam trajectory of any selected particle bunch over two consecutive revolutions anywhere during the acceleration cycle. However, measurements cannot be spaced closer than 5 ms apart and it does not handle bunch splitting and merging operations very gracefully. Also, part of the equipment dates back to 1988 and is in need of replacement.

A new system has been developed that is entirely digital, to be implemented in FPGA logic, and which deals smoothly with any existing and foreseeable beam manipulations (but limited to the regimes where the PUs deliver exploitable signals). It will also be able to provide measurements anywhere during an acceleration cycle without timing restrictions, to several clients simultaneously.

The centre of charge of a bunch is measured by integrating both the sum and the delta signals over the length of a bunch and applying :

$$x = S_x \frac{\Delta_x}{\Sigma}$$

where S_x is a scaling factor to yield a result in mm.

The gate and base line restitution (BLR) timing signals, required for integration are derived from the digitized beam signal using a numerical phase locked loop (PLL).

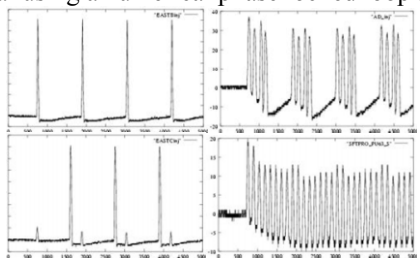

Figure 1: Beams in PS: EASTB, AD, EASTC, SFTPRO [3].

THE PLL ALGORITHM

Referring to Figure 2, a direct digital synthesizer (DDS) block generates a local oscillator (LO) square wave signal, which is then mixed with the PU sum. The product, after low pass filtering, controls the DDS frequency. The filter time constant, pole/zero arrangement and loop gain were chosen as a compromise between loop stability and lock-in time. The PLL ensures a fixed phase relation between the DDS and the beam [2].

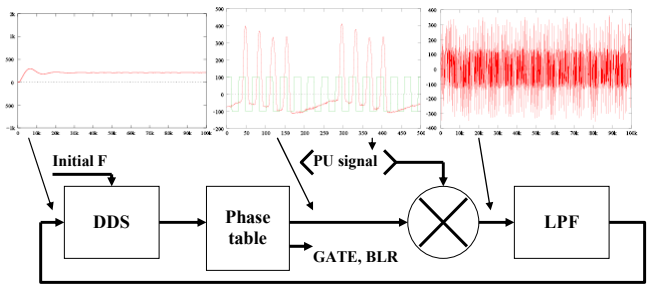

Figure 2: The numerical PLL algorithm principle.

BASELINE RESTORATION AND INTEGRATION

The beam signal originates from an electrostatic shoebox-type pick-up measuring both horizontal and vertical axes in one device. Since the PU does not pass DC, the signal has a baseline droop which needs to be removed before actual processing can be performed. The baseline restoration circuit consists of a filter, which corrects the PU frequency characteristics and a switched DC restorer synchronised by the BLR timing signal. It also protects the digital correction filter against saturation. The baseline correction is applied to the Σ, Δ_x and Δ_y signals. The baseline restoration block output is then integrated numerically over the period specified by the

gating signal. The integration results are stored in a large circular buffer.

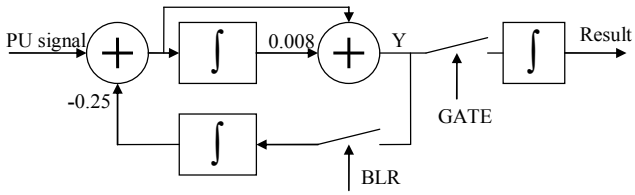

Figure 3 Baseline restorer and integrator.

HARDWARE IMPLEMENTATION

The algorithm is actually independent on the target hardware used. It has been implemented on 2 different hardware platforms, both providing fast 14bit ADCs, big Xilinx Virtex field programmable gate arrays (FPGAs) and fast memory (Figure 5Error! Reference source not found.).

The ADCs and all the processing logic run at a 125MHz clock rate and the FPGA internal data bus is 24 bits wide. Because the beam harmonic number may change during the acceleration cycle, and it varies for different beam types, a phase table was implemented as a double block of RAM in which the integration gate length, baseline removal and local oscillator pulses can be defined separately for each beam type.

The input signal, after baseline restoration, is fed into three numerical integrators which calculate sum and difference components. The integration results are then stored into the 128MB DDRII SDRAM circular buffer. The depth of the buffer allows storing results for more than one full acceleration cycle which takes approximately 2 s. The speed of the SDRAM is not critical, since only the final integration results are stored.

To make navigation over the buffer possible, there is a pointer array, implemented as separate embedded RAM memory, which points to specific events in the SDRAM memory, like harmonic changes, injection triggers and the 1 ms machine reference timing. The information about these events is delivered as external hardware triggers. The results from the buffer are then read out on user request and processed further in software running on a remote machine. There also are diagnostic facilities (Figure 4) that provide remote access to recordings of critical algorithm signals. It has the form of a logical analyser embedded in the main FPGA. Users can set triggers, choose delay times and signals to be recorded. It allows capturing the chosen signals on different time scales. It is controlled by a small program that writes the recordings into text files on the remote machine.

The acquisition and signal processing modules are managed by an embedded ARM-based single board computer (SBC) running the Linux operating system [1].

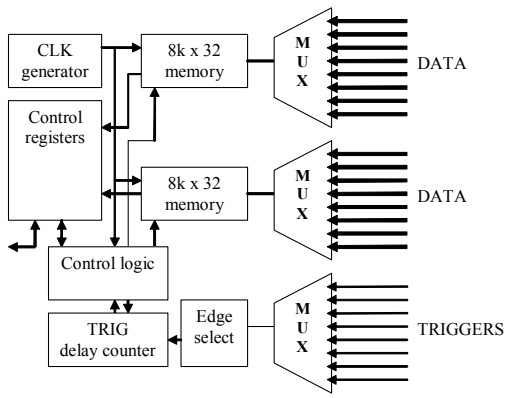

Figure 4: Embedded signal analyser.

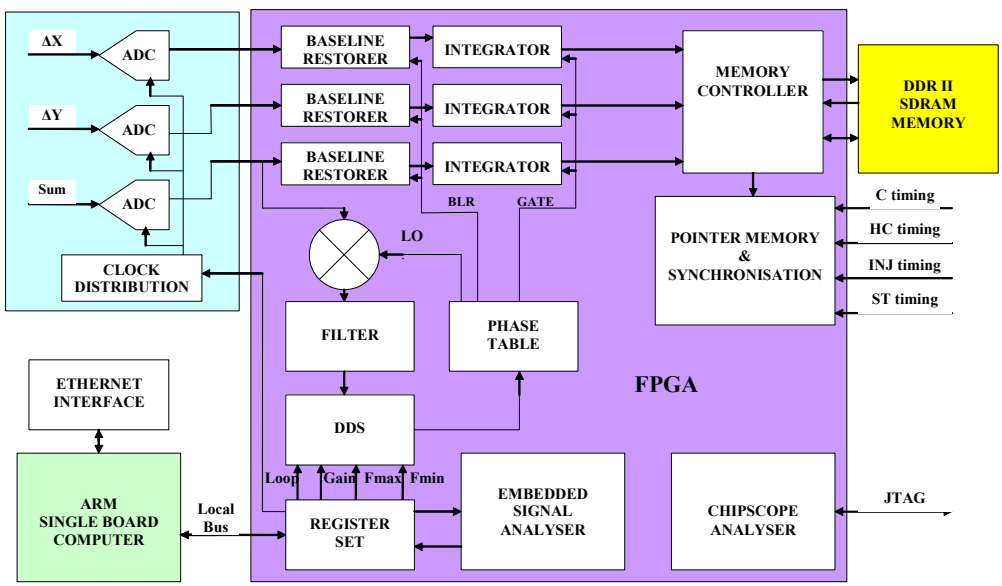

Figure 5: Hardware implementation.

MEASUREMENT RESULTS

Several tests with real signals from a single PU were performed in August 2006 on the CERN PS and in January 2007 on the GSI SIS-18. The results were captured using the embedded logical analyser (Figure 4). Figure 6 shows a raw PU signal (EASTB beam), its baseline corrected version and the gating signal that was generated by the synchronisation algorithm (Figure 2). The gate signal stays locked in phase with the beam pulses.

We also captured the evolution of the reconstructed revolution frequency (DDS frequency register content) during a full acceleration cycle (Figure 7).

It clearly shows that the algorithm stays locked in case of both the PS and SIS-18 accelerator. At the PS the injected beam is already bunched by the preceding PS Booster and the algorithms locks to an external RF system until the beam is injected into the machine. As soon as the beam is circulating in the machine and PU signals are seen, the algorithm switches synchronisation to the PU sum signals.

In case of the SIS-18, the beam is injected from a Linac and is completely unbunched at injection. The RF system bunches the beam shortly before starting acceleration. As soon as the bunch structure appears, the algorithm locks to the beam.

Figure 8 shows the measured sum and horizontal difference integration results, bunch per bunch. The position of the beam is then finally calculated off-line using these results.

The measurement results are rather noisy due to the limited clock frequency used during the preliminary tests (62.5 MHz). The RMS noise of the position measurement is about 0.6 mm, far beyond the target resolution of 0.1 mm. However it was shown, using the offline version of the algorithm on data measured with the full sampling rate, that the target resolution can be reached [1].

Figure 9 shows beam position results with betatron oscillations observed at one of the PUs just after a kicker pulse. An offline FFT allows us to calculate the tune of the accelerator.

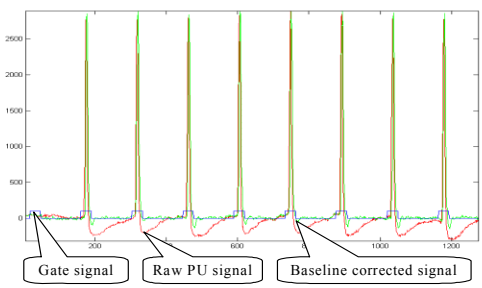

Figure 6: Signals of the PLL algorithm.

CONCLUSION

A prototype digital trajectory measurement system for the CERN PS is being realized. It consists of fast sampling ADCs, big FPGAs and large RAM memories. The FPGAs are used to implement a synchronisation algorithm, baseline correction and numerical integration of sum and difference signals from the electrostatic pickups in the PS.

A first implementation of the algorithms, running in an FPGA, was tested with beam at the CERN PS and the GSI SIS-18. Even though the sampling rate was only half the target frequency of 125 MHz, correct synchronisation with the beam could be demonstrated on both machines. Baseline correction as well as integration procedures worked as expected.

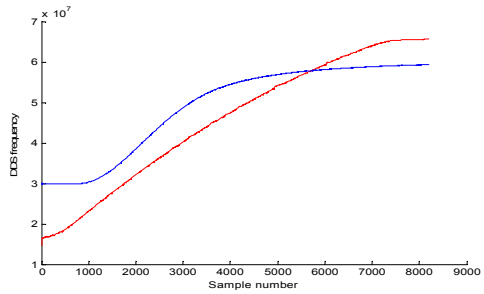

Figure 7: Revolution frequency during acceleration (DDS frequency) PS (blue) and SIS18 (red).

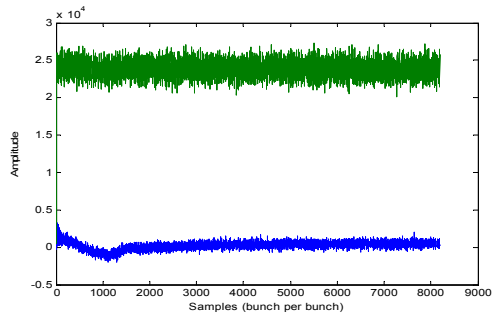

Figure 8: Sum and difference results.

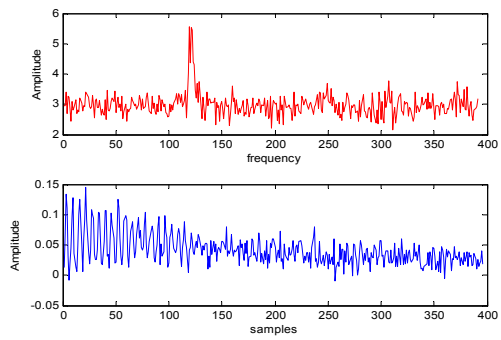

Figure 9: Betatron oscillations and its spectrum.

REFERENCES

[1] J.M. Belleman, "Using a Libera signal processor for acquiring position data from the PS orbit pick-ups", CERN AB-Note-2004-059 BDI, http://documents.cern.ch//archive/electronic/cern/others/ab/ab-note-2004-059.pdf .

[2] J.M. Belleman, "A new trajectory measurement system for the CERN PS", DIPAC2005 slides, http://cern.ch/jeroen/slides/DIPAC05slides.pdf .

[3] Beams in PS, CERN website http://jeroen.web.cern.ch/jeroen/beams.html .