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THE LEIR LLRF DSP-CARRIER BOARD:

PERFORMANCE, CPS RENOVATION PLAN AND RECOMMENDATIONS

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Abstract

The LEIR LLRF project started in late 2003 and included designing, manufacturing and commissioning a novel, all-digital beam control system. The project was first to provide the LEIR machine with a beam control system satisfying the many performance requirements. This was achieved in 2006 with the successful LEIR LLRF system commissioning. In addition, the project was to act as a pilot to export the same technology to the other machines of the PS Complex (CPS), such as PS, PSB and AD. New machines currently being proposed (e.g. ELENA) will also rely on it. The evaluation of the LEIR experience and the recommendations on how to best pursue this migration strategy are therefore integral parts of the LEIR LLRF project. A fundamental building block of the LEIR LLRF system is the DSP-carrier board where all beam control loops are implemented. This note examines the main features of the DSP-carrier board release 1.0 used in LEIR and evaluates their impact on the LEIR LLRF implementation and operational performance. An outline of the intermediate release 1.bis, currently under way, is given. The requirements for a future DSP-carrier board release 2 are outlined, as they were discussed and planned since 2004. The benefits of this new implementation are evaluated and it is recommended that this DSP-carrier board release be studied, designed and manufactured, particularly in view of ever more demanding RF gymnastics and requirements from the different CPS accelerators.

Geneva, Switzerland

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1. INTRODUCTION

The LEIR LLRF system has been tested in the CERN PS Booster [1, 2] during 2004 and 2006 and successfully commissioned in LEIR [3] during 2006. It is based upon RF custom hardware that heavily exploits Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs) processing power. A fundamental building block is the DSP-carrier board which hosts one Analog Devices DSP and that can carry up to two, 2-sites-each daughtercards. In fact, all beam control loops, as well as reference function generation, timing interfacing and diagnostic acquisition, are implemented in the DSP-carrier board

This note is an integral part of the LEIR LLRF evaluation for the definition of a new-generation digital beam control system for the PS complex (CPS). The medium and long-term plans call for the same digital beam control technology used in LEIR to be migrated to the other accelerators in the CPS, namely PS, PSB and AD; new accelerators currently being proposed (e.g. ELENA [4]) will also rely on it. To better address the needs of these machines, and in view of ever more demanding RF gymnastics and requirements, a release 2.0 of the DSP-carrier board is recommended. In fact, while the DSP-carrier board release 1.0 satisfies LEIR's needs and will be instrumental for tests and for partial system implementations [5], new and demanding beam control systems would profit form a number of improvements.

Paragraph 2 outlines the main features of the DSP-carrier board used in LEIR together with their impact on the LEIR LLRF implementation and operational performance. Paragraph 3 summarises the main board improvements planned in the DSP-carrier board release 2.0; the corresponding benefits as they have been discussed and planned since 2004 are also mentioned. An outline of the intermediate release 1.bis, currently under way, is given in paragraph 4.

2. DSP-CARRIER BOARD RELEASE 1.0: OPERATIONAL PERFORMANCE IN LEIR

The LEIR LLRF system is based upon the DSP-carrier board, release 1.0 (EDA-00990-V1). This board, initially designed at Brookhaven National Laboratory, has a 6U VME bus form factor and a 32-bit VME slave interface. It is interfaced through the J2/P2 connector of the VME64x bus to the Rear Transition Module (RTM) located in the rear part of the VME crate and providing additional digital input/outputs and fast inter-processor digital data links.

The DSP-carrier board carries one ADSP-21160M DSP and five Altera FPGAs. The ADSP-21160M DSP is a floating-point, 80 MHz processor which uses an input/output voltage of 3.3 Volt and a core voltage of 2.5 Volt DC. The main DSP task is digital signal processing for one or more beam control loops. The FPGAs belong to the FLEX and MAX families and implement glue logic and interfacing, bus arbitration and some simple digital signal processing activities (e.g. B-train counter). The reader is referred to the DSP-carrier board release 1.0 user manual [6] for detailed information on hardware and FPGA software characteristics.

Figure 1 shows an overview of the LEIR LLRF system: three DSP-carrier board exchange data in real time for the low-level loops implementation. Up to two daughtercards are carried by each board. A fourth DSP-carrier board (namely DSP D) was initially planned for transverse diagnostics but has not yet been implemented. Each DSP is programmed prior to any user cycle with control data coming over the VME bus; diagnostics data are also retrieved over the VME bus at the end of each cycle. Implemented capabilities include frequency program, cavity servoing, radial, phase and synchronisation loops.

This paragraph details the operational performance obtained with the DSP-carrier board release 1.0 during the LEIR 2005 and 2006 operation runs. The main board characteristics are considered together with their implications on the LEIR machine operation.

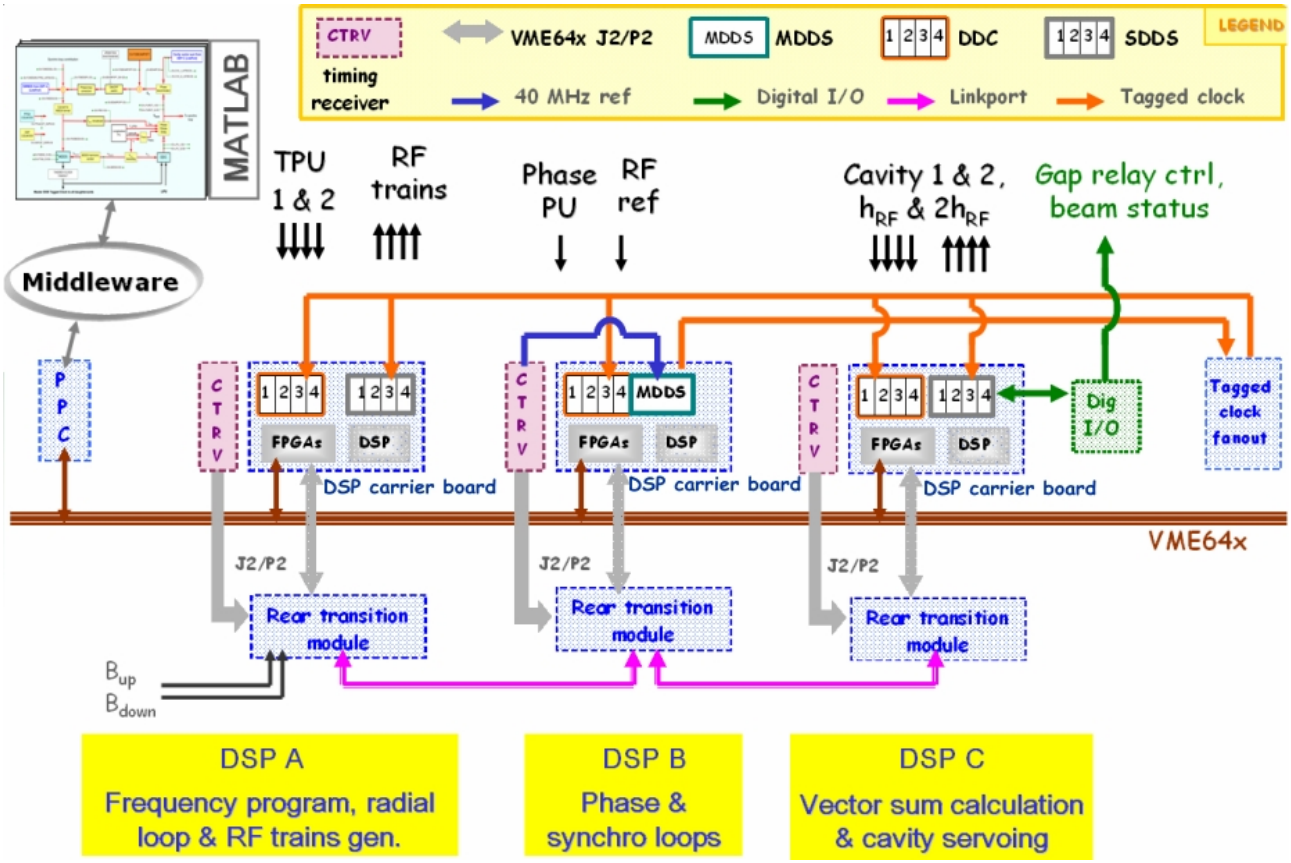

Figure 1: *LEIR LLRF system – schematic view. Keys: MDDS – Master Direct Digital Synthesiser; SDDS - Slave Direct Digital Synthesiser; DDC – Digital Down Converter; TPU –Transversal Pick-Up; CTRV – Timing Receiver module; PPC – Power PC.* B_{up}/B_{down} *– measured magnetic field.*

2.1 Tasks-sharing FPGAs

Glue logic and basic data processing tasks are shared by several FPGA devices hosted on the DSP-carrier board. For instance, VME addresses are decoded in two devices, namely *MEM select* and *VME interface* FPGAs. Digital inputs such as B-train pulses are received in the *Timing interface* FPGA but are passed to the *DSP to receiver* FPGA for the B-train counter implementation.

This task-sharing approach works but reduces the flexibility of the overall design as not all information is available to each and every FPGA. For instance, information such as the up and down ticks of the B-train has to be routed via the "emergency bus" from the *Timing Interface* FPGA to the *DSP to Receiver* FPGA where the B-train counter is implemented. Other signals that have to be routed from one FPGA (namely the *DSP to receiver* FPGA) to another (namely the *VME interface* FPGA) are the DSP WRL/ and RDL/, needed for MEAS SRAM access. The additional routing introduces delays which may have a negative impact on time-critical activities or address decoding.

2.2 DSP processing power

The LEIR LLRF system allows one to monitor, from the application program, the minimum and maximum time required by the DSP to execute specific actions during each cycle. Monitoring the DSP execution time is especially important for the Interrupt Service Routine (ISR) implementing beam control actions. This ISR is triggered by the *DSP sample clock* timing input mentioned in paragraph 2.6 and is called *fastloop*. A new frequency control value is sent to the hardware every time the *fastloop* ISR is executed, hence the *DSP sample clock* frequency strongly influences the beam control loops bandwidth. The *DSP sample clock* frequency should consequently be as high as possible. However, it is essential that its duration still allows the DSP to carry out all required actions; failing this, an error condition is raised and the user cycle is aborted.

Beam control loop implementation is the main function carried out by the DSP in the *fastloop* execution. Other functions, described in a) to e) below, were implemented to make the system flexible, efficient and reliable.

a) Soft-GFAS implementation. In CPS jargon a GFAS [7] is software-plus-VME-hardware system to generate vector-based reference functions. The LEIR LLRF system implements a novel approach to the generation of reference functions: in fact, it is the DSP that generates the actual values to be used by the *fastloop*, as a function of the current cycle time. The DSP-implemented reference functions are called soft-GFAS. Examples of GFAS used in the LEIR LLRF system are radial and frequency steering, radial loop gain and cavity voltage.

b) Soft-timing generation. In the LEIR LLRF system most of the timings are software events that modify the DSP behaviour. This prompted the design and implementation of the DSP code for generating these events, which are called soft-timings. In this way, they can be distinguished them from the pulses-on-a-cable timings, a.k.a. hard-timings. The soft-timings are divided into two tables; each table is referred to a machine-related hard-timing. Typically, for each DSP there are two such hard-timings, one linked to the start of the cycle and another linked to the start of the extraction process. More details are given in paragraph 2.6.

c) DSP-Oasis. In the operation of a digital system it is extremely important for the user to be able to see what is happening inside the system. Failing that, the system becomes a black box and its operation and control become extremely difficult. To avoid this risk, the DSP code has been equipped with the DSP-Oasis functionality. This is a digital data acquisition subsystem allowing the user to store in memory up to four digital signals, chosen from the many signals acquired or calculated by the DSP itself. Such signals are for instance GFAS functions, radial position, raw data from DDCs, phase error. Users may store up to 1024 samples per signal. The sampling rate must be chosen to be a sub-multiple of the *DSP sample clock*.

d) Error messages treatment. Each DSP checks regularly for error messages coming from the other DSPs, so that the whole system can abort one cycle in a safe and controlled way if necessary.

e) Housekeeping activities. Many values are exchanged between DSPs. One example is the revolution frequency, which is known only to DSP B as it calculates it. This value is broadcast to the other DSPs every 100 μs to allow them to update internal parameters such as their rotator vectors.

Table 1 shows the number of GFAS, soft-timings and signals available to DSP-Oasis, currently enabled in each DSP of the LEIR LLRF; these activities correspond to the above points a) to c). Up to six GFAS can be enabled on each DSP, while there are no limits for the number of soft-timings and DSP-Oasis signals.

	DSP A	DSP B	DSP C
Number of GFAS	3	1	3
Number of soft-timings (injection and extraction tables)	31	22	32
Number of signals selectable for DSP-Oasis	34	46	70

Table 1: *Number of GFAS, soft-timings and signals selectable for DSP-Oasis used in each of the three DSP composing the LEIR LLRF system.*

Figure 2 shows the general *fastloop* ISR processing organisation, which is common to all DSPs. There are three main parts, namely *prologue*, *beam control* and *post beam control*. For DSP A and DSP C the end of the *beam control* part means sending the processed data to DSP B; for DSP B the end of the *beam control* part means writing the new revolution frequency value to the hardware.

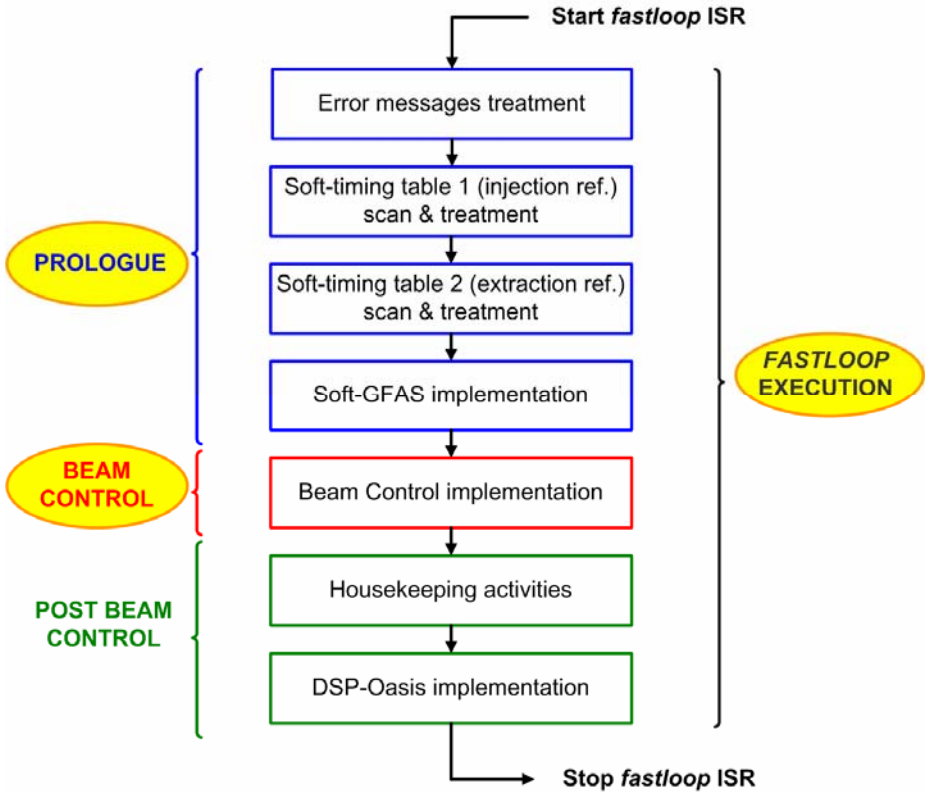

Figure 2: *General fastloop ISR processing organisation, divided into its different composing parts. The execution time of the yellow-circled parts circled can be monitored from the application program in PPM fashion.*

It is possible to monitor the execution time of the *prologue*, of the *beam control* and of the whole *fastloop* ISR. Table 1 shows their maximum and minimum execution times in µs for the typical MDEARLY cycle, i.e. a cycle where beam capture, acceleration and extraction are performed. These measured execution times include a consistent amount of time-consuming diagnostics activity. This involves writing monitoring and debugging data onto the DSP external memory, visible form the VME bus. More details on the time it takes the DSP to access the external SRAM are given in paragraph 2.4.

		DSP A execution time [μs]	DSP B execution time [μs]	DSP C execution time [μs]
PROLOGUE	**min**	1.4	1.4	1.3
	max	3.1	2.8	4.3
BEAM CONTROL	**min**	3.6	2.9	1.2
	max	4.7	6.5	1.5
***FASTLOOP* EXECUTION**	**min**	5.7	5.4	5.1
	max	8.5	11.4	10.6

Table 2: *Maximum and minimum execution time expressed in μs for the prologue, beam control and fastloop ISR.*

It should be noticed that the values in Table 2 do not include the context switching time required before and after executing the actual *fastloop* code. The *fastloop* ISR uses a super-fast interrupt dispatcher, hence 0.425 μs are required before calling the dispatcher and 0.125 μs are required before returning to the interrupted code. A total of 0.55 μs should then be added to the *fastloop* execution time when computing its lowest possible duration.

The DSP sample clock frequency used in LEIR is 80 kHz, corresponding to a *fastloop* ISR repetition period of 12.5 us. This is adequate for LEIR and allows a typical phase loop bandwidth of 10 kHz, as shown in paragraph 2.9.

2.3 Memory arbitration between VME Bus and DSP

The DSP-carrier board has two separate memory blocks, the DSP SRAM and the MEAS SRAM, with different access characteristics.

Data transfer between the 4 MB DSP SRAM and the VME bus as well as between the 4 MB DSP SRAM and the DSP takes place via the DSP external bus. In case of competition between DSP and VME bus, priority is given to the latter; hence the DSP remains stalled until the VME bus access is completed. To prevent this from happening, DSP and VME bus accesses are staged during each LEIR user cycle.

Figure 3 shows the memory access staging during a 2.4 seconds-long cycle (user MDEARLY). The horizontal scale gives the time in ms from the beginning of each cycle, commonly called ctime; the vertical scale is the magnetic field *B*. The green horizontal bar indicates DSP control of the external bus, while the red horizontal bar indicates VME bus control. The DSP retains external bus control from ctime = 0 to ctime = 2000, i.e. when it controls the beam. The VME bus controls the external bus for the next 350 ms, i.e. after beam extraction; during this time diagnostics data are retrieved from the current cycle and controls data for the following cycle are downloaded. DSP-based RF actions are not possible during these 350 ms, as the DSP is mostly stalled. Finally the last 50 ms of each cycle are dedicated to the DSP initialisation for the following cycle. The external bus control sharing between DSP and VME bus for the last 400 ms is the same for any LEIR cycle; this has been discussed and agreed upon with the LEIR operation crew.

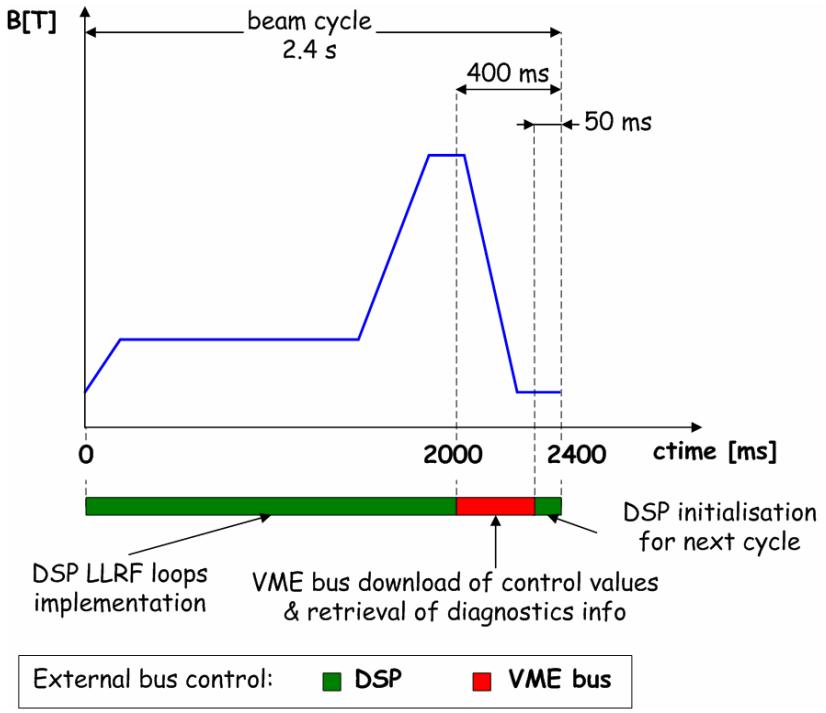

Figure 3: *Qualitative overview of magnetic cycles in LEIR. The horizontal bars shows when the DSP and the RTT respectively have control of the memory during a 2.4 s cycle.*

The 350 ms reserved to the VME bus access at the end of each cycle include a safety margin of about 20%. For each DSP up to 9 kwords have to be downloaded to the DSP SRAM and slightly above 4 kwords must be retrieved. Each word is 32-bit long and can have an integer as well as a floating point format. The D32 VME interface of the DSP-carrier board allows transferring one 32-bit word in a single VME transfer. The net time required for the VME data transfer on one DSP is therefore about 14 ms, which becomes about 45 ms for the whole, three-DSP system. Unfortunately, the global transfer time is much higher as data are logically divided into several data structures and into several programs running on the PowerPC board. This implies that the board driver must be invoked several times; this dominates over the net transfer time.

Data transfer between the VME bus and the MEAS SRAM is carried out through an independent data path which allows transfer to/from the VME bus without using the DSP global bus. However, the shared access to this memory space must be arbitrated by a software semaphore; if this scheme is violated, indefinite data results without any error message. The MEAS SRAM has been tested and validated; it is not currently operationally used in LEIR.

2.4 External memory access time from the DSP

The DSP accesses the external memory (i.e. DSP SRAM, MEAS SRAM) and the memory-mapped I/O (namely the daughtercards space) as bus master and in asynchronous access mode. This access mode is set in the DSP code as one of the first instructions after a reboot; it is also implemented in the FPGAs interfacing the DSP to the memory blocks as well as in the daughtercard FPGA. Programmable Wait States (WS) and one additional hold cycles are foreseen in this access mode to allow the DSP to interface to a wide range of peripherals and memories.

The external memory and the memory-mapped I/O are defined as one block hence the DSP allocates to them the same number of Wait States (WS) when accessing a location within this

space. Two is the minimum WS number to reliably access this block; one additional hold state is added by the DSP, hence the maximum time needed to access an external memory location is 100 ns. The time required to access external memory locations impacts the duration of both DSP cycle initialisation and *fastloop* ISR. In fact, during the cycle initialisation the DSP must access several locations in external memory to retrieve the control data; the *fastloop* ISR runs mostly with internal memory data, however a consistent amount of debug information and all DSP_Oasis data are written directly to the external memory.

2.5 Fast inter-processor digital data links

Two types of digital data links are routed to the DSP-carrier board J2/P2 connector: DSP serial ports and DSP linkports. The former are not connected to the Rear Transition Module (RTM) hence are not used. The latter implement the inter-DSP digital communication. Linkports are half-duplex, byte-serial devices clocked at 40 MHz and designed to maintain signal integrity at high frequency. Data are transferred from the internal memory of a DSP to the internal memory of another DSP via chained DMA transfer; one 32-bit data transfer takes about 110 ns.

As shown in paragraph 1, three DSPs exchange data to implement the LEIR beam control loops processing. Alarm information is also exchanged, thus allowing the system to abort a cycle in a controlled way if abnormal conditions are detected.

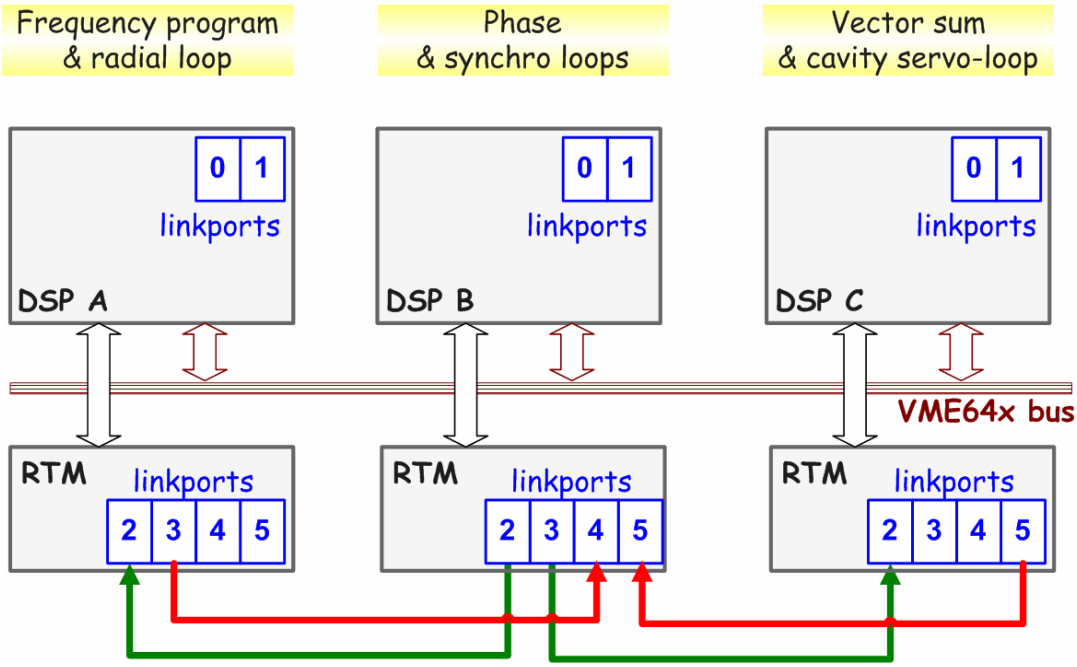

Figure 4: *Schematic view of data exchange via linkports in the LEIR LLRF system.*

Figure 4 shows the LEIR LLRF linkport data transfer as red and green lines. Red lines correspond to the data flow directly required for the beam control implementation: contributions from DSP A and DSP C are passed on to DSP B during every *fastloop* execution. The latency for this data transfer must be as short as possible, as it impacts directly on the control loop bandwidth. Green lines indicate information broadcasted from DSP B to DSP A and DSP B, such as the current revolution frequency value expressed in Hz, which allows them to update their vector rotators. Dedicated initialization code was added for the unidirectional linkport transfer to overcome a recognized ADSP-21160M anomaly [8]. A scheme with bidirectional linkport data transfer (token-passing algorithm) was not included in the final LEIR LLRF system because of the large processing power required by its housekeeping.

2.6 Digital input/output signals

The DSP-carrier board includes six digital input/output signals (TTL levels), used to feed the DSP-carrier board with timing as well as with B-train inputs. Figure 5 shows how timings and B-train inputs are mapped to the board digital inputs. Their allocation among the three DSPs is also shown. Inputs 1, 2 and 3 are machine-related hard-timings. Input 4 is the trigger for the *fastloop* ISR described in paragraph 2.2. Inputs 5 and 6 the B-train pulses generated by the LEIR machine magnetic system.

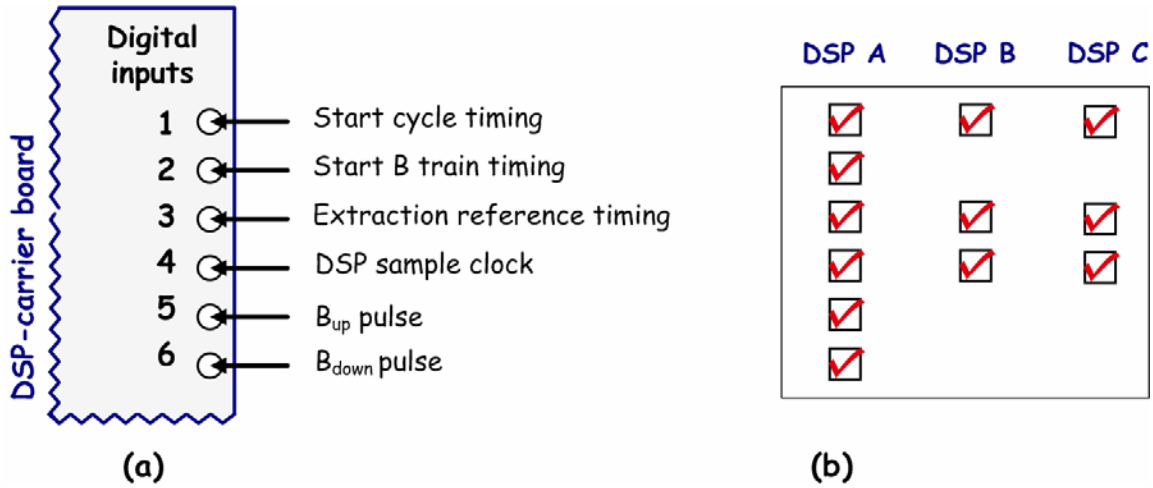

Figure 5: *Digital input allocation to the DSP-carrier board* ***(a)*** *and what is required by each DSP* ***(b)****.*

Table 3 shows the high-level name of the hard-timings used by the LEIR system.

	Trigger number	**Timing name**
DSP A	**1**	EAX.SDSPA
	2	EAX.SRFBTRAIN
	3	EAX.SFLT-M
	4	EAX.DSPCLKA
DSP B	**1**	EAX.SDSPB
	3	EAX.SFLT-M
	4	EAX.DSPCLKB
DSP C	**1**	EAX.SDSPC
	3	EAX.SFLT-M
	4	EAX.DSPCLKC

Table 3: *Timings connected to each DSP-carrier board in the LEIR LLRF system.*

Six digital input/output signals were enough to satisfy LEIR requirements; however, for DSP A it is not possible to timestamp any DSP event owing to the lack of available lines.

2.7 Overall reliability

The DSP-carrier board release 1.0 is functioning reliably. The LEIR LLRF system has been controlling the beam since 2005; from the summer 2006 it has been working in full PPM mode, thus controlling all LEIR users.

The high reliability achieved confirms BNL's experience. In fact, ten DSP-carrier boards release 1.0 are operationally used in three BNL accelerators, namely Booster, AGS and RHIC; many of them have been operational since 2003. In the AGS and Booster they control the Booster-to-AGS synchronization process and produce analog functions. Additionally, they generate the local oscillator frequencies, provide calculated vector sum signals as references and carry out B-train-to-frequency calculations. In RHIC they are used to generate synchronization signals for beam injection. Two release 1.0 DSP-carrier boards are also operationally used in the SNS LLRF implementation.

It should however be mentioned that during lab tests a "bus grant" error was discovered, whereby access to the board was lost and a board cold boot was required. The "bus grant" error was generated by divide-by-zero operations carried out on the DSP following erroneous data being loaded from the VME bus. The reasons for this behaviour are not completely understood yet, in particular it is not clear whether it comes from the DSP or from the *VME interface* FPGA. Adequate data check and protections have been included in the DSP code to protect against such happenings and the error never occurred again.

A second potential problem discovered in some DSP-carrier boards release 1 is an occasional erroneous DSP power-up sequence. This results in the DSP not booting up correctly. The three DSP-carrier boards used for LEIR do not suffer from this problem, which has been understood and hopefully solved in the release 1.bis (see paragraph 43).

2.9 Operational performance conclusions

The board is performing reliably for the implementation of the LEIR LLRF system, which works to full users' satisfaction. The system beam control capabilities, its flexibility as well as the amount of diagnostics data available are fully appreciated and exploited. Distinctive advantages over analogue beam control implementations include the possibility of remotely controlling all parameters in a PPM fashion. Extensive diagnostics information is also available in a PPM way. Examples of these characteristics are given below. The data shown are generated by the LEIR LLRF DSP-Oasis system as well as by independent and parallel systems.

Figure 6 shows a trapezoidal radial steering applied to the beam. Data were acquired during the 2005 LEIR run. The red trace is the beam radial position measured as the average of two radial pick-ups; the blue trace is the magnetic field intensity acquired by the system. These traces are plotted as a function of the ctime. The green arrow highlights the moment when the radial loop was actually closed, thus bringing the beam radial position to the centre of the beam pipe. The dynamics of both radial and phase loops were previously measured and found in agreement with the expected values [3].

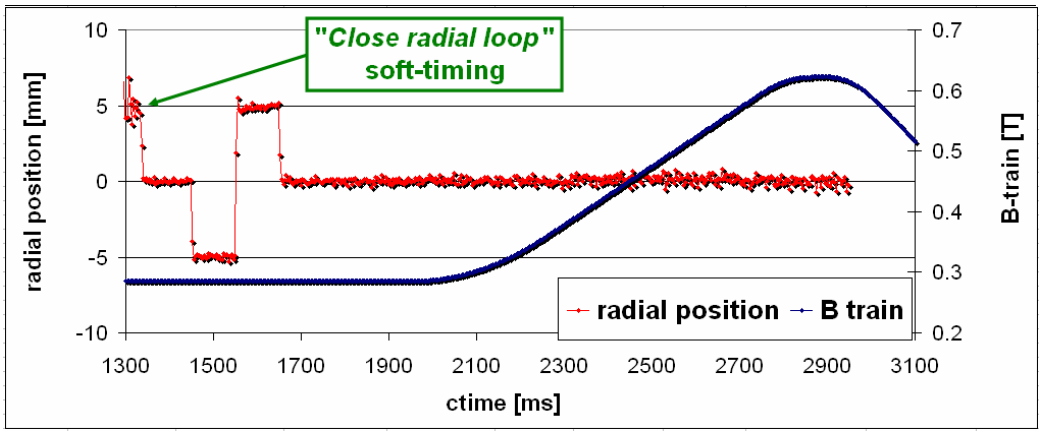

Figure 6: *Keys: B-train - blue trace; beam radial position - red trace. The green arrow shows when the radial loop has been closed. Data refer to the LEIR 2005 run and the beam was not extracted from the LEIR machine*

Figure 7 shows the measured beam-to-cavity phase φ (pink trace) and the magnetic field intensity acquired by the LLRF system (blue trace) as a function of the ctime. The green arrow indicates the ctime when the phase loop was actually closed. Data were acquired on the 2006 LEIR run. A frequency-dependent rotation was carried out on the beam data to align beam and cavity vectors. This rotation was fully implemented by software, providing a considerable advantage in terms of flexibility, remote controllability and cost with respect to the traditional hardware implementation.

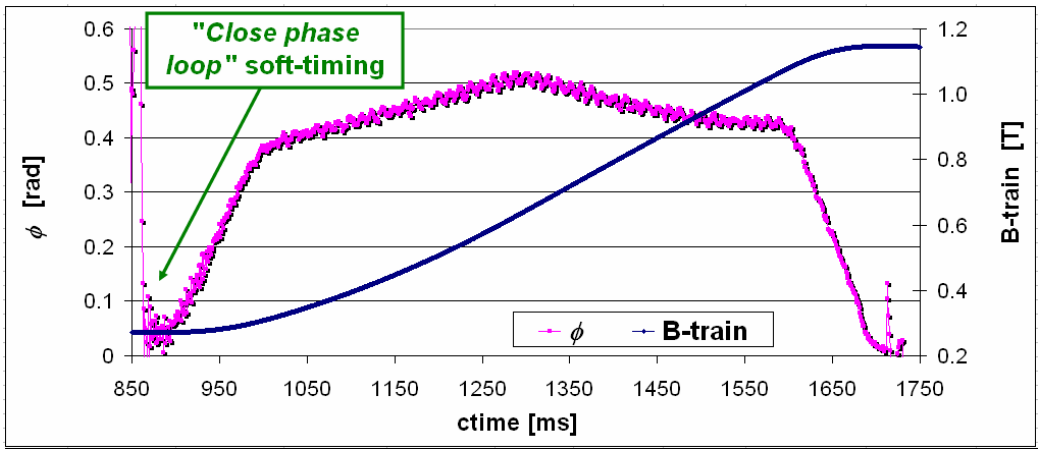

Figure 7: *Keys: B-train - blue trace; measured beam-to-cavity phase - pink trace. The green arrow shows when the phase loop has been closed. Data refer to the 2006 LEIR run.*

Figure 8 shows the measured beam-to-cavity phase φ (pink trace) and the magnetic field intensity (blue trace) as a function of the ctime. Data were acquired on the 2005 LEIR run. Plots (a), (b) and (c) correspond to the same cycle for different acquisition rates; in particular, plots (b) and (c) give a zoomed vision around ctime = 1500. Plot (d) refers to a different cycle where a different phase loop gain was used.

A 0.2 rad step is added to the measured beam-to-cavity phase φ at ctime 1500 ms and the beam phase loop response is observed to determine the maximum phase loop bandwidth attainable. Two different phase loop gains are used: a gain equal to 7000 for plots (a), (b) and (c); a gain equal to 15000 for plot (d). The gain of 7000 corresponds to a phase loop bandwidth BW of about 7 kHz while the gain of 15000 corresponds to a BW of about 15 kHz. Plot (d) shows an oscillatory

behaviour in the step response, due to a low phase stability margin. This indicates that the maximum BW attainable by the phase loop is of about 15 kHz.

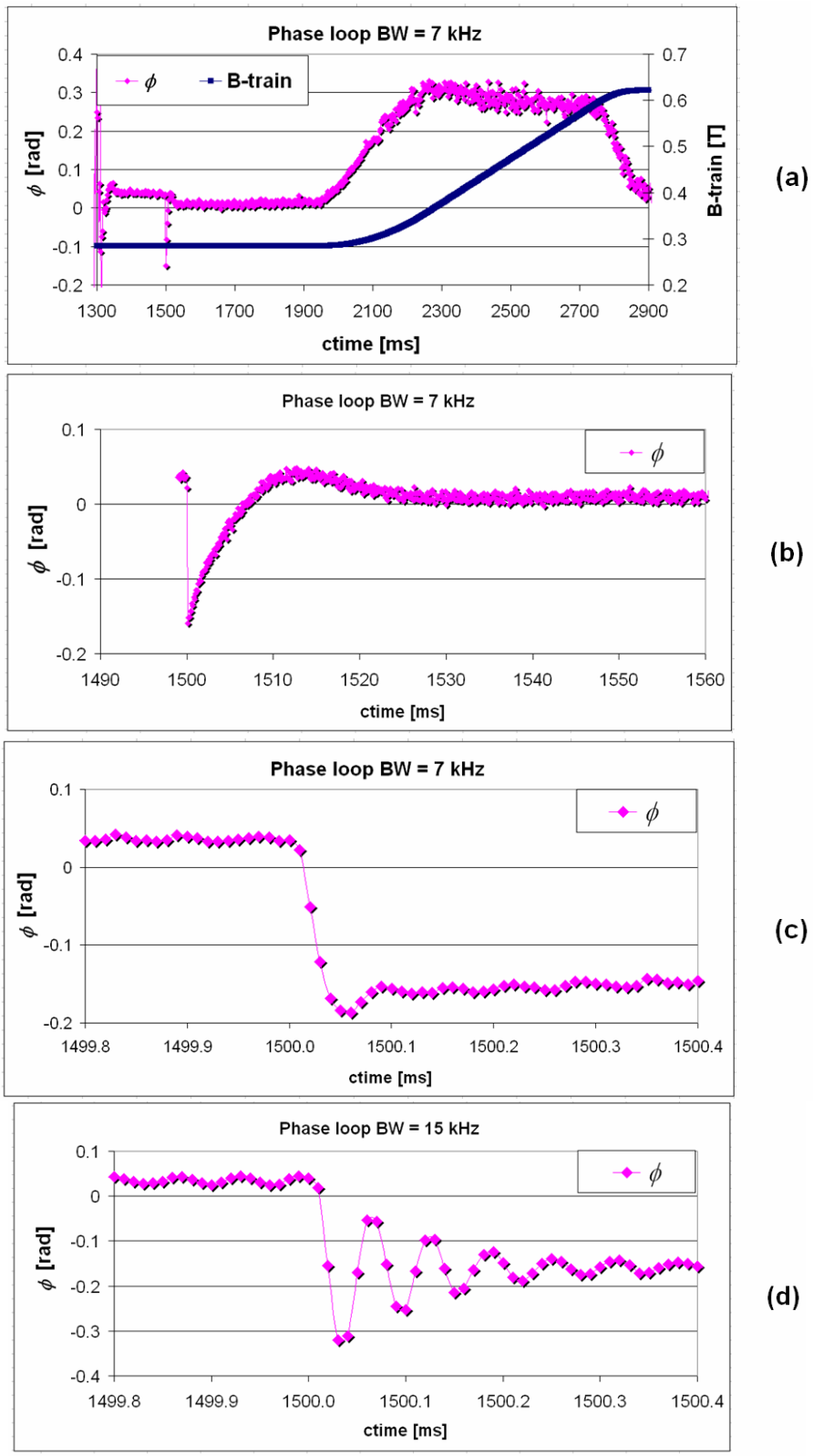

Figure 8: *Keys: B-train - blue trace; measured beam-to-cavity phase - pink trace. The plots show the response of the system to a 0.2 rad step added to the measured beam-to-cavity phase φ. Plots (a), (b) and (c) belong to the same cycle.*

The typical phase loop BW used during routine operation is 10 kHz; this allows accelerating the beam satisfactorily. The beam intensity available in the machine when the data was taken was low, thus explaining the noise present in the measured beam-to-cavity phase.

Figure 9 shows a typical MDEARLY cycle, where the beam is captured, accelerated and finally extracted to the PS machine. Data were taken on October 9th 2006 and refer to a still non-optimised machine. Plot (a) shows the magnetic field (pink trace), the electron cooler grid programmed voltage (blue trace) and the beam intensity (yellow trace) as a function of ctime. About 2.2 E8 ions are captured, accelerated and extracted with minimal losses. Plot (b) shows the bunch at extraction as seen from two pick-ups (yellow and pink traces) together with the extraction kicker (yellow trace). The white traces are references from previous cycles, indicating that the beam synchronisation loop works extremely well.

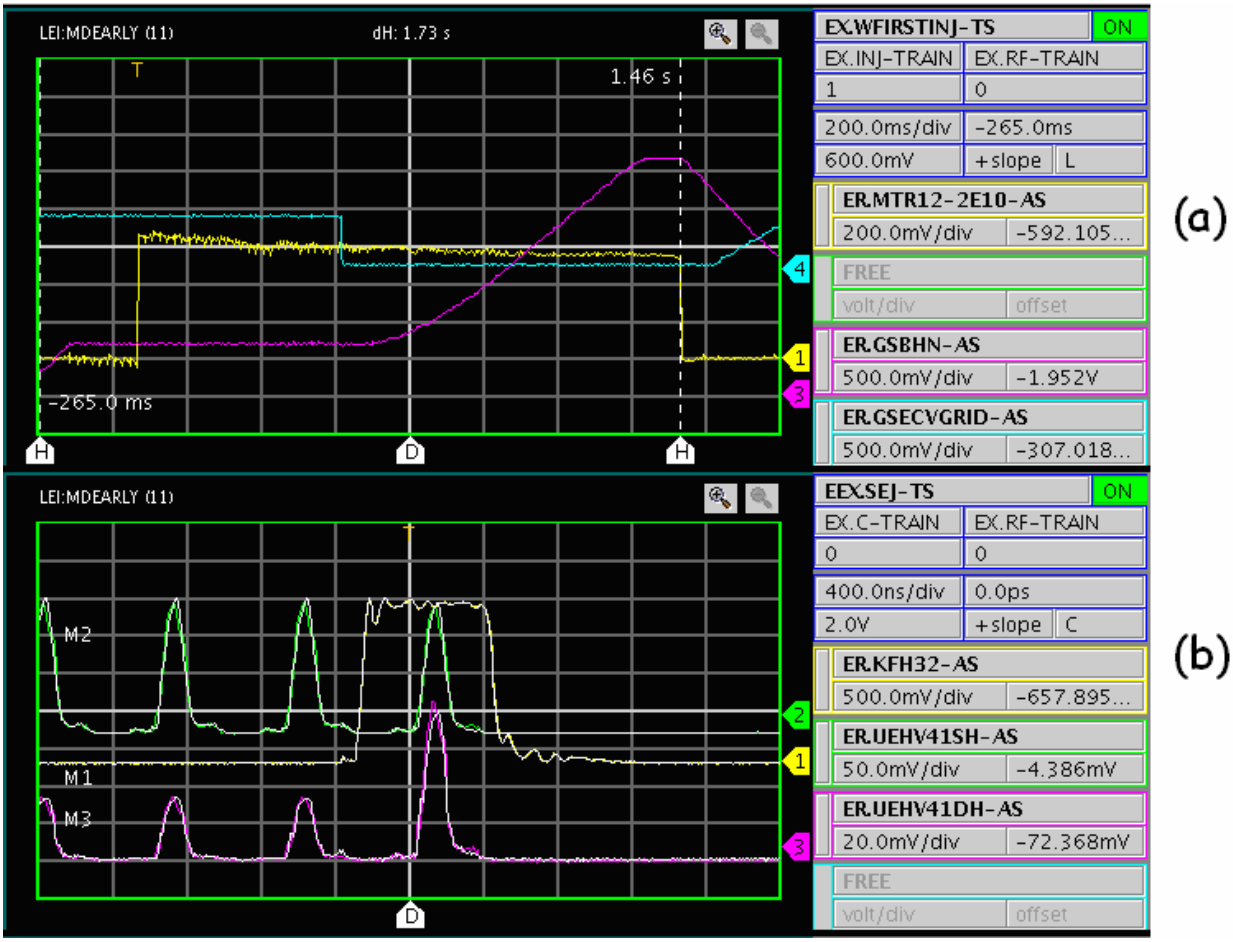

Figure 9: *Data from Oct 9 2006, user MDEARLY. Plot* ***(a)*** *keys: magnetic field - pink trace; beam intensity – yellow trace; electron cooling gun voltage – blue trace. Plot* ***(b)*** *keys: extraction pick-ups – green and pink traces; extraction kicker – yellow trace.*

Figure 10 shows the beam orbit just before extraction for the same MDEARLY of Figure 9. The horizontal axis indicates the section number for the linearized LEIR, starting with section 1 on the left. The grey boxes represent the bending magnets separated by straight sections.

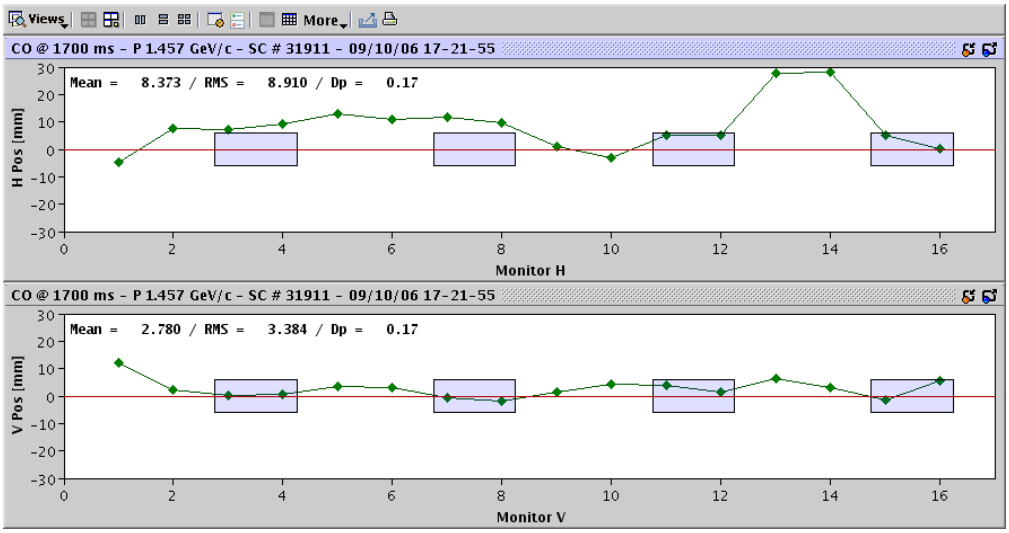

Figure 10: *Snapshot of beam orbit just before extraction. Beam phase and synchronisation loops are active; radial loop is not active.*

3. PLANS FOR THE DSP-CARRIER BOARD RELEASE 2.0

The DSP-carrier board release 2.0 has been under discussion since early 2004 and its implementation was planned for the fall 2005. The RTM implemented at CERN in 2005 was designed to be compatible with this new DSP-carrier board release. The requirements summarised in this paragraph derive from many brainstorming sessions and discussions carried out at CERN and at BNL; specific CPS machine needs have been also taken into account. In fact, while the release 1.0 satisfies LEIR's needs, as shown in paragraph 2, and will be instrumental for tests and for partial system implementations [5], new and quite demanding beam control systems would profit from the new features described.

3.1. Single FPGA tasks manager

A single and powerful FPGA should take the place of the five smaller FPGAs which share glue-logic and simple processing tasks in the DSP-carrier board release 1.0. This would increase the flexibility as well as the digital signal processing capabilities of the system.

Figure 11 shows the planned conceptual design for release 2.0 : a FPGA is at the core of the system and interfaces to the main actors, namely on-board memory, DSP(s), daughtercard sites, VME bus, front panel and RTM. The major functions of this device are:

a) VME interface including interrupt capability.
b) Memory subsystem interface.
c) Timing interface.
d) DSP start-up sequencing.
e) Clock distribution.
f) Reset control and distribution.

To accomplish these tasks a complex FPGA with a large pin count is required. Other features such as considerable DSP and memory capabilities may also be useful, as additional data processing could be carried our by the FPGA itself. The FPGA configuration flash devices should be accessible via the VME bus, so as to be able to remotely re-program the FPGA.

An additional FPGA, not shown in Figure 11 and with minimal processing power but medium/high pin counter, is considered to act as linkport multiplexer (see paragraph 3.2).

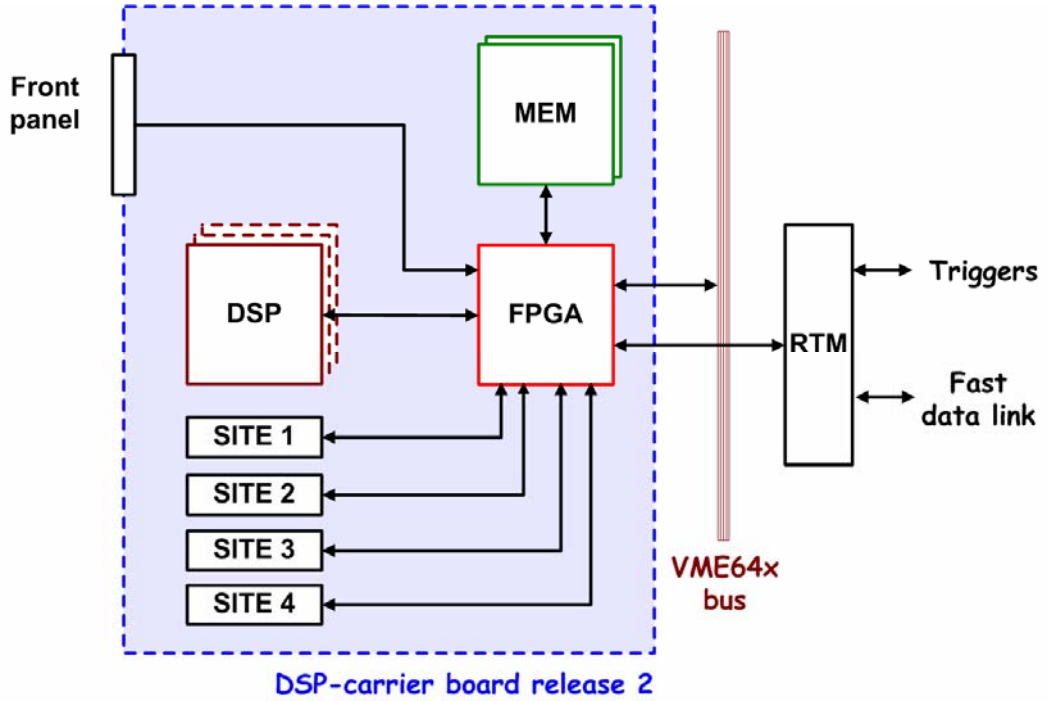

Figure 11: *Planned conceptual design of the DSP-carrier board release 2.0.*

3.2 Increased DSP processing power

The DSP processing power available on the board should be increased as it might limit the beam control loop bandwidth. It should be underlined however that the actual control loop sampling time depends not only on the DSP processing power but also on the external memory access time and on possible external bus bottlenecks. All these aspects should be taken into consideration when designing the new board release and the corresponding software architecture.

The plan for the DSP-carrier board release 2.0 was to include two SHARC ADSP-21160N DSPs sharing the same external bus and common DSP memory space.

ADSP-21160N are SHARC DSPs code compatible with and functionally identical to the ADSP-21160M hosted in the DSP-carrier board release 1.0; however, the ADSP-21160N run at a 100 MHz core hence providing a 25% boost in processor speed with respect to the ADSP-21160M. Additionally, most of the ADSP-21160M chip anomalies have been solved on the ADSP-21160N. Other differences include the nominal core voltage requirements, power-up sequencing and pin allocation. The move from the ADSP-21160M to the ADSP-21160N is well documented [9].

SHARC DSPs are chips designed to interface without additional glue logic, hence the two-DSPs hardware layout is relatively simple. With two DSPs, the DSP-carrier board would be equipped of a total of twelve linkports, hence gaining in board interconnectivity. All linkports should be routed through a multiplexer, which would increase the flexibility with regard to inter-processor data transmission as well as between daughtercards and RTM. A separate and small FPGA could be used for this function, owing to the number of connections and the speed required.

The possibility to move to two DSPs of a different and more powerful type, such as the TigerSHARC, was also considered. The following points should be taken into consideration when evaluating this possibility:

a) Time needed to move the existing DSP code (especially the assembly part) to the new DSP.

b) DSP read/write cycles, particularly regarding memories and daughtercards interface.

c) Inter-DSPs connectivity: TigerSHARC have 4 linkports instead of 6 and they are not compatible with the linkports available in the SHARC DSP family.

3.3 Memory size and interleaved memory arbitration

An increase of the board storage capabilities might be useful for more complex beam control systems or for locally storing "resident users" data. It is therefore suggested that the total SRAM size on the board be increased by a factor of four to a 32 MB total. Cypress now have SRAM of 1M x 16 bit available in a size package similar to what is used for the board release 1.0 (CY7C1061AV33, 54 pin package compared with 44 pins in the release 1.0 memory 256k x 16 bit); hence the additional SRAM would not significantly increase the required real estate amount on the board itself. The memory could be arranged in a single bank (unified memory space) or divided into two banks with separate control, similarly to what is done for release 1.0.

SRAM data should be piped through the large FPGA mentioned in paragraph 3.1. This will make possible to buffer the VME bus data and provide fast hardware arbitration between almost simultaneous access from both VME and DSP. There are true dual port chips available in 256k x 16 from IDT (ex. IDT70V631S – 128 or 256 pin package due to true dual ports) but this might be an overkill as few wait states will be introduced due to access conflicts with the hardware arbitration scheme proposed above. Fast hardware arbitration between VME bus and DSP memory access will allow retrieving diagnostics data during the cycle; while this is not essential for the relatively short LEIR cycles (duration up to 3.6 seconds), this is quite convenient for long cycles, such as the AD cycle (duration about 90 seconds).

Finally, it is felt that introducing DRAM on the board in order to get even more external memory space on the board in release 2.0 would not be convenient, owing to the extra complexity of DRAM interfacing and to the fact that the access time is often optimised for burst data transfers.

3.4 External memory access time from the DSP

The relatively long DSP access time to the external and daughtercard memory space on the DSP-carrier-board release 1.0 impacts on the required total processing time hence on the loops bandwidth. It is essential that this access time is minimised in release 2.0. This could be achieved with a optimised FPGA code as well as with a global bus running at a higher frequency.

3.5 Fast inter-processor digital data links

The number of high-speed, low-latency, inter-processor digital data links should be increased to address the needs of accelerators with a high number of cavities. An example is the PS machine, where data from eleven cavities have to be combined to generate the vector sum value to be used by the beam phase loop DSP. It is essential that this value is calculated and passed to the phase loop DSP as fast as possible, as any delay in this action will directly be reflected onto the phase loop bandwidth.

ADI linkports, i.e. half-duplex, byte-serial devices, are used satisfactorily in LEIR; their number would be increased in the DSP-carrier board release 2.0 owing to more than one ADI DSP being hosted in the same board. However, their number and electrical characteristics depend entirely on the DSP family chosen.

It is felt that additional high speed, low-latency inter-processor communication means should be made available in the DSP-carrier board trough the front panel. High-speed serial I/O is the best choice owing to the small number of pins needed, the absence of simultaneous switching output problems and the lower electromagnetic interference. Serial links with clock-data recovery not only help reduce the number of traces (compared to parallel links) but also eliminate clock-to-data skew. Differential-transmission standards are used (e.g. RapidIO and Infiniband). Many interfaces and protocols are currently widely adopted: FPGA protocols include Aurora (Xilinx) and SerialLite (Altera).

3.6 Digital inputs/outputs

The number of digital inputs/outputs connected to the DSP-carrier board through the J2/P2 connector and the RTM should be increased. A RTM [6] has been manufactured at CERN that allows connecting up to 16 digital input/outputs; the DSP-carrier board release 2 should be compatible with it.

3.7. Miscellanea improvements

Additional improvements planned are as follows.

a) The address lines passed from the DSP-carrier board to each daughtercard site should be shifted by one, i.e. address lines A[1] to A[15] should be passed instead of A[0] to A[14]. In fact, only the 32 MSBs of the DSP data bus are used for DSP-to-daughtercards interfacing, hence the memory addresses are all odd. This means that the A[0] line does not carry any information. By shifting the addresses by one as detailed above the addressed space will be doubled.
b) The DSP-to-daughtercard interface should include a reset line as well as DMA interrupt lines. JTAG lines should also be added, so that the daughtercard FPGA code could be reloaded directly from the VME bus and not only with a local ByteBlaster cable through the JTAG header.
c) The DSP soft reset reliability should be improved by connecting the DSP RESET pin to the central FPGA.
d) Changing the VME base address and Status/ID vector by hardware (on-board switch) instead of by FPGA software only should be allowed.
e) The same set of read and write strobe (WRH/ and RDH/ for the ADSP-21160M DSP) should be sent to on-board memory and memory-mapped I/O. This will allow the DSP to access them in a more uniform way.

4. DSP-CARRIER BOARD RELEASE 1.BIS

In early 2006 the DSP-board release 1.bis (EDA-00990-V3) was started. This slightly modified version of the DSP-carrier board release 1.0 aims at correcting some bugs in the design. It also adds some capabilities, most notably an interleaved memory access between VME bus and DSP. Other features, such as the number of digital I/O to the DSP-carrier board and the address space to the daughtercards remain unchanged. The main modifications with respect to the release 1.0 are

listed in points 4.1 to 4.6 below. Some release 1.bis PCBs have been manufactured but not yet assembled at the time of writing. Modifications of the FPGA code are also required. It is recommended that this release, even if its features are somewhat limited, is completed and made operational.

4.1. Interleaved VME bus – DSP memory access

On the DSP-carrier board release 1.0 it is impossible to interleave VME bus and DSP accesses to the on-board memory; in fact, there is no register available to buffer the data for the long VME cycles, which would be required to release access to the DSP external bus during VME transfers. On the DSP board release 1.bis the SN74LVCH16245 directional buffers present in the release 1.0 are replaced by the SN74LVCH16543 registered directional buffers. These buffers not only transfer data from one side to the other but can also store the data until they are transferred. This requires the use of 6 control lines rather than the two being used in release 1.0. These buffers would be controlled by the *VME interface* FPGA via the pins used for testing in the release 1.0.

4.2. Short-circuit on the *Receiver to DSP* FPGA

The *Receiver to DSP* FPGA (U35) could not be physically installed on the DSP-carrier board release 1.0 as its VCCINT pin is shorted to the ground plane via pin W20 on the FPGA itself. In fact, the board layout does not correspond to the schematics and the whole W row is displaced by one pin. This problem has been understood and solved in the release 1.bis.

4.3. DSP power-up correct sequencing

The power-up sequence of the 3.3 Volt and 2.5 Volt power supplies is wrong for DSP operation; this results in the DSP sometimes not booting correctly after a system power off. According to Analog Devices, the 3.3 Volt power supply must come on after the 2.5 Volt supply. A 3.3 Volt linear regulator with a shutdown pin was added to the DSP-carrier board release 1.bis. The shutdown pin will be pulled up by the 2.5 Volt regulator, hence the 2.5 Volt will come on first. This regulator should only be used for the DSP power supply rather than for the whole 3.3 Volt plane on the DSP-carrier board, which also powers the daughtercards.

4.4. Daughtercard FPGA reset

The daughtercard FPGAs can be reset only by powering the crate OFF and then ON again. The reason of this is because the FPGA RESET lines are not included in the daughtercard-DSP-carrier board interface. In the release 1.bis the reset lines are included in the Site 1 and Site 3 interface, hence will work for the current 2-sites each daughtercards. These reset lines are also connected to both the FPGA-reset front-panel button and to the VME interface, thus allowing a daughtercard reset from the VME bus.

4.5. DSP remote reset

The DSP can be reset from the VME bus by software; however, this mechanism does not always work and a hardware reset is preferred. With the DSP-carrier board release 1.0 this is not possible as the DSP RESET line which needs to be pulled low for a hard boot can only be activated by a front panel switch. In the DSP-carrier board release 1.bis the DSP RESET line is routed to both the VME Interface FPGA and the front panel switch. The VME interface FPGA will activate the DSP RESET line upon a bit being written to a certain address or the VME SYSRESET line being pulled low.

4.6. Correct clock pins for some FPGAs

For at least two FPGAs on the DSP-carrier board release 1.0 it appears that the clock signals were not connected to the dedicated FPGA clock pins but to a general input/output pin. This had no negative effects on the FPGA performance, however it is a bad practice that has been corrected in release 1.bis.

5. CONCLUSIONS AND RECOMMENDATIONS

The DSP-carrier board release 1.0 has allowed to successfully implement the LEIR LLRF system. This note has examined the DSP-carrier board main characteristics and has shown that they have had only a limited impact on the LEIR LLRF implementation and operational performance. The LEIR LLRF works reliably, to the full satisfaction of the users and provides distinctive advantages over analogue beam control implementations.

Thirteen DSP-carrier boards are currently available at CERN, only three of them used in LEIR. The remaining ones can be used for testing new schemes and for implementing subsystems within already-existing beam control system. This could lead to improved beam-related performances on different CPS machines. It would also allow gaining experience in digital technology for beam controls and related aspects. It is also recommended that the DSP-carrier board release 1.bis be assembled, programmed and made operational, as an intermediate platform for developments provided with additional capabilities with respect to the DSP-carrier board release 1.0.

The RF group medium and long-term plans call for the digital beam control technology used in LEIR to be migrated to the other CPS accelerators, namely PS, PSB and AD; new accelerators currently being proposed, such as the ELENA ring, will also rely on it. The benefits derived from a new and more powerful DSP-carrier board release have been described and analysed; it is recommended that a DSP-carrier board release 2.0 be studied, designed and manufactured. This will allow to better address the needs of the CPS machine, particularly in view of ever more demanding RF gymnastics and requirements,

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