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Development of VHDL Code for the DAQ and Monitoring Boards of the VELO Subdetector of the LHCb Experiment

Diploma Thesis

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I declare that I have elaborated this thesis independently, citing all information sources that I used.

Praha, 11.5.2007 Pavel Stejskal

Název práce:	**Vývoj VHDL kódu pro monitorovací moduly a moduly sběru dat VELO subdetektoru experimentu LHCb.**
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Abstrakt

Subdetektor VELO, založený na křemíkových stripových senzorech, je hlavním trackovým detektorem, sloužícím zároveň k vyhledávání vertexů. Součástí detektoru jsou i desky monitorovacích obvodů – „temperature board" a „low voltage interlock board" – jež slouží ke sledování teploty senzorů a k jejich ochraně před přehřátím. Hlavním předmětem vývoje je rozhraní SPI (část slave) sloužící procesoru Atmel umístěném na modulu ELMB k přístupu k uživatelským registrům v hradlovém poli. Na desce TELL1, sloužící ke sběru dat, jsou na tato data aplikovány algoritmy detekující a odečítající jejich stejnosměrnou složku (pedestal), filtrující přeslechy, potlačující korelovaný šum, zajišťující přeuspořádání dat a vyhledávání a formátování dat tvořících jednu událost (clusters).

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Abstract

The VELO subdetector is the main tracking and vertex finding detector based on silicon strip sensors. The monitoring boards are the 'temperature board' and the 'low voltage interlock board' aimed at measuring temperature of the sensors and protect them against overheating. The main development consists of an SPI slave to interface the FPGA user registers to the Atmel processor on the ELMB mezzanine. For the DAQ board ('TELL1') the online data algorithms are the pedestal tracking and subtraction, cross-talk filtration, correlated noise suppression, reordering of data, cluster finding and formatting.

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List of Abbreviations

ADC	Analog to Digital Converter
ALICE	A Large Ion Collider Experiment
ATLAS	A Toroidal LHC Aparatus
CAN	Controller Area Network
CERN	Organisation (originally Conseil) Européenne pour la Recherche Nucléaire
CMS	Compact Muon Solenoid
CPU	Central Processing Unit
DAQ	Data Acquisition
DELPHI	Detector with Lepton Photon and Hadron Identification
DSP	Digital Signal Processor
ECAL	Electromagnetic Calorimeter
ECS	Experiment Control System
ELMB	Embedded Local Monitoring Board
ENC	Equivalent Noise Charge
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GPIF	General Programmable Interface
HCAL	Hadronic Calorimeter
I^2C	Inter-Integrated Circuit Control Bus
JTAG	Joint Test Action Group
LAN	Local Area Network
LED	Light-Emitting Diode
LEP	Large Electron Positron Collider
LHC	Large Hadron Collider
LHCb	Large Hadron Collider Beauty Experiment
LVDS	Low Voltage Differential Signaling
Mbps	Megabits per Second
NTC	Negative Temperature Coefficient
PC	Personal Computer
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PLL	Phase-Locked Loop
PVSS	Prozessvisualisierungs und Steuerungssystem
RAM	Random Access Memory
RICH	Ring Imaging Čerenkov Detector

RMS	Root Mean Square
ROM	Read-Only Memory
SNR	Signal-to-Noise Ratio
SPECS	Serial Protocol for the Experiment Control System of LHCb
SPI	Serial Peripheral Interface
SUSY	Supersymmetry
TELL1	Trigger Electronics Level 1
TFC	Timing and Fast Control
TOTEM	Total Cross Section and Elastic Scattering Measurement
TTC	Timing and Trigger Control
VELO	Vertex Locator
VHDL	VHSIC Hardware Description Language
VHSIC	Very-High-Speed Integrated Circuit

Introduction

Since the down of time, Man has been trying to understand the origin of the world, to find the answer to the fundamental question: "Where it all comes from?" The modern field of High Energy Physics continues this search for an explanation, throwing light upon the indivisible building blocks of matter and their mutual interaction.

At the present time it is believed that the fundamental blocks of matter consist of six *quarks* and six *leptons* with their mirror particles, so called antiparticles. These particles interact by the exchange of force-mediating particles known as *bosons*. We identify four fundamental forces: *strong*, *electromagnetic*, *weak* and *gravitational*. All of them have their mediating particles that facilitate the corresponding interaction. For the strong force it is a gluon, the electromagnetic interaction is mediated by a photon, weak force is caused by the exchange of $W^{\pm}$ and Z^0 bosons and it is assumed that the gravitational force is allowed for by gravitons. These elementary building block of matter along with the force-mediating particles (except the gravitational one) are described together by a single theory, the *Standard Model of Particle Physics*.

The Standard Model (SM) is a very successful theory which explains, within experimental precision, all experimental phenomena yet witnessed in the laboratory and also predicts the new ones. However, it is not a definitive theory and it suffers from several limitations. First of all, it does not account for the gravity. The essence of the mass is not resolved; whenever the mass of a particle is to be known, it has to be determined experimentally. Furthermore, the Standard Model cannot explain some cosmological phenomena like the origin of *Dark Matter* and why the excess of matter over anti-matter is observed in the Universe.

A fundamental requirement of any theory attempting to explain matter-antimatter imbalance in the early universe is that CP symmetry can be, at some level, violated. This simultaneous violence of parity P and charge conjugation C symmetries was first observed in 1964 in the decay of neutral kaons. The Standard Model can explain CP violation through the Cabibbo-Kobayashi-Maskawa (CKM) mechanism, but this is not enough to explain the asymmetry in the Universe.

Large uncertainties still remain in transitions involving b-quarks. Hence, B-meson decays play an important role in the study of CP violation. Theoretical calculations of decays of B-mesons within the Standard Model framework predict large CP violation effects so the interest is in pushing the precision of the measurement to a level at which, hopefully, the Standard Model predictions will fail.

The new high precision experiments can lead to the failure of SM predictions so the New Physics can be revealed. In the domain of B-physics and CP violation studies such an experiment is the currently build LHCb at the LHC at CERN which is optimized for the reconstruction of B-decays.

The physics reach of all particle physics experiments is very closely linked to the sophistication of the available electronic instruments. They are used to collect the electrical signal from the sensors to amplify, digitize, process and store it with the highest possible speed and precision. Such tasks are very demanding in terms of resources, and therefore very expensive and sophisticated systems must be built. One of these state-of-the-art instruments is the vertex-locating subdetector (VELO), a subdetector of the LHCb experiment which plays a crucial role in reconstruction of the tracks and vertices of particles produced in the LHC collisions. This thesis describes the development of a part of the monitoring and data acquisition system for the VELO.

Scope of the Thesis

The main topic of thesis deals with the monitoring circuitry and the data acquisition system of the VELO subdetector. In the first chapters the motivation and an overview of the whole LHCb experiment is presented, placing emphasis on the VELO subdetector. The fourth chapter is dedicated to the development of VHDL code for the temperature monitoring board. The last chapter describes the proposed upgrade of the 'TELL1' algorithm for the Level-1 data acquisition.

Chapter 1

Theoretical Overview

This chapter gives a brief overview of the background of high energy physics and serves as a motivation for the next parts of the thesis. First, the Standard Model of Particle Physics is outlined. The second chapter describes how the B-meson system can be used to probe for the New Physics. In conclusion, B-meson decay channels of interest at LHCb are summarized.

More than 20 years ago, S. Glashow, A. Salam and S. Weinberg elaborated the *Standard Model of Electro-Weak Interactions* which earned them the Nobel Prize in 1979. This theory combined with *Quantum Chromodynamics* (QCD), forms more general theory called *Standard Model* (SM), which is the most successful theory of elementary particles at the present time.

The Standard Model is a low-energy model, consistent with existing experimental observations of a more fundamental theory, the *Grand Unified Theory* (GUT) – not elaborated yet. This model is able to describe a vast amount of experimental data but unanswered questions still exist. One of them is a fact that *Charge conjugation* (C – transforms particle into its antiparticle), *Parity* (P – creates the mirror image of a physical system), *Time reversal* (T) symmetries and even the CP product of two symmetries are slightly violated during certain types of weak decays. In contrary these symmetries are conserved in strong and electromagnetic interactions.

For the first time the CP violation effects have been observed in the weak kaon decays. For the precise measurement of the CP violation phenomena high statistics experimental data are needed to constrain the theoretical models and to discover New Physics beyond the Standard Model. One of the experimental facilities able to fulfill these requirements is the LHC accelerator complex.

1.1 The Standard Model

The Standard Model of particle physics is a theory which describes three of the four known fundamental interactions between the elementary particles that make up all matter. These three

forces are the strong, weak and electromagnetic force described by the interactions via gauge boson exchange.

1.1.1 Constituents of Matter

Among fermions, the fundamental constituents of the matter with non-integer spin, the leptons and the quarks can be distinguished. They present a definite structure of twelve particles (six leptons and six quarks) with their antiparticle counterparts and are classified in three families, the so called generations (see Table 1.1).

	1st Generation	2nd Generation	3rd Generation
Quarks	u *up* d *down*	c *charm* s *strange*	t *top* b *bottom*
Leptons	ν_e *electron neutrino* e *electron*	ν_μ *muon neutrino* μ *muon*	ν_τ *tau neutrino* τ *tau*

Table 1.1: Organization of fundamental fermions.

Leptons and quarks form two different groups of particles. The main difference between them is that quarks unlike the leptons reacts in strong interactions. Other characteristics of quarks and leptons are:

- Each quark carries one of three color charges: red, green or blue. This color charge enables them to feel the strong force.
- The up-type quarks (up, charm and top) carry an electric charge of +2/3, and the down-type quarks (down, strange and bottom) carry an electric charge of –1/3, enabling both types to participate in electromagnetic interactions.
- Leptons do not carry any color charge.
- The up–type leptons (the neutrinos) carry no electric charge. They are not participating in electromagnetic or strong interactions.
- The down-type leptons (electron, muon and tau) carry an electric charge of –1 so they are sensitive to electromagnetic field.
- Both quark and leptons feel the weak force.

Up to the present time, all stable matter is formed only from the quarks and leptons of the first generation.

1.1.2 Force-Mediating Particles

In the Standard Model all interactions are mediated by the exchange of particles. These particles are bosons, i.e. they have an integer spin. The different types of force-mediating particles are:

- **Photons** – massless particles which mediate the electromagnetic force between electrically charged particles.
- $\mathbf{W^+}$, $\mathbf{W^-}$ and $\mathbf{Z^0}$ **gauge bosons** – massive particles mediating the weak interaction between quarks and leptons.
- Eight **gluons** – massless particles responsible for the strong interactions. These particles can interact between themselves.

The Standard Model predicts also one boson that has not been observed yet. It is a so called *Higgs boson*, a hypothetical massive elementary particle playing a key role in explaining the origins of the mass of elementary particles. The search for this particle is very intensive, but the evidence for the existence of Higgs boson is indirect. It is expected that LHC will be able to confirm or to deny its reality.

1.1.3 The Limitations of the Standard Model

As already stated, the Standard Model is a successful description of particle physics, however, some weaknesses are still present. Firstly, it incorporates a rather high number (19) of free parameters. Furthermore, neither the gravitational force is included nor the origin of the mass is explained in the Standard Model – masses have to be determined experimentally. The observed difference between the presence of matter and antimatter in the universe cannot be explained by the Standard Model, either. However, despite of its drawbacks, the Standard Model remains the most accurate and experimentally proved theory in Particle Physics. On the other hand it is the major ambition of Particle Physics to detect effects unexplainable by the Standard Model.

1.2 B-meson System

The B-mesons are quark-antiquark bound states that contain one b-quark. Table 1.2 gives the masses and lifetimes of the different B-mesons.

If only the strong and the electromagnetic interactions were present, then the B_q^0 and the $\overline{B}_q^0$ where $q \in \{u, d, c, s\}$ would be stable. However, due to the presence of weak interactions, these mesons decay. The B_q^0 and the $\overline{B}_q^0$ can oscillate among themselves before decaying. This phenomena is known as mixing.

b-particle		Mass [MeV/c^2]	Lifetime [ps]
B_u^+	$(u\overline{b})$	5279.0 ± 0.5	1.638 ± 0.011
B_d^0	$(d\overline{b})$	5279.4 ± 0.5	1.530 ± 0.009
B_s^0	$(s\overline{b})$	5367.5 ± 1.8	1.466 ± 0.059
B_c^+	$(c\overline{b})$	6286.0 ± 5.0	0.460 ± 0.180

Table 1.2: Masses and lifetimes of different b-particles. Data taken from [1].

1.2.1 B-meson Mixing

Mixing is the process in which a neutral meson such as K^0, B_s^0 or B_d^0 oscillates from its particle state to its antiparticle state and vice versa. This is a second-order weak interaction illustrated in Figure 1.1 for the B-mesons where only the top quark contributes significantly to the $B_q^0 - \overline{B}_q^0$ mixing. Unlike in the case of kaon, the charm and the mixed top-charm contributions are here negligible.

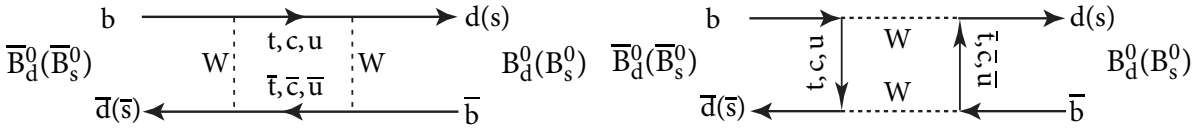


Figure 1.1: The Standard Model box diagrams which generate $B_q^0 - \overline{B}_q^0$ oscillations. Adapted from [2].

1.2.2 B-meson Decays

The B-mesons can decay either hadronically where the products are all hadrons, semi-leptonically where the weak boson converts to a lepton and neutrino or, very rarely, to a purely leptonic final state. For the SM description of CP violation the most important are non-leptonic B-meson decays. For CP violation studies of the quark sector, hadronic decays are the most relevant. These decays are based on the quark transitions $b \to q\overline{q}d(s)$ where $q \in \{u, d, c, s\}$. There are two categories: tree decays in which the b-quark decays by radiating a W boson which decays to a quark antiquark pair in the final state and decays involving quantum loops (so called penguin decays) in which massive, off-shell, non-SM particles may have influence on the observed products. These two categories of decays are illustrated on Figure 1.2 (tree diagram) and Figure 1.3 (penguin diagram).

1.3 The SM description of CP violation

The CP violation was firstly discovered in neutral kaon decays $K_L^0 \to \pi^+ + \pi^-$ in 1964. The Standard Model with three quark families can naturally generate CP violation in both weak and strong interactions even though the CP violation in strong interactions has never been observed.

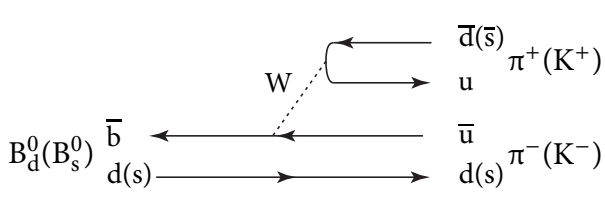


Figure 1.2: The tree diagram which generates $B^0_d \to \pi^+ + \pi^-$ and $B^0_s \to K^+ + K^-$. Adapted from [2].

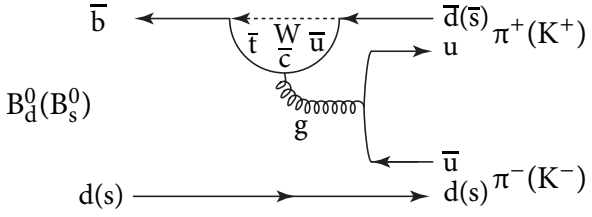


Figure 1.3: The penguin diagram which generates $B^0_d \to \pi^+ + \pi^-$ and $B^0_s \to K^+ + K^-$. Adapted from [2].

The CP violation in the weak interactions is generated by a single complex phase in the 3×3 unitary matrix known as the Cabibbo-Kobayashi-Maskawa (CKM) matrix.

Up to the present, all observed CP-violating phenomena have been consistent with the Standard Model. However, precision tests of CP violation physics is an interesting probe of physics beyond the SM because it is entirely reasonable to expect beyond the Standard Model physics to introduce new complex phases and hence additional CP violation effects.

As already mentioned, the Standard Model gives no answer to the domination of matter over antimatter in the universe, since the level of CP violation generated by the Standard Model is insufficient for the observed asymmetry.

It is then necessary to search for new sources of CP violation beyond the Standard Model. An excellent laboratory for beyond the SM searches is the B-meson system, in which many decay modes are available. Moreover, the Standard Model gives precise predictions concerning the number of these decays, therefore a precision measurements of such decays is of interest.

1.3.1 The CKM Matrix

The elements V_{ij} of the CKM matrix

$$\mathsf{V}_{\text{CKM}} = \begin{pmatrix} V_{\text{ud}} & V_{\text{us}} & V_{\text{ub}} \\ V_{\text{cd}} & V_{\text{cs}} & V_{\text{cb}} \\ V_{\text{td}} & V_{\text{ts}} & V_{\text{tb}} \end{pmatrix},$$

are related to the relative strengths of the transition of down-type quarks $j \in \{\text{d}, \text{s}, \text{b}\}$ to up-type quarks $i \in \{\text{u}, \text{c}, \text{t}\}$. A convenient parametrisation is that proposed by Wolfenstein [3], which expands the matrix in powers of the Cabibbo angle λ:

$$\mathsf{V}_{\text{CKM}} = \mathsf{V}^{(3)}_{\text{CKM}} + \delta\mathsf{V}_{\text{CKM}},$$

where the expansion up to the third order in λ is

$$\mathsf{V}^{(3)}_{\text{CKM}} = \begin{pmatrix} 1 - \lambda^2/2 & \lambda & A\lambda^3(\rho - \text{i}\eta) \\ -\lambda & 1 - \lambda^2/2 & A\lambda^2 \\ A\lambda^3(1 - \rho - \text{i}\eta) & -A\lambda^2 & 1 \end{pmatrix}.$$

The measurement of this angle is possible from decays involving s-quarks and the value is 0.2272 ± 0.0010 [1]. The series expansion is truncated at order $\mathcal{O}(\delta V_{\text{CKM}}) = \mathcal{O}(\lambda^4)$ which is sufficient for measurements at the B-factories. At LHCb, where a high statistics sample of B-meson decays will be recorded, a more accurate determination of the V_{CKM} matrix elements, including $\mathcal{O}(\lambda^5)$ corrections is required. These corrections are given by:

$$\delta V_{\text{CKM}} = \begin{pmatrix} -\lambda^4/8 & 0 & 0 \\ A^2\lambda^5\left[1-2(\rho+i\eta)\right]/2 & -\lambda^4(1+4A^2)/8 & 0 \\ A\lambda^5(\rho+i\eta)/2 & A\lambda^4\left[1-2(\rho+i\eta)\right]/2 & -A^2\lambda^4/2 \end{pmatrix} + \mathcal{O}(\lambda^6).$$

The unitarity of the CKM matrix is given by the following set of equations:

$$\sum_k V_{ki} V_{kj}^* = \delta_{ij},$$

where k indexes all the quarks. Six of the nine unitarity conditions of the CKM matrix can be drawn as triangles in the complex plane. The two triangles relevant for the B-meson systems are shown in Figure 1.4 (they become identical if δV_{CKM} is ignored). The related unitarity conditions are given by:

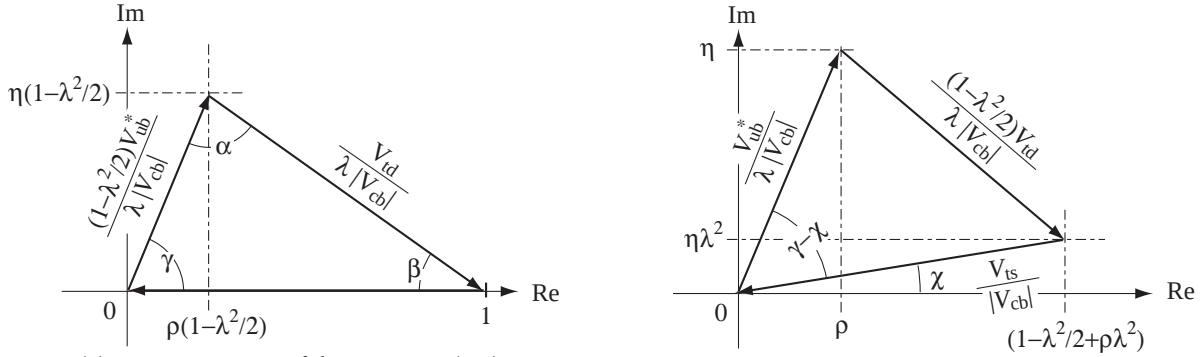
$$V_{\text{ud}} V_{\text{ub}}^* + V_{\text{cd}} V_{\text{cb}}^* + V_{\text{td}} V_{\text{tb}}^* = 0 \tag{1.1}$$

$$V_{\text{tb}} V_{\text{ub}}^* + V_{\text{ts}} V_{\text{us}}^* + V_{\text{td}} V_{\text{ud}}^* = 0. \tag{1.2}$$

The parametrization implies the relations between the angles of the unitarity triangles and the elements of the CKM matrix to be as follows:

$$\arg V_{\text{td}} \approx -\beta \qquad \arg V_{\text{ub}} \approx -\gamma \qquad \arg V_{\text{ts}} \approx \chi + \pi.$$

All other elements are real.



(a) Representation of the equation (1.1). (b) Representation of the equation (1.2).

Figure 1.4: Two unitarity triangles in the Wolfenstein's parameterization with an approximation valid up to $\mathcal{O}(\lambda^5)$. Taken from [2].

1.3.2 Measurement of the Unitarity Triangles Parameters

The angles of the triangles can be obtained either indirectly by measuring the lengths of the sides, or, within the Standard Model, directly from CP asymmetries. If the angles acquired by the two different methods will disagree, this would indicate a serious inconsistency with the present theory, opening a pathway to new physical model behind.

Since λ is well known, the two triangles are completely determined by ρ and η which can be derived from $|V_{cb}|$, $|V_{ub}|$ and $|V_{td}|$, as seen from Figure 1.4. Values of $|V_{cb}|$ and $|V_{ub}|$ are extracted from various B-meson decays while the ratio of $|V_{td}/V_{ts}|$ is derived from the frequency of B_s^0 – $\overline{B}_s^0$ oscillations.

The different angles of the unitarity triangles can be measured through specific decays:

- α: This angle can be determined directly in $B_d^0 \to \pi^+\pi^-$ decays or indirectly through the triangle relation $\alpha = \pi - \beta - \gamma$.
- β: The very active search for the New Physics is in the measurement of this angle in penguin decays like $B_d^0 \to J/\psi K_s^0$.
- γ: This angle can be measured in several ways. An important method at LHCb is to measure the time-dependent rates of $B_s^0 \to D_s^{\pm} K^{\mp}$ which give access to the $\gamma - 2\chi$ angle. Another possibility is to use $B_d^0 \to \pi^+\pi^-$ channel giving an information on the $\beta + \gamma$ angle. The γ angle can be also extracted from D^0– $\overline{D}^0$ mixing. This can be done by measuring the time-integrated decay rates for $B_d^0 \to D^0 K^{*0}$, $B_d^0 \to \overline{D}^0 K^{*0}$ and $B_d^0 \to D_{CP}^0 K^{*0}$ where $D_{CP}^0 = (D^0 + \overline{D}^0)/\sqrt{2}$ denotes the CP-even eigenstate of the D^0– $\overline{D}^0$ system
- χ: This angle is accessed through the $B_s^0 \to J/\psi\phi$ decay channel. In the Standard Model this angle is expected to be of the order of 10^{-2}, but any New Physics could, however, generate a large CP-violating effect in this decay channel.

As demonstrated above, B-mesons play a crucial role in the search for the New Physics. A highly accurate study of many decay modes serves as an excellent probe and gives an insight into properties of the New Physics.

The summary of the expected signal efficiencies for various decay channels at the LHCb as well as the annual signal yields are stated in Table 1.3.

The total signal efficiency is obtained as the fraction of events containing a signal B-decay that are triggered, reconstructed, and selected with offline cuts for physical analysis. It can be expressed as:

$$\varepsilon_{tot} = \varepsilon_{det} \times \varepsilon_{rec/det} \times \varepsilon_{sel/rec} \times \varepsilon_{trg/sel},$$

where ε_{det} is the detection efficiency, $\varepsilon_{rec/det}$ is the reconstruction efficiency on detected events, $\varepsilon_{sel/rec}$ is the efficiency of the offline selection cuts on the reconstructed events and $\varepsilon_{trg/sel}$ is the combined Level-0 and Level-1 trigger efficiency on offline-selected events. The high-level trigger, which is hoped to have a very high efficiency, is not considered here.

Decay channel	Factors [in %] forming ε_{tot} [in %]					Annual signal yield [10^3]
	ε_{det}	$\varepsilon_{rec/det}$	$\varepsilon_{sel/rec}$	$\varepsilon_{trg/sel}$	ε_{tot}	
$B_d^0 \to \pi^+ \pi^-$	12.2	91.6	18.3	33.6	0.688	26.00
$B_d^0 \to K^+ \pi^-$	12.2	92.0	25.2	33.2	0.940	135.00
$B_s^0 \to \pi^+ K^-$	12.0	92.1	13.5	36.7	0.548	5.30
$B_s^0 \to K^+ K^-$	12.0	92.5	28.6	31.1	0.988	37.00
$B_d^0 \to \rho \pi$	6.0	65.5	2.0	36.0	0.028	4.40
$B_d^0 \to D^{*-} \pi^+$	9.4	77.7	18.5	27.4	0.370	206.00
$B_d^0 \to \overline{D}^0 (K\pi) K^{*0}$	5.3	81.8	22.9	35.4	0.354	3.40
$B_d^0 \to D_{CP}^0 (KK) K^{*0}$	5.2	81.4	29.4	31.2	0.390	0.59
$B_s^0 \to D_s^- \pi^+$	5.4	80.6	25.0	31.1	0.337	80.00
$B_s^0 \to D_s^\pm K^\mp$	5.4	82.0	20.6	29.5	0.269	5.40
$B_d^0 \to J/\psi (\mu\mu) K_s^0$	6.5	66.5	53.5	60.5	1.390	216.00
$B_d^0 \to J/\psi (ee) K_s^0$	5.8	60.8	17.7	26.5	0.164	25.60
$B_d^0 \to J/\psi (\mu\mu) K^{*0}$	7.2	82.7	35.1	69.9	1.462	670.00
$B_d^+ \to J/\psi (\mu\mu) K^+$	11.9	89.6	44.8	68.7	3.280	1740.00
$B_s^0 \to J/\psi (\mu\mu) \phi$	7.6	82.5	41.6	64.0	1.672	100.00
$B_s^0 \to J/\psi (ee) \phi$	6.7	76.5	22.0	28.0	0.315	20.00
$B_s^0 \to J/\psi (\mu\mu) \eta$	10.1	69.6	10.1	64.8	0.461	7.00
$B_s^0 \to \eta_c \phi$	2.6	69.5	15.8	27.0	0.078	3.20
$B_s^0 \to \phi \phi$	6.7	79.7	37.9	23.2	0.470	1.20
$B_d^0 \to \mu^+ \mu^- K^{*0}$	7.2	82.4	16.1	73.5	0.704	4.40
$B_d^0 \to K^{*0} \gamma$	9.5	86.8	5.0	37.8	0.156	35.00
$B_s^0 \to \phi \gamma$	9.7	86.3	7.6	34.3	0.220	9.30
$B_c^+ \to J/\psi (\mu\mu) \pi^+$	11.5	89.3	20.7	60.8	1.300	14.00

Table 1.3: Individual channels of various B-mesons decays with their assumed detection efficiencies. The annual signal yields include both the indicated decays and their charge conjugates. Data taken from [2].

Chapter 2

The LHCb Experimental Apparatus at the LHC

The aim of this chapter is to give an overview over individual components of the LHCb detector. It begins with the description of the Large Hadron Collider, then the LHCb experiment and its subdetectors are introduced. In the conclusion the triggering and data acquisition system is outlined.

2.1 The Large Hadron Collider

The Large Hadron Collider is a two-ring, superconducting accelerator and collider built in the 27 km long LEP tunnel. It is constructed to deliver up to 14 TeV center of mass collision energies. Its main purpose is the search for the Higgs and SUSY particles (ATLAS and CMS), study of quark gluon plasma in Pb-Pb collisions (ALICE) and of CP violation and B-physics mainly in the frame of LHCb experiment. Possible effects of physics beyond the Standard Model as well as the measurements of total cross section, elastic scattering and diffractive processes (TOTEM) are also of interest.

In Figure 2.1 an overview of the whole LHC accelerator complex is shown and the locations of individual detectors using LHC beam are indicated. Acceleration of protons up to 50 MeV starts in the linear accelerator (Linac). The next accelerating stage is composed of two rings, a so called *Proton Synchrotron Booster* (PSB) which can boost the particles up to 1.4 GeV and *Proton Synchrotron* (PS) with the proton energy of 26 GeV before extraction. The final link in the injector chain for the LHC is the *Super Proton Synchrotron* (SPS), accelerating protons from the PS to 450 GeV.

2.1.1 Performance of the LHC

The number of events per second N_{ev} generated in the LHC collisions is given by:

$$N_{\text{ev}} = L\sigma_{\text{ev}} \tag{2.1}$$

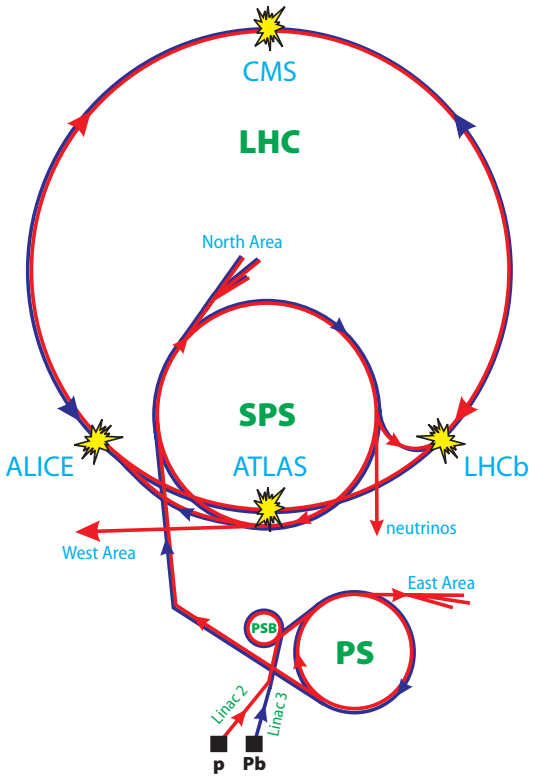


Figure 2.1: The LHC accelerator complex. The accelerating path for the protons and Pb ions is marked in red and blue respectively.

where L is the luminosity of the machine and σ_{ev} is the cross section for the event under study.

The machine luminosity depends only on the beam parameters and is expressed (for the Gaussian beam) as:

$$L = \frac{N^2 n_{\text{b}} f \gamma}{4\pi \varepsilon_n \beta^*} F \tag{2.2}$$

where N is the number of protons per bunch, n_{b} the number of bunches per beam, f the revolution frequency, γ the relativistic gamma factor, ε_n the normalized transverse beam emittance which characterizes the compactness and divergence of the bunches, β^* the beta function at the collision point which measures the ability of magnets to focus the beam at the *Interaction Point* (IP) and F the geometric luminosity reduction factor due to the crossing angle at the IP. The nominal values of chosen accelerator parameters are presented in Table 2.1.

There are two major experiments at the LHC demanding the highest possible luminosity. These are ATLAS and CMS aiming at peak luminosity of $L = 1.0 \times 10^{34}$ cm^{-2}s^{-1}. In addition to these high luminosity experiments there exist two others experiments that require low luminosity (for the proton operation of the LHC). One of them is the LHCb with peak luminosity of $L = 2.0 \times 10^{32}$ cm^{-2}s^{-1} and second is TOTEM ($L = 2 \times 10^{29}$ cm^{-2}s^{-1} with 156 bunches). Peak luminosity required by dedicated ion experiment ALICE is of $L = 1.0 \times 10^{27}$ cm^{-2}s^{-1} for nominal Pb-Pb ion operation with 600 bunches.

The high beam intensities implied by a luminosity of $L = 1.0 \times 10^{34}$ cm^{-2}s^{-1} exclude the

Parameter	Units	Injection	Collision
Proton energy	[GeV]	450	7000
Stored energy per beam	[MJ]	23.3	362
Circulating beam current	[A]	0.582	
Number of particles per bunch	[-]	1.15×10^{11}	
Number of bunches	[-]	2808	
Revolution frequency	[kHz]	11.245	
Synchrotron radiation power per ring	[W]	6.15×10^{-2}	3.6×10^{3}
Peak luminosity in IP_1 and IP_5	$[cm^{-2}s^{-1}]$	-	1.0×10^{34}
Geometric luminosity reduction factor F	[-]	-	0.836
Relativistic gamma factor γ	[-]	479.6	7461
Normalized transverse beam emittance ε_n	[µm]	3.5	3.75
Beta function at IP_1 and IP_5	[m]	18	0.55
Beta function at IP_2	[m]	10	0.5 for Pb
Beta function at IP_8	[m]	10	1–50

Table 2.1: Relevant LHC beam parameters for the peak luminosity and proton operation (data taken from [4]).

use of anti-proton beams and one common vacuum and magnet system for both circulating beams. To collide two beams of equally charged particles requires that opposite magnet dipole fields are excited in both beams. The LHC is therefore designed as a proton-proton collider with separate magnet fields and vacuum chambers in the main arcs and with common sections only at the insertion regions where the experimental detectors are located. The two beams share an approximately 130 m long common beam pipe along the *Interaction Regions* (IR). Together with the large number of bunches (2808 for each proton beam), and a nominal bunch spacing of 25 ns, the long common beam pipe implies 34 parasitic collision points for each experimental insertion region. Dedicated crossing angle orbit bumps separate the two LHC beams left and right from the central interaction point in order to avoid collisions at these parasitic collision points.

Since there is not enough room for two separate rings of magnets in the LEP tunnel, the LHC uses twin bore magnets which consist of two sets of coils and beam channels within the same mechanical structure and cryostat.

The peak beam energy in a storage ring depends on the integrated dipole field along the storage ring circumference. Aiming at peak beam energies of up to 7 TeV inside the existing LEP tunnel a peak dipole field of 8.33 T is required as well as the use of superconducting magnet technology operating at a temperature of 1.9 K.

2.2 The LHCb Detector

The LHCb detector is designed to study CP violation in the B-meson system and other rare phenomena using b-quark production at LHC. At LHC energies heavy quarks are mainly produced by gluon fusion (since proton is not an elementary particle almost all observed collisions are

essentially gluon-gluon fusion). Simulations of these processes shows that B-hadrons formed by both b and $\overline{\text{b}}$-quarks are predominantly produced in the same forward cone (see Figure 2.2). This particular polar angle distribution leads to the specific design of the LHCb detector.

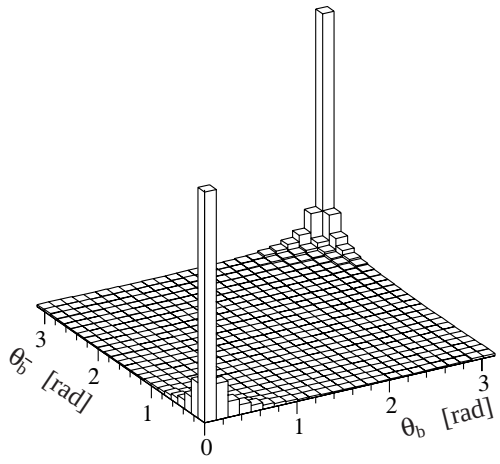


Figure 2.2: Polar angle θ of b and $\overline{\text{b}}$ hadrons directions at LHC. This picture is taken from [5].

The LHCb detector is, unlike the three other detectors at LHC, a forward single-arm spectrometer (only one of two possible directions is employed) and not a central detector. This geometry has several advantages. Among others it simplifies mechanical design and it allows more precise detection of the correlated $\text{b}\overline{\text{b}}$ production (without the need for expensive and complicated civil constructions as the whole detector is sitting in the existing experimental hall previously used by DELPHI experiment of the LEP era). On the other hand the specific topology of events under study leads to the high particle density in the narrow angle of the acceptance of the detector. Due to that fact one has to use radiation hard components in proximity of the Interaction Point.

To exploit all the advantages that this specific geometry offers, the experiment has to assure that only events in which b-quarks are present are selected (all the "uninteresting" events are efficiently filtered out). To achieve this objective several conditions has to be fulfilled.

First of all a high performance trigger is needed. To make the trigger decision easier the beam luminosity is to be locally decreased so the probability of multiple interactions per bunch crossing (each 25 ns) is minimal, i.e. there is only one "interesting event" every 25 ns in average. The luminosity needed by LHCb is about 2.0×10^{32} cm^{-2}s^{-1}. To identify B-mesons and to measure their lifetime accurately, the primary and especially the displaced secondary vertex (which is a distinctive characteristic of b-hadron decays) coordinates have to be determined with the best possible precision. This is a task for the *Vertex Locator* (VELO) solid-state detector. The momentum information of charged particles will be reconstructed by the magnetic spectrometer composed of dipole magnet and tracking detectors. Particle identification is based on RICH detectors. The LHCb detector has also electromagnetic and hadronic calorimeters together with muon chambers for the measurement of energy. In the following sections the individual subsystems of the LHCb (except for VELO to which the whole chapter 3 is dedicated) are described more in detail.

The overall schematic of the LHCb detector is shown in Figure 2.3. It's about 20 m long and

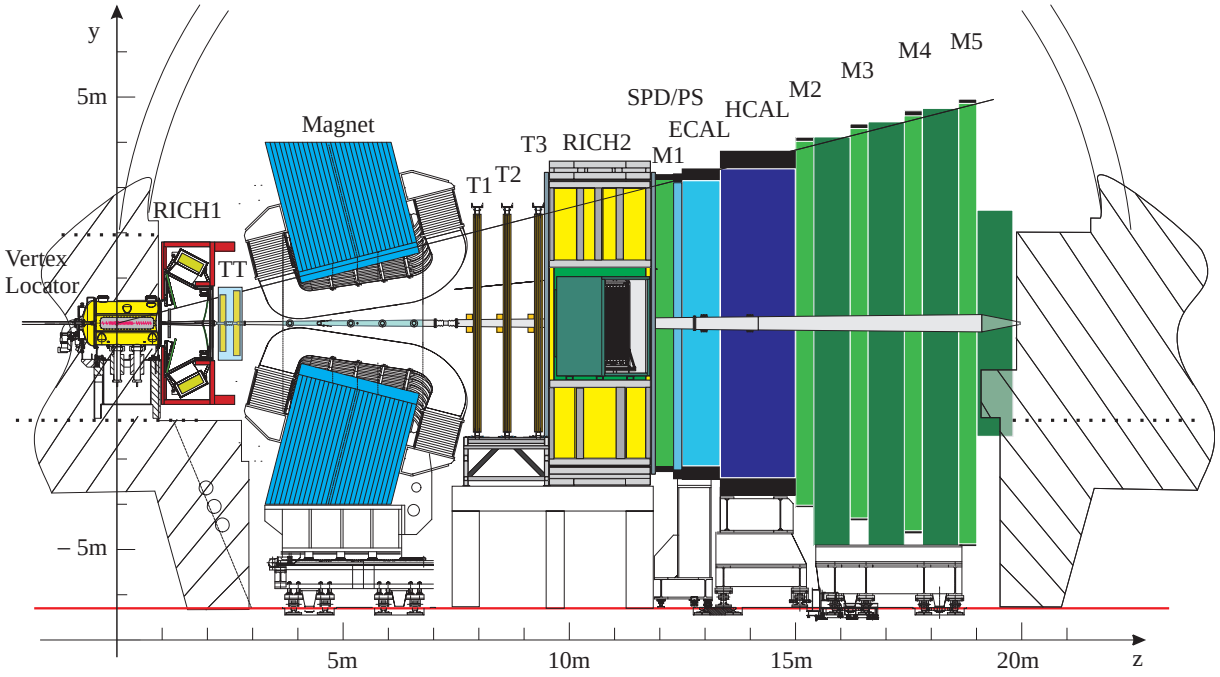


Figure 2.3: Side view of the LHCb detector (non-bending plane). This Figure is taken from [2].

10 m wide. The polar angle coverage around the direction of the proton beams ranges from 10 mrad to 300 (250) mrad in the bending (non-bending) plane.

2.3 The Subdetectors of LHCb

The subdetectors of the LHCb detector can be divided into two groups according their purpose.

- **The tracking system** which consist of
  - *Vertex Locator* (VELO) silicon detector which is used for the reconstruction of vertices and also as the event trigger.
  - *Trackers and dipole magnet* providing information on the trajectories of charged particles so that the track momenta can be determined.
- **The particle identification system** comprises
  - *Ring Imaging Čerenkov detectors* (RICH) that play an important role in particle identification by the separation of pions and kaons.
  - *Electromagnetic and hadronic calorimeters* (ECAL and HCAL), which measure total energy of high momenta electrons, photons and hadrons and are as well used to trigger on $b\bar{b}$-events.
  - *Muon chambers* serving to identify muons for the trigger and to tag the b-flavor.

2.3.1 The Magnet

A dipole magnet with normal aluminum conductor of 50 t and with 1450 t heavy steel yoke has a bending power of 4 Tm with a maximal field strength of 1.1 T. To reduce the power dissipation to about 4.2 MW, the pole faces are shaped to follow the acceptance angles of the experiment. The aperture is of ±300 mrad horizontally (bending plane) and ±250 mrad vertically (non-bending plane).

The polarity of the field can be changed to reduce systematic errors in the CP violation measurements that could result from a left-right symmetry of the detector. Magnetic field penetrate the upstream part of the detector in such a way to allow a rough momentum analysis at the early stage of the triggering process.

The magnet already assembled in the pit can be seen in Figure 2.4.

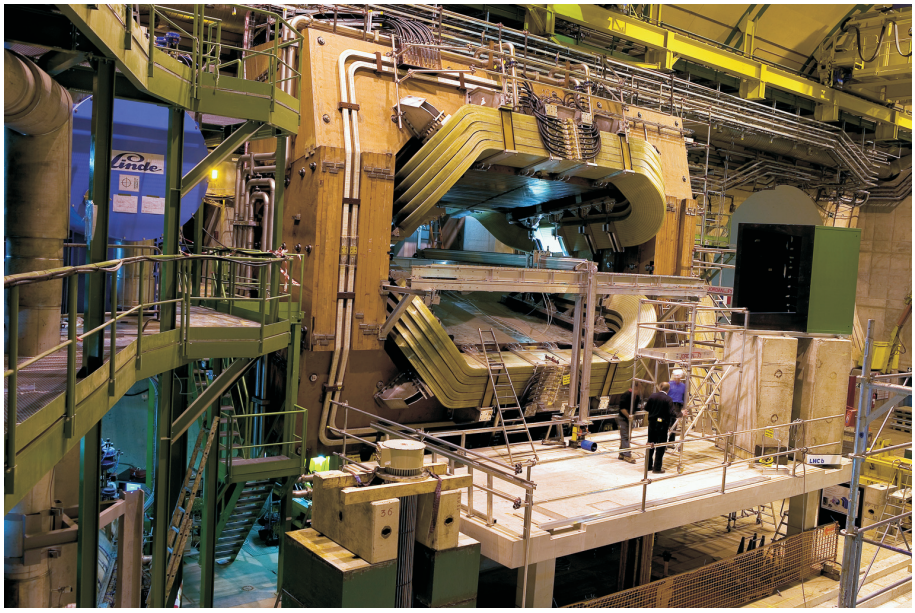


Figure 2.4: The LHCb magnet with surrounding iron yoke in the pit. This picture is taken from [6].

2.3.2 The Trackers

The main goal of the tracking system is to provide the momentum measurement of charged particles with a relative particle momentum resolution of ~ 0.4 % for every charged particle issued from a B-decay. The main tracking system consist of four stations. These are (see Figure 2.3):

- **The Trigger Tracker** (TT) located between the RICH1 and the magnet.
- **Three Tracking Stations** (T_1 to T_3) located between the magnet and the RICH2.

The Trigger Tracker is a microstrip silicon detector while the Tracking Stations are divided into two parts. The central part around the beam pipe, which represents only 2 % of the total area of the Tracking Stations (but receives roughly 20 % of the particle flux), is made of microstrip Si detectors. The outer part called the Outer Tracker uses drift straw tubes.

The Trigger Tracker

The Trigger Tracker station fulfills a two-fold purpose. First, it is used in the Level-1 trigger to assign transverse momentum information to the tracks (using the fringe field of the magnet). Second, in the offline analysis the trajectories of low-momentum particles that are bent out of the detector acceptance in the field of the magnet (they never reach Tracking Stations T_1 to T_3) and trajectories of long lived neutral particles that decay outside the volume of the VELO are reconstructed using the TT station.

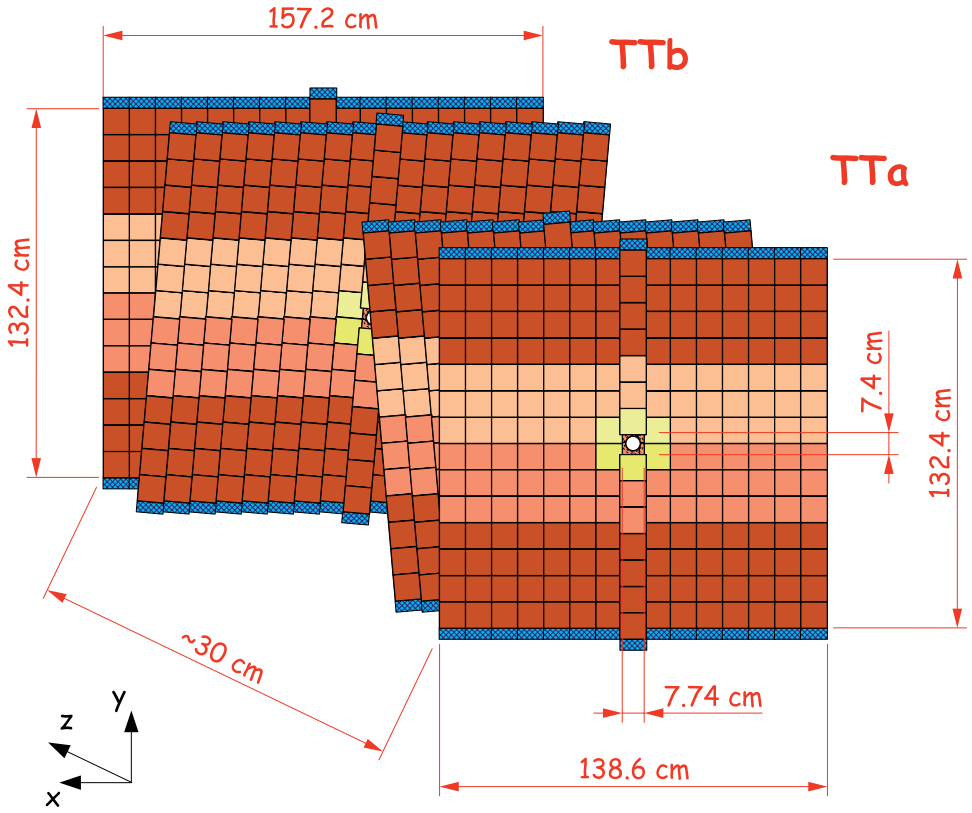


Figure 2.5: Front view of the LHCb Trigger Tracker modules. This Figure is issued from [7].

The TT station is made of four plates of silicon strip sensors with a strip pitch of 183 µm covering a rectangular area of approximately 130 cm in height and 160 cm in width. The 1st and 4th plane have vertical strips while the 2nd and 3rd plate have a stereo angle of +5° and −5° respectively (see Figure 2.5). To reduce the leakage current the detector is operated at about 5 °C.

The Inner Tracker

As was previously stated, the Inner Tracker is based on silicon strip detectors covering the area around the beam pipe. It uses the same sandwich architecture as the TT (each station has four detection layers – two inner layers with stereo angle) with up to 22 cm long strips of pitch about 198 µm (see Figure 2.6). The overall dimensions of the Inner Tracker are 120 cm in width and 40 cm in height. All stations are located just in front of their neighboring Outer Trackers stations allowing an overlap of about 1 cm.

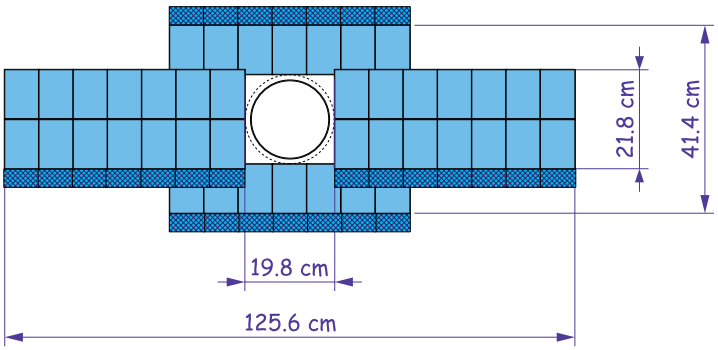


Figure 2.6: The layout of the Inner Tracker module with the straight strips (no stereo angle). This Figure is issued from [7].

The Outer Tracker

The Outer Tracker detects the tracks which have a radial angle larger than 15 mrad. They are based on gas drift chambers filled with the mixture of Ar(75 %) – CF_4(15 %) – CO_2(10 %).

The Outer Tracker is made of drift cells – straw tubes – with an anode in the middle. The radius of these tubes is limited to 5 mm due to the maximum required drift time of 50 ns. This time corresponds exactly to two bunch crossings so it can happen that two events are piled-up.

The stations are made again of four layers of vertical modules where the inner layers have stereo angle of ±5°. The readout electronic is placed at the tubes end outside the acceptance.

2.3.3 The RICH

Ring Imaging Čerenkov detectors allow the hadron identification in LHCb (pions and kaons). They allow a separation of hadrons in the momentum range of 1–100 GeV/c. This wide range of momentum scale cannot be covered by a single detector so two RICH detectors are used in LHCb, RICH1 and RICH2. The RICH1 detector located between the VELO detector and the Trigger Tracker is able to identify low-to-intermediate momentum tracks (1–60 GeV/c) while the RICH2 (positioned between T_3 station and first muon chamber) is designed to cover the momentum range up to 100 GeV/c.

The RICH counters detect ring images formed by Čerenkov photons emitted along the track of a charged particle traversing the detector. From the measurement of the radii of detected rings, the separation of particles of different masses is possible providing the information of the momentum by the tracking system. As radiators, three different materials are used:

- Silica aerogel for low momentum particles (RICH1).
- C_4F_{10} for intermediate momentum particles (RICH1).
- CF_4 for high momentum particles (RICH2).

The architecture of both RICH1 and RICH2 detectors is shown in Figures 2.7, 2.8.

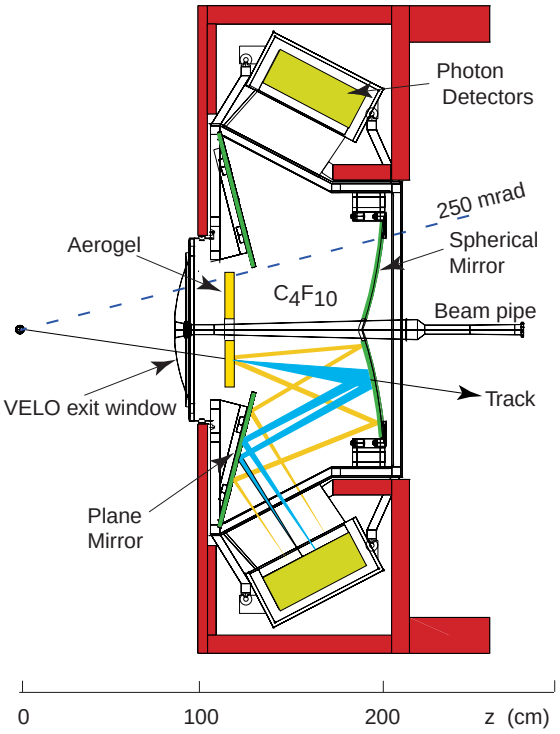


Figure 2.7: Layout of the RICH1 detector in the vertical plane (non-bending). Figure issued from [2].

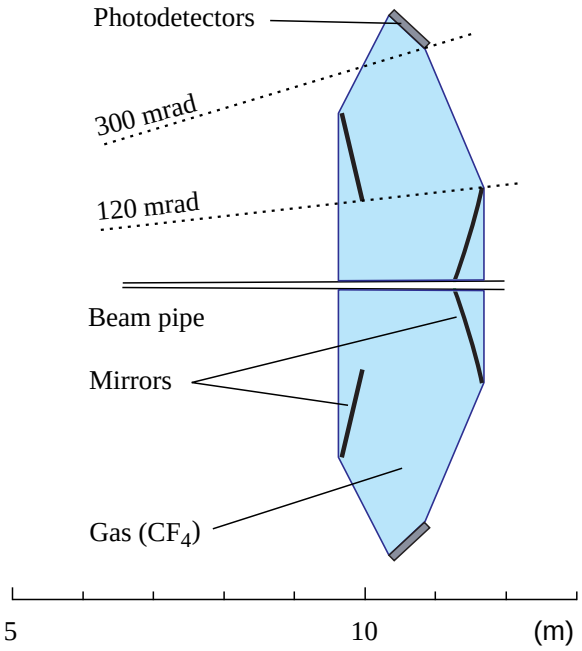


Figure 2.8: Layout of the RICH2 detector in the horizontal plane (bending). Figure issued from [5].

2.3.4 The Calorimeters

The main task of the calorimeters is to detect and measure the total energy of photons, electrons and hadrons with sufficiently high momenta (so that they are not separated by the magnet). The information of the single-particle energy is provided as the input to the Level-0 trigger. The calorimeters are also used as the initial part of the muon filter system. Since the calorimeters are used in the Level-0 trigger the acquisition of the data is taken every 25 ns. The whole calorimetric system consists of four parts (see Figure 2.3).

- **Scintillator Pad Detector**: The main purpose of the SPD is to distinguish between charged and neutral particles (electrons and photons). If there is no signal in the PSD in front of the ECAL cluster, the particle is photon and vice-versa. The SPD is located in front of a 12 mm (two radiation lengths[1]) lead converter.

- **Pre-Shower**: This subdetector allows to separate electrons from pions by the topology of electromagnetic showers subsequently measured in the ECAL. It's located just after the 12 mm thick lead converter. The electron/pion separation is based on the fact that electrons produce a shower that starts in the lead absorber with a bulk of secondary particles leaving the lead and reaching the scintillator, thus inducing a signal that is much larger than a typical signal from a charged pion.

- **Electromagnetic Calorimeter**: The aim of the ECAL is to measure the energy of electrons and photons and provide information for π^0 reconstruction. The LHCb Electromagnetic Calorimeter is built of individual modules that are made of 66 lead absorber plates (2 mm thick) interspaced with scintillator tiles (4 mm in thickness) as an active material. The overall thickness of the ECAL corresponds to 25 radiation lengths.

- **Hadronic Calorimeter**: The HCAL provides data for the Level-0 hadron trigger. It is a sampling device made of steel as the absorber and scintillator as the active material. The special feature of this sampling structure is the orientation of the scintillating tiles that is parallel to the beam axis. The total thickness of the HCAL is 1.2 meters which corresponds to 5.6 interaction lengths[2]

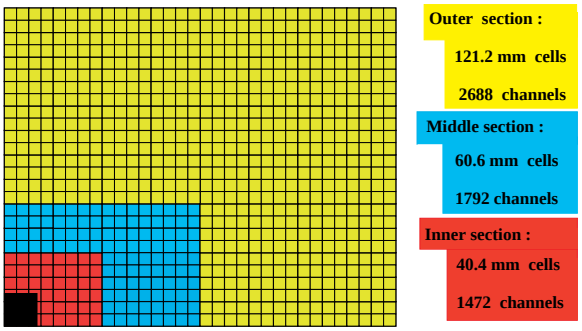


Figure 2.9: Transverse segmentation of the SPD, PS and ECAL cells. Only one quarter of the detector front face is shown. Figure taken from [8].

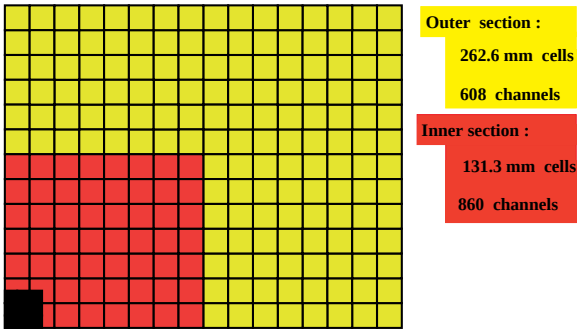


Figure 2.10: Transverse segmentation of the HCAL cells. Only one quarter of the detector front face is shown. Figure taken from [8].

All the modules of the LHCb calorimetric system are divided into regions with different cell sizes. First three detectors have their cells gathered in three areas (inner, middle and outer) as shown on Figure 2.9. The Hadronic Calorimeter is made only of two regions (see Figure 2.10).

[1]The radiation length of a material is defined as the distance over which the electron energy is reduced by the factor 1/e due to the radiation loss only.

[2]The interaction length of a material is defined as the distance at what a particle undergo an interaction that is neither elastic nor quasi-elastic.

2.3.5 The Muon Detector

Muon triggering and offline muon identification are fundamental requirements to the LHCb experiment, since muons are present in several final states of B-decays sensitive to CP violation. Moreover, muons will provide a clean identification of the B-flavor through its semi-leptonic decay. The muon trigger is designed in such a way that information from all five muon chamber is required.

The Muon Detector system consists of five stations (M_1 to M_5) covering the acceptance of ±300 mrad horizontally and ±200 mrad vertically. The first detector (M_1) is placed in front of the SPD-PS block, stations M_2 to M_5 are located behind the HCAL. They are separated by a 800 mm thick iron filters. The whole absorber block (including the calorimeters) has a thickness of approximately 20 interaction lengths. Each station is divided into four regions with increasing distance from the beam axis (see Figure 2.11). The granularity of the readout is finer in the horizontal plane, in order to give an accurate measurement of the track momentum.

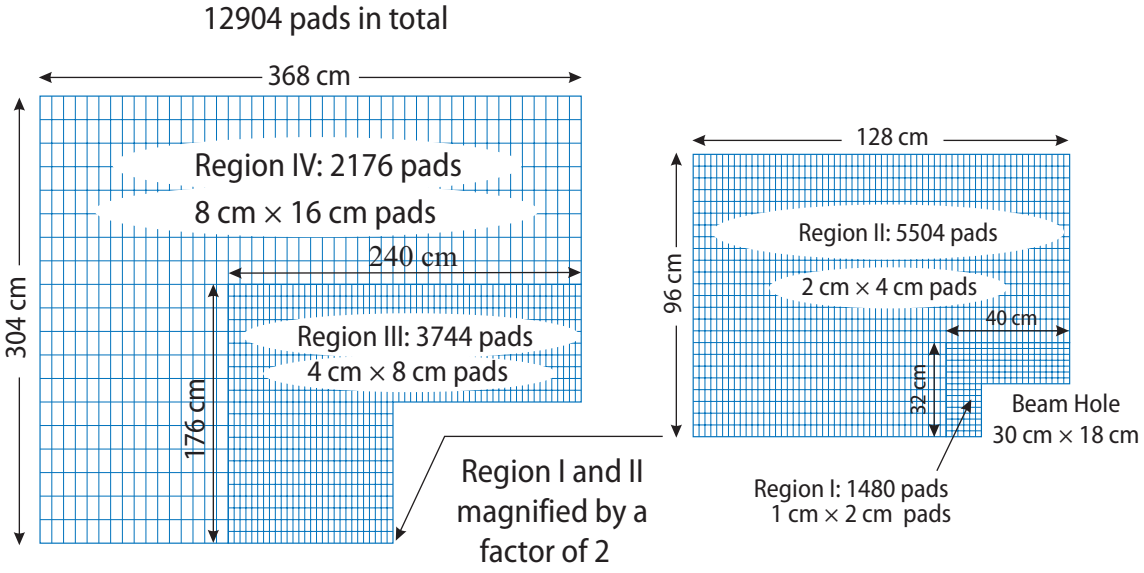


Figure 2.11: Configuration of the M_1 regions.

Since the Muon Detector is part of the Level-0 trigger system (40 MHz), the detectors are optimized for a high speed data acquisition. For the innermost region of the M_1 module which has to sustain a high particle flux, Triple-GEM[3] detectors are used. For all remaining regions Multi Wire Proportional Chambers were chosen with 2 mm wire spacing and a small gas gap of 5 mm.

[3]The triple-GEM is a multi-step gas avalanche detector that exhibits a high rate capability with a time resolution below 10 ns

2.4 Triggering and Data Acquisition at LHCb

Trigger and data acquisition systems in high energy physics have grown to powerful processing and high bandwidth data networks. In Figure 2.12 an overview of achieved throughput in trigger systems in various high energy physics experiments is given.

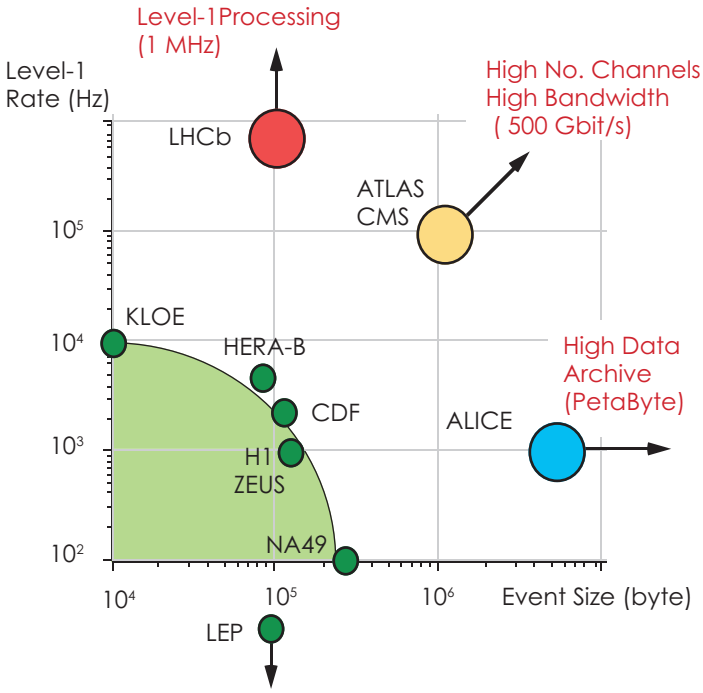


Figure 2.12: Level-1 rate (before the L1 trigger) of the data processing versus the event size of the various high energy physics experiments. This Figure is issued from [9].

Trigger systems for high energy physics detectors select events according to a trigger logic derived from the physical processes under study. Fast rejection (low latency) is essential since the information from all detector channels need to be buffered. High overall rejection is achieved by progressive filtration of the data at each stage reducing the data rate after the trigger selection, therefore, more and more powerful computational techniques can be used at higher trigger levels.

A brief description of both trigger and data acquisition systems of the LHCb is given in the following sections.

2.4.1 Trigger

With the given LHC bunch density and locally reduced luminosity at LHCb the data flow from the detectors generated by p-p interactions exceeds by far the potential of the acquisition system (even not all reconstructible B-meson events can be registered). It is required to reduce the data flow to an acceptable limit (200 events/s) by selecting the most interesting events.

The LHCb detector has about one million readout channels. At a bunch crossing frequency of 40 MHz this corresponds to a data flow of 40 TB/s whereas only 200 MB/s can be stored. The data reduction must be at least of order 10^5. Due to small cross-section of $b\bar{b}$ pair production compared to the inelastic scattering of protons only a small fraction of bunch crossings give birth to "interesting" events. The expected $b\bar{b}$ pair production rate is 100 kHz from which only 15 % of the events will have one B-meson with its decay products in the acceptance of the detector. Among these events only a small fraction ($\sim 10^{-3}$) is relevant for the CP violation studies. In principle the high initial data rate (bunch crossing every 25 ns) has to be reduced to a usable event rate of the order of several events per second.

For this purpose the LHCb detector features a multi-level trigger system, based on calorimeter and muon systems at the Level-0 trigger (L0), on displaced vertices at the Level-1 (L1) and on a complete event reconstruction at the last High Level Trigger (HLT).

Level-0 Trigger

The first reduction of the data stream is performed by the Level-0 trigger which reduce the event rate from the initial 40 MHz down to the rate of 1 MHz at which all subdetectors except for RICH can contribute to the next trigger level. The L0 trigger exploits for the decision the relatively high transverse momentum or energy of the B-decay products that are leptons, hadrons or photons. Four triggers run in parallel for the search of electrons, photons, hadrons and muons with the highest energy or momentum. The first three use raw calorimeter informations while the last one takes the data from the Muon Detector. The Level-0 trigger is looking for:

- The highest energy electron, photon and hadron clusters in the calorimeters.
- The two highest momentum muons in the Muon Chambers.

At this trigger level one special component for rejecting multiple events per bunch crossing is used. It is a *Pile-Up Veto* that detects primary vertices using the VELO sensors placed on the other side of the interaction point. As a relatively large fraction ($\sim 40\,\%$) of the bunch crossings create more than one p-p interaction and as these events are preferably selected by the triggers (due to the *pile-up* effect), they have to be removed (by a detection of multiple primary vertices).

The final decision is taken by the L0 Decision Unit which combines all the informations from the subtriggers. The maximum delay of the L0 trigger decision is set to 4.2 μs which corresponds to 168 events. It implies that for the Level-0 trigger a minimum buffer of 168 events has to be used for each subdetector.

Level-1 Trigger

The second trigger level, Level-1, reduces the event rate from 1 MHz down to 40 kHz. It uses the information of the VELO and TT subdetectors and matches them to the previously selected

events by the Level-0 trigger. It also measures momenta of the tracks with the help of the fringe field of the magnet. Events are selected according to their momenta while the events with high impact parameters with respect to the primary vertex position (calculated independently) are preferred. The Level-1 trigger is a software-based trigger (as well as the HLT) and is executed on the 1800 nodes CPU farm located in the counting room (radiation protected environment). Its latency is about 50 ms.

High Level Trigger

The HLT trigger takes all the subdetectors data (except for RICH). In the first step it recalculates the VELO tracks and primary vertex with better precision. A fast pattern recognition algorithm then links the VELO tracks to the TT and then to the tracking stations T_1–T_3. In second step a set of selection cuts dedicated to specific final states is applied. The HLT has the latency of 200 ms and reduces the event rate from 40 kHz to 200 Hz. At this frequency the events are fully reconstructed and the particle identification from the RICH is applied. The events selected by the HLT are then stored for the off-line analysis.

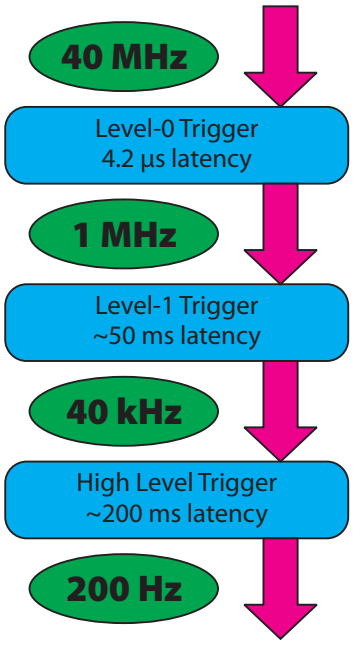


Figure 2.13: The LHCb trigger dataflow diagram.

2.4.2 Data Acquisition

The data acquisition systems in the high energy physics experiments are generally very demanding in terms of event rate, data bandwidth and resistance to radiation. The DAQ system at LHCb is not an exception. In the proximity of detectors the radiation level is high, therefore one is trying to minimize the amount of electronics which has to be placed close to the detector. At the LHCb

experiment the data are sent over long cables to the counting rooms where further processing takes place.

The data acquisition system at LHCb is implemented as a multi-level system following the hierarchy of different trigger levels (see Figure 2.13). Before the positive decision of the corresponding trigger the data must be stored in the buffers for the whole trigger latency. The general architecture for each trigger level electronics is as follows: it consists of a buffer with a correct length defined by the appropriate trigger latency, an interface to receive the trigger decision signal and the output stage. On the top level, the set of elements is controlled by the processing logic.

To distribute the system clock, the trigger decisions, resets and special commands to all components of the LHCb DAQ system, the dedicated *Timing and Fast Control* (TFC) network is used. This network is driven by the *Readout Supervisor* which is responsible for scheduling the trigger decisions in order to avoid *the buffer overflow* effects. This is done by the throttle control of the Level-0 trigger when the trigger rate becomes dangerously large.

The DAQ system incorporates also the *Experiment Control System* (ECS) which monitors and controls the operational state of the LHCb detector and the associated experimental equipment such as high voltages, readout electronics, etc.

Chapter 3

Subdetector VELO

This part deals in more detail with the VELO subdetector. The overall concept as well as the individual building blocks of the VELO are described. The working principle of the VELO electronics is presented with emphasis given on those parts which are essential for further reading.

3.1 Overview of the VELO Subdetector

Vertex reconstruction is a fundamental requirement for the LHCb experiment. The Vertex Locator subdetector has to provide precise measurements of track coordinates close to the interaction region within the LHCb acceptance $1.6 < \eta < 4.9$, where η is the pseudo-rapidity[1]. The measured coordinates are used to reconstruct the production and decay vertices of hadrons and to provide an accurate measurement of their decay lifetimes. The VELO data are also a vital input to the second and third level trigger (Level-1 and HLT), informing the acquisition system about possible displaced vertices which are a signature of the B-mesons in the event.

The VELO features a series of silicon stations placed along the beam direction. They are positioned at a radial distance from the beam which is smaller than the aperture required by the LHC during injection and therefore must be retractable. This is achieved by mounting the detectors in a setup similar to Roman pots (see Figure 3.1).

The required performance of the VELO demands positioning of the sensitive area of the detectors as close as possible to the beams and with a minimum amount of material in the detector acceptance. The placement of the sensors close to the beam is allowed by the forward detector geometry. This also means that the detectors have to operate in an extreme radiation environment. For this reason almost all the processing electronics is placed in the shielded

[1]The pseudo-rapidity η is a quantity used to approximate the rapidity when the mass and the momentum of a particle are not known. It is defined via the angle θ between the particle momentum and the beam axis, as $\eta = -\ln[\tan(\theta/2)]$, so $\eta = 1.6$ corresponds to the angle of 400 mrad and $\eta = 4.9$ to the angle of 15 mrad.

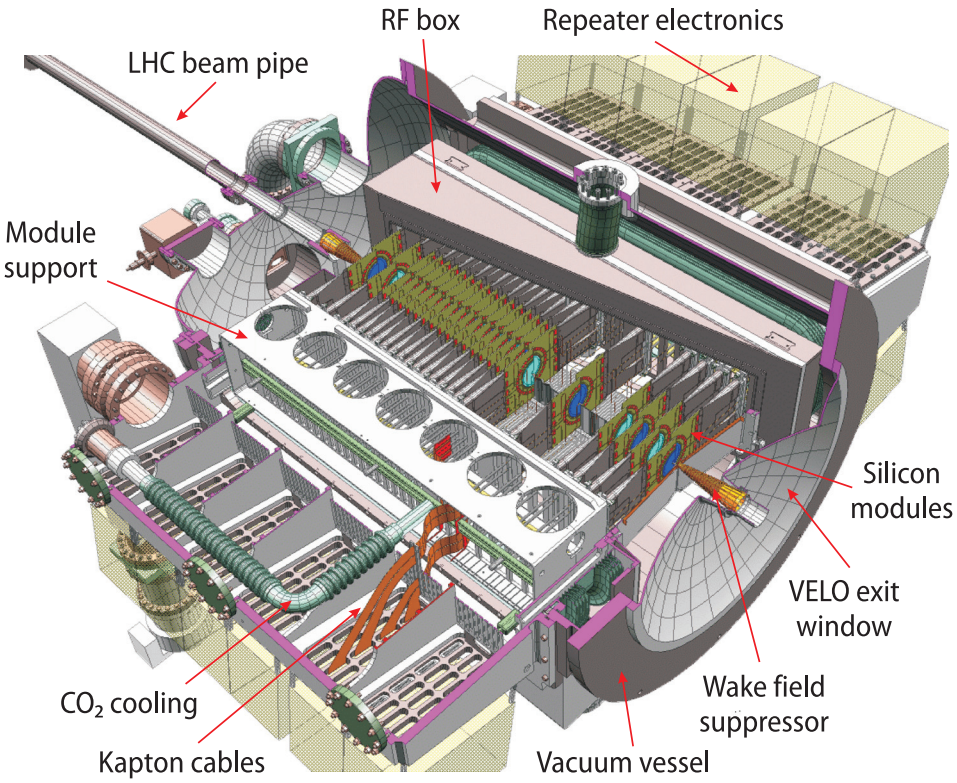


Figure 3.1: The VELO.

counting room. Only the necessary monitoring and repeater electronics is placed in proximity of the VELO.

Figure 3.2 represents the layout of the VELO and the pile-up veto stations. The VELO consists of 21 silicon disk-shaped stations placed along the beam direction. Each station is made of two planes of sensors, measuring the radial and the angular components of all tracks. Apart from covering the full LHCb forward angular acceptance, the VELO also has a partial coverage of the backward hemisphere to improve the primary vertex measurement. To facilitate the task of the Level-0 trigger to select events with only one p-p interaction per bunch crossing, two additional R sensors are placed upstream of the VELO stations forming the pile-up veto stations.

In order to minimize the amount of material close to the beam to avoid any unwanted interactions, the VELO is operating in the vacuum. To protect the primary LHC vacuum, the detector modules are placed in the secondary vacuum container separated by a 0.3 mm thin aluminum foil (see Figure 3.4). This aluminum structure also acts as a wake field[2] suppressor and shields the detector modules from the high-frequency fields of the LHC beams.

The VELO subdetector uses two types of silicon strip sensors, R and Φ, to measure the radial and the angular coordinates of the tracks (see Figure 3.3). The inner active radius of both sensors is limited to 8 mm due to the LHC machine constraints and the outer radius of 42 mm is imposed

[2]Wake fields, generated by a moving particle in the accelerator pipe and objects such as RF cavities, affect the motion of particles in the tail part of the beam causing the parasitic loss, beam energy spread, instabilities and electromagnetic interference.

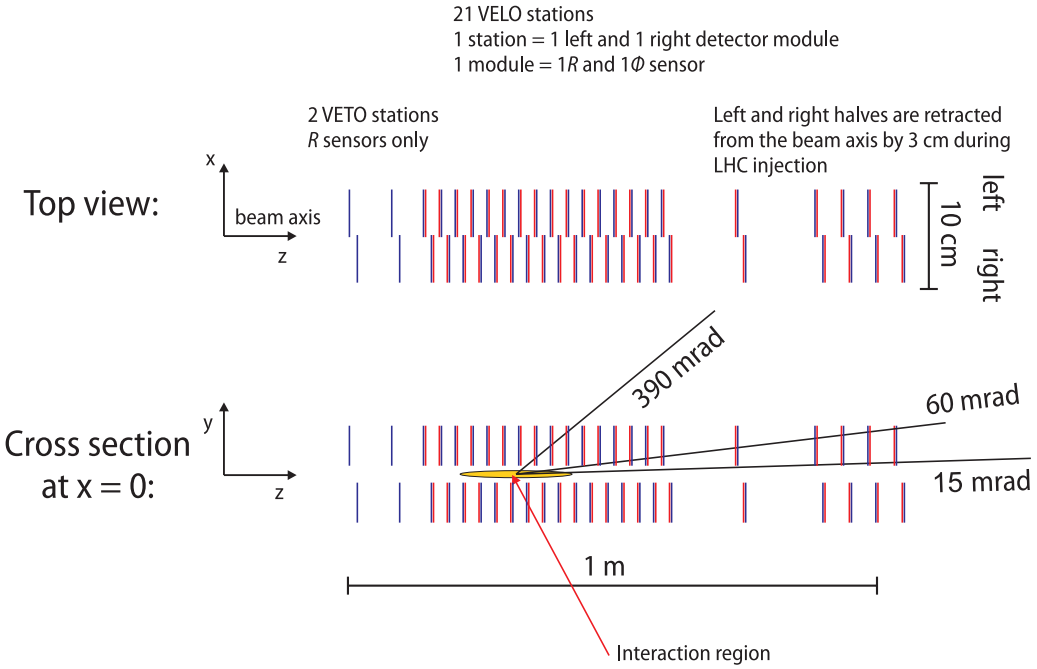


Figure 3.2: Arrangement of the VELO detectors along the beam axis. Picture adapted from [10].

by the magnet acceptance. The both sensors are made from 300 µm thick n-on-n single sided silicon wafers and span 182°.

3.1.1 Detector Cooling System

Cooling of the detector modules is highly required since the sensors operate in vacuum and high positioning accuracy of the detector is required. For this reason the temperature gradients should be minimal to avoid heat dilatation. Silicon detectors will be operated in the adjustable temperature range from −25 °C to +10 °C while the temperature of the electronic components is kept below 40 °C.

The total heat produced in the whole detector reaches 1.2 kW so the required cooling capacity is about 2.5 kW. The cooling system must be radiation resistant and the amount of material around the detector should be minimized in order to limit the undesired production of background. A mixed-phase CO_2 cooling system is used for the VELO detector. Besides being an adequate coolant for applications in high radiation environments (no free radicals and toxic compounds are expected to be produced in the high-radiation environment of the VELO detector), CO_2 exhibits excellent cooling properties.

The CO_2 is supplied as a liquid and expanded into a number of stainless steel capillaries via flow restrictions. The capillaries and flow restrictions are vacuum-brazed to a manifold that is attached to the detector modules by an aluminum coupler and a soft metal indium joint. A carbon-fiber substrate of the modules provides a mechanical and thermal link to the sensors.

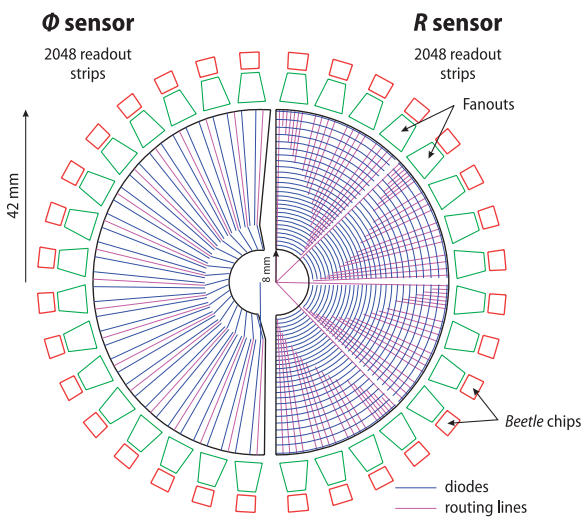


Figure 3.3: Schematic view of the R and Φ silicon sensors with adjacent *Beetle* chips. The R sensor has azimuthal strips at constant radius, whereas a Φ sensor has radial strips with a stereo angle between 10° and 20°. Figure taken from [10].

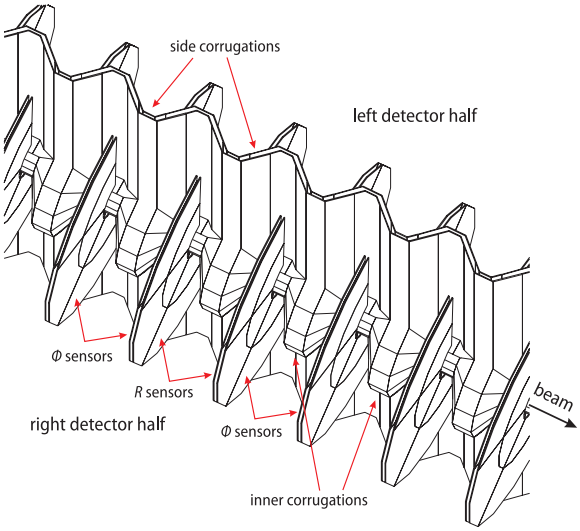


Figure 3.4: Close-up of the secondary vacuum container showing the position of the silicon sensors. The corrugations close to the beam axis are needed to minimize the material seen by tracks before the first measured point. Figure taken from [10].

3.2 Architecture of the VELO Modules

The VELO module consists of three main parts, the silicon sensor, the hybrid and the paddle, and serves it a three-ply purpose.

- It provides the mechanical infrastructure to support the sensors rigidly, stably and in a defined position.
- It acts as a base on which the electronic readout for the sensor can be mounted.
- It allows the heat removal from the front-end chips and sensor.

The module is designed to allow for precision alignment of the sensors relative to the platform on which all modules are mounted. Also the thermal properties of the modules are vital to control the operating temperature of the sensors, so the carbon fiber material is used to provide mechanical and thermal link to the sensors.

3.2.1 The Hybrid

The hybrid is shown on Figure 3.5. It is a part of the VELO module that provides a support for the 2×16 front-end chips – *The Beetles* – and two silicon sensors. Again, very good thermal and

mechanical properties of hybrids are required. All the chips are bonded to the hybrids so apart from providing the electronic support to the chips, hybrids also have to act as heat conductors. Furthermore, a low mass design is required, because most of the hybrids are within the LHCb acceptance.

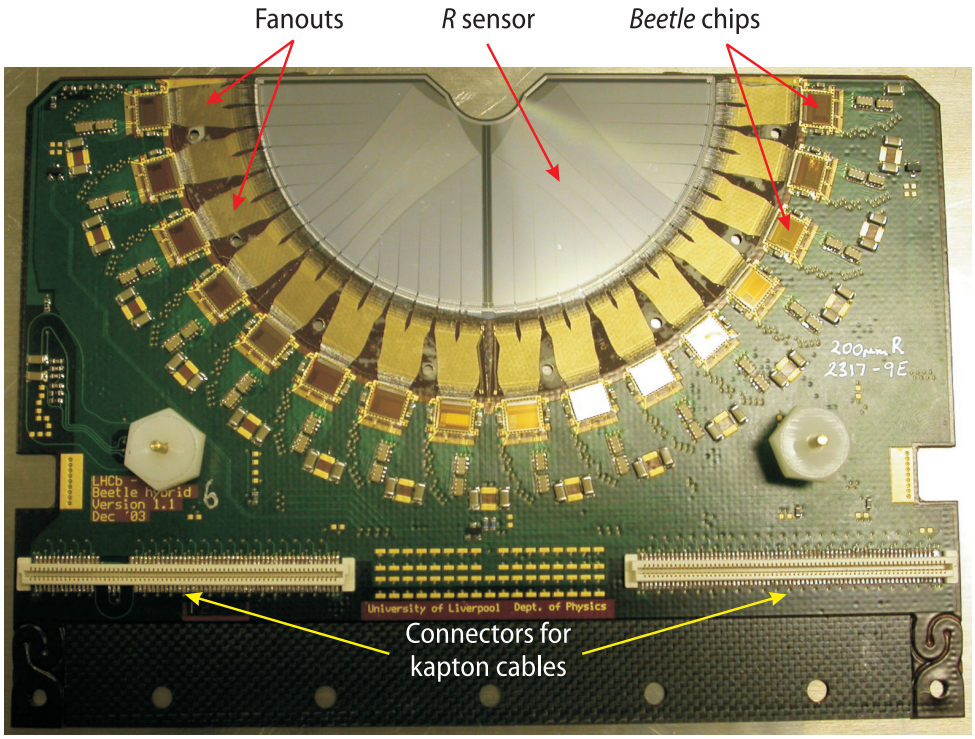


Figure 3.5: View of the fully equipped *R*-side VELO hybrid including 16 *Beetle* front-end chips. Picture taken from [6].

3.2.2 Silicon Sensors

The LHCb VELO silicon sensors are very complex devices. The design of the sensors arise from the need of varying strip lengths, the double metal layer, and regions of very fine pitch. The high performance of the sensors is required even after irradiation and not only for a brand new sensors.

The both *R* and Φ sensors are shown in Figure 3.6. They are made of 300 µm thick *n*-on-*n* single sided silicon wafers with AC coupling to the readout electronics covering the angle of 182°. In order to ensure effective trigger performance even after irradiation, the LHCB VELO aims for an initial signal to noise ratio, SNR, of more than 14 while maintaining the efficiency of detection of a charged particle above 99 % for SNR > 5.

The resolution on the primary vertex position is ~ 40 µm in z and ~ 10 µm in x and y. For secondary vertices the spatial resolution depends on the number of tracks but on average it varies from 150 to 300 µm in z. This roughly corresponds to a resolution of 50 fs for the B-lifetime.

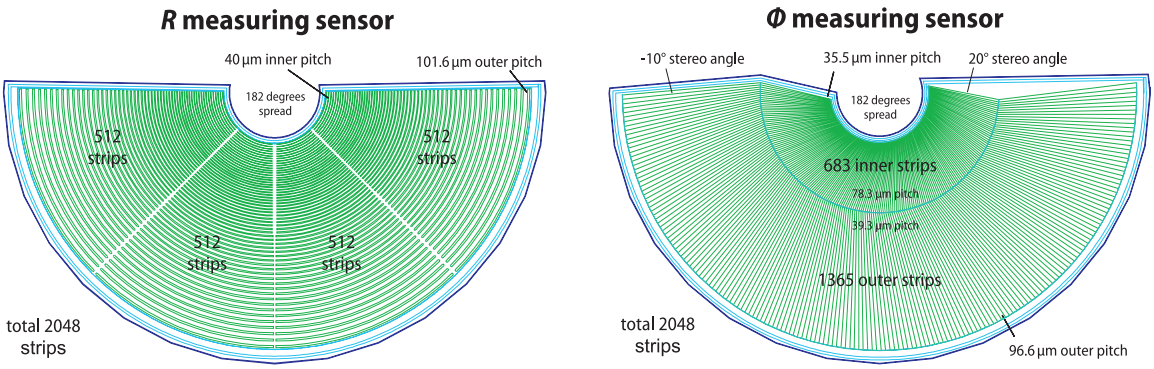


Figure 3.6: The schematic view of R and Φ silicon sensors. Schematic adapted from [10].

The R Sensor

The R sensor contains 2048 strips and is divided into four regions each containing 512 strips. The radial coverage of sensor varies from the inner radius of ~ 8.2 mm to the outer radius of ~ 41.9 mm. The pitch between individual strips increases linearly with the radius from 40.0 µm to 101.6 µm according to the following formula:

$$40 + (101.6 - 40) \times \frac{r - 8190}{41949 - 8190},$$

where r stands for the radius and all dimensions are in µm.

The Φ Sensor

All of the 2048 strips of the Φ sensor are divided azimuthally into an inner and outer region with 683 and 1 365 strips respectively, chosen to equalize the occupancy in the two regions. Here, the pitch of the inner region varies from 35.5 µm to 78.3 µm and of the outer region from 39.3 µm to 96.6 µm. The sensors are flipped from station to station and the strips are tilted with a stereo angle, which is different in sign and magnitude for the inner and outer region (see Figure 3.6).

3.3 Read-Out and Control Electronics

The read-out electronics can be divided into Level-0 (Front-End) electronics which deals with the data before the L0 decision and is situated close to the VELO detector (front-end chips, hybrids), and Level-1 (Off-Detector) electronics, mostly located in a radiation safe environment, that process the data between L0 and L1 trigger decisions (repeater cards, analog links, digitizer boards).

The key components of the read-out electronics architecture are shown in Figure 3.7. One silicon sensor is read out by 16 front-end chips (*Beetles*) mounted on one side of the hybrid. Two

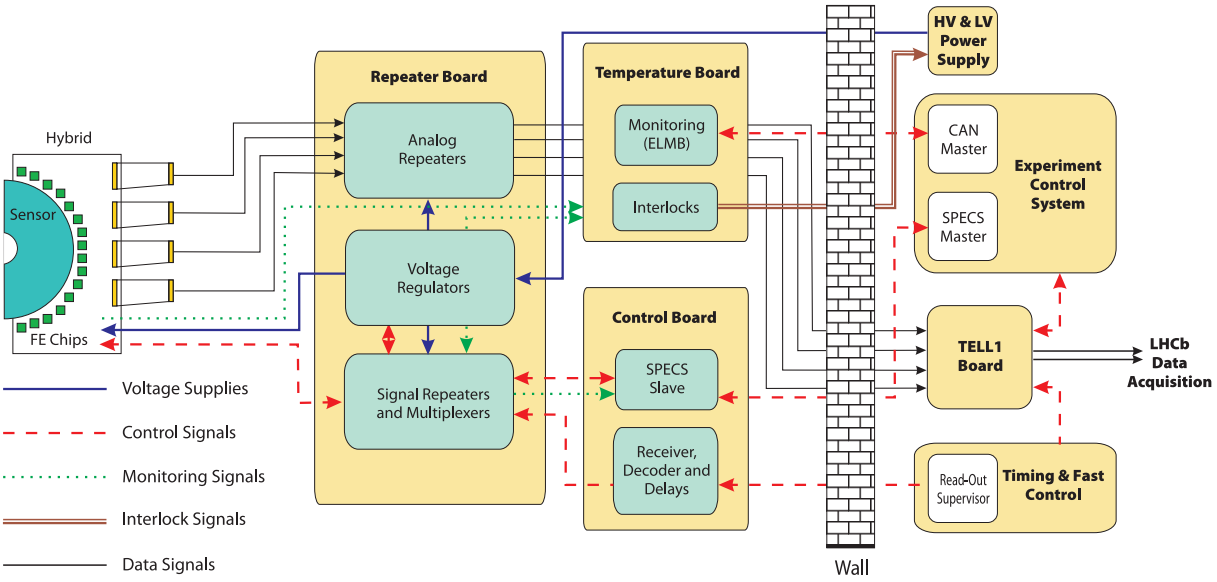


Figure 3.7: Block diagram of the VELO read-out, control and monitoring electronics.

repeater cards per module are placed directly on the exterior of the vacuum tank. These cards drive the analog signals over 60 m long twisted pair cables to the digitizer boards (TELL1 boards) in the counting room. There is also one control board per three VELO modules receiving the timing and control signals and the low voltage for the front-end chips as well as the bias voltage for the sensor. All analog data from one sensor are received and processed by one TELL1 board (two per module). The low voltage and high voltage power supplies with the TELL1 boards are situated behind the shielding wall in the radiation safe environment.

3.3.1 The Level-0 Electronics

As already stated, the Level-0 electronics deals with data before the Level-0 trigger decision. It has to process the signals that comes from the silicon sensors at a rate of bunch crossings of 40 MHz. These signals has to be kept in an analog pipeline until the Level-0 trigger decision is received. All this processing is performed by the *Beetle* chips.

The *Beetle* Readout Chip

The block diagram of the *Beetle* chip can be seen in Figure 3.8. The chip integrates 128 channels, each consisting of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. The equivalent noise charge (ENC) of the amplifier is: $\text{ENC} = 497\ e^- + 48.3\ e^-/\text{pF} \cdot C_{\text{in}}$, where C_{in} is a load capacitance in pF [11].

A comparator discriminates the front-end's output pulse that has a rising time below 25 ns. The threshold is adjustable per channel and input signals of both polarities can be processed.

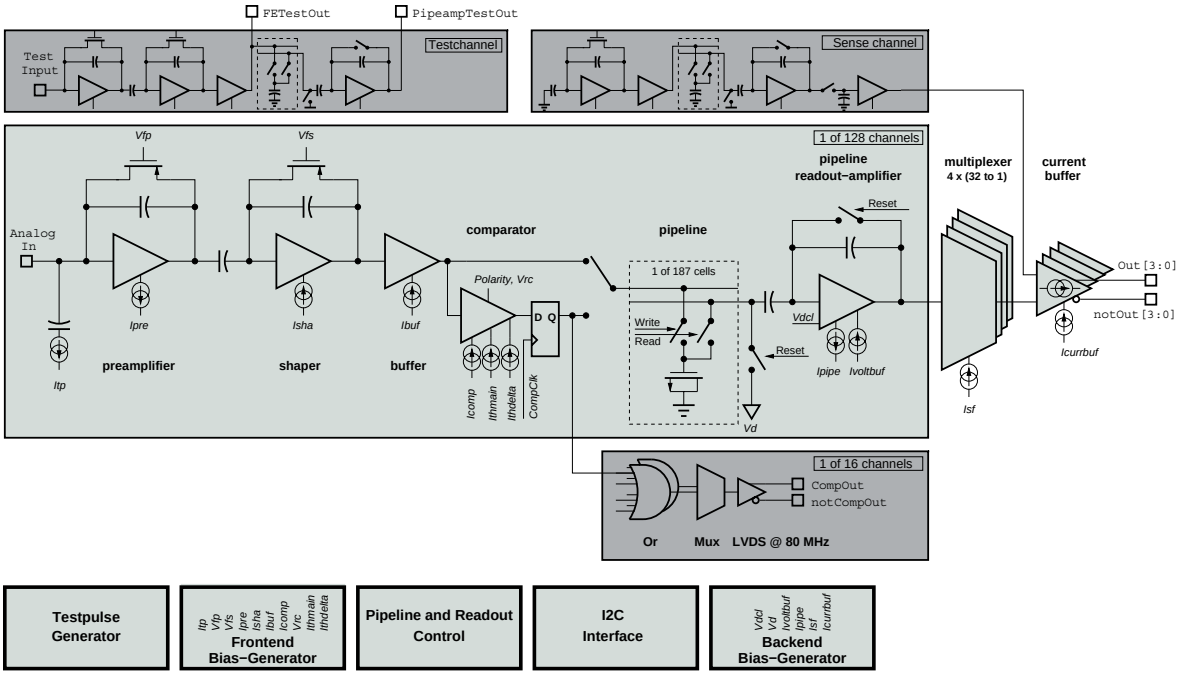


Figure 3.8: Block diagram of the *Beetle* readout chip. Picture issued from [11].

Four adjacent comparator channels are grouped by a logic OR, latched, multiplexed by a factor of 2 and routed off the chip via LVDS ports at 80 MHz.

The analog pipeline which has a programmable latency of max. 160 sampling intervals and an integrated multi-event buffer of 16 stages is used to store the data before the Level-0 trigger decision. Either the shaper or the comparator output sampled at 40 MHz (the LHC bunch-crossing frequency) is used as an input to the analog memory.

The signal stored in the pipeline is transfered to the multiplexer via a resettable charge-sensitive amplifier. The voltage level of one dummy channel is subtracted from all multiplexed channels to compensate for the common mode effect. The data format of four serialized output channels is shown in Figure 3.9.

For testing and calibration purposes a charge injector with adjustable pulse height is implemented. The bias settings and other parameters like the trigger latency can be controlled via a standard I^2C interface. All digital control and data signals, except for those at the I^2C ports, are routed via LVDS ports.

3.3.2 The Level-1 Electronics

The purpose of the Level-1 electronics is to digitize the analog data sent out by the repeater boards and to preprocess the data for the L1 trigger. The different components of the Level-1

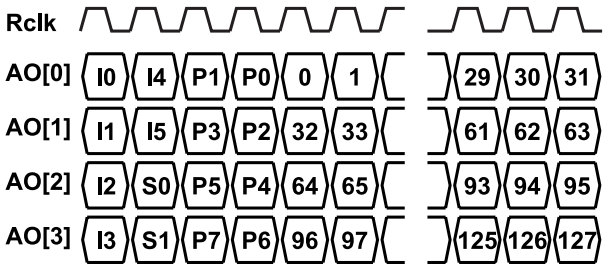


Figure 3.9: *Beetle* analog readout data format. In every channel the first four bits form the header. The header bits I_0–I_5 with S_0 and S_1 are signalization bits while P_0–P_7 indicate the pipeline column number. The readout clock frequency is 40 MHz. Picture issued from [11].

electronics are:

- The repeater cards located on the outside of the vacuum tank.
- The analog data transmission.
- The TELL1 boards in the counting room.

Repeater Cards

The 64 analog outputs of one sensor comes to one repeater card from where they are transmitted via ~ 60 m long cables to the TELL1 board. The repeater card also transfer the control signals (reset, clock, trigger and configuration signals) and low voltages plus high bias voltage from the control module to the hybrid.

Analog Data Transmission

The analog data are transmitted at a rate of 40 MHz via twisted pair cables to the ADC modules on the TELL1 board, which are placed in the counting room at a distance of about 60 m. The schematic of the analog data transmission line is shown in Figure 3.10

The TELL1 Board

The TELL1 board receives 64 analog data links from one sensor and accommodates in addition four more input-output interfaces. These are: Timing and Fast Control TFC, Experiment Control System ECS, Level-1 trigger interface and Data Acquisition DAQ interface. The processing chain of the TELL1 board is described in chapter 5.

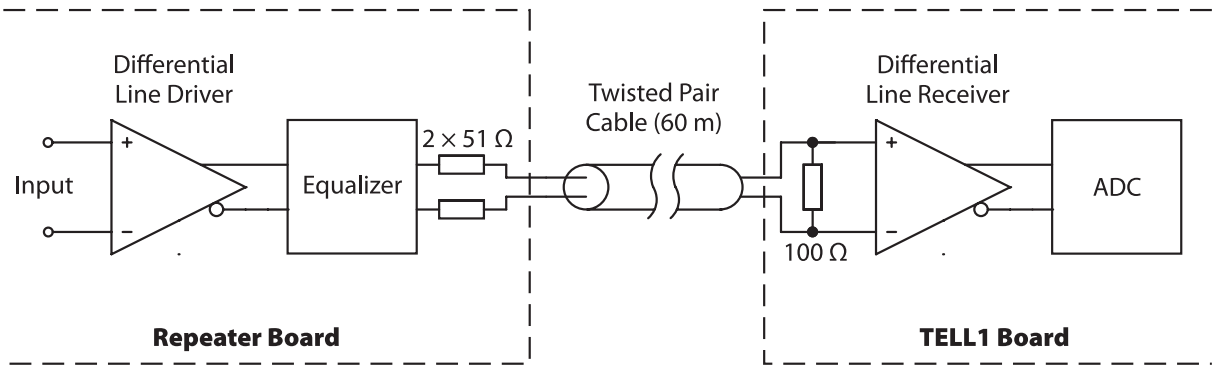


Figure 3.10: The schematic diagram of the analog data transmission line. The function of the equalizer is to compensate for the transmission line loss in high frequency (preemphasis).

3.3.3 The Experiment Control System

The VELO detector is controlled by the Experiment Control System (ECS). The interface between the ECS and read-out electronics is provided by the SPECS bus [12]. The SPECS is a one-master n-slaves bus where the master is implemented in a PCI board mounted in a PC in the counting room. For the communication, the bus requires four unidirectional differential pairs. Up to 112 SPECS slaves can be addressed by one master and be operated at 10 Mbit/s over a maximum distance of 100 m.

The overview of the VELO monitoring and control system is shown in Figure 3.7. All the VELO modules are controlled by the Control board that is configured through the SPECS bus. The Control board also redistributes the optical TFC signals that are sent from the Readout Supervisor sitting in the counting room.

To avoid the destruction of the modules by overheating, the temperature of the hybrids has to be monitored. This is accomplished by the Temperature board which evaluates the signals from the temperature sensors and if some of them is out of an acceptable range the logic of the Temperature board will fire the interlocks that cut out power supplies. The Temperature board is described in more detail in chapter 4.

Chapter 4

Temperature Board

This chapter describes the temperature board and documents the firmware implemented in the FPGA. The interconnection between individual components of the temperature board as well as the safety mechanism of interlocking are discussed.

4.1 Conception of the Temperature Board

The temperature board is a part of the VELO Experiment Control System and it serves two purposes:

- **Measurement** of temperature.
- **Security** in case of cooling system failure.

Each temperature board hosts one ELMB and four Interlock Box (IBox) mezzanines and controls 16 repeater boards (i.e. 8 VELO modules). The temperatures of the hybrids and voltage regulators on the repeater boards are monitored by the Negative Temperature Coefficient (NTC) resistors connected to the temperature boards via a 16 RJ-45 sockets, each carrying four signals (two per hybrid and two per voltage regulator) from the NTC temperature sensors. In the case of the cooling system failure, the control logic of the temperature board generates interlock signals which cut off all power supplies to the VELO detector. This represents the last safety mechanism which is applied if the cooling system fails. The schematic view of the temperature board is found in Figure 4.1. The main components of the temperature board are described in following sections.

4.1.1 The ELMB Mezzanine

The ELMB mezzanine provides a stand-alone system for temperature monitoring. It is connected in parallel with the Interlock Boxes, passively monitoring the voltage level at the NTC resistors and

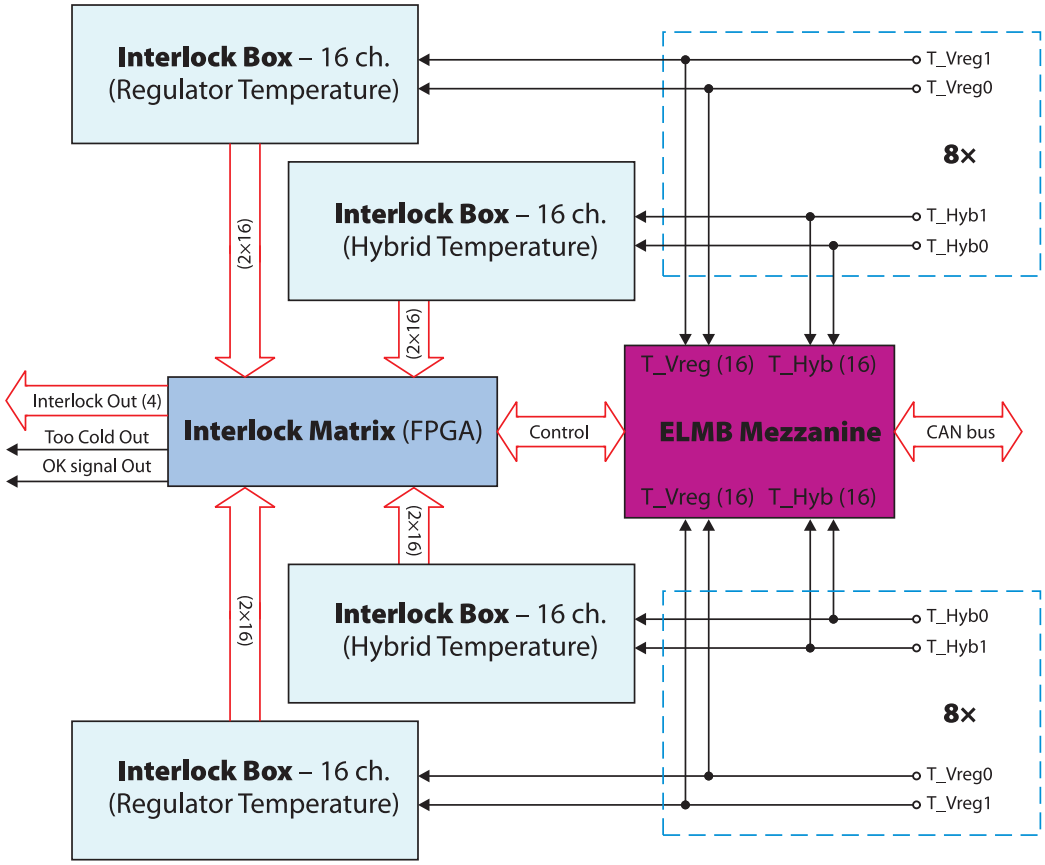


Figure 4.1: Schematic view of the Temperature Board.

hence the temperature. The ELMB has an embedded Atmel ATMega128 processor with 64 16-bit ADC channels and a voltage reference circuit, which are systematically sampling the voltages of the temperature sensors. The ELMB is also used as a configuration and supervisor module for the FPGA. The communication with the supervisory system (ECS) is accomplished via a CAN bus.

4.1.2 Communication Between Atmel and FPGA

The ATMega128 microcontroller sitting on the ELMB mezzanine can communicate with the on-board FPGA via an SPI bus and 8 general purpose pins. The SPI bus uses four pin interface which consist of:

- **SS#** (*Slave Select*) – low-active signal to select the slave (e.g. the FPGA).
- **SClk** (*SPI Clock*) – serial clock used to synchronize the data transfer.
- **MOSI** (*Master-Out Slave-In*) – high-active data transfer from Atmel to FPGA.
- **MISO** (*Master-In Slave-Out*) – high-active data transfer from FPGA to Atmel.

The SPI data frame for the communication between the Atmel and FPGA is shown in Figure 4.2. It uses the standard 16-bit format with the clock polarity (cpol) and phase (cpha) equal to 0, i.e. data are transferred on the rising edge of SClk.

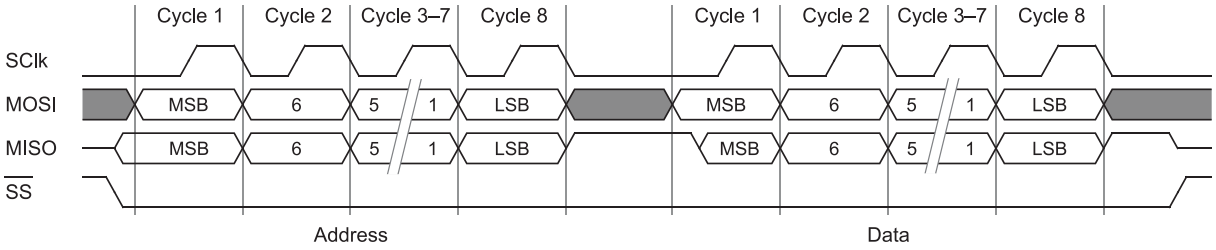


Figure 4.2: The SPI data frame.

Each SPI transfer consists of two bytes:[1]

- **Address** – provides register address in the 7 lower bits and a read/write flag in the highest one.
- **Data** – reads or writes the register content.

After the Atmel microcontroller has sent the 7-bit address with a read/write flag (log. '1' is read, log. '0' is write), the FPGA returns the content of the status register. On the data cycle the FPGA sends out the data stored in the addressed register (for both read and write mode). The individual registers implemented in the FPGA are described in section 4.2.3.

Apart from the SPI interface, two more signals (from eight available general purpose pins) are used:

- **Reset** – low active signal to reset the FPGA.
- **Interrupt** – low active signal to alert the Atmel microcontroller.

4.1.3 Interlock Box Mezzanine

The wiring diagram of the Interlock Box mezzanine is shown in Figure 4.3. The IBox supplies voltage to the NTC resistor and a precision resistor connected in series. The voltage drop across the NTC resistor is compared to the internal reference voltages and two bits per temperature channel are generated.

[1]Only two-byte transfers are allowed. Single byte transfers are effectively ignored (the *SPI error* flag is set) and for transfers longer than two bytes only first two bytes are recognized.

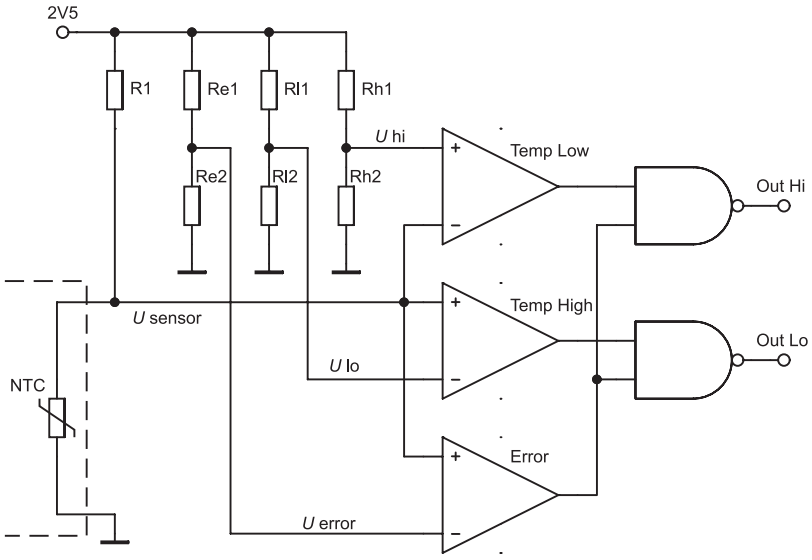


Figure 4.3: Wiring diagram of the Interlock Box.

Temperature Events

The Interlock Box recognize three following temperature events:

- **Too Warm** – when the temperature goes above a given limit.
- **Too Cold** – when the temperature is below a pre-set limit.
- **Too Error** – when the NTC sensor is not mounted (open circuit).

The coding of these three events as well as the considered thresholds are summarized in Table 4.1.

Status	Comparators	Out Hi	Out Lo
Temperature within limits	$U_{hi} < U_s < U_{lo}$	log. '1'	log. '1'
Temperature too high or short circuit	$U_s < U_{hi}$	log. '0'	log. '1'
Temperature too low	$U_{lo} < U_s < U_{err}$	log. '1'	log. '0'
Error, open circuit or power failure	$U_s > U_{err}$	log. '0'	log. '0'

Table 4.1: Description of the logic output of the interlock box versus the temperature of the sensor where $0 < U_{hi} < U_{lo} < U_{err} < 2V5$.

4.2 Temperature Board Firmware

The interlock logic implemented in the FPGA takes into account only temperature signals from the hybrids, i.e. two signals from each connector resulting in 32 signals in total. Information

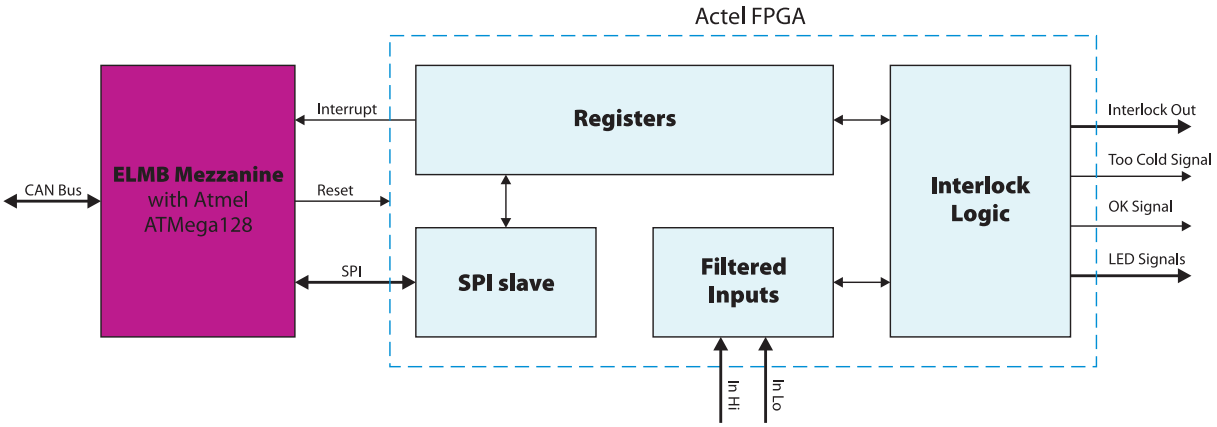


Figure 4.4: Block diagram of the interlock system.

about the temperature of the voltage regulators is ignored by the processing logic in the FPGA and is monitored only by the ELMB mezzanine.

The block diagram of the temperature board firmware is shown in Figure 4.4. It collects the information of the temperature range for each of 32 channels and generates four corresponding interlock signals. It means that two detector modules is the minimal unit that can be switched off via a hard-wired interlock. The status of all channels is stored in the internal registers of the FPGA and can be read-out via the SPI interface.

Apart from the interlock signals, a Too Cold and OK signals are available. In normal operation the OK signal should be active. If in any of the 32 channels the Too Cold event occurs, a Too Cold signal is generated indicating a problem with the cooling system regulation. A LED indicator corresponds to each of the interlock Too Cold and OK channels.

The whole logic is implemented in the Actel APA150 FPGA. The clock signal is supplied by the on-board clock generator running at 20 MHz. The source VHDL files can be found in [13].

4.2.1 Module of Filtered Inputs

The two-bit information of the channel status is decoded into Too Warm, Too Cold and Error high-active signals. For every of these channels an input filter is implemented to avoid the unwanted firing of interlocks caused by the noise or ripples in the transmission line connecting the sensors with the temperature board. The filter is realized as a counter that is reset by the input signal of log. '0' (no events). In the case of event in any of the channels the counter leaves the reset mode and starts to count. The overflow of the counter signals an event that is later treated by the processing logic.

The counting frequency is deduced from the system clock frequency by a frequency divider and is set to 625 kHz (division by 32). The counter itself is 10-bit resulting in an event latency of ~ 1,6 ms.

4.2.2 Interlock Logic

The filtered events for each channel are processed by the interlock logic, following the setting stored in the control and mask registers (see section 4.2.3). The events of all channels are stored in resettable event registers, to each of which one mask register corresponds. The mask register enables or masks the appropriate events and only enabled events are treated by the interlock logic.

If there is at least one unmasked Too Cold event, a *Too Cold* flag is set in the status register and a Too Cold signal is sent out to the control room. The 32 channels are combined in four interlock groups (channels 1–8, 9–16, 17–24 and 25–32). The interlock is fired if at least one of the Too Warm or Error enabled events in the corresponding interlock group is active. Interlocks can be fired also by setting the *Interlock Set* flag in the control register.

The Interlocks and Too Cold signals can be reset by setting the corresponding reset flag in the control register. For safety reason the reset signals are allowed only to be active during one clock cycle.

4.2.3 The FPGA Registers

For controlling and monitoring purposes a set of 8-bit addressable registers is implemented in the FPGA. The individual registers with their addresses are listed in Table 4.2.

Address range	Register	Access
0x4B 0x40	Event registers	R
0x2B 0x20	Enable registers	RW
0x10	Control register	W
0x08	Status register	R

Table 4.2: Addressable 8-bit registers of the FPGA.

Status Register

This read-only register indicates the status of the interlock logic. The value of the register is sent out in the first SPI cycle. All the bits except the *SPI error* bit are latched, which means that if once set they must be reset via a flag in the control register. The *SPI error* flag is set if during the SPI cycle the SS# signal goes high and is reset if the SPI cycle pass with no errors. The interrupt signal is generated if any of bits of the status register are set to log. '1'.

Bit	Function	Comments
7	*Interlock 3* active	set when interlock from sockets 12–15 is fired
6	*Interlock 2* active	set when interlock from sockets 8–11 is fired
5	*Interlock 1* active	set when interlock from sockets 4–7 is fired
4	*Interlock 0* active	set when interlock from sockets 0–3 is fired
3	*Error* event	set when at least one error event occurred
2	*Too Warm* event	set when at least one too warm event occurred
1	*Too Cold* event	set when at least one too cold event occurred
0	*SPI error*	set when SPI transfer is invalid

Control Register

The individual flags of the status register can be reset by writing this register, however, the cause of the event flag has to be removed beforehand, e.g. by masking the appropriate channel. For safety reasons all reset signals are valid only for one clock cycle, therefore if the reason for the event flag still persist, the reset is ineffective.

Bit	Function	Comments
7	*Interlock 3* reset	resets the interlock for sockets 12–15
6	*Interlock 2* reset	resets the interlock for sockets 8–11 is fired
5	*Interlock 1* reset	resets the interlock for sockets 4–7 is fired
4	*Interlock 0* reset	resets the interlock for sockets 0–3 is fired
3	*Error* event reset	resets the error event flag and registers
2	*Too Warm* event reset	resets the too warm event flag and registers
1	*Too Cold* event reset	resets the too cold event flag and registers
0	*Interlock* set	forces the interlock (for testing and manual interlocking)

Enable Registers

In this registers, setting a bit to log. '1' enables the corresponding event to participate in the interlock generator logic.

Address	Function
0x28–0x2B	$4 \times 8 = 32$ enable bits for *Too Cold* events
0x24–0x27	$4 \times 8 = 32$ enable bits for *Too Warm* events
0x20–0x23	$4 \times 8 = 32$ enable bits for *Error* events

Event Registers

All the bits in the event registers are latched, i.e. a corresponding flag must be set in the control register in order to remove an event, e.g. after masking.

Address	Function
0x48–0x4B	4 × 8 = 32 status bits for *Too Cold* events
0x44–0x47	4 × 8 = 32 status bits for *Too Warm* events
0x40–0x43	4 × 8 = 32 status bits for *Error* events

Power-Up and Reset State of Registers

To ensure the system security after a power-up or reset stages all the events are enabled and all interlocks are set. In principle the reset signal is applied by the ELMB mezzanine during a power-up. The user must disable the unused channels and then reset all the events and the four interlocks. Only then the interlocked power supplies can be brought up.

4.2.4 The SPI Slave Module

All the configuration and read-out of registers implemented in the FPGA is made by the SPI bus. The block structure of the SPI module is shown in Figure 4.5.

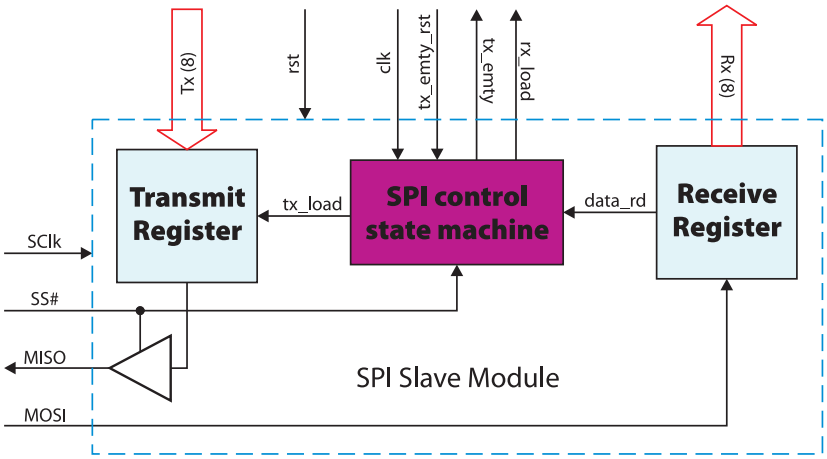


Figure 4.5: Schematic diagram of the SPI module.

The SPI slave module consist of two separate transmit and receive 8-bit shift registers operated on SClk frequency. Every transfer cycle begins by activating the slave select signal (SS#) by master (ELMB). Since the SPI bus is one master – multiple slaves interface the output of the transmit register (MISO) has to be tri-stated if the device is not selected by the SS# signal.

The proper operation of the SPI module is ensured by the control state machine[2]. In the beginning of every 8-bit transfer cycle the content of the status or addressed register has to be uploaded into the transmit shift register. It is accomplished by placing the data on the bus

[2]The SPI control state machine also synchronize the SPI module which runs on SClk frequency with the rest of the circuitry implemented in the FPGA. The minimum system clock frequency is quadruple of the SPI clock frequency (SClk).

and asserting the tx_empty_rst signal. The state machine then activates the tx_load signal that loads the data to the transmit register. One clock cycle after the activation of tx_load signal, the tx_empty flag is asserted indicating a successful loading of data. If the new data are not uploaded before the SPI transfer, the default content (all bits in log. '1') of the transmit register is sent out.

Immediately after the last clock period of the 8-bit transfer cycle the data_rd signal is activated. The control state machine synchronize this signal with system clock and asserts the rx_load flag indicating that the data are received and ready to upload. The transmission is over once the SS# signal is deactivated. The timing diagram of the SPI transfer cycle is shown in Figure 4.2.

Chapter 5

The TELL1 Algorithm

This chapter outlines the present and the future upgrades to the TELL1 algorithm, originally developed at École Polytechnique Fédérale de Lausanne (EPFL) [14]. It focuses mainly on those upgrades which implemented as a part of this diploma thesis, i.e. the pedestal subtraction and the FIR filter block. The future prospects are mentioned at the end of this chapter.

5.1 Overview of the TELL1 Board

The TELL1 board is a part of the Level-1 electronics which processes the data after the Level-0 trigger decision. The layout of the TELL1 board is shown in Figure 5.1.

As discussed above, each *Beetle* chip processes 128 detector strips. There are 16 chips located on one hybrid performing the readout of one sensor of 2048 strips. The *Beetle* chip transmits the L0 accepted data on four serial analog links at 40 MHz, which is 64 analog serial links in total. The analog interface on the TELL1 must be capable to digitize these data streams at 40 MHz. Four analog receiver cards with sixteen 10-bit-ADC and adjoint pre-processing FPGA are used to handle this data throughput. The digitization process is synchronized via the Timing and Trigger Control (TTC) system. This system uses optical fiber links to distribute all the clock and trigger signals over the whole experiment.

The main Level-1 processing is implemented in the so called pre-processing FPGA (PP-FPGA). The outputs of four PP-FPGA are linked by the SyncLink FPGA and sent out over a read-out quad gigabit ethernet card (RO-TxCard).

The ECS interface is used to upload the processing parameters to all programmable chips on the motherboard. No fast acquisition is needed for this task, therefore the standard microprocessor interfaces I^2C and JTAG are used with the GPIF pins required by several chips on the motherboard. The ECS interface of the TELL1 board is based on a credit-card-size Linux-bassed PC and connected to a 10/100 Ethernet LAN. The same PC is also used for debugging the firmware of the FPGAs.

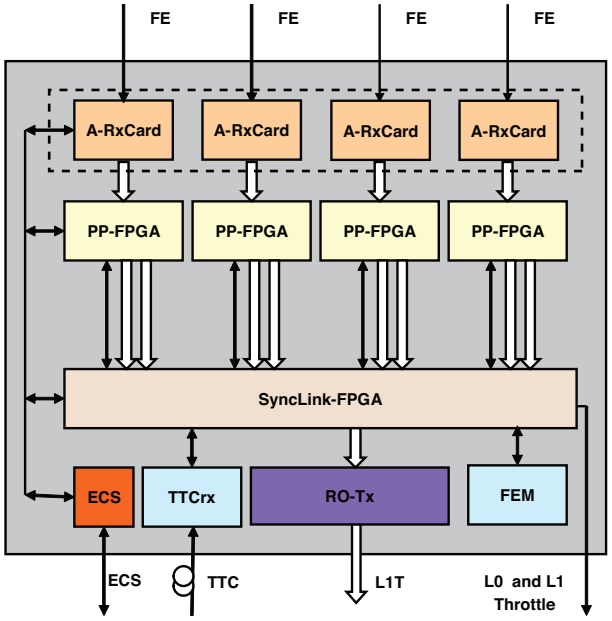


Figure 5.1: Block diagram of the TELL1 board. Figure adapted from [14].

For the synchronization of the VELO readout a Front Emulator (FEM) card is used. This card uses a a fully operational reference *Beetle* chip bonded directly on the PCB and interfaced via I^2C bus.

5.2 Data Processing Chain for the VELO Detector

An overview of the input processing done in the Altera *Stratix* PP-FPGA is given in Figure 5.2. Each PP-FPGA handles 16 analog channels sampled by the ADC which are multiplexed by two in eight processing streams.

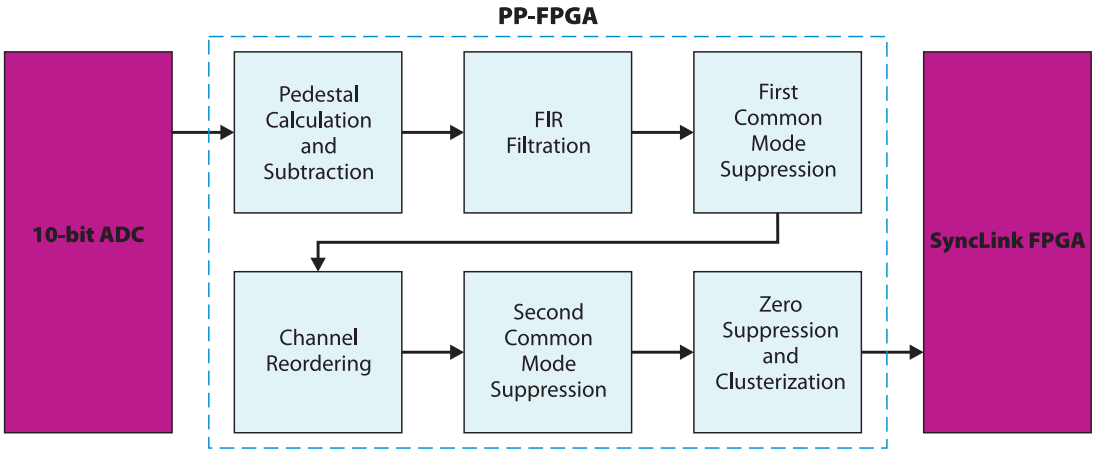


Figure 5.2: The processing chain implemented in the PP-FPGA.

Due to different skew of the data in individual analog links caused by the 60 m long transmission lines the digitization process has to be synchronized. This problem is solved by a delay of the clock signals that drive the ADC. Hereafter the pedestal subtraction, FIR filtration, reordering of strips, common mode suppression and zero suppression blocks follow. These are described in the next sections.

5.2.1 Pedestal Calculation and Subtraction

In order to make the data set as uniform as possible, the individual voltage offset levels ("pedestals") must be subtracted from each VELO channel. The pedestals must be calculated periodically as they can change with time (due to temperature changes, for instance). The values of pedestals for every channel must be accessible via ECS for later processing.

The running sum over a set of N events is used to calculate the pedestals. The pedestal $P[n]$ of a channel at a time slot n is given by the ratio:

$$P[n] = \frac{P_{\text{sum}}[n]}{N},$$

where $P_{\text{sum}}[n]$ can be calculated by a recursion:

$$P_{\text{sum}}[n+1] = P_{\text{sum}}[n] + x[n+1] - P[n], \quad P_{\text{sum}}[0] = \text{C}^{\text{te}}, \tag{5.1}$$

where $x[n+1]$ is the value of the data sample at $n+1$. The pedestal corrected data sample is given by the difference $y[n+1] = x[n+1] - P[n]$, which is already calculated in the expression (5.1).

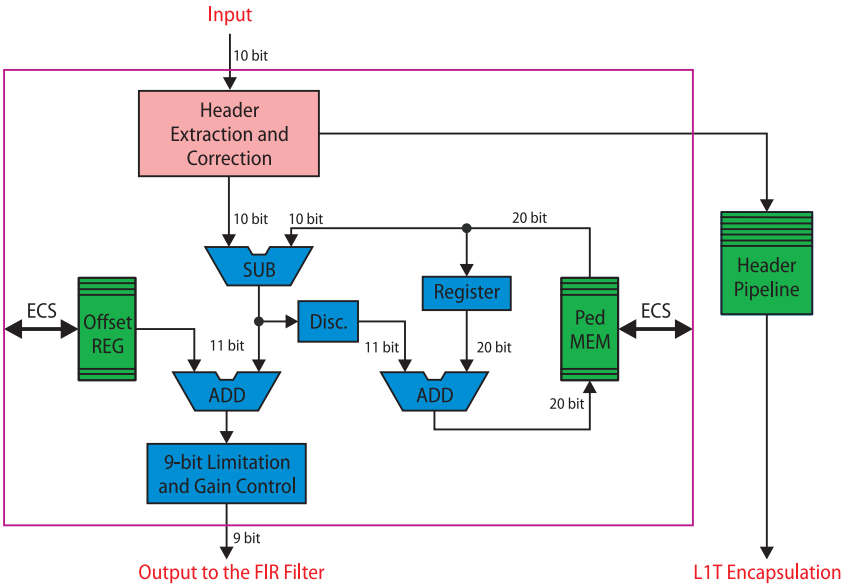


Figure 5.3: Block diagram of the pedestal subtraction with the bit limitation for one processing channel.

This procedure can be implemented using the scheme shown in the diagram in Figure 5.3. To store the sum of 10-bit pedestal values over 2^{10} samples, a total width of 20-bit is required.

These 20-bit values, one per strip, need to be stored in the pedestal RAM. Only the strips with no hits, i.e. the signals with a value below a certain threshold are used for the pedestal calculation.

For further calculation the width of the data has to be limited to save the resources of the Altera *Stratix* FPGA. Since the hard-wired DSP blocks used for multiplication in the FPGA are using 9-bit operands, the most reasonable resolution is 9-bit. The data values of the strips are mostly positive, therefore in order to effectively exploit the whole dynamic range of 512 possible values the unsigned representation with a predefined offset is used, where the offset value corresponds to zero. The offset can be set via ECS and should be high enough to prevent any underflow (the negative values are represented by the range 0 to offset value).

The output of the pedestal subtraction block after the bit reduction can be amplified by a factor of one, two and four. Any overflow or underflow is detected and the signal is limited to the lowest or the highest value.

The 4-bit header of every 32-bit stream is separated in the pedestal subtraction block and pipelined, while the last bit of the header is used for the header correction[1] of the first strip in a 32-bit frame. This correction is needed due to the cross talk in the transmission line (see section 5.2.2).

5.2.2 The FIR Filter

Due to the cross-talk effect in the transmission path (*Beetle* chips and cables), the received signal is distorted (see Figure 5.4). The cross talk caused by the transmission line can be partially compensated by equalization.

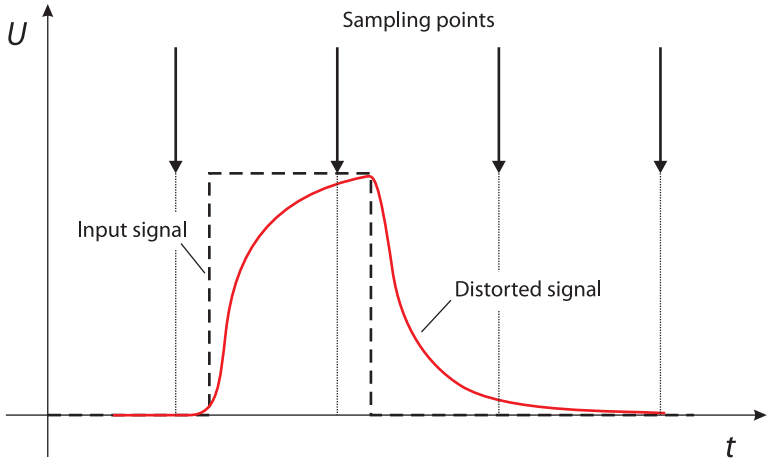


Figure 5.4: The cross-talk caused by the sampling of the signal distorted by the transmission line.

The cross-talk effect can be minimized by digital filtration of the sampled input signal. The

[1] If the last bit of header is high, a predefined value is subtracted from the first strip in a 32-bit frame and vice versa.

FIR filter of the 4th order is implemented in the PP-FPGA with a transfer function:

$$G(z) = \sum_{n=-1}^{2} b_n z^{-n},$$

where b_n are the filter coefficients. In the time domain the output $y[n]$ of the filter is expressed by the following relation:

$$y[n] = b_{-1}x[n+1] + b_0 x[n] + b_1 x[n-1] + b_2 x[n-2],$$

where $x[n]$ is the input signal. The sum of all filter coefficients should be equal to the required gain of the FIR filter.

This filter is obviously not causal, which reflects the fact that the both previous and next strips are affected by a cross-talk effect. The non-causality of the filter does not present any obstruction since the substitution $y[n] \rightarrow y[n+1]$ solves the problem. This substitution corresponds to a signal delay by one clock cycle.

The implemented FIR filter is shown in Figure 5.5. It uses the hard-wired DSP blocks of the Altera *Stratix* FPGA. The set of four 9-bit signed coefficients is unique for every analog link, i.e. there is 16×4 9-bit coefficients per one PP-FPGA. The individual coefficients are uploaded via ECS. When the FIR filter is disabled, all coefficients are set to zero except the b_0 which equals to one. In that case the signal is only delayed by one clock cycle.

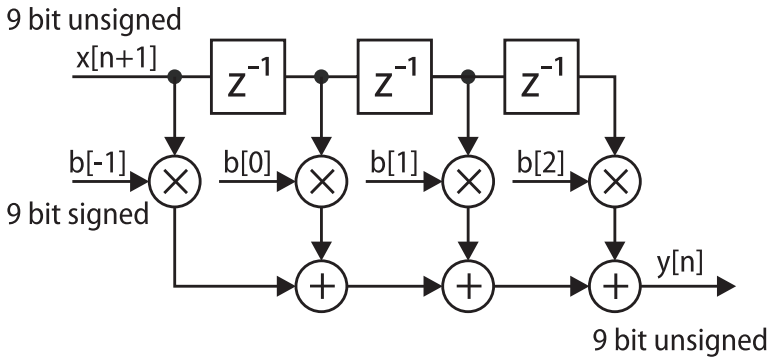


Figure 5.5: The 4th order 9×9-bit FIR filter.

The coefficients of the FIR filter can be measured by injecting a single pulse to the *Beetle* and by measuring the impulse response. By assuming the linearity of the transmission path, the required transfer function of the filter can be obtained by inverting the measured impulse response so that

$$H(z)G(z) = 1.$$

Here $H(z)$ is the impulse response of the transmission path and $G(z)$ is the transfer function of the FIR filter.

5.2.3 Common Mode Suppression and Reordering

The common mode suppression and reordering of the channels hinders the unwanted low-frequency noise (which is almost constant for the 32-bits frame). Main sources of this noise are the long term instabilities of the power supplies, parasitic grounding loops, or the radio-frequency pickup from the sensor. Since the readout of the sensor is not consecutive, especially for the Φ sensor which has two kind of strips (inner and outer), it is important to distinguish between common mode noise induced at the sensor level, and therefore dependent on the spatial location of the silicon strip, and the common mode noise that comes from the readout chain.

In the original version of the TELL1 algorithm [14] only the correction for the common mode noise induced at the sensor level is performed. It turns out, that the common mode noise that comes from the readout chain is also significant and needs to be suppressed. The proposed solution is to use two common mode suppression blocks. One for the compensation of the noise induced by the readout chain and the second after the reordering of sensors for the sensor dependent noise.

Linear Common Mode Suppression Algorithm

This linear approximation method is legitime only for a noise varying in a time domain much larger than the 25 ns width of a VELO sample. This criterion is fulfilled for both sensor induced and readout chain induced common mode noise.

The linear common mode subtraction method is performed on a set of 32 detector channels (strips). The method consist of two identical iterations, in which a linear approximation of the common mode noise present in one VELO sample is calculated. The formal description of the linear common mode suppression algorithm is:

- **First iteration** that consist of
  - Mean value calculation
  - Mean value subtraction from the input data
  - Slope calculation
  - Linear common mode subtraction
- **Hit detection** by comparing the absolute value of the sample amplitude to an adaptive limit determined from the RMS of the sample distribution.
- **Second iteration** is the same as the first one (second mean value and slope is calculated and subtracted) except that detected hits are masked.

For a low and in amplitude stable common mode noise, a simplification of the hit detection is possible. Instead of calculating the RMS of the sample distribution, hits can be tagged by a discriminator with a preset threshold.

Channel Reordering

The channel reordering is mainly needed for the Φ sensor because of its particular connection topology. The inner and outer strips are mixed together in the readout, and hence, for the sensor induced common mode suppression the inner and outer strips has to be separated.

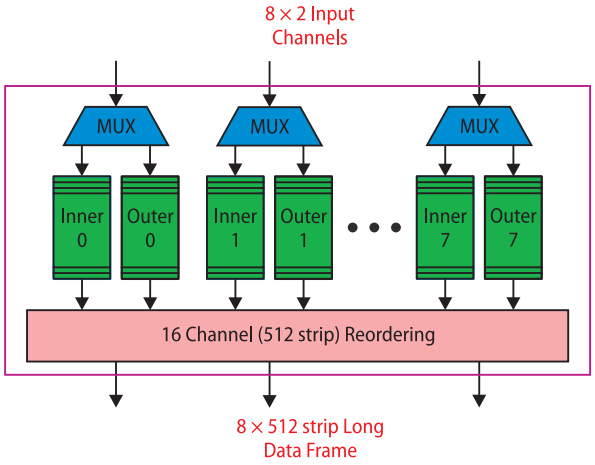


Figure 5.6: The channel reordering scheme for the Φ sensor.

The proposed reordering algorithm is shown in Figure 5.6. The inner and outer strips are written to the corresponding memory in accordance with the reordering scheme. From the memory, the 512-bits data frame (¼ of the sensor) with separated inner and outer strips is formed.

The masking of dead or particularly noisy channels can be done at this stage of data processing, e.g. by setting the strip value to zero, so that the following common mode suppression for the strip induced noise will not process them.

5.2.4 Zero Suppression and Cluster Finding

The zero suppression processing block receives the common mode corrected data sample values. The low occupancy (~ 1 %) of the vertex detector makes zero suppression an obvious way to reduce the redundancy of the data. Moreover, in the Level-1 trigger the suppressed data (clusterized) are required.

A possible procedure for the clustering is to search for hits in two iterations in a set of 512 strips. In the first search, a high threshold is applied to identify the hits that have a high signal to noise ratio. In the second step, the neighboring strips to the found hits are searched for signal with a less stringent cut to find the complete cluster signal. The total charge deposited in a cluster can be calculated by summing the signal of all strips in the concrete cluster. The cut whether a cluster is accepted or not can then be done on the basis of the total signal of the cluster compared to an appropriate threshold. Last step is the weighted average calculation of the inter strip position. The 16-bit cluster encoding format is shown in Table 5.1.

Bit	Description
0–2	Inter strip position (set to zero in case of one strip cluster).
3–13	11-bit strip number (0 to 2047).
14	The cluster size bit distinguishes between 1 or 2 and 3 or 4 strip clusters. Set to zero for 1 or 2 strip clusters and to one for 3 or 4 strip clusters.
15	The spillover bit indicates if the total charge corresponding to the sum of all ADC values in the cluster is above a certain fixed threshold. This is to distinguish between the signal clusters and clusters caused by the signal spillover from the previous event or noise.

Table 5.1: The VELO cluster format for the Level-1 trigger.

Conclusion

The driving motivation of the LHCb experiment was discussed in this thesis and the LHCb detector as well as the VELO subdetector were introduced. The emphasis was placed at the the temperature monitoring board and the DAQ TELL1 board of the VELO, for which the the VHDL code was developed and implemented.

The TELL1 framework as originally proposed is documented in [14]. Further development to this framework includes a new concept of the TELL1, for which the VHDL code for the pedestal calculation and subtraction block, and the newly realized FIR filter was written. In the near future the common mode suppression block will be implemented. The new concept of the channel reordering and cluster finding blocks, discussed in the conclusion of the last chapter, is a long time prospect and needs further discussion.

The temperature board firmware was completed and successfully tested. Long term stability and robustness tests has yet to be performed, which is to be done as soon as a new firmware of the ELMB mezzanine is implemented and a PVSS software support is created.

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