XXIII. CIRCUIT THEORY*

Prof. S. J. Mason	Prof. R. D. Thornton	R. Huibonhoa
Prof. H. J. Zimmermann	J. T. Andreika	D. G. Kocher
Prof. C. L. Searle	B. L. Diamond	W. C. Schwab

RESEARCH OBJECTIVES

Our long-range objective is to achieve a better understanding of the properties of electric networks. This includes investigation of such fields as topology, conventional and parametric amplifiers, analysis and synthesis of nonlinear circuits, and of linear circuits with characteristics distinctly different from RLC circuits.

Short-range projects include studies of parametric amplifiers, frequency multipliers, synthesis by means of inert transformations.

S. J. Mason, H. J. Zimmermann, C. L. Searle, R. D. Thornton

A. INERT TRANSFORMATIONS AND NETWORK CONSTRAINTS

1. Inert Transformations

Network design usually consists of finding some way to interconnect available components so as to achieve some desired result. An important problem is to determine how the characteristics of the individual components constrain the type of network that may be realized. Brune (1), Bode (2), and others have derived a number of constraints, but most of these depend upon a simple component characteristic and/or a specified topology. If we are not willing to limit the components and the topological possibilities, the problem must be attacked from a more general point of view. For example, we are still able to derive a number of basic limitations if we assume a simple property for the interconnection network. We could assume that the interconnections are lossless; but let us go one step farther and assume that they are conservative of complex power. For simplicity, a network that conserves complex power will be called "inert."

Inert networks, by our definition, are unable to absorb power at any power angle, and hence $P = [V]^X [I] = 0$ ([V] and [I] are the column matrices of node-to-datum voltages and in-flowing current, and $[V]^X$ is the conjugate transpose of [V]). The term "inert" has been used primarily to distinguish the network from what is commonly called a lossless network. Lossless, by longstanding convention, implies that $\mathrm{Re}(P) = \mathrm{Re}([V]^X [I]) = 0$ for $s = j\omega$, or, in other words, only the real power is conserved. By this definition, inductors, capacitors, gyrators, circulators, and many other circuit components are lossless. None of the components that have been mentioned are inert, however, because, with a proper choice of excitation, $\mathrm{Im}\ P \neq 0$. We can think of an inert network as a

*This research was supported in part by Purchase Order DDL-B222 with Lincoln Laboratory, a center for research operated by M.I.T., which is supported by the U.S. Air Force under Air Force Contract AF19(604)-5200.

lossless network with the additional restriction that Im P = 0.

The restriction to inert interconnections seems to be much more restrictive than if we allowed lossless components. However, the result need not be more restrictive, since an inductor, gyrator, or the like, may be considered as an additional available component. The advantage of treating lossless elements as components distinctly separate from the interconnection network is that in this case analysis may be performed at any complex frequency. Clearly, a capacitor is not lossless for right half-plane excitation, since growing waveforms must supply real power to charge the capacitor. In brief, an inert network must have $P = [V]^X [I] = 0$ for all possible excitations at all complex frequencies.

2. Canonic Forms under Inert Transformations

We can now visualize network design as shown in Fig. XXIII-1. The available components or devices will be assumed to be linear but otherwise unrestricted. Let us assume that the interconnection network may be frequency dependent but must be inert at all frequencies. In order to simplify calculations, it is expedient to perform the synthesis in three steps, as shown in Fig. XXIII-2. First, we reduce the individual components to a canonic form by means of transformations T_1, T_2, ..., then synthesize the desired network in a canonic form, and finally convert the canonic form to a desired

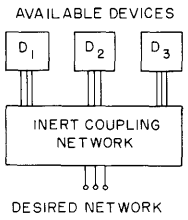

Fig. XXIII-1. Synthesis with inert interconnections.

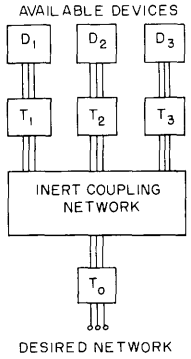

Fig. XXIII-2. Synthesis with inert interconnections but with the use of canonic forms.

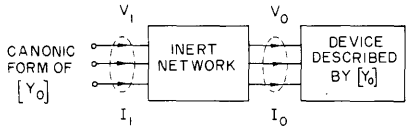

Fig. XXIII-3. Inert transformation of Y_o into Y_c.

network. It is the purpose of this report to consider some appropriate canonic forms for two- and three-terminal devices and to determine the power constraints for networks constructed from these components.

If we express the characteristics of the interconnection network by a chain matrix, we can readily derive some of the restrictions necessary to insure inertness. For the purpose of finding canonic forms, it is desirable to insist that this chain matrix be nonsingular. The matrix can be partitioned into four $n \times n$ square matrices A, B, C, D. Defining variables as in Fig. XXIII-3, we can write

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \qquad \begin{aligned} V_1 &= AV_o + BI_o \\ I_1 &= CV_o + DI_o \end{aligned}$$

Applying the inert restriction $P = 0$, we have

$$V_1^x I_1 = \left(V_o^x A^x + I_o^x B^x\right)(CV_o + DI_o) = V_o^x I_o$$

for all V_o and I_o. If $V_1^x I_1 = V_o^x I_o$ for all possible values of V_o and I_o, we must clearly have $A^x C = B^x C = B^x D = 0$, and $A^x D = I$. Thus A^x and D must be nonsingular, and hence $B = C = 0$. For convenience, we define $A = T_1^{-1}$, and then we see that $D = T_1^x$. Hence

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} T^{-1} & 0 \\ 0 & T_1^x \end{bmatrix} \begin{bmatrix} V_o \\ I_o \end{bmatrix} \qquad \begin{aligned} V_1 &= T_1^{-1} V_o \\ I_1 &= T_1^x I_o \end{aligned}$$

If we now express Y_1 in terms of Y_o, we have

$$I_1 = T_1^x I_o = T_1^x Y_o V_o = T_1^x Y_o T_1 V_1 = Y_1 V_1$$

and therefore

$$Y_1 = T_1^x Y_o T_1 \qquad Y_o = \left(T_1^{-1}\right)^x Y_1 \left(T_1^{-1}\right) \tag{1}$$

Equation 1 expresses the simple fact that Y_1 is a conjunctive transform of Y_o, and that Y_o is a conjunctive transform of Y_1; hence an inert transformation has an inverse so that all networks that are conjunctively equivalent to a given network are also conjunctively equivalent to each other. It is natural to expect that among all networks conjunctively equivalent to Y_o, there might be one with a particularly simple form. We could then choose this simple network, with relatively few variables, to represent a more general admittance Y_o. This simple network is a canonic form that completely

represents the more complicated network, as long as we allow any inert interconnection for circuit synthesis.

As an example,

$$Y_o = \begin{bmatrix} 1 & -1 \\ -1 & 0 \end{bmatrix} \quad \text{and} \quad Y_1 = \begin{bmatrix} -1 & j \\ -j & 1 \end{bmatrix}$$

are conjunctively equivalent. The transforming matrices are

$$T_1 = \begin{bmatrix} j & j \\ -1+j & 0 \end{bmatrix} \quad \text{and} \quad T_1^{-1} = \begin{bmatrix} 0 & -(1+j)/2 \\ -j & (1+j)/2 \end{bmatrix}$$

Thus networks described by

$$Y_1 = \begin{bmatrix} -1 & j \\ -j & 1 \end{bmatrix} \quad \text{and} \quad Y_o = \begin{bmatrix} 1 & -1 \\ -1 & 0 \end{bmatrix}$$

are identical as far as our assumed restrictions are concerned. Notice that we have a reciprocal admittance equivalent to a nonreciprocal admittance, and hence reciprocity is not preserved under an inert transformation. The Hermitian property of a network is preserved, however, as can be seen in this example.

If we go farther and ask for the simplest network equivalent to the Y_o and Y_1 of our example, we have the possibility

$$Y_2 = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \qquad T_2 = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix}$$

Although Y_2 is the simplest for this example, it is not, in general, possible to achieve this diagonal form. Simple and more general forms are

$$Y_c = e^{j\theta} \begin{bmatrix} 1 & 2a \\ 0 & 1 \end{bmatrix} \quad \text{or} \quad e^{j\theta} \begin{bmatrix} 1 & 0 \\ 0 & \pm 1 \end{bmatrix} \qquad \text{for } Y \text{ nonsingular}$$

$$Y_c = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \quad \text{or} \quad \begin{bmatrix} e^{j\theta} & 0 \\ 0 & 0 \end{bmatrix} \qquad \text{for } Y \text{ of rank 1}$$

Any Y_o can be converted to one, and only one, of the above forms. For the case in which Y_c is nondiagonal, we can use a slightly different form

$$Y_c = \begin{bmatrix} e^{\gamma} & 2 \\ 0 & e^{\gamma} \end{bmatrix} \qquad \gamma = \alpha + j\beta = -\ln|a| + j\theta$$

and hence a single complex quantity, γ, offers a complete description of Y_o. If $\alpha = -\infty$, we have the singular case, and if $\alpha = +\infty$, we have the equivalent of $a = 0$. The γ is closely related to the familiar γ of transmission-line theory, and $-\alpha$ indicates that there will be gain if a signal is applied at the appropriate terminal pair and a matched load (not conjugate matched) is applied at the other terminal pair. There is also a close relation between γ and the unilateral gain of S. J. Mason, $u = e^{-2\alpha}(\cos\beta)^{-2}$. It can also be shown that the region of the complex plane in which $\alpha \leq 0$ is the same as the region of possible natural frequencies for networks constructed from devices equivalent to Y_c only.

A detailed proof of these comments is included in a monograph that is being prepared for publication, but a simple example can be given now.

3. Transistor Example

A transistor can often be approximated by the model shown in Fig. XXIII-4. The admittance matrix is, then

$$Y = \frac{1}{r}\begin{bmatrix} 1 & 0 \\ \frac{\omega_o}{s} & rC(s+\omega_o) \end{bmatrix} \tag{2}$$

Calculating γ, we find that

$$2\gamma = \ln 4rC(s+\omega_o)\,|s|^2 - \ln\left[\omega_o^2 + 2rC|s|^2(|s+\omega_o| - \sigma - \omega_o)\right]$$

The region of allowed natural frequencies for networks containing only transistors of

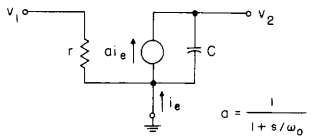

Fig. XXIII-4. Transistor model.

this type is the region bounded by the equation $2rC|s|^2(|s+\omega_o|+\sigma+\omega_o) = \omega_o^2$. The maximum frequency of sinusoidal oscillation can be determined by letting $\sigma = 0$. Thus

$$\frac{rC}{\omega_o^3}\omega^6 + \omega^2 - \frac{\omega_o}{4rC} = 0 \qquad \text{for } \omega = \omega_{max} \tag{3}$$

This expression is different from the more familiar relation

$$\omega_{max} = \frac{1}{2}\left(\frac{\omega_o}{rC}\right)^{1/2} \tag{4}$$

because the derivation of Eq. 4 assumes that inductors and capacitors are available.

R. D. Thornton

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1. O. Brune, Synthesis of reactance four poles, J. Math Phys. 10, 191 (1931).

2. H. W. Bode, Network Analysis and Feedback Amplifier Design (D. Van Nostrand Company, Inc., New York, 1945).

B. LOW-ORDER FREQUENCY MULTIPLIERS

Leeson and Weinreb (1, 2) have developed a theory for frequency multiplication which utilizes the nonlinear capacitance of a semiconductor diode. It has been found that frequency doublers have an optimum efficiency of approximately -1 db. If three doublers were cascaded to multiply by eight, it would be reasonable to expect an efficiency of approximately -3 db.

Since cascading requires impedance matching between stages, it is desirable to make the input and output impedances of all stages equal. This factor has led

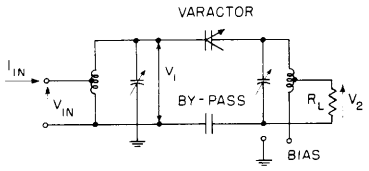

Fig. XXIII-5. Impedance matching circuit.

to the study of the circuit of Fig. XXIII-5. Using a fixed-load resistance R_L, and a fixed bias, we have tested the circuit to determine the variation of efficiency and input resistance as a function of the input signal level, and as a function of the settings of the coil taps. Some representative results are shown in Fig. XXIII-6.

It has been found that the peak efficiency of this circuit depends principally on the Q of the output tuned circuit (setting of the output coil tap). Conversely, varying the input coil tap has little effect on the circuit efficiency, but the transformer action makes it possible to change the input resistance of the circuit.

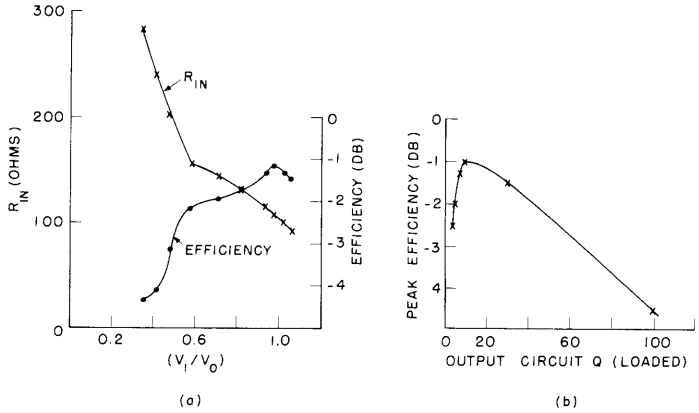

Fig. XXIII-6. Variation of efficiency and input resistance as a function of input signal level and of the settings of coil taps.

Present studies indicate that doublers of the type shown in Fig. XXIII-5 can be easily designed and adjusted one at a time, and then finally connected together in cascade to give the desired result. Further studies are in progress to determine the best procedure for designing cascaded frequency multipliers.

B. L. Diamond

References

1. D. B. Leeson and S. Weinreb, Frequency multiplication with nonlinear capacitors, Quarterly Progress Report No. 53, Research Laboratory of Electronics, M.I.T., April 15, 1959, p. 203.

2. D. B. Leeson and S. Weinreb, Nonlinear reactance frequency multipliers, Quarterly Progress Report No. 54, Research Laboratory of Electronics, M.I.T., July 15, 1959, p. 200.