Current Mode Linear Driver for High Energy Physics Applications

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***Abstract*—A single-ended to differential linear current driver has been designed and implemented in a 0.25 μm CMOS technology. This full-custom cell is intended for analogue data transmission in large-scale High-Energy Physics (HEP) experiments in the future CERN's Large Hadron Collider (LHC). Intrinsic technology radiation tolerance and specific design methodologies qualify this device to operate over 10 years in the LHC high radiation environment. High linearity and low power-overhead are achieved through a local feedback input stage and a current push-pull output stage. Linearity error is less than 0.1% in the specified operating range and 1% in close to full-swing operation. Static, dynamic and noise performance have been proven to be stable after a total ionising dose of 20 Mrad (SiO_2) and after accelerated annealing.**

***Index Terms*—CMOS analog integrated circuits, current measurement, data acquisition, driver circuits, radiation hardening.**

I. Introduction

In some data acquisition systems, it is desirable to perform the A/D conversion of the analogue signals representing the physical quantities being measured in a remote location. This is the case when power constraints in the measurement site impose the reduction of power dissipating elements, or when the measurement site represents a harsh environment for the electronic devices. Such are conditions commonly encountered in modern High Energy Physics (HEP) experiments where the electronics equipment is required to be tolerant to total doses exceeding 10 MRad over 10 years [1]. In these cases it is desirable to transmit the electrical signals to a distant location where A/D conversion can be made free from the above mentioned constraints. The signal has to be transmitted to the signal processing elements with a high degree of fidelity and with minimal electrical interference.

In the application targeted by this work, the measurement device produces an output current that is directly proportional to the electrical charge deposited by an ionising particle on a silicon micro-strip detector element [2]. It was chosen to convert this current into a differential current signal and transmit it to the next element in the chain using a low impedance transmission line (100 Ω), as is represented in Fig. 1. The current signal is converted to a voltage by the termination impedance, before it is fed to the next element in the signal chain that can be either an A/D converter or the input to another element in the communication channel for transmission over longer distances [3], [4].

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This configuration is known to have low noise sensitivity and noise radiation.

In the following sections, an implementation of a linear single-ended to differential current driver is described and its performance is fully evaluated.

II. Principles of Operation

A basic differential current driver (providing bipolar current signals) can be implemented using a differential pair stage as suggested in Fig. 2. The input impedance $\mathbf{Z}_{\rm in}$ converts the input current into a voltage $\mathbf{V}_{\rm in}$ (the signal source being, for the moment, assumed to be floating). The voltage $\mathbf{V}_{\rm in}$ is then transformed by the non-linear transconductance $\mathbf{G}_{\rm m}$ of the long tail pair, to generate the desired output currents $\mathbf{I} = \mathbf{G}_{\rm m}(\mathbf{V}_{\rm in})$. If the input impedance $\mathbf{Z}_{\rm in}$ is made to be the inverse function of $\mathbf{G}_{\rm m}(\mathbf{V}_{\rm in})$, that is $\mathbf{Z}_{\rm in}(\mathbf{I}) = \mathbf{G}_{\rm m}^{-1}(\mathbf{I})$, then the overall relationship between input and output currents is linear.

To see how the non-linear input impedance $\mathbf{Z}_{\rm in}(\mathbf{I}) = \mathbf{G}_{\rm m}^{-1}(\mathbf{I})$ can be implemented, let's consider the case of a general non-linear transconductor represented in Fig. 3(a). If feedback is implemented around it to form an unity-gain follower, as shown in Fig. 3(b), then the relation between the input voltage ($\equiv$ output voltage) and the input current is $\mathbf{I}_{\rm in} = \mathbf{G}_{\rm m}(\mathbf{V}_{\rm in})$, that is $\mathbf{V}_{\rm in} = \mathbf{G}_{\rm m}^{-1}(\mathbf{I}_{\rm in})$, the desired non-linear dependence between the input current and the input voltage. If two transconductors are connected as shown in Fig. 3(c), and if $\mathbf{G}_{\rm m2}(\mathbf{V}_{\rm in}) = \mathbf{K}\cdot\mathbf{G}_{\rm m1}(\mathbf{V}_{\rm in})$, then linear current amplification with gain $\mathbf{K}$ is achieved. This is a general principle independent of the type of non-linearity and of the particular transconductor implementation: it is the operation principle of a current mirror. The transconductor of Fig. 2 is connected as shown in Fig. 3(c) to implement a *differential current mirror*.

The circuit of Fig. 3(c) can also be used to implement a single-ended to differential conversion stage, if connected as shown in Fig. 4(a). In this case the signal source is taken between one of the inputs and signal ground (instead of across both input terminals) and a low impedance signal path (ideally 0 Ω) is added to the other node of the input transconductor. Here, the voltage generated by the "$\mathbf{Z}_{\rm in}$ " stage still displays the desired non-linearity but it is no longer "strictly" differential. However, the common mode voltage changes are rejected by the following differential gain stage. Straightforward implementation of this topology is represented in Fig. 4(b). Notice that, besides providing a low impedance signal path to ground, $\mathbf{Z}_{\rm low}$ is also used to set the desired operation point (in terms of voltage) for the differential pair. The two current sources present in this topology ($\mathbf{I}_{\rm bias}$ and $\mathbf{I}_{\rm bias}/2$) must be matched in order to reduce the circuit offset to a minimum. The input signal range is limited to $-\mathbf{I}_{\rm bias}/2 < \mathbf{I}_{\rm s} < +\mathbf{I}_{\rm bias}/2$.

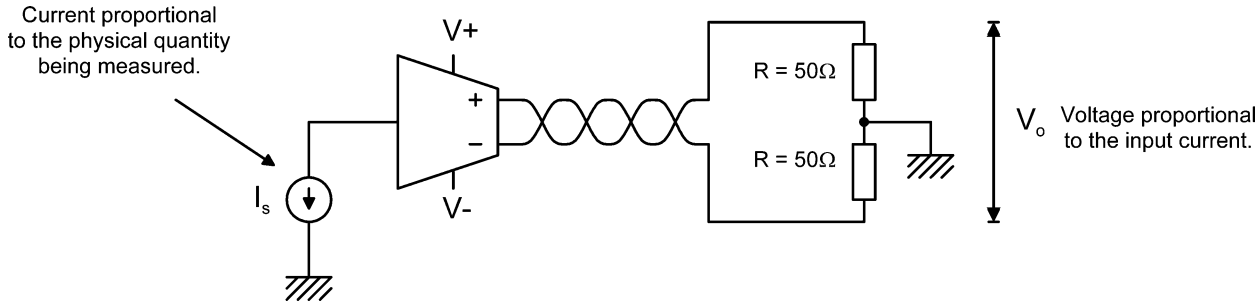


Fig. 1. Signal flow.

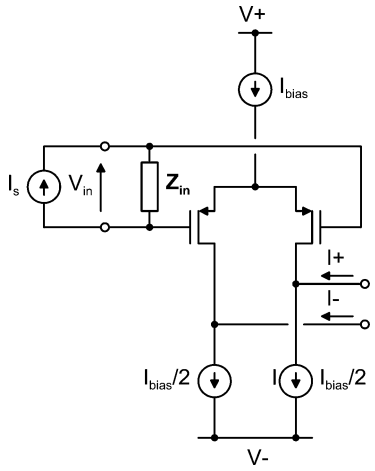


Fig. 2. Basic differential current driver using a differential-pair.

Alternatively, the topology of Fig. 4(c) can be used. In this case, the NMOS current mirror balances the transconductance stage in the absence of signal (that is, $\mathbf{I}_s = 0$) and allows for symmetrical current swings around zero. The current mirror implements at the same time the low impedance signal path to ground from one of the two inputs. Besides, this scheme has a current gain reduced to one half, since only half of the signal current $\mathbf{I}_s$ circulates in every transistor, i.e., $\mathbf{\Delta I} = \mathbf{I}_s/2$ (from Fig. 4(c), by equating the currents in the two mirror branches, summing the currents at the input node, and solving for $\mathbf{\Delta I}$). The input signal range, however, is doubled ($-\mathbf{I}_{\rm bias} < \mathbf{I}_s < +\mathbf{I}_{\rm bias}$), so that the output dynamic range is the same.

From the large signal transconductance view-point, it actually turns out that, due to the presence of the M3-M4 current mirror, the signal current can be applied indistinguishably either to the gate of M1 or M2. In the final implementation, it was chosen to use the gate of M1 as the input node. This node has the advantage of providing intrinsically lower impedance due to the presence of the diode-connected transistor M3.

III. Circuit Description and Layout

The final circuit is shown in Fig. 5. The circuit has been implemented in a commercial 0.25 μm n-well CMOS digital technology that requires a power supply of ± 1.25 V, leaving limited room for the voltage swings. The differential pairs are implemented using PMOS transistors with the bulk contacts tied to the sources (bulk-effect free). As compared to the basic linear single-ended to differential converter implementation (shown Fig. 4(a)), a few extra features have been introduced:

a) The output circuit is a differential push-pull stage where each output node is connected to a pair of PMOS/NMOS transistors, which are driven in opposition of phase. The output current swing results to be the double of the current swing in each transistor, and thus the tail current of the differential pair can be as low as the maximum output current swing required (I). In this circuit, all the output transistors play an active role. The overall power dissipation is thus reduced when compared with that required by the simpler scheme of Fig. 2. In practice, however, some margin is taken to ensure that the linearity requirements are satisfied over the entire operating range. Moreover, the push-pull topology requires an intermediate stage to generate the control signals for the NMOS transistors in the push-pull stage. This intermediate stage has the secondary effect of delaying the half-wave in the lower part of the circuit. Depending on the frequency range of operation, care must be taken so that this effect does not have an impact on the overall dynamic performance of the circuit. For our application (settling time < 10 ns), some non-negligible power had to be invested to improve the intermediate stage dynamic response. However, the net power dissipation is still 25% less than for the standard differential-pair output, with an overall current gain of $\mathbf{K} = 10$.
b) All the NMOS current mirrors are implemented using the basic cascode configuration. This improves the precision of the circuit and reduces the output offset to a minimum. The output impedance of the circuit is still dominated by the differential pair output conductance of the PMOS transistors. The use of cascode NMOS transistors in the input stage also allows to naturally voltage bias the input differential pair close to half of the power supply voltage.
c) The differential-pairs tail currents are mirrored from a single reference, which is implemented using a standard $\mathbf{V}_{\rm T}$-reference circuit [5]. Since all transistor sizes are scaled with the bias currents, that is, the current densities are kept constant, the $\rm V_{ds}$ voltage of the PMOS tail current sources are identical and the current mirroring operation is done with the accuracy of a cascoded current mirror. Nonetheless, the output common mode voltage is set by the external load (see Fig. 5). If this voltage is made to be too close to either of the power supply rails, then the output transistors will leave the saturation

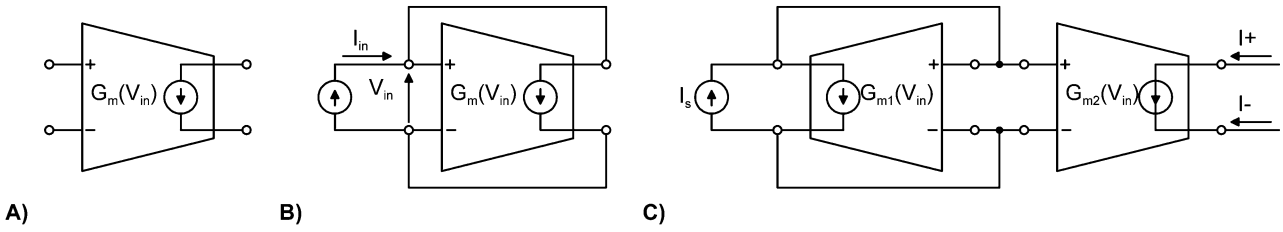


Fig. 3. Transconductor linearisation technique.

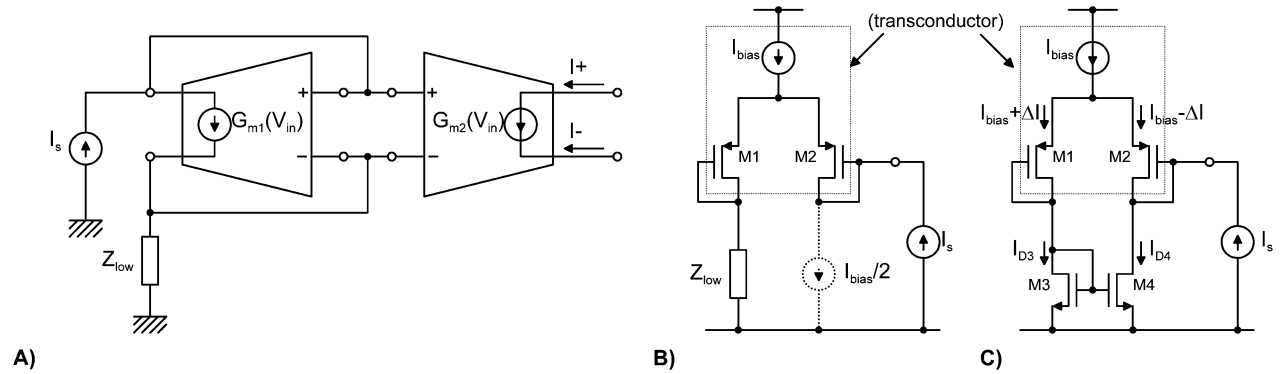


Fig. 4. Using the linear connected transconductors to obtain single-ended to differential conversion.

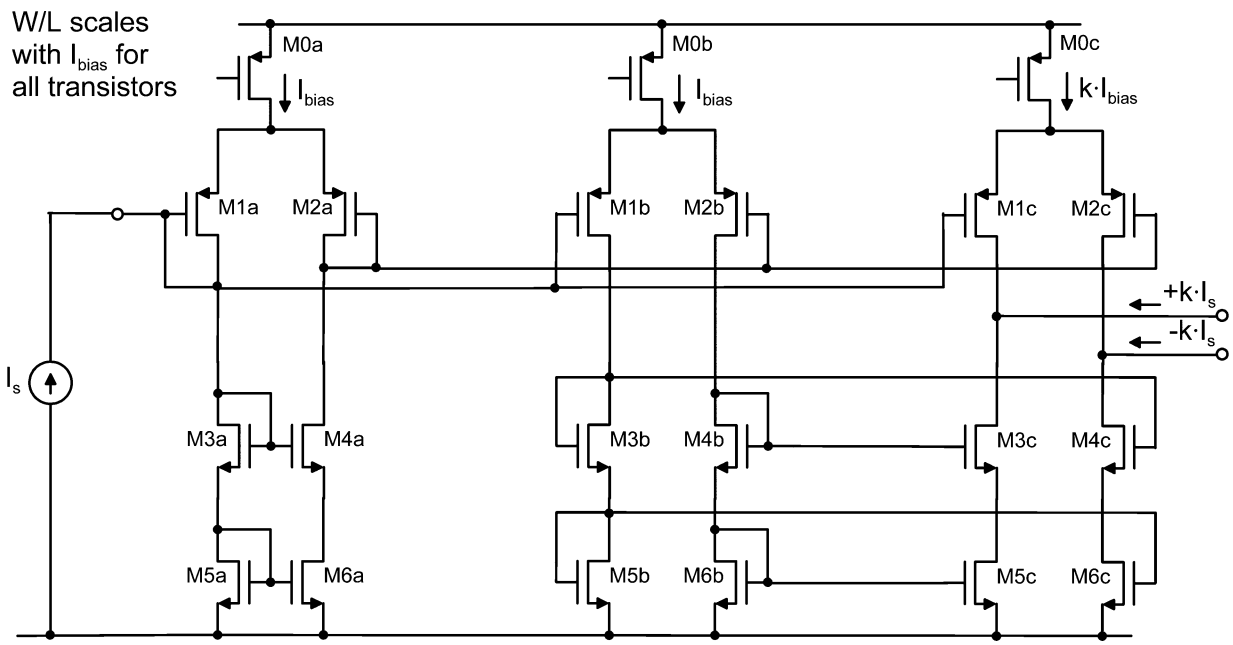


Fig. 5. Linear single-ended to differential current driver.

region and a current mirroring error will result that will degrade the linearity performance of the driver. This effect will be illustrated in the following section by a set of measurement results.

The circuit has been implemented both as a stand-alone test structure and as part of a complete system [6]. Particular care has been taken to match the three differential pairs and the three current mirrors. A micrograph of the circuit implemented as a stand-alone test structure is shown in Fig. 6.

The radiation tolerance results from the use of specific layout techniques and from the use of commercial deep submicron technologies. On the one hand, the systematic use of Enclosed Layout Transistors (ELT) and isolation guard-rings prevents the formation of parasitic radiation-induced conductive channels between source and drain terminals in the same transistor or between terminals in adjacent transistors. This is a long known technique for effectively preventing leakage currents in irradiated integrated circuits [7], [8]. On the other hand, the ultra thin gate oxides encountered in modern deep submicron technologies (such as the 0.25 μm CMOS that was used in this project) feature much better intrinsic tolerance to total dose radiation than those used in previous less advanced technologies. Overall,

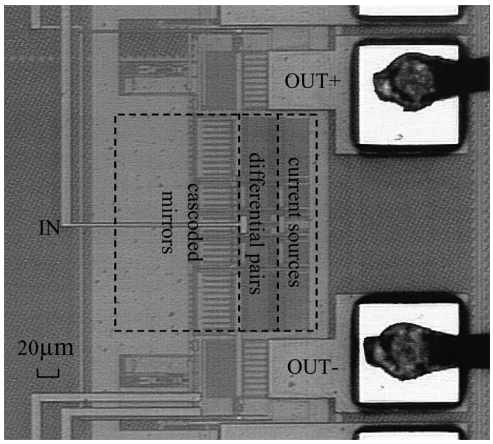


Fig. 6. Micrograph of the circuit.

modern technologies associated with extended layout and simulation practices (supporting the use of ELT transistors) have the potential to match the radiation tolerance required for the application in the HEP experiments. A vast documentation has been produced in the context of the CERN RD49 research and development program targeted at providing the HEP community with design tools, models and experimental evidence of the improved radiation tolerance [9]–[11].

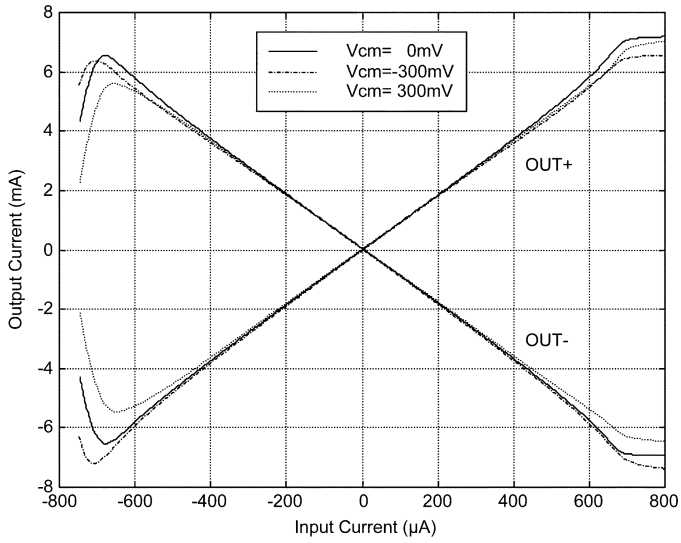
IV. Experimental Results

The linear single-ended to differential converter has been tested extensively for static, dynamic and noise performance. Results are presented for a typical channel. Differences from channel to channel have been shown to be very limited.

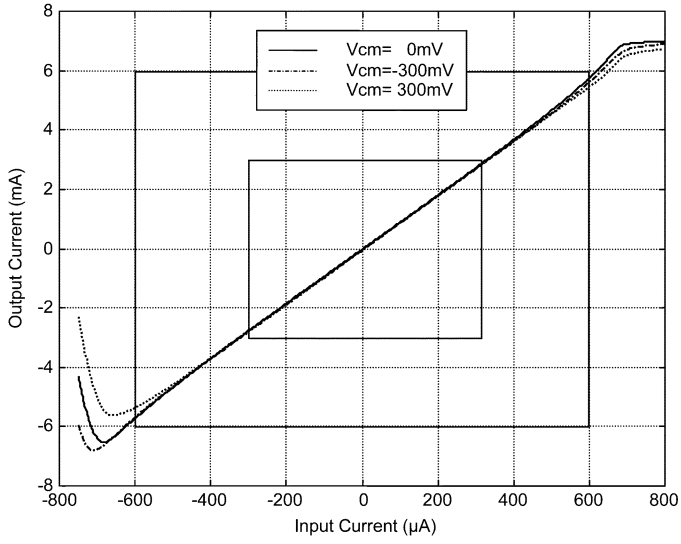
The driver cell was designed to transmit a stream of analogue sampled data from different channels, at a rate of 40 Ms/s. Each analogue data block is preceded by a digital header, for both channel identification and signal synchronisation [2]. In this scheme, ± 4 mA pulses are used to transmit the digital header while the analogue samples typically modulate the output current in the ± 3 mA range. The output stage of the circuit has been sized for $\mathbf{I}_{\rm bias} = 6$ mA, in order to achieve optimum linearity (to better than 0.1%) in the ± 3 mA range and to allow modulation of the output current up to ± 6 mA.

The static performance of the devices has been measured with a semiconductor parameter analyser. Each current output was terminated on a 50 Ω resistor to ground, and both currents and voltages across the resistors were measured while the input current was being swept.

Fig. 7 shows the static transfer characteristics of the circuit. In particular, Fig. 7(a) shows the output double-ended current and Fig. 7(b) shows the output differential voltage across the load, as a function of the input current, for different output common-mode voltages. Fig. 8 shows the corresponding linearity error, calculated as the absolute difference between the real output current and its linear fit. The linear error is expressed as a percentage of the specified operating range (integral nonlinearity). The error is less than 1% in close to full-swing operation (± 6 mA) and less than 0.1% in the ± 3 mA output current range. The output common-mode voltage has some impact on linearity. However, performance degradation is negligible for an



(a)



(b)

Fig. 7. Transfer characteristics: (a) double-ended output current, and (b) output differential voltage (on 100 Ω) versus. single ended input current, for different values of the output common-mode.

output common mode between ± 300 mV. If an integral nonlinearity of 1% was accepted over the smaller range, the output common mode could be extended to ± 50 0 mV.

The time response has been measured with input pulses of different widths and frequency. The step response exhibits very little overshoot and ringing, and the measured rise and fall times are within 3.6 and 4.4 ns. Fig. 9 shows a 5-levels eye diagram, with 25 ns pulses continuously sent at a 40 Ms/s rate.

The noise has been measured with a large bandwidth instrument. The equivalent input noise is 0.8 μA. The measured power consumption is between 25 mW and 30 mW.

Three identical cells on a same chip have been irradiated from an X-ray source, to investigate possible performance degradation related to ionising effects. The experiment has been carried out according to ESA/SCC recommendation for IC qualification with respect to total dose effects [12]. The chip has been irradiated in three steps, up to 1 Mrad, 10 Mrad, and 20 Mrad (SiO_2)

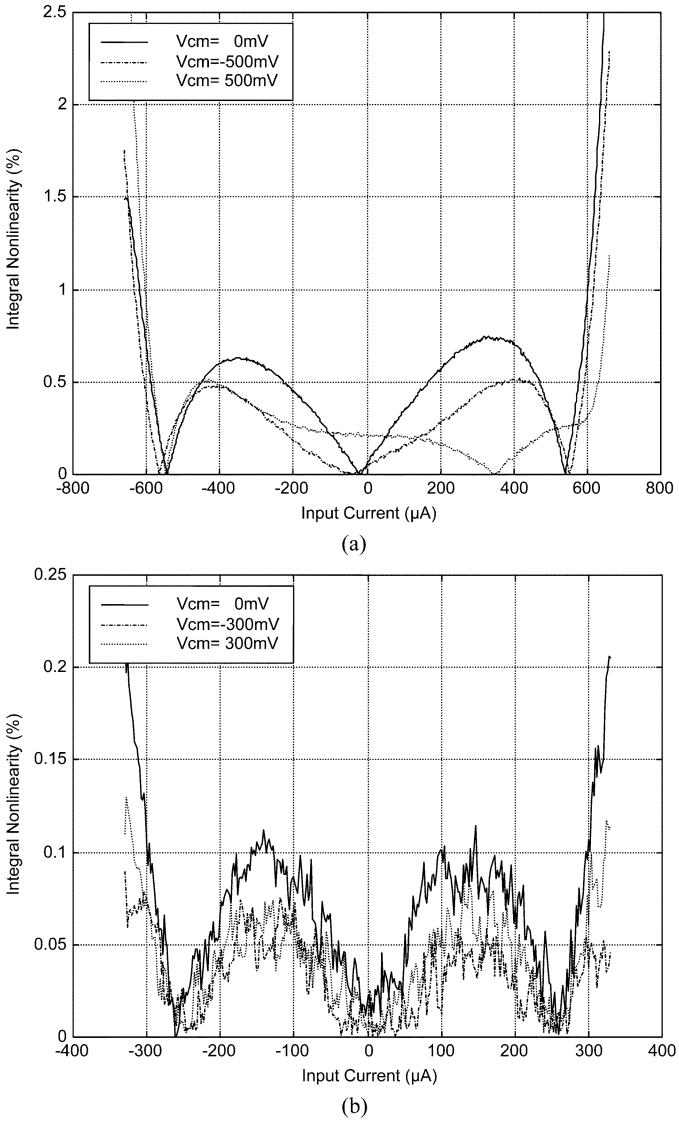


Fig. 8. Integral non-linearity for different values of the output common-mode and different operating modes: (a) maximum signal swing and (b) sampled data range (improved linearity).

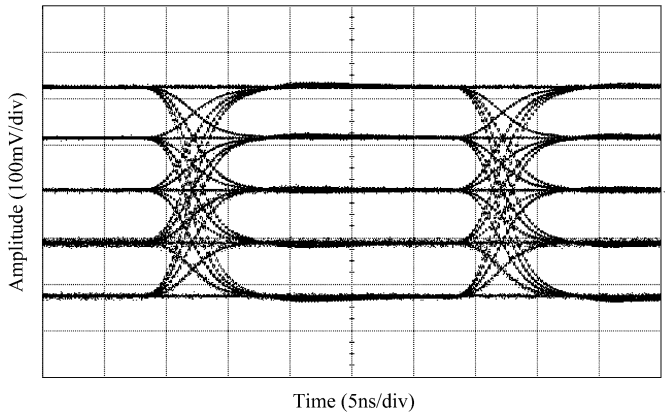


Fig. 9. Multi-level 'eye' diagram of the output differential voltage (measured over 100 Ω).

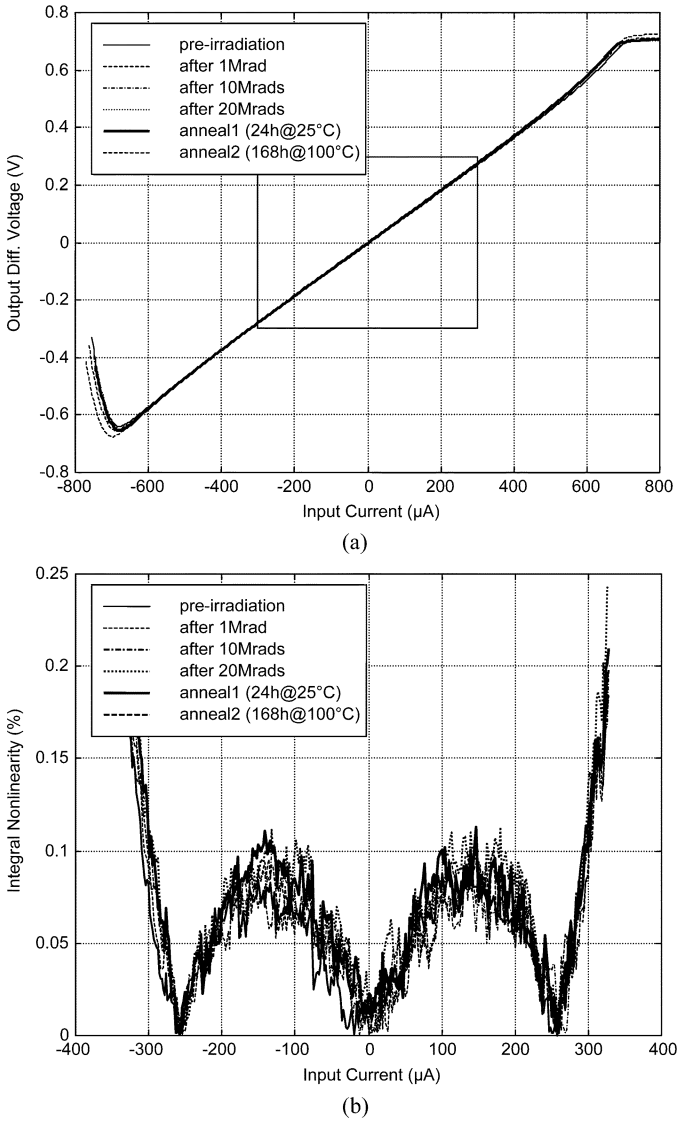


Fig. 10. Output differential voltage (a) and corresponding integral non-linearity (b) during qualification for total dose hardness (ESA recommendation).

respectively, at a constant dose rate of 21.2 Krad/min. After irradiation the chip has annealed for 24 hours at room temperature, and then for 168 hours at 100°C. The full set of static and dynamic measurements has been carried out after each step in order to assess any change or evolution in performance. The chip was under nominal bias during the irradiation. Fig. 10 shows the evolution in static performance, with 0 V common mode voltage on the outputs. Fig. 10(a) shows the output differential voltage across 100 Ω, and Fig. 10(b) shows the corresponding integral non-linearity. Any change is hardly visible on these plots, the linearity error being always in the order of 0.1% over the analogue amplitude modulation range (-3 mA to $+3$ mA).

V. Conclusion

A linear current-mode driver was designed for analogue data transmission in HEP-Experiments. The circuit has been developed and produced, both as a stand-alone device and as an output buffer cell in a complex analogue-processing chip. A commercial 0.25 μm CMOS technology was used for this purpose. A local feedback circuit solution proved to be efficient in combining very good linearity with minimal

power dissipation. Dynamic performance (time response and noise) has been scaled to the needs of the present application. The intrinsic radiation tolerance of the thin oxide combined with specific layout methodologies, succeeded in making the device reliable for application in a harsh radiation environment. Analogue performance remained basically unchanged, even after 20 Mrad (SiO_2) of total ionising dose.

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