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# Impact of 24-GeV Proton Irradiation on 0.13-$\mu$m CMOS Devices

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***Abstract*—We studied the response of a commercial 0.13-$\mu$m CMOS technology to high-energy (24-GeV) proton irradiation, which emulated the environment the front-end electronics of future high-energy accelerators will have to operate in, for fluences up to $10^{16}$ p/cm$^2$. After irradiation, large negative shifts in the threshold voltage and large drops in the maximum transconductance were observed in PMOSFETs, whereas comparatively smaller effects were present in NMOSFETs. Furthermore, both kinds of devices exhibited an increase in the drain off-current and in the gate leakage current. All the observed effects were roughly proportional to the proton fluence. For the PMOSFETs only, the amount of the degradation depended on the device channel length. The changes in the characteristics of the irradiated devices were attributed to the build-up of positive charge in the LDD spacer oxide and to the creation of defects in the gate oxide.**

***Index Terms*—CMOS, high-energy physics experiments, ultra-thin gate oxides.**

## I. Introduction

TODAY, the most challenging project in high energy physics (HEP) is the Large Hadron Collider (LHC) which is currently being built at the CERN laboratory in Geneva, CH and is expected to start operation in 2007. In the LHC, collisions between hadrons, i.e., subatomic particles that experience the strong nuclear force, will occur with unprecedented energy (14 TeV c.m. for protons) [1].

The electronic equipment necessary to the operation of this complex system will have to face severe conditions from a radiation standpoint. Yet, even the highest radiation levels expected for the LHC appear to be adequately matched by a solid quarter-micron commercial CMOS technology, modified to include radiation-hardening design solutions [2]. The steps taken to harden this 0.25 $\mu$m technology encompassed guard rings and transistors with enclosed layout. Though very effective at minimizing radiation induced leakage currents related to the lateral isolation [3]–[5], those measures meant a new cell library had to be developed, the cost of which was not trivial in terms of time and resources. Nevertheless, introducing a non rad-hard, commercial CMOS technology in a radiation harsh environment was necessary, given the scarcity of foundries for radiation-hard electronics.

As new technologies are introduced, older ones are phased out and the 0.25-$\mu$m technology will not be available forever. In addition to that, newer technologies offer better digital performance and, due to the thinner gate oxide, are inherently more radiation-tolerant, even though this does not necessarily reduce the need for drain-source leakage mitigation strategies. As a result, enclosed layout and guard rings may not be necessary anymore and standard cells may be used instead of undertaking the demanding task of porting the previously developed library to a more advanced technology.

Another important consideration is that any possible LHC upgrade would increase the experiment luminosity and consequently the radiation levels. For instance, as foreseen in the SuperLHC proposal [6], hadronic fluences as high as $10^{16}$ particles/cm$^2$ could be reached close to the beam line and in regions where frontend electronics could actually be placed, these fluences may be even higher. The suitability of any commercial CMOS technology for use in this extreme environment has never been demonstrated. Hence, there is a growing need in the HEP community to assess the suitability of commercial, state-of-the-art CMOS technologies to the extreme radiation challenge presented by future high-energy physics experiments, such as the SuperLHC.

The purpose of this study is to investigate the degradation of a commercial, non-hardened 0.13 $\mu$m CMOS technology following high energy (24 GeV) proton irradiation at very high fluences, up to $10^{16}$ p/cm$^2$. As a first step towards studying the suitability of these devices for use in the SuperLHC, we performed unbiased irradiation. This work will focus on actual MOSFETs designed with a standard layout, i.e., non-enclosed, as opposed to large capacitors often used for similar experiments. In the following, we will examine the responses of the devices in terms of DC characteristics as a function of the proton fluence, substrate type, and transistor geometry.

## II. Experimental and Devices

The devices used in this study were n-and p-channel MOSFETs manufactured by STMicroelectronics, Agrate Brianza, Italy in a commercial (non hardened) 0.13 $\mu$m CMOS technology. The gate oxide was oxynitride, its thickness 2.5 nm. The channel width (W) ranged from 10 $\mu$m down to 0.35 $\mu$m, the channel length (L) from 10 $\mu$m to 0.13 $\mu$m. The gate

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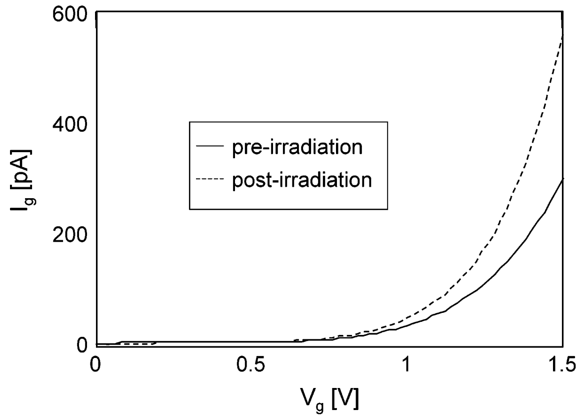


Fig. 1. Gate leakage current of an array of NMOSFETs ($\mathrm{total\ gate\ area} = 210\mu\mathrm{m}^2$) before and after 24-GeV proton irradiation with a fluence of $10^{16}$ p/cm$^2$($\mathrm{V_s = V_d = V_b = 0}$).

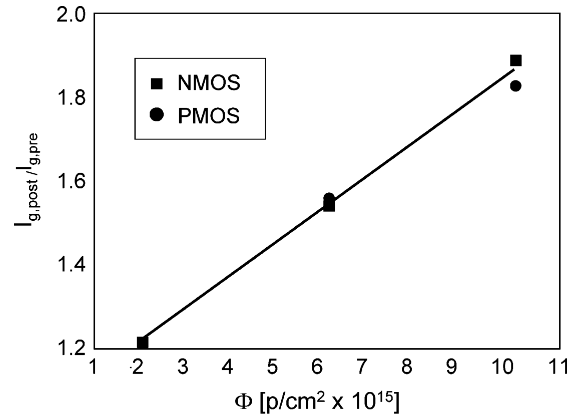


Fig. 2. Gate leakage increase as a function of the irradiation fluence for some arrays of NMOSFETs and PMOSFETs ($\mathrm{total\ gate\ area} = 210\mu\mathrm{m}^2$) irradiated with 24-GeV protons ($\mathrm{V_s = V_d = V_b = 0}$).

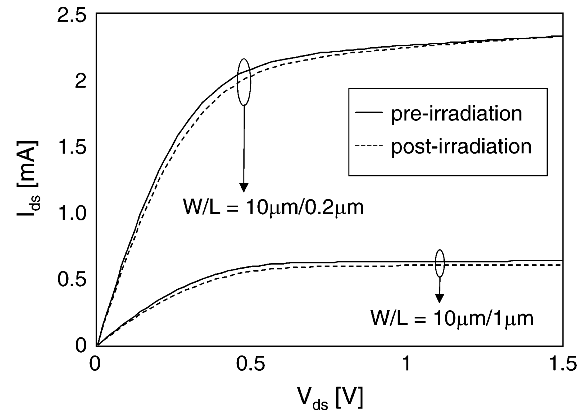


Fig. 3. $\mathrm{I_{ds}-V_{ds}}$ ($\mathrm{V_{gs}} = 1.2\mathrm{V}$) of two NMOSFETs with different aspect ratios, before and after 24-GeV proton irradiation with a fluence of $10^{16}$ p/cm$^2$.

electrode was n-doped (p-doped) polysilicon for p-substrate (n-substrate). Ligthly Doped Drains (LDD) were used to reduce hot carrier effects. The LDD spacers were made of nitrided oxide. Shallow Trench Isolation (STI) was used to isolate one device from the other. The transistors were arranged in arrays of given channel width or length with common gate, source, and bulk terminals and separated drain contacts. Some arrays were provided with a protection diode at the common gate. In the following we will refer to n-channel devices built on p-type substrates as NMOSFETs, and to p-channel devices built on n-type substrates as PMOSFETs. The 24-GeV proton irradiation was carried out at the CERN facilities [7] in Geneva, Switzerland, on May 2004. Three different fluences were used, namely $2.10^{15}, 6.10^{15}$, and $10^{16}$ p/cm$^2$. A total of more than 300 devices were measured, irradiated at the die level with all the terminals floating, and measured again after they cooled down to a safe level, at the beginning of 2005. Hence, about eight months elapsed between irradiation and post-irradiation measurements. During this time the devices were stored at $-20°$C to minimize annealing. The high fluence irradiation was unfeasible on packaged devices, since material activation would have prevented safe manual handling for several years. Before and after irradiation, the gate leakage ($\mathrm{I_g - V_g}$), transfer ($\mathrm{I_{ds} - V_{gs}}$) and output characteristics ($\mathrm{I_{ds} - V_{ds}}$) of the MOSFETs were measured.

## III. Results

### A. NMOSFETs

Fig. 1 shows the degradation of the gate leakage current in an array of n-channel MOSFETs with a total gate area of 210 $\mu$m$^2$ after 24-GeV proton irradiation with a fluence of $10^{16}$ protons/cm$^2$. After irradiation, the gate leakage current almost doubles. As Fig. 2 shows, the increase in gate leakage is proportional to the proton fluence. As can been seen from Fig. 3, where the $\mathrm{I_{ds} - V_{ds}}$ characteristics of two NMOSFETs with different aspect ratios, namely $\mathrm{W/L} = 10\mu$m/1 $\mu$m and $\mathrm{W/L} = 10\mu$m/0.2 $\mu$m, are plotted, the drain current is slightly reduced following proton irradiation. Fig. 4 displays the transconductance versus gate voltage for the same two devices of Fig. 3. Even though there is no shift in the curves, i.e., no change in the threshold voltage, the transconductance peak is significantly decreased. Transconductance peak drops as large as 10% are observed after the highest fluence irradiation. Fig. 5 displays the $\mathrm{I_{ds} - V_{gs}}$ characteristics of the same two samples. A moderate increase (hundreds of pA) in the off-current, i.e., the drain current for $\mathrm{V_{gs}} = 0$, and at the same time a small increase in the subthreshold swing are present.

After showing the phenomena occurring after irradiation, we now analyze the dependence of the degradation on the proton fluence and device geometry. Fig. 6 presents the reduction in transconductance as a function of the channel length and irradiation fluence for samples with fixed $\mathrm{W} = 10\mu$m. As far as the channel length is concerned, no clear dependence emerges from our data. All the devices are affected in a similar measure by the irradiation. On the contrary, a rough proportionality is observed between the induced damage and the proton fluence.

### B. PMOSFETs

Whereas the gate current degradation is quite similar, see again Fig. 2, significant differences appear in the behavior of the drain current of PMOSFETs as compared to NMOSFETs following high-energy proton irradiation. Fig. 7 displays the degradation of the $\mathrm{I_{ds} - V_{ds}}$ for two p-channel MOSFETs with the same aspect ratio ($\mathrm{W/L} = 10$ $\mu$m/1 $\mu$m and $\mathrm{W/L} =$

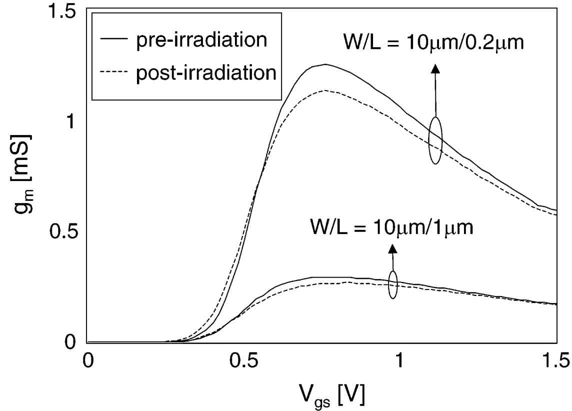


Fig. 4. Transconductance ($V_{ds} = 100$ mV) of two NMOSFETs with different aspect ratios, before and after 24-GeV proton irradiation with a fluence of $10^{16}$ p/cm$^2$.

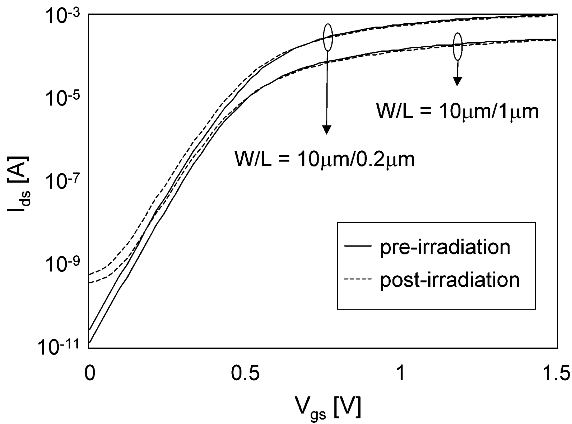


Fig. 5. Transfer characteristics ($V_{ds} = 100$ mV) of the same NMOSFETs of Fig. 1, before and after 24-GeV proton irradiation with a fluence of $10^{16}$ p/cm$^2$.

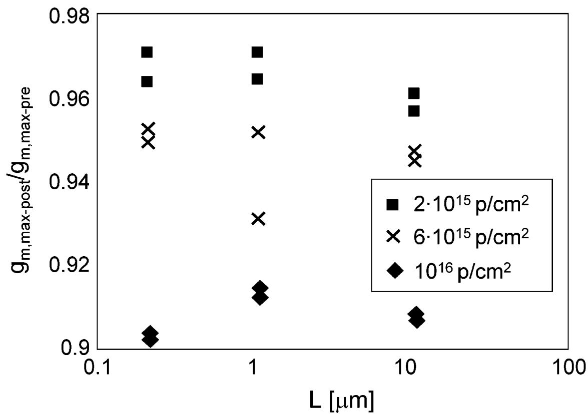


Fig. 6. Normalized transconductance degradation for several NMOSFETs with the same channel width (W= $10\mu$m) but with different channel lengths, after 24-GeV proton irradiation at three different fluences.

10 $\mu$m/0.2 $\mu$m) as the two NMOSFETs of Fig. 3. A large reduction in the saturation drain current is observed (even 40% in some cases). Fig. 8 displays the degradation of the transconductance versus gate voltage for the same two PMOSFETs of Fig. 7. In this case, the transconductance peak not only decreases, as in the case of NMOSFETs, but also shifts to lower values of $V_{gs}$.

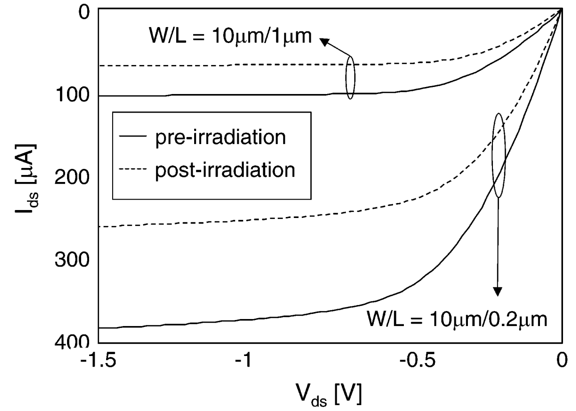


Fig. 7. $I_{ds}-V_{ds}$ (Vgs= $-1.2$V) of two PMOSFETs with different aspect ratios, before and after 24-GeV proton irradiation with a fluence of $10^{16}$ p/cm$^2$.

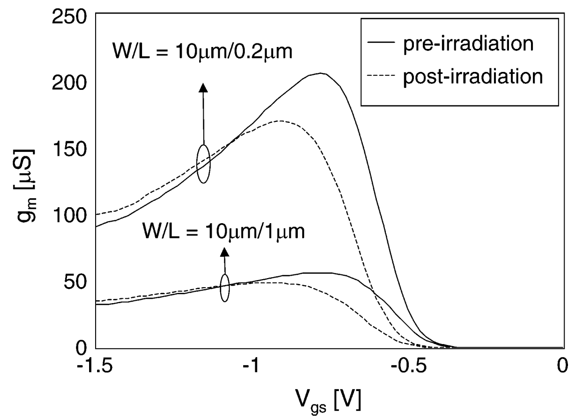


Fig. 8. Transconductance ($V_{ds} = 100$ mV) of two PMOSFETs with different aspect ratios before and after 24-GeV proton irradiation with a fluence of $10^{16}$ p/cm$^2$.

The shift in the threshold voltage is particularly remarkable and can be as large as 150 mV after the highest fluence ($10^{16}$ p/cm$^2$). The $g_m$ peak drop is also larger (up to 18%) than in nMOS devices. Fig. 9 displays the $I_{ds}-V_{gs}$ characteristics of the same two devices of Fig. 7: besides the already mentioned threshold voltage shift, it is interesting to observe that the subthreshold swing does not change appreciably following irradiation. Again there is a modest increase (some pA) in the off-current, although it is less pronounced than for NMOSFETs.

We now present the dependence of the radiation induced changes on the proton fluence and device geometry. Figs. 10 and 11 show the dependence of the transconductance peak drop and threshold voltage shift, respectively, on the channel length and irradiation fluence for samples with fixed W $=$ $10\mu$m. As far as the transconductance is concerned, short p-channel devices seem to suffer a higher degradation than long channel ones. As for the threshold voltage, the situation is reversed: long-channel devices exhibit a larger shift. Again a rough proportionality is observed between the induced damage and the proton fluence.

## IV. Discussion

One first observation is that all the effects described in the previous section (gate leakage and off-current increase, threshold

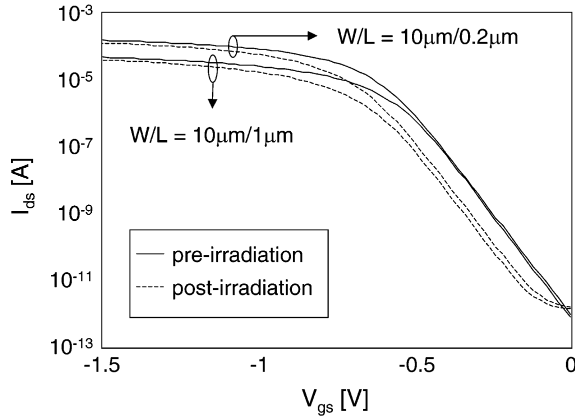


Fig. 9. Transfer characteristics ($V_{ds} = 100$ mV) of the same PMOSFETs of Fig. 4 before and after 24-GeV proton irradiation with a fluence of $10^{16}$ p/cm$^2$.

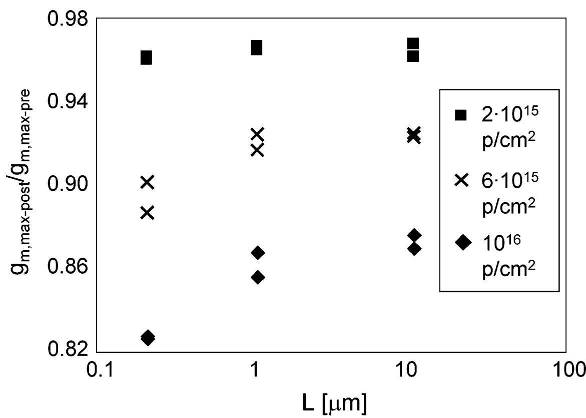


Fig. 10. Normalized transconductance degradation for several PMOSFETs with the same channel width (W= $10\mu$m) but with different channel lengths after 24-GeV proton irradiation at three different fluences.

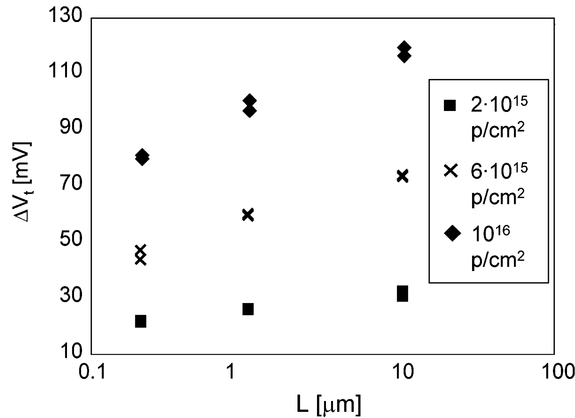


Fig. 11. Threshold voltage as a function of the channel length for PMOSFETs with the same channel width (W= $10\mu$m) at three different fluences.

voltage shift, and transconductance drop) depend on the irradiation fluence and are found to increase with it in a roughly linear way, Figs. 2, 6, 10, and 11.

In the following subsections, we will examine these changes occurring following irradiation one by one, comparing n-and p-type devices, but before doing so, we must make a couple of observations. Since the post-irradiation measurements were carried out eight months after exposure (due to safety reasons), it may be possible that some annealing took place in the elapsed time, even though as we mentioned before, the devices were kept at $-20°$C. Furthermore, the devices were left floating during irradiation, which may not be the worst case condition.

### A. *Gate Leakage*

The increase in gate leakage current (Figs. 1 and 2) can be ascribed to the creation of defects inside the gate oxide, a phenomenon which has been observed after irradiation with low LET particles (gamma and X rays, electrons, and low LET ions) and is known in literature as radiation induced leakage current [8]–[10]. The radiation-induced defects in the gate oxide act as "stepping stones" for the carriers that tunnel through the gate oxide, thus reducing the thickness of the barrier and increasing the gate current through trap-assisted tunneling conduction.

### B. *Off-Current*

The first effect of importance concerning the drain current is the increase in off current. The excess current which is present after irradiation in the NMOSFETs (Fig. 5) flows between the source and drain terminals and is likely due to the build-up of positive charge in the STI [3]–[5]. This positive charge causes the threshold voltage of the parasitic lateral transistors to decrease. Since the threshold of the "real" transistor is unaffected (Figs. 4 and 5) the net result is an increase in current for $V_{gs} = 0$. On the contrary, the excess current in the PMOSFETs (Fig. 9) flows between the drain and bulk terminals (as opposed to drain and source). This contribution may be present also in the NMOSFETs, but it is masked out by the parasitic transistors.

### C. *Threshold Voltage*

As far as the drain current of the devices after proton irradiation is concerned, one of the most striking feature is the difference between NMOS and PMOS devices. The large leftward shifts in the threshold voltage of PMOSFETs, Fig. 8, suggest the presence of positive charge somewhere in the proximity of the conducting channel. Yet, the same positive charge should cause a leftward shift of the transconductance peak in the NMOSFETs too, but that is not the case (Figs. 4 and 8). One possible explanation for this different behavior between NMOS and PMOS devices is that the threshold voltage is not altered "globally," i.e., everywhere in the channel, by the irradiation, but only "locally," i.e., in some parts of the channel along its length, for instance only close to the drain and source regions. In this way, after irradiation, when an NMOSFET is turned on by raising the gate voltage, the conducting channel would form first for $V_{gs} < V_{t,pre}$ close to the drain and source diffusions, and only later for $V_{gs} = V_{t,pre}$ in the remaining part. Since no conduction is possible when only a part of the channel is present, no change in the threshold voltage of the whole device is observed, so that $V_{t,post} = V_{t,pre}$. On the contrary, the conducting channel of PMOSFETs would form first in the central part, far from the source and drain diffusions, for $V_{gs} = V_{t,pre}$. Yet, without a connection to the source and drain, the transistor would remain off until the channel forms also close to the source and drain extensions for $V_{gs} < V_{t,pre}$, hence $V_{t,post} < V_{t,pre}$.

Local changes in the threshold voltage, namely close to the drain, occur also during channel hot carrier stresses [11].

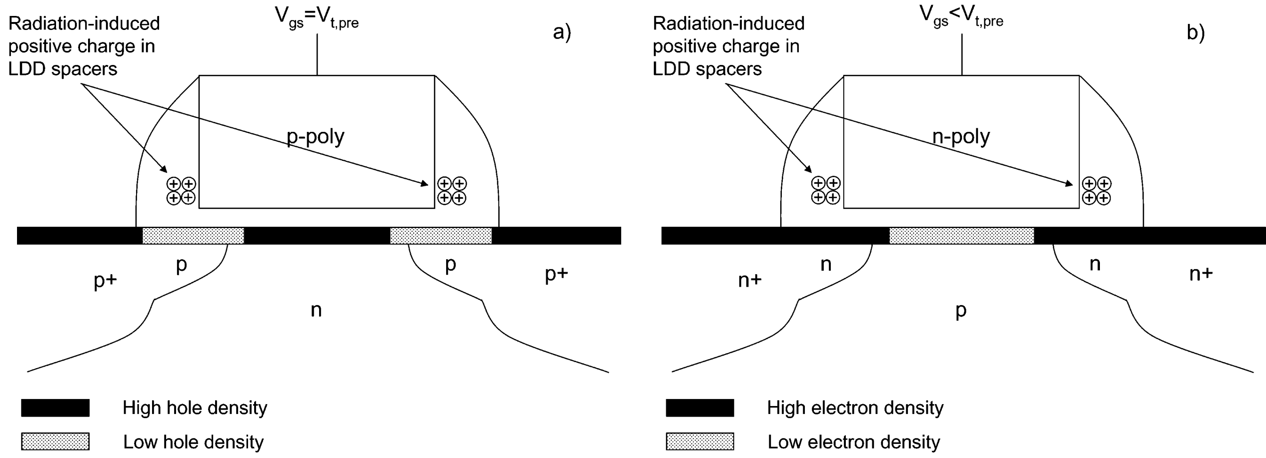


Fig. 12. Positive charge in the LDD spacers and its effect on the threshold voltage for (a) PMOSFETs and (b) NMOSFETs.

Whereas when the device is biased in the ohmic region the effects of a local change in $\mathrm{V_t}$ are indistinguishable from a global one, i.e., one that affects the whole gate area, in saturation one can tell if the change is local from the output resistance. If there is no decrease, then the $\mathrm{V_t}$ shift is global or, for accuracy's sake not localized to the terminal used as drain, otherwise it is localized there. No changes in the output resistance are present in our devices, see Fig. 7, but that is not because the shift is global, just because the damage is on both sides, i.e., both at the source and drain terminals.

As it is clear from the $\mathrm{I_{ds}}-\mathrm{V_{gs}}$ curves in semi-log scale, Fig. 8, the threshold voltage shift in the PMOSFETs is not due to a change in the subthreshold swing. This rules out the creation of interface states (or of any other defects that get charged and discharged with the gate voltage) as the reason for these shifts. So, it must be fixed charge.

As for the location of this fixed positive charge, it is unlikely that it is trapped in the gate oxide, because in that case the tunneling distance would be so short that it would be quickly neutralized. Given the fact that the shifts occur also in devices with large width ($\mathrm{W} = 10\mu\mathrm{m}$), one can also exclude that the cause is the charge in the lateral isolation responsible for the increase in the off current.

Instead, it is much more likely for trapped charge buildup to occur within the spacers used for the implantation of LDDs. These are made of a thick oxide and therefore prone to charge trapping. Fig. 12 schematically depicts the location of the trapped positive charge and its effects on the inversion layer for both PMOS and NMOS devices. As seen in the figure, the spacers are located above the LDDs, which are regions with a relatively low doping. The LDDs in the PMOSFETs are p-doped and the positive charge in the spacers tends to deplete them. If the charge in the LDD spacers is very large and the doping and size of the p-doped regions are small enough, the electric field generated by the charge in the LDD spacers will be felt also beyond the p-doped region, i.e., in the n-doped active region. If that is the case, the $\mathrm{V_t}$ of the MOSFET will change. A quantitative approach could better illustrate the point. Unfortunately, it is not possible to analytically solve Poisson's equation in a stack consisting of an oxide layer, an n-type (p-type) material, and a p-type (n-type) material, not even in one dimension, unless some large approximations are made. Nevertheless, even a simplified quantitative approach may be useful to illustrate our understanding of the problem in pMOSFETs. Assuming that $10^{12}$ q/cm$^2$ (a typical charge saturation density) positive charge is trapped in the LDD spacers and that the LDD doping is about $10^{17}$ acceptors/cm$^3$, the corresponding LDD depletion depth would be about 1 $\mu$m, which is far more than the depth of a modern LDD implantation. As a consequence, not all the trapped charge is simply mirrored by the LDD ionized acceptors, but an excess negative charge due to diffusing electrons from the n-substrate is needed to ensure a global charge neutrality below the LDD spacers. Due to the LDD full depletion, the trapped charge reverberates into an increase of the threshold voltage, as observed indeed.

Another interesting point is that, for the PMOSFETs, the threshold voltage shift increases with the channel length (Fig. 11). This is due to the fact that, before irradiation, $\mathrm{V}_{t,\mathrm{pre}}$ increases for decreasing channel length (at least in the range we analyze here) due to the halo implantation, whereas, after irradiation $\mathrm{V}_{t,\mathrm{post}}$ is independent of the channel length. As a consequence, the shift, $\Delta\,\mathrm{V_t} = \mathrm{V}_{t,\mathrm{post}} - \mathrm{V}_{t,\mathrm{pre}}$, is larger in the long channel devices. $\mathrm{V}_{t,\mathrm{post}}$ does not depend on L, possibly because it is determined by the charge trapped in the LDD spacers, which is independent of the channel length.

According to the view we presented here, the shift in the threshold voltage depends heavily on the trapping characteristics of the spacer oxide. Since there is not a single recipe for spacer oxides (for example for the amount of nitridation), large variations can be expected from one technology to the other, resulting in very different responses to high-energy proton irradiation.

### *D. Transconductance*

In general, the peak in the $\mathrm{g_m}-\mathrm{V_{gs}}$ curves of a MOSFET occurs when the device enters the ohmic region, i.e., when $\mathrm{V_{gs}}-\mathrm{V_t} = \mathrm{V_{ds}}$. In this region, the following relation holds [12]:

$$g_m = C_{\mathrm{ox}} \frac{W}{L} \frac{\mu_0}{1 + \theta_1 (V_{\mathrm{gs}} - V_{\mathrm{t}})} \cdot V_{\mathrm{ds}}. \qquad (1)$$

When $C_{ox}$ is the oxide capacitance per unit of area, $\mu_0$ is the low field mobility, and $\theta_1$ is the mobility attenuation. For high gate voltage, the transconductance is reduced because of the mobility degradation with the vertical field, which is accounted for by $\theta_1$, and the series resistance, which reduces the effective $V_{ds}$ [12]. So, there are two ways in which the irradiation can reduce the transconductance peak, either through the series resistance or through the mobility.

When the $g_m$ peak occurs, the drain current is quite low, so the voltage drop in the series resistance should be negligible and then have no impact on the transconductance peak. Furthermore, we can rule out the series resistance as the culprit also on the account of the NMOSFETs. As discussed in the previous section, the positive charge in the spacers changes the distribution of the carriers inside the LDD regions. This has an impact on the series resistance of the devices. In particular, the series resistance of the NMOSFETs should be reduced due to the higher density of carriers in the LDDs, whereas the one of the PMOSFETs should be increased. Since the transconductance drops also in NMOSFETs, the series resistance is probably not involved.

So, a reduction in mobility is the likely culprit for the observed degradation in the transconductance peak. The fact that the amount of the degradation depends on the channel length for the PMOSFETs, and in particular it decreases for increasing channel length, means that for PMOSFETs the mobility may be reduced more on the edges of the transistors, i.e., close to the drain and source regions, than in the center. On the contrary, there is no clear dependence on the channel length for the NMOSFETs, meaning the mobility is reduced all along the channel lentgh. However, in both cases the degradation for the device with $L = 10\ \mu m$, where edge effects should be negligible, is significant and of about the same amount in the two cases (compare Figs. 6 and 10), so there is a considerable contribution by the central part of the channel which seems to be independent of the substrate doping type.

As a result, we can split the reduction in mobility into two contributions, one independent of the channel length and present both in NMOSFETs and PMOSFETs, and the other of increasing importance for decreasing gate length and present only in PMOSFETs.

The first contribution can be related to the creation of interface traps in the gate oxide. This is probably true both for NMOSFETs and PMOSFETs, even though only in the first case there is direct evidence in the form of an increased subthreshold swing, Fig. 5. On the contrary, no or very little changes occur in the subthreshold region of PMOSFETs, but this can be explained by the fact that the behavior in the subthreshold region after irradiation is determined by the regions close to the drain and source, i.e., the last ones to turn on as we explained earlier, so it is less affected by defects in the central part of the channel.

The second mechanism which causes the additional degradation occurring in PMOSFETs may be attributed to the positive charge present in the LDD spacers. In fact, the electric field originating from it may increase the Coulomb scattering, thus reducing the mobility close to the source and drain. This contribution is not present in NMOSFETs because of the more effective screening of the positive charge by the LDD regions.

Furthermore, 24-GeV protons may provoke a variety of nuclear reactions with the emission of high-LET ions or neutrons which could give rise to an anomalous degradation in some devices from time to time. Some transistors may indeed deviate from the illustrated "typical" behavior (see for instance the two nominally identical samples with $L = 1\ \mu m$ of Fig. 6, one of which exhibits a larger-than-expected degradation).

Before concluding, we want to stress the fact that the mechanisms we presented here are still mere conjectures and that further evidence in the form of independent experiments or simulations is needed to say the final word about the causes of the degradation in these devices.

## V. Conclusion

We have shown for the first time the response of a commercial 0.13 $\mu$m CMOS technology to high-energy (24 GeV) proton irradiation for fluences up to $10^{16}$ p/cm$^2$, which emulate the environment expected in future high energy physics experiments for the front-end electronics. We irradiated MOSFETs with p-and n-type substrates and different aspect ratios. Though still completely functional, the devices exhibited several important changes after the exposure. The gate leakage and off current increased. Large shifts in the threshold voltage and large drops in the transconductance of PMOSFETs and to a much lesser extent of NMOSFETs were observed. In particular, the saturation drain current of the PMOSFETs seems to be the most critical parameter, dropping by as much as 40% after $10^{16}$ p/cm$^2$.

We attributed these changes to the build up of positive charge in the LDD spacers and to defects in the gate oxide.

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## References

[1] *LHC*, [Online]. Available: http://public.web.cern.ch

[2] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: Practical design aspects," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1690–1696, Dec. 1999.

[3] M. Turowski, A. Raman, and R. D. Schrimpf, "Non uniform total-dose-induced charge distribution in shallow-trench isolation oxides," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3166–3171, Dec. 2004.

[4] F. T. Brady, J. D. Maimon, and M. J. Hurt, "A scalable, radiation hardened shallow trench isolation oxides," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1836–1840, Dec. 1999.

[5] M. R. Shaneyfelt, P. E. Dodd, B. L. Draper, and R. S. Flores, "Challenges in hardening technologies using shallow-trench isolation," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2583–2592, Dec. 1998.

[6] F. Gianotti, Physics Potential and Experimental Challenges of the LHC Luminosity Upgrade Apr. 2002, hep-ph/0204087.

[7] M. Glaser, L. Durieu, F. Lemeilleur, M. Tavlet, C. Leroy, and P. Roy, "New irradiation zones at the CERN-PS," *Nucl. Instrum. Meth. Phys. Res. A*, vol. 426, pp. 72–77, 1999.

[8] A. Scarpa, A. Paccagnella, F. Montera, G. Ghibaudo, G. Pananakakis, G. Ghidini, and P. G. Fuochi, "Ionizing radiation induced leakage current on ultra-thin gate oxides," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 1818–1825, Dec. 1997.

[9] M. Ceschia, A. Paccagnella, A. Cester, A. Scarpa, and G. Ghidini, "Radiation induced leakage current and stress induced leakage current in ultra-thin gate oxides," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2375–2382, Dec. 1998.

[10] A. Cester and A. Paccagnella, Radiation Effects and Soft Errors in Integrated Circuits And Electronic Devices 2004, vol. 34, pp. 279–290.

[11] G. Groeseneken, R. Degraeve, T. Nigam, G. Van den bosch, and H. E. Maes, "Hot carrier degradation and time-dependent dielectric breakdown in oxides," *Microelectron. Rel.*, vol. 49, pp. 27–40, 1999.

[12] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electron. Lett.*, vol. 24, p. 543, 1988.