Implementation of the Timing, Trigger and Control System of the CMS Experiment

J. Troska, E. Corrin, Y. Kojevnikov, T. Rohlev, and J. Varela

***Abstract*—This paper presents the implementation of the Timing, Trigger and Control (TTC) system of the CMS Experiment currently under construction at CERN. The TTC system distributes the system clock for the experiment as well as the first level Triggers and synchronization commands. The overall system is described, highlighting the differences from the original concept of the CERN RD-12 collaboration in terms of overall system architecture. Details are given of the two VME-format electronics boards that implement the necessary functionality required by the system design changes.**

***Index Terms*—Command and control systems, high-speed electronics, particle collisions, timing circuits, trigger circuits, triggering.**

I. Introduction

THE Compact Muon Solenoid (CMS) Experiment [1] is currently under construction for operation at the CERN Large Hadron Collider (LHC). CMS is one of two General Purpose Experiments at the LHC that is designed to be able to measure the full spectrum of particle interactions available at the LHC. Accurate sampling of the particle transitions and assignment of detector data to the same interaction across many millions of detector channels require a high performance clock and control distribution system. The CERN RD-12 collaboration produced a system design capable of meeting this requirement that was adopted by all LHC experiments to some extent [2]. The key features of the Timing, Trigger and Control (TTC) system as developed by the RD-12 collaboration [3] are:

- Clock distribution with individual adjustable phase adjustment per destination.
- Clock distribution with low jitter (30–50 ps r.m.s.) at each destination.
- Provision of two independent channels for control commands.
- Clock and control data are Bi-Phase Mark (BPM) encoded and transmitted via an optical fiber distribution tree.

The key enabling parts that allow this system to achieve the required functionality are:

i) Low-jitter optical encoder and transmitter modules [2], [4].
ii) Optical fiber distribution network based on optical couplers.
iii) Radiation-tolerant Receiver ASIC (TTCrx) [5].

The TTC system as developed by the RD-12 collaboration fulfilled its design goals and parts of this system are used by all four LHC experiments (ATLAS [6], ALICE [7], CMS and LHCb [8]). All systems use the RD-12 components for the transmission and reception of signals, but each experiment implements a slightly different system for generation of the trigger and fast commands. The common system is also used by each experiment to receive the timing information from the LHC machine (40.0786 MHz bunch clock and orbit marker). In CMS, the design of the Trigger and Data Acquisition (DAQ) systems required further functionality that was not available from the TTC system in its original form [9]. The CMS TTC system is partitioned, allowing for certain geographically-distinct parts of the detector to be operated independently. While this was possible with the RD-12 system, the module at the head of a partition (called TTCvi) [10] imposed some limitations on the number of distinct fast commands that could be sent over the TTC system.

In the TTC system design, two command data channels are distinguished: A and B. Channel A is reserved for Trigger Accept commands that last a single clock cycle and are transmitted with minimum latency. Channel B is used to send framed commands that can: (i) be broadcast to all destinations; (ii) individually address the internal registers of the receiving TTCrx; or (iii) send data to external electronics connected to an individually addressed TTCrx. Fully framed B-channel commands can take either 16 or 42 clock cycles to transmit and are used to initiate processes vital for the synchronization of the different subsystems in CMS. In order to achieve this synchronization, the CMS TTC system requires sending of a larger number of distinct B-channel commands and is thus incompatible with the TTCvi module.

Furthermore, the RD-12 TTC system is clearly uni-directional. This means that status information vital to the smooth running of CMS data-taking cannot be collected by this system. CMS has thus developed a Trigger Throttling System (TTS) [11] to allow real-time response to synchronization-loss within the system.

II. CMS TTC System Implementation

For CMS, the basic distribution system architecture was maintained with a change to distribution via single-mode optical fiber rather than the original multimode design. The CMS TTC System architecture is shown in Fig. 1, illustrated for a single sub-detector TTC system containing three partitions.

Manuscript received June 19, 2005; revised March 10, 2006.

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Digital Object Identifier 10.1109/TNS.2006.874888

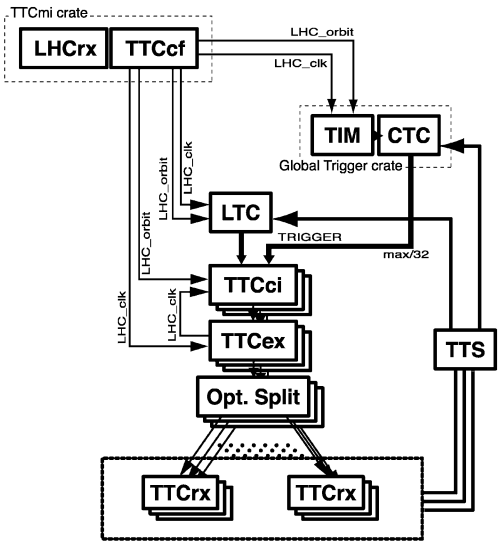

Fig. 1. CMS TTC distribution system. A single sub-detector tree consisting of three partitions is shown. See text for module descriptions.

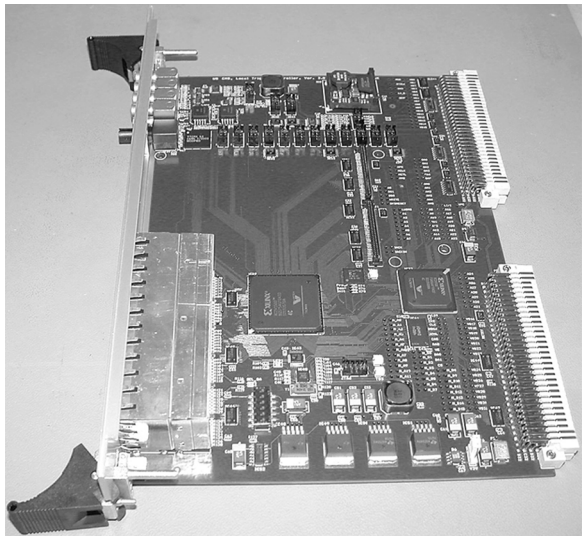

Fig. 2. Assembled LTC VME module. One can see the large number of connectors for I/O on the front panel and the two FPGA's used to implement the logic. The left-hand FPGA contains the logic for functional tasks while the right-hand one contains the VME interface.

The LHC bunch clock and beam orbit signals are received via the TTC Machine Interface (TTCmi) crate housing the LHC receiver (LHCrx) and TTC Clock Fanout (TTCcf) modules. The latter distributes the clock and orbit signals as single-ended, DC-coupled ECL logic to the various destinations within the CMS TTC system. At the top of each distribution tree, called a partition, the CMS-specific VME interface module (TTCci) decodes B-Go signals from either a Local- or Central Trigger Controller (LTC & CTC respectively). CMS defines 16 distinct B-Go signals (B-Go1 through B-Go16) that instruct the TTCci to transmit a particular framed command on the TTC B-channel [9]. As an example, B-Go1 corresponds to BC0 that resets the bunch crossing counters to mark the start of each LHC orbit. B-Go signals in CMS are LVDS logic signals lasting for a single clock cycle. A- and B-channels are encoded by the TTC encoder and transmitter (TTCex) VME module and sent via optical couplers (TTCoc) housed in the same VME crates to the TTCrx receivers that pass on clock and control information to the detector front-ends.

On the return path, CMS has a Trigger Throttling System (TTS) [9], [11] that allows the detector front-ends to report their synchronization status and whether their buffers remain sufficiently empty to receive further triggers. Four states are possible: Ready—ok to receive more triggers; Busy—Buffers are full, do not send more triggers; Warning—Buffers are almost full, reduce trigger rate; and Information is collected via the synchronous TTS (sTTS) from sub-detector electronics and via the asynchronous TTS (aTTS) from the DAQ. The two systems differ essentially in their latency, the aTTS having a longer latency, a fact that is mitigated by the larger buffers in the DAQ system.

The Global Trigger of CMS, that contains the CTC module, has been previously described [12], [13]. In this paper we will concentrate on the descriptions of the LTC and TTCci in the sections that follow.

III. CMS-Specific TTC Modules

Three new modules are required by the CMS implementation outlined above—two electronic and one optical. All three are VME format and are housed in VME crates under the control of individual sub-detectors.

A. Local Trigger Controller

The LTC allows for the operation of sub-detectors in stand-alone mode using the sub-detector Local DAQ (VME readout) and local triggers. This mode of operation is used in the test beams and during CMS commissioning and maintenance phases. The LTC controls the delivery of L1 Trigger Accepts depending on the status of the sub-detector readout systems and the data acquisition system. This status is derived from information provided through the Trigger Throttling System (TTS) and from the status of front-end Emulators. The LTC is also responsible for generating synchronization and fast reset commands, as well as to control the delivery of test and calibration triggers.

The LTC can control the TTC partitions of a sub-detector, replacing the Central Trigger Controller (CTC). The LTC controls up to six TTC partitions for which the control signals are identical. This means that each partition receives the same instructions from the LTC, in contrast to the CMS CTC which can provide different data to different partitions. The LTC thus allows the synchronous running of up to six partitions together.

The LTC is implemented as a double-width 6U VME module. The VME interface can be configured via jumpers to be either VME64x plug and play compatible or to read its base address from switch settings on the PCB. The fully assembled board is shown in Fig. 2.

The LTC logic design has split into two FPGAs: a Xilinx XC2V500 is used for the VME interface while a larger Xilinx XC2V1500 is used for the LTC state machine logic. The LTC

VME module is essentially size-limited by its input/output signals. It provides the following interfaces to other parts of the system:

1) Input to 6 external triggers (2 NIM; 4 LVDS).
2) Interface to LHC machine Clock and Orbit signals (two cables, ECL). Internal clock and orbit generation is possible.
3) Clock output (1) in ECL.
4) Interface to 6 TTCci modules, to distribute L1A and Fast Commands to the subdetector partitions (6 cables with 8 LVDS signals: L1A, B-Go3...0, Strobe, Orbit, Clock).
5) Interface to one TTCvi module: L1A (ECL), B-Go3...0 (NIM).
6) Interface to the sTTS to collect information on the status of the front-end electronics (6 cables with 4 bits parallel LVDS, RJ45).
7) Interface to Emulators: 4 cables to emulators, each sending Clock, L1A, BC0, L1 Reset, ECR, OCR. For each connection, 4bit, LVDS, RJ45 link.
8) Interface to the DAQ Event Manager (S-Link), to transmit L1A blocklet (Event Number, Partition, Trigger Type, Trigger bits).
9) Interface to the aTTS: 1 aTTS input and 1 aTTS output.
10) Interface to Beam Synchronous Timing system, one TTC input link to a dedicated TTCrx.
11) Interface to Run Control/Detector Control Systems (VME interface).

The LTC firmware is complete and has been functionally simulated during its design phase. The module has been successfully tested to provide accurate clock, trigger and command generation. The on-board clock is provided from a crystal-based PLL developed for TTC applications at CERN (QPLL [14]), which allows generation of a very low jitter clock reference and provides the means the tune the internal clock by ± 3.7 kHz around the LHC frequency of 40.0786 MHz. Measurements have shown that the Trigger latency is 4 bunch crossings. Generation of fast-commands has been verified to occur on the programmed bunch crossing within one orbit. More complete User-level software is currently being written to provide a simple Graphical User Interface.

B. TTCci

The TTCci (TTC CMS Interface) is the CMS version of the TTCvi module [9]. The TTCci is the top element of each of the 32 TTC partitions. It provides the interface between the (central or local) Trigger Controller and the TTC destinations for transmission of L1A and fast commands. Switching between central and local trigger control is achieved by software programming. For test purposes, the TTCci can operate in standalone mode. The TTCci can either deliver Channel A and Channel B signals to the TTCex for transmission and encoding if a large number of destinations must be served, or directly to a single optical distribution tree to up to 32 destinations via the on-board laser module.

Channel A is used to transmit L1A and Channel B is used to transmit framed and formatted commands and data. These can be either: short-format (8-bit) broadcast command/data cycles (deskewed in the TTCrx ASIC); or long-format (32-bit) individually-addressed or broadcast command/data cycles (not deskewed in the TTCrx).

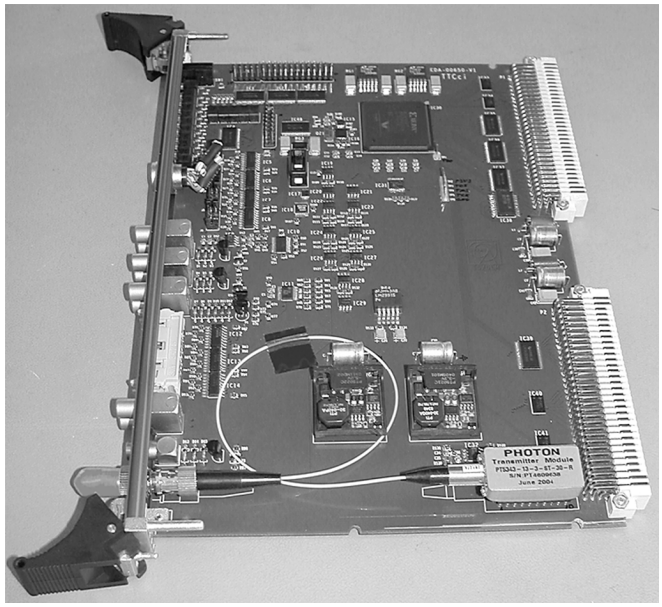

Fig. 3. Assembled TTCci VME module. One can see the single FPGA used for all logic functions (including VME interface) and the laser transmitter module mounted on the bottom-right of the board. The remaining parts are essentially for logic-level translation and I/O buffering.

There are four methods to transmit commands/data:

i) synchronous to external B-Go signals
ii) synchronous to Orbit input signal
iii) asynchronously, under software control
iv) through auxiliary B-data input channel.

The TTCci is implemented as a single-width 6U VME module. It will sense whether it is in a VME64x crate automatically and will either use the geographical address provided by such a crate or revert to an address set by switches on the board if not in a VME64x crate. Fig. 3 shows the fully assembled board. All logic functions are implemented in a single Xilinx XC2V1500 FPGA.

The firmware design is in progress, with all input/output blocks already completed and successfully tested. The locking range of the on-board QPLL has been found to be ~ 2 kHz too low and while this does not preclude operation with the LHC machine frequency the cause has been identified and will be corrected for the final production of modules. All logic-level translation and signal selection has been verified. User software is in the process of being written that will also aid the complete testing of the firmware once the latter is complete.

C. VME-Format Optical Splitter

The original RD-12 design for the optical splitter TTCoc was a 19"-rack width module which was 1U or 2U high depending upon the configuration of the module. The inconvenience of this module was that if mounted in a rack containing other electronics that required cooling, the TTCoc would block the airflow to other units in the same rack. The advent of small form-factor

Fig. 4. 1×16 Optical Splitter mounted in 9U VME crate. The input is at the top, with 16 outputs below. A 9U front-panel supports the card in the VME crate.

optical connectors of type MU has allowed us to re-package the optical parts into the more compact unit shown in Fig. 4.

The splitter unit can now be fitted with a single-width 6U or 9U front panel to allow it to be mounted directly in a VME crate adjacent to either the source or destination of the optical fibers to minimize the amount of cabling. Both 6U and 9U options are needed since the various sub-detectors within CMS have different requirements on positioning within their electronics.

The performance of these single-mode splitters is excellent. The excess loss does not exceed 1.6dB, measured on delivered samples from the manufacturer. Standard Corning SMF-28 fiber is used internally, so radiation-effects are expected to be negligible for use in the periphery of CMS.

IV. Conclusion

All CMS-specific modules for the distribution of TTC signal within the CMS experiment have now been prototyped. A further period of testing will be required, both by the design engineers responsible for the modules and by the CMS community in system tests. It is expected that these tests will take until early 2006, when the designs will be fully qualified for use in CMS.

Acknowledgment

The authors would like to thank I. Church of the CLRC Rutherford Appleton Laboratory for his implementation of the 9U VME front-panel for the optical splitter.

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