Design & Optimization of Automotive Power Electronics Utilizing FITMOS MOSFET Technology

by

Wei Li

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Abstract

Power electronics are essential to many automotive applications, and their importance continues to grow as more vehicle functions incorporate electronic controls. MOSFETs are key elements in automotive power electronic circuits and MOSFET characteristics can strongly affect circuit size, cost and performance. Advances in MOSFET technology are thus of great importance to the advancement of automotive electronics.

The new Floating Island and Thick Bottom Oxide Trench Gate MOSFET (FITMOS) developed at Toyota has tremendous potential for automobile applications due to its reduced on-resistance, improved temperature coefficient of resistance and reduced gate charge and input capacitance. In this research, we investigated the detailed characteristics of FITMOS devices, developed the SPICE model for simulation and explored their applications in the design of automotive power electronics. Specifically, we identified how to best utilize the FITMOS characteristics to benefit power circuit design and on quantifying the gains that can be achieved through their use. We also expose a previously unrecognized phenomenon in the FITMOS MOSFET. In particular, we show that the on-state resistance of the device depends on both frequency and on peak di/dt at a given frequency. This dynamic on resistance variation can have a significant application impact.

Thesis supervisor: David J. Perreault
Title: Associate Professor of Electrical Engineering

Acknowledgements

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Chapter 1 Introduction

Power electronics are essential to many automotive applications, and their importance continues to grow as more vehicle functions incorporate electronic controls. MOSFETs are key elements in automotive power electronic circuits and MOSFET characteristics can strongly affect circuit size, cost and performance. Advances in MOSFET technology are thus of great importance to the advancement of automotive electronics.

The new Floating Island and Thick Bottom Oxide Trench Gate MOSFET (FITMOS) developed at Toyota has tremendous potential for applications requiring devices with blocking voltages on the order of 60V. As described in [1], advantages of this structure as compared to conventional power MOSFETs include reduced on-resistance, improved temperature coefficient of resistance and reduced gate charge and input capacitance. These characteristics yield new design opportunities which can be exploited in numerous ways to benefit power electronic circuits.

In this report, we will investigate the use of FITMOS devices in the design of automotive power electronics. Specifically, we will identify how to best utilize the FITMOS characteristics to benefit power circuit design and on quantifying the gains that can be achieved through their use. To achieve these research goals, behavioral model for FITMOS in Spice will be developed. Their characteristics will also be evaluated and compared with the commercial state-of-the-art MOSFETs. The system design opportunities and tradeoffs with FITMOS will be analyzed. We will make use

of analytical modeling, simulation and simulation optimization to identify the achievable design space and reveal the impact of these new devices on design. These results will be used in the development and experimental evaluation of a FITMOS-based prototype converter design to validate the analytical results and provide a concrete demonstration of the impact of FITMOS transistors on power circuit designs.

Chapter 2 shows the characterization of the FITMOS. It includes capacitance modeling, on-resistance measurement, threshold voltage measurement, I-V characteristic modeling, gate charge measurement, and reverse recovery modeling. In the end, the complete SPICE model of the FITMOS is created based on the characterization results.

Chapter 3 demonstrates the proto-type DC-DC converter design. It is a bi-directional 14V/42V DC-DC converter, which is suitable to automobile applications. The purpose of this proto-type converter to do verify our SPICE model and does a quick performance comparison between FITMOS and other commercial power MOSFETs.

Chapter 4 shows the result of the comparison between the SPICE simulation and proto-type converter measurement. During the study of the simulation and measurement result, our SPICE model has been updated and achieved a better accuracy by capturing more detail loss mechanism.

Chapter 5 discusses the V_{ds} saturation problem in the FITMOS. As the stress on the device reaches certain level, the on-state drain-source voltage V_{ds} of FITMOS

saturates at 3V. This phenomenon can cause significant conduction loss and which is not able to be captured in static measurements.

Chapter 6 documents the optimization process for the FITMOS. The simulation result suggests that soft-switching mode is the optimal working condition for FITMOS. However, the mismatch between simulation and measurement led to the suspicion about the dynamic behavior of the on-resistance in FITMOS.

Chapter 7 demonstrates the dynamic on-resistance study result for FITMOS. The experimental result shows that the on-resistance of FITMOS is not only frequency dependent, but also di/dt dependent. This phenomenon can have significant impact on applications.

Chapter 2 Device Modeling

In order to study the performance of the device and how to utilize the device, an accurate analytical model is very important. From creating the device model, we can have a better understanding of the device parameters and its loss mechanism. For example, the gate capacitance affects the gating loss in hard switching; the drain-source capacitance affects the switching loss; the on-resistance affects the conduction loss. Studying the relationship between the device parameters and loss mechanism can help for the DC-DC converter optimization process in the future. Furthermore, an accurate device model can predict the converter performance under simulation. As a result, we can use simulation to design the suitable values for the components in our converter and shorten our optimization process.

II.1 Capacitance Modeling

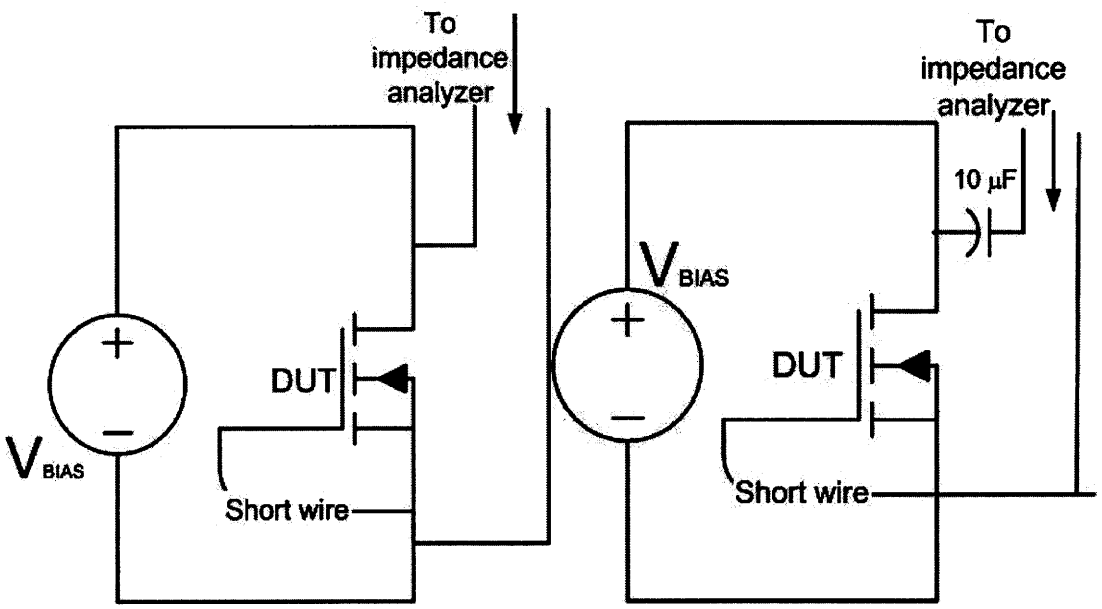
Device capacitances are very important parameters in the loss mechanism. They majorly affect the gating loss and switching loss. And these losses are the dominant components in high switching frequency converters. This section describes the measurement and modeling of the Toyota FITMOS device capacitance. (Note: Data from this section is collected by Bill Page.)

II.1.1 Measurement setup

The device capacitances C_{GS}, C_{GD}, and C_{DS} are determined as a function of

measured capacitances, C_{OSS} (C_{DG}+C_{DS}), C_{ISS} (C_{DG}+C_{GS}), and C_C, where C_C is the input capacitance measured with the Gate ac shorted to the Drain (C_{GS}+C_{DS}). Capacitances were measured as a function of Drain–Source bias voltage, with no Gate-Source bias. All bias voltages were applied across Drain (positive)-Source (negative) with a Tektronix PS280 DC power supply. All capacitances were measured with an Agilent Impedance Analyzer at 1 MHz using 201 points with a frequency range of 100 kHz-10 MHz.

C_{OSS} was measured as a function of Drain-Source bias voltage. Since C_{OSS} is a measurement of C_{DG}+C_{DS}, the Gate-Source port was shorted with a simple wire soldered onto the two leads. For low bias voltages (3-35 V), the Drain and Source leads were attached directly to the impedance analyzer as illustrated in Figure II.1.1A. In this case the bias voltage was directly applied across Drain-Source through the impedance analyzer test adapter, which allows bias voltages up to 42 volts. Data from 3-35 volts was taken in 1-volt increments. At a V_{DS} of less than 3 volts the device did not behave like a capacitor, so data was not taken at these points. Because the impedance analyzer test adapter cannot handle bias voltages above 42 volts, a different procedure was used for voltages starting at 35 volts. In this case, a 10μF ceramic blocking capacitor was placed between the MOSFET drain and the impedance analyzer; the bias voltage was applied directly across the MOSFET Drain and Source (through long connection leads, yielding a high ac impedance of the bias supply), as illustrated in Figure II1.1B. Capacitance measured from 35-60 volts was taken in 5-volt increments (i.e. 35, 40, 45…).



(A) (B)

Figure II.1.1 Diagrams showing connections for measuring C_{OSS}.
(A) At low voltages the bias voltage is applied via the impedance analyzer. (B) At higher voltages, a 10μF, 50V Ceramic blocking capacitor is placed between the Drain and impedance analyzer, and bias voltage is applied directly at the Drain and Source leads. The long (~0.5m) connection leads to the bias supply provide a high ac impedance of the bias supply relative to the device capacitances.

C_{ISS} was measured with a bias voltage applied directly across Drain-Source as illustrated in Figure II.1.2. Since C_{ISS} is a measurement of $C_{DG}+C_{GS}$, the Drain-Source junction was ac shorted by soldering a 10μF ceramic capacitor across the two leads. The Gate and Source leads were attached to the impedance analyzer in order to measure capacitance. The bias voltage was supplied via micro clips attached to the Drain and Source from the power supply. Capacitance was measured for bias voltages from 0-25 volts in 1-volt increments and was measured from 25-60 volts in 5-volt increments.

C_C, defined as the input capacitance with Drain AC shorted to Gate, was also measured with a bias voltage across Drain-Source using the setup of Figure II.1.3.

Since C_C is a measurement of $C_{GS}+C_{DS}$, the Gate and Drain were ac shorted by soldering a 10μF ceramic capacitor from Drain to Gate. The Gate and Source leads were attached to the impedance analyzer in order to measure capacitance. Because the bias voltage supply appears in parallel to the Drain-Source port, bias voltage was supplied through a 1MΩ resistor (representing an approximate AC open circuit). This avoids any possible skewing of the capacitance measurements due to the bias supply. Capacitance measured from bias voltages in the range of 0-15 volts was taken in 1-volt increments and measurements for bias voltages in the range of 15-60 volts were taken in 5-volt increments. See capacitance modeling section for C_{OSS}, C_{ISS}, and C_C versus Drain-Source voltage graphs for B_2, B_3, B_4, and B_5.

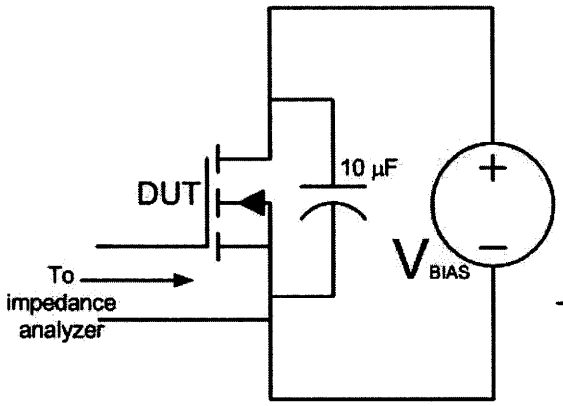


Figure II.1.2 Circuit connection for measuring C_{ISS}. A 10μF, 50V Ceramic capacitor is used to ac short the Drain-Source port.

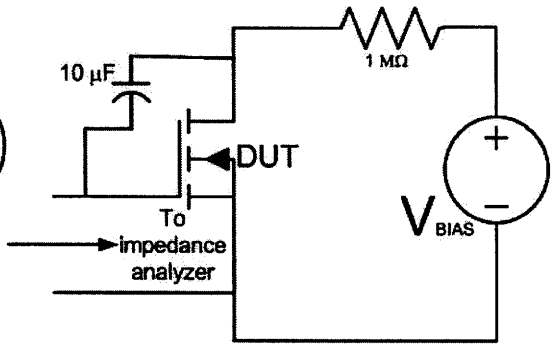


Figure II.1.3 Circuit connection for measuring $C_C = C_{GS}+C_{DS}$.
A 10μF, 50V Ceramic capacitor is used to ac short Drain to Gate. A 1 MΩ resistor was used between the bias power supply and the Drain such that the ac impedance of the bias supply is high.

II.1.2 Parameter Calculation

The measurements of C_{OSS}, C_{ISS}, and C_C as a function of Drain-Source voltage were used to calculate the capacitances C_{DG}, C_{DS}, and C_{GS}.

Starting with:

$$C_{OSS} = C_{DG} + C_{DS} \qquad (2.1.1)$$

$$C_{ISS} = C_{DG} + C_{GS} \qquad (2.1.2)$$

$$C_C = C_{GS} + C_{DS} \qquad (2.1.3)$$

It is readily shown that:

$$C_{DG} = \frac{C_{OSS} + C_{ISS} - C_C}{2}$$

$$C_{DS} = \frac{C_{OSS} - C_{ISS} + C_C}{2} \qquad (2.1.4)$$

$$C_{GS} = \frac{-C_{OSS} + C_{ISS} + C_C}{2}$$

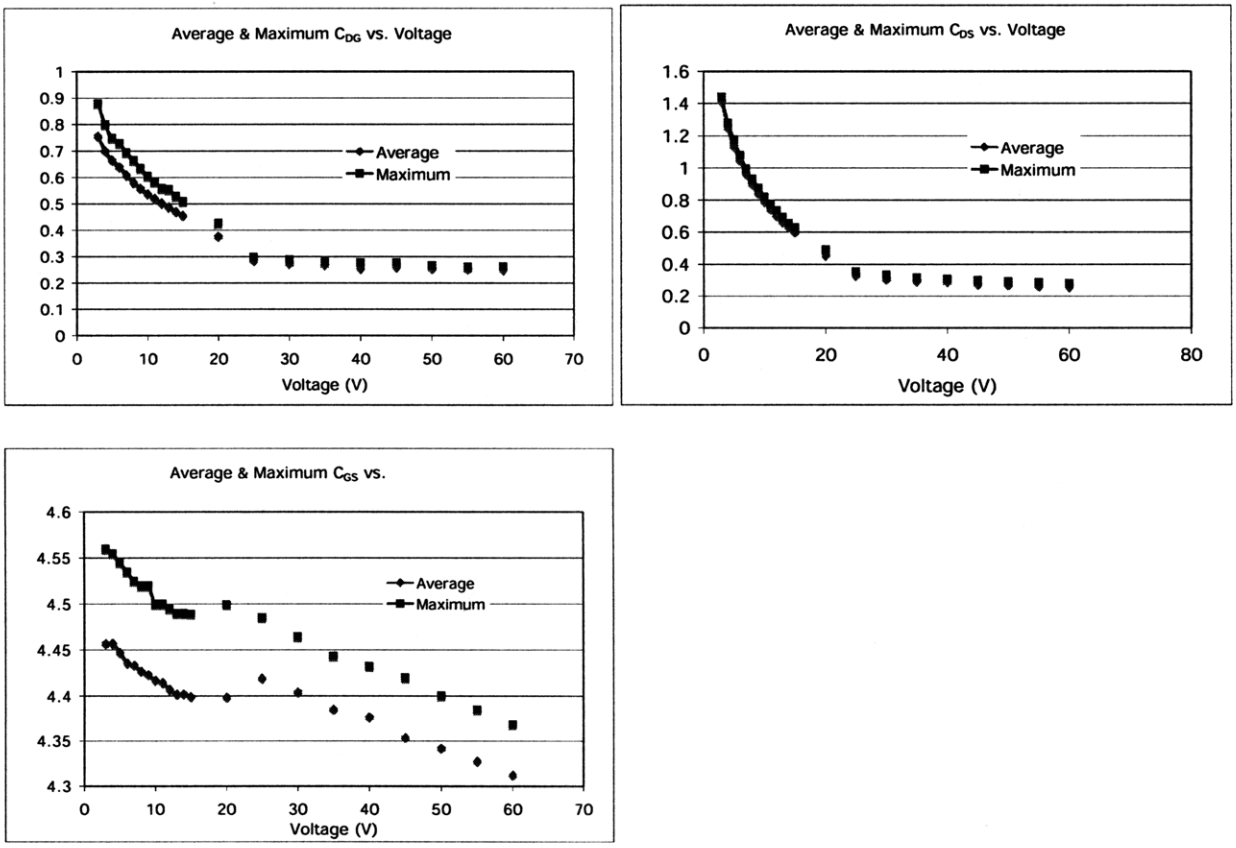


Figure II.1.4 The Average and Maximum curves of the devices for C_{DG}, C_{DS}, and C_{GS} versus voltage.

After solving for C_{DG}, C_{DS}, and C_{GS} for a given bias voltage for MOSFETs B_2, B_3, B_4, and B_5, these voltages versus capacitance relationships were graphed for every device. The data was condensed from graphs of all four MOSFETs into average and worst case (maximum) graphs resulting in 6 curves: average and maximum of C_{DG}, C_{DS} and C_{GS} versus drain-source voltage. See Figure 5 for these graphs. Not surprisingly, there was more variation in C_{DG} from device to device than in C_{DS} and C_{GS}.

II.1.3 Capacitance Modeling

To facilitate simulation, the device capacitances are modeled using appropriate functional forms. These models are intended as simple behavioral models, and do not necessarily reflect physical behavior.

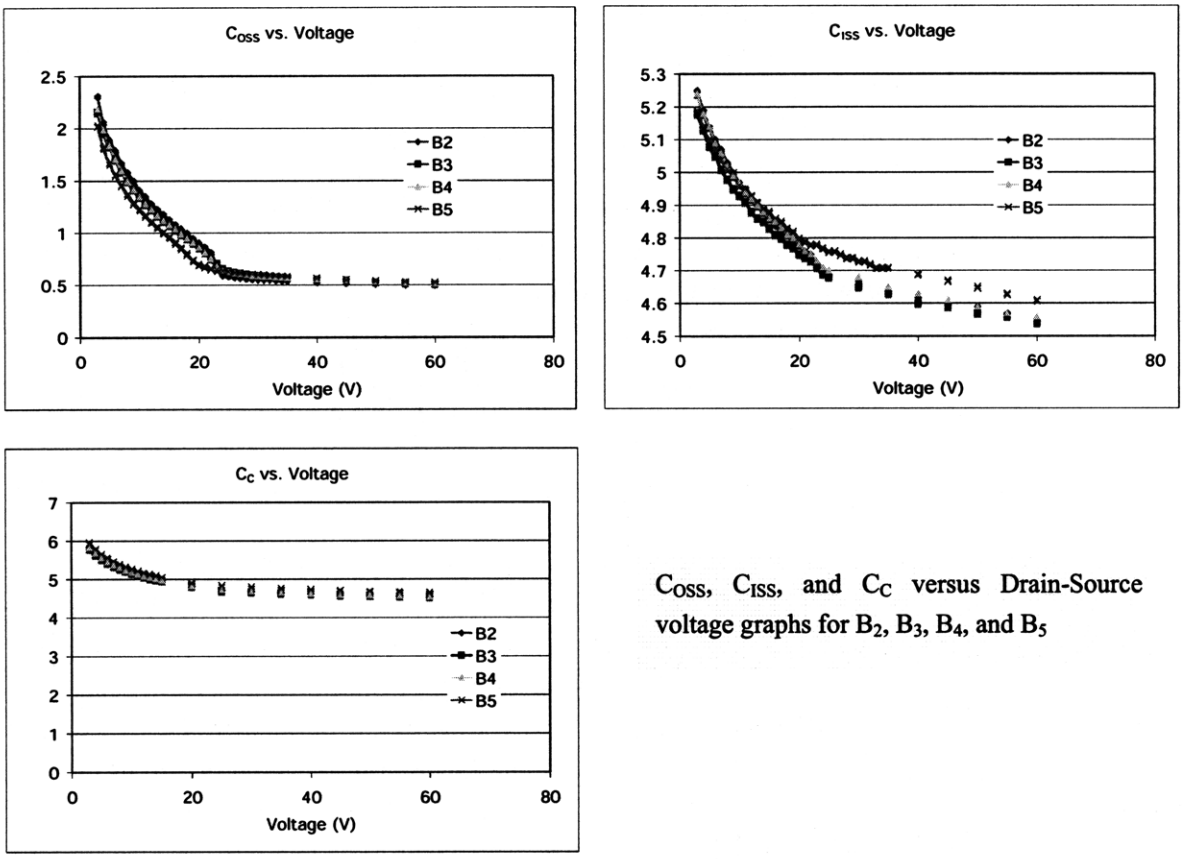
As expected, C_{GS} is approximately constant versus Drain-Source bias voltage, and is thus modeled as a constant capacitance. Conversely, as expected, C_{DG} and C_{GS} vary with drain-source bias, decreasing as Drain-Source bias voltage increases. A simple junction capacitance model was selected to model this variation, with parameters selected to fit the observed variation. The model used is:

$$C(V) = \frac{C_{j0}}{\left(1 + \frac{V}{\phi}\right)^m} \qquad (2.1.5)$$

With C_{j0}, m, and Nselected to fit the data.

This junction capacitance model was selected both because it is simple and fits the data and because it is readily available in many simulation tools. See Figure

II.1.6 - 9 for the graphs of the functions and calculated parameters for C_{DG} and C_{DS}.



C_{OSS}, C_{ISS}, and C_C versus Drain-Source voltage graphs for B_2, B_3, B_4, and B_5

Figure II.1.5 These charts illustrate the capacitances measured for each of the devices B2, B3, B4, and B5.

The model for capacitance vs. voltage used to match the data is:

$$C(V) = \frac{C_{j0}}{\left(1 + \frac{V}{\phi}\right)^m} \qquad (2.1.6)$$

Parameters were selected to match each of the Average and Maximum curves of C_{DG} and C_{DS} versus voltage. In each case, three data points (V_1, C_1, V_2, C_2, V_3, C_3) from a curve were chosen from which a fit was determined. The data points were selected to yield a good overall match to the curves. It was found that selecting data points at V=3, 9, and 15 V yielded a good overall match to the curves.

The value of parameter ϕ was calculated by finding the zero of the function:

$$f(\phi)=\frac{\ln(\phi+V_2)-\ln(\phi+V_1)}{\ln(\phi+V_3)-\ln(\phi+V_1)}-\frac{\ln(C_1/C_2)}{\ln(C_1/C_3)} \qquad (2.1.7)$$

This value of ϕ was calculated numerically in MATLAB as the zero of the function given input values for V_1, C_1, V_2, C_2, V_3, C_3.

Values for m and C_{j0} were then calculated as:

$$m=\frac{\ln(C_1/C_2)}{\ln(\phi+V_2)-\ln(\phi+V_1)} \quad \text{Or} \quad m=\frac{\ln(C_1/C_3)}{\ln(\phi+V_3)-\ln(\phi+V_1)} \qquad (2.1.8)$$

And

$$C_{j0}=C_1(1+\frac{V_1}{\phi})^m \quad \text{or} \quad C_{j0}=C_2(1+\frac{V_2}{\phi})^m \quad \text{or} \quad C_{j0}=C_3(1+\frac{V_3}{\phi})^m \qquad (2.1.9)$$

After identifying candidate values of ϕ, m, and C_{j0}, using this method for given points (e.g., capacitances at V=3, 9, and 15 V) the function was plotted on top of the raw data graphs to verify a good fit to the data.

The Parameters of the function that best fit our average data for C_{DG} were:

$$\boxed{\begin{array}{l}\phi=7.12\\ m=0.6441\\ C_{j0}=0.9500\end{array}} \quad \text{When} \quad \boxed{\begin{array}{l}V_1=3\\ V_2=9\\ V_3=15\end{array}}$$

Giving the function graph:

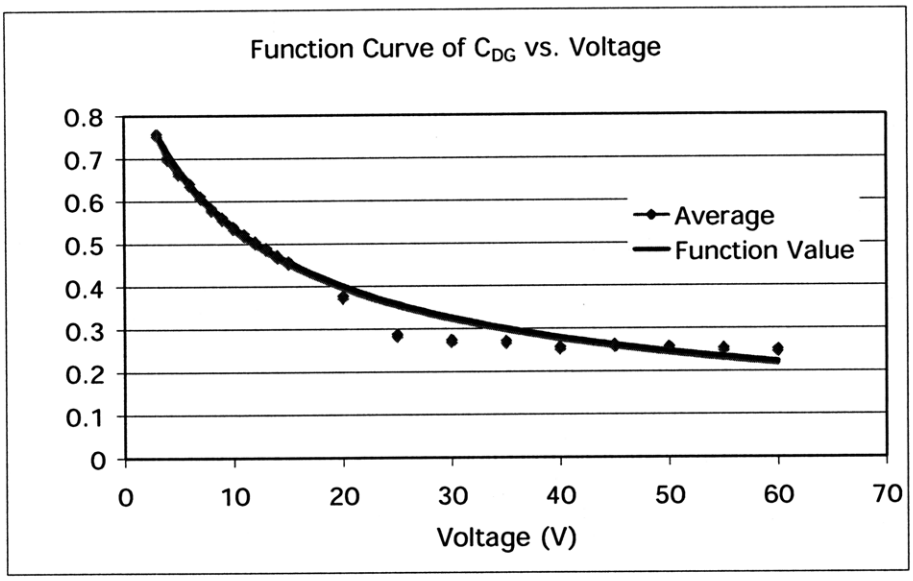


Figure II.1.6 Average C_{DG} plot comparison for function fitting and measurement

The Parameters of the functions that best fit our average data for C_{DS} were:

$$\begin{boxed}\phi = 5.67 \\ m = 0.9774 \\ C_{j0} = 2.143\end{boxed} \quad \text{When} \quad \begin{boxed}V_1 = 3 \\ V_2 = 9 \\ V_3 = 15\end{boxed}$$

Giving the function graph:

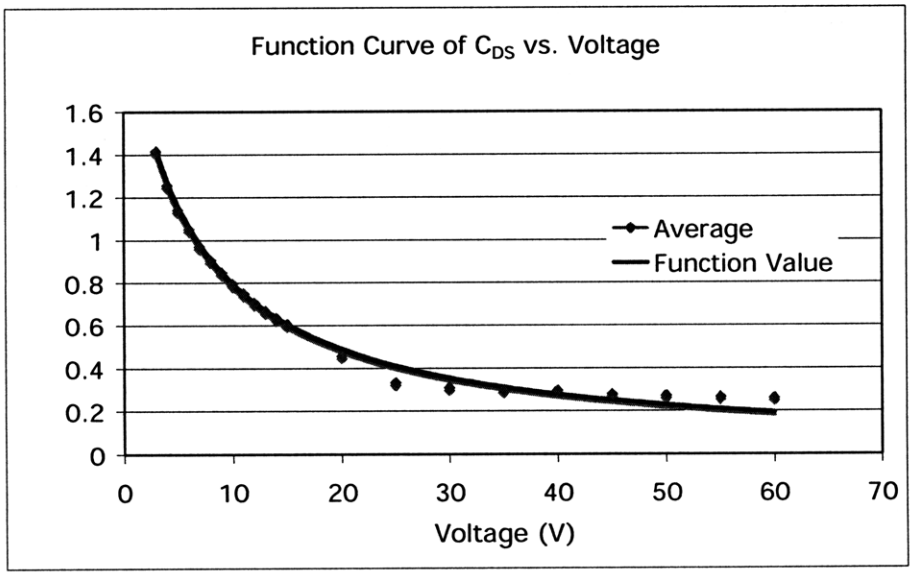


Figure II.1.7 Average C_{DS} plot comparison for function fitting and measurement

The Parameters of the function that best fit our maximum data for C_{DG} were:

$$\begin{boxed}\phi = 6.67 \\ m = 0.6760 \\ C_{j0} = 1.131\end{boxed} \quad \text{When} \quad \begin{boxed}V_1 = 3 \\ V_2 = 9 \\ V_3 = 15\end{boxed}$$

Giving the function graph:

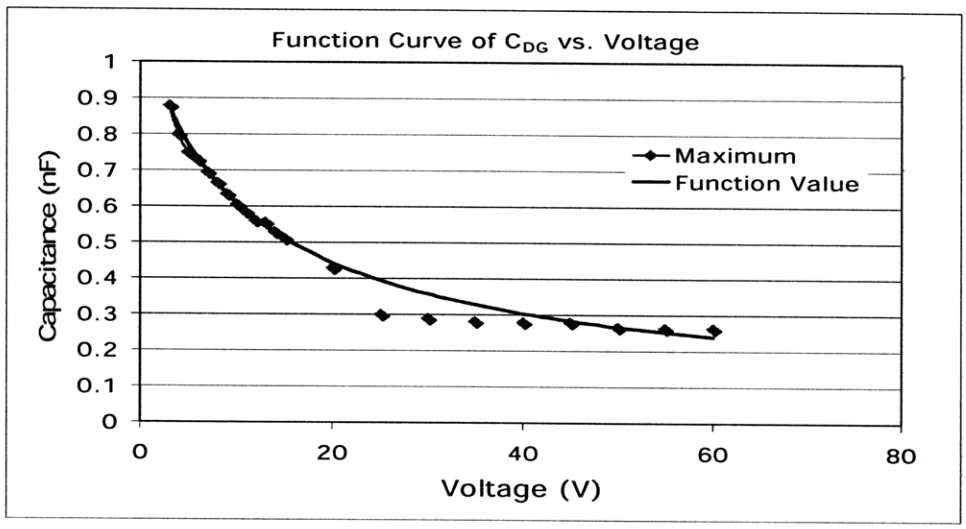


Figure II.1.8 Maximum C_{DG} plot comparison for function fitting and measurement

The Parameters of the functions that best fit our maximum data for C_{DS} were:

$$\begin{boxed}\phi = 6.04 \\ m = 0.9786 \\ C_{j0} = 2.136\end{boxed} \quad \text{When} \quad \begin{boxed}V_1 = 3 \\ V_2 = 9 \\ V_3 = 15\end{boxed}$$

Giving the function graph:

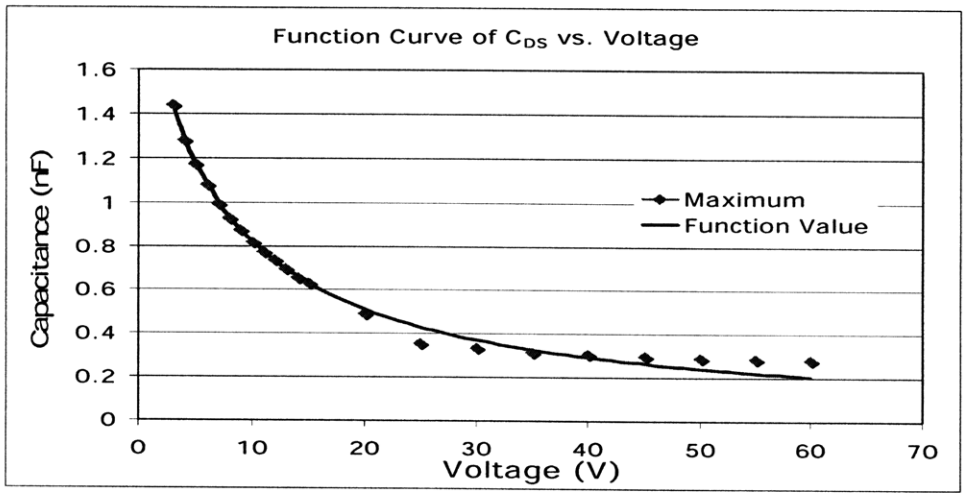


Figure II.1.9 Maximum C_{DS} plot comparison for function fitting and measurement

II.2 On-resistance Measurement

Conduction loss of a device is linear proportional to its on-resistance. In high power area, conduction loss is a one of the dominant loss mechanisms in the converter. As a result, the FITMOS on-resistance is also important to us. This section describes the measurement of the Toyota FITMOS device On-Resistance versus Temperature.

II.2.1 Measurement Methods

The circuit for making measurements is shown in Fig.II.2.1. In order to turn on the FITMOS device, a 10V Gate-Source bias voltage was applied with a DC power supply (Tektronix PS280). In addition, a current-limited DC power supply (HP 6011A) in series with a 2 Ω power resistor was used to apply either 1A or 10A Drain-Source current to the MOSFET. A multimeter (Agilent 34401A) was used to measure the drain-to-source voltage across the MOSFET. To make an accurate measurement of the Drain-Source current (I_{DS}), a 5m Ω current-sense resistor was placed in series with the 2 Ω resistor and the Drain-Source port of the MOSFET. A multimeter (Agilent 34401A) was used to measure the voltage across the 5m Ω resistor. In this way, we were able to calculate the On-Resistance by using the Ohm's Law, $R_{on} = V_{ds}/I_{ds}$. Since we want a plot for On-Resistance versus temperature, the MOSFET was clamped to a hot plate (Omega LHS-720) via an electrically insulating pad. The hot plate was used to control the case temperature of the MOSFET.

On-resistance measured from 25 °C to 150 °C was taken in 25 °C increments (i.e. 25, 50, 75…).

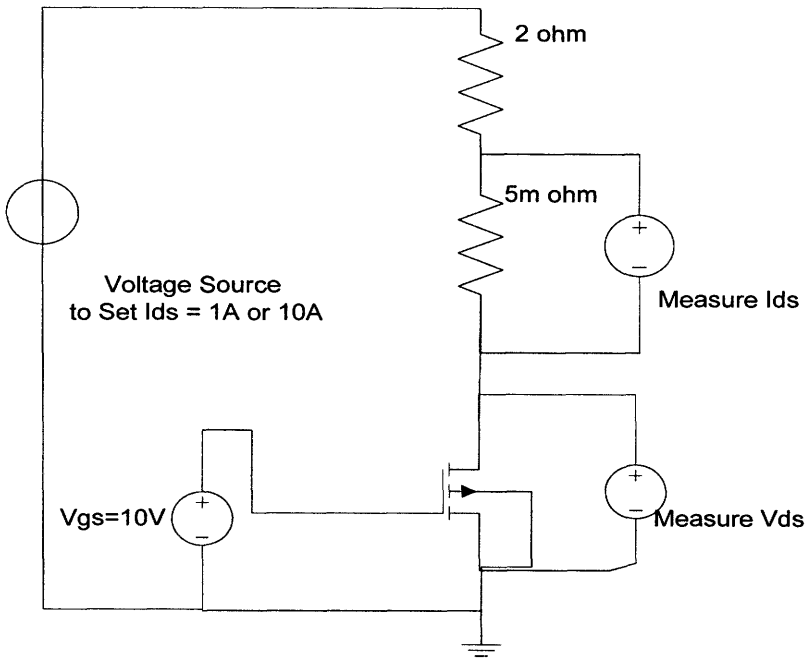
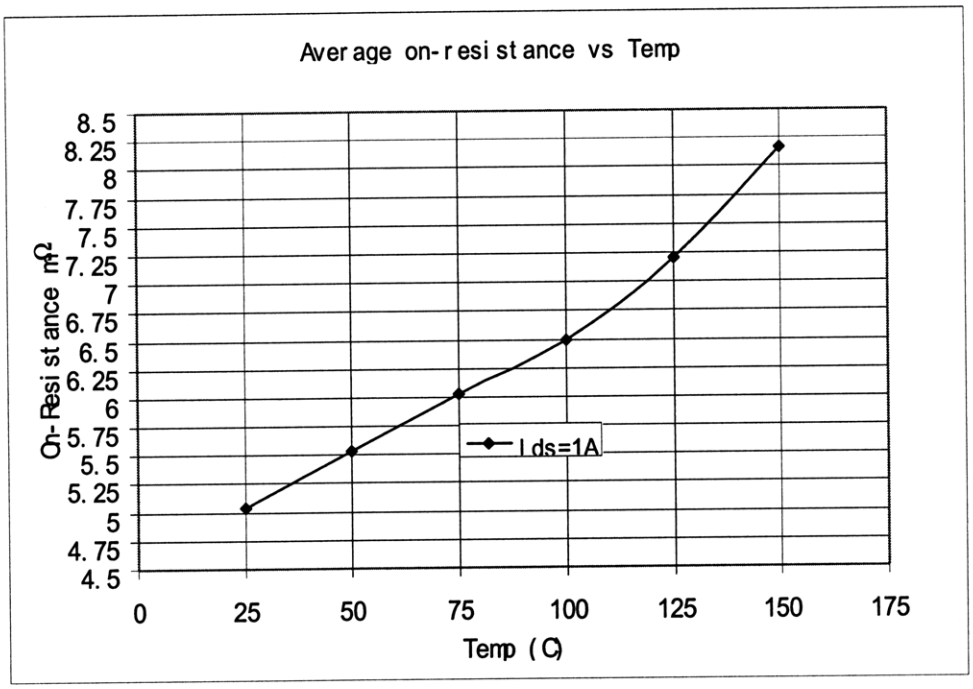


Figure II.2.1 Circuit setup for the FITMOS On-Resistance measurements. A 10V V_{gs} was applied. A DC current source was used to apply either 1A or 10A Drain-Source current for the measurement.

II.2.2 Measurement Result

From the measurement, we can see that the on-resistance measurement is consistent with different Drain-Source current level. The $R_{ds\text{-}on}$ is about 5.25Ω at the room temperature T = 25 ℃ and it goes up to 8.25Ω when the temperature is increased to T = 150 ℃.



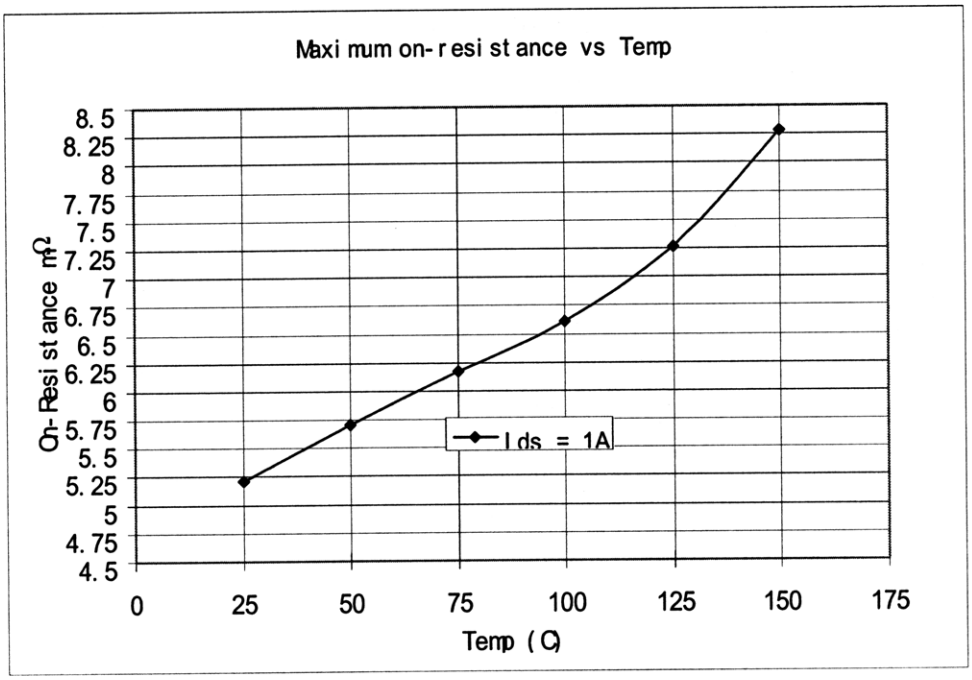
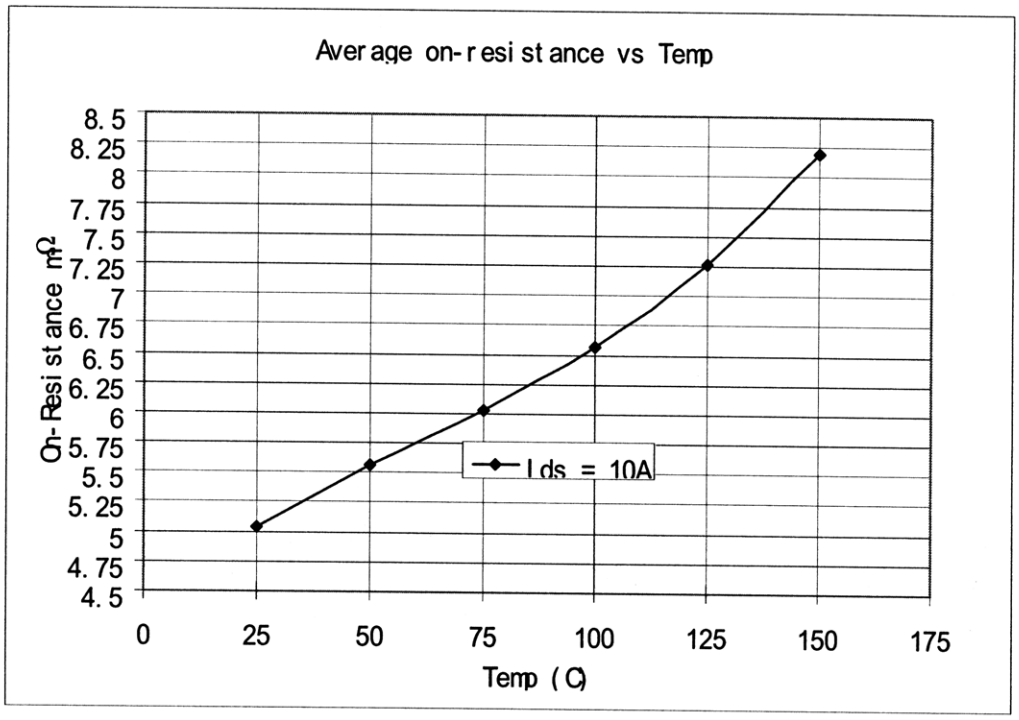


Figure II.2.2 The average and maximum FITMOS On-Resistance versus temperature when the Drain-Source (I_{ds}) current is equal to 1A.



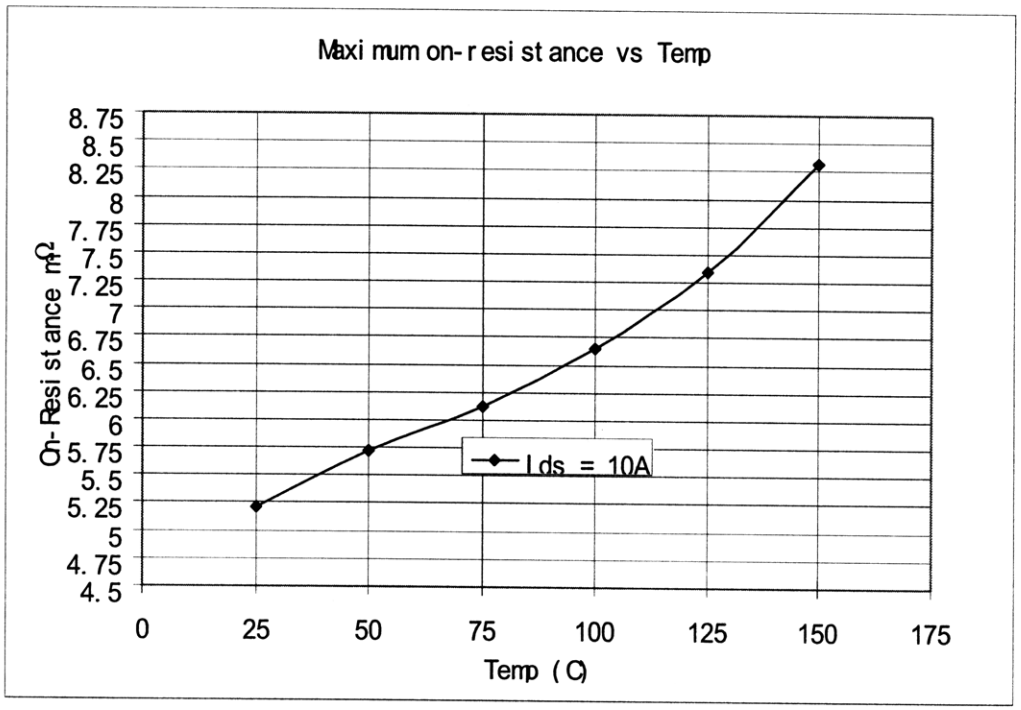


Figure II.2.3 The average and maximum FITMOS On-Resistance versus temperature when the Drain-Source (I_{ds}) current is equal to 10A.

II.3 Threshold Voltage Measurement

Threshold voltage is an important parameter for a device. It determines the minimum gate voltage for the converter. Furthermore, threshold voltage is also critical for our later I_V characteristic modeling. We define the threshold voltage as the required gate-source voltage V_{gs} to give 1mA drain-source current I_{ds}.

II.3.1 Threshold Voltage Measurement Methods

The circuit for making measurements is shown in Fig.II.3.1. A DC power supply (Tektronix PS280) was used to sweep the Gate-Source voltage of the MOSFET. Between the power supply and the gate of the MOSFET, a 50K Ω resistor was added to prevent the DC power supply from oscillating. In addition, a current-limited DC power supply (HP 6011A) in series with a 2 Ω power resistor was used to apply either 5V or 10V supply voltage. A multimeter (Agilent 34401A) was used to measure the gate-to-source voltage across the MOSFET. For the drain current measurement, a multimeter (Agilent 34401A) was used to measure the voltage across the 2 Ω resistor. In this way, we were able to calculate the drain current by using the Ohm's Law, $I_{ds} = V_{ds}/R$. The MOSFET was clamped to a hot plate (Omega LHS-720) via an electrically insulating pad. So the off hot plate acted like a huge heat sink for the MOSFET.

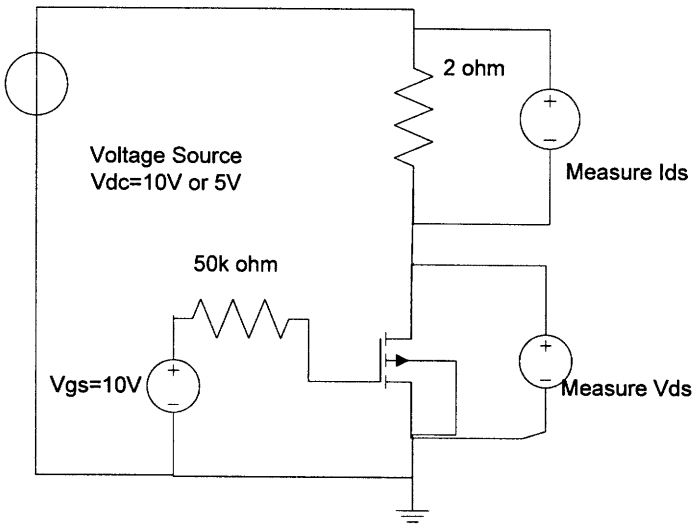


Figure II.3.1 Circuit setup for the FITMOS Threshold voltage measurements. A 5V or 10V V_{DD} was applied. A DC voltage source was used to sweep the Gate-Source voltage for this measurement. The Drain-Source current is measured from the volt-meter across the 2 Ω resistor.

II.3.2 Data and Summary

The threshold voltage was defined as the gate-source voltage when the drain-source current is 1mA. An average of 3.16V threshold voltage was measured for our samples.

On average, the FITMOS has a 3.16V threshold voltage. On the temperature versus gate-source voltage graph, when the V_{gs} is less than threshold voltage, the device is off, so the device temperature is low. Once the V_{gs} is slightly above the threshold voltage, the device is on. But the device has large V_{ds} and the device is in saturation region. At this region, the device experiences large current and large voltage drop, so there is big power dissipate on the device and hence the device temperature increases. If the gate-source voltage keeps increasing, the device will go into the linear region, in which the V_{ds} across is low. In this region, the power

dissipate on the device is low, so the temperature drops back.

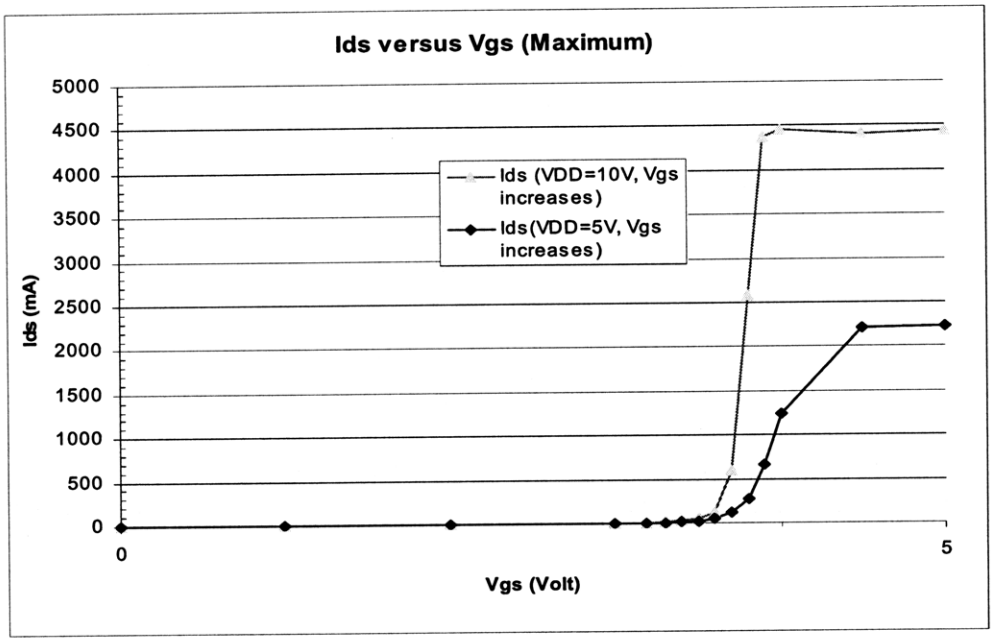


Figure II.3.2 The maximum FITMOS drain-source current versus gate-source voltage when V_{DD} =5V or 10V. (Current is limited by the 2 Ω resistor for high V_{gs}).

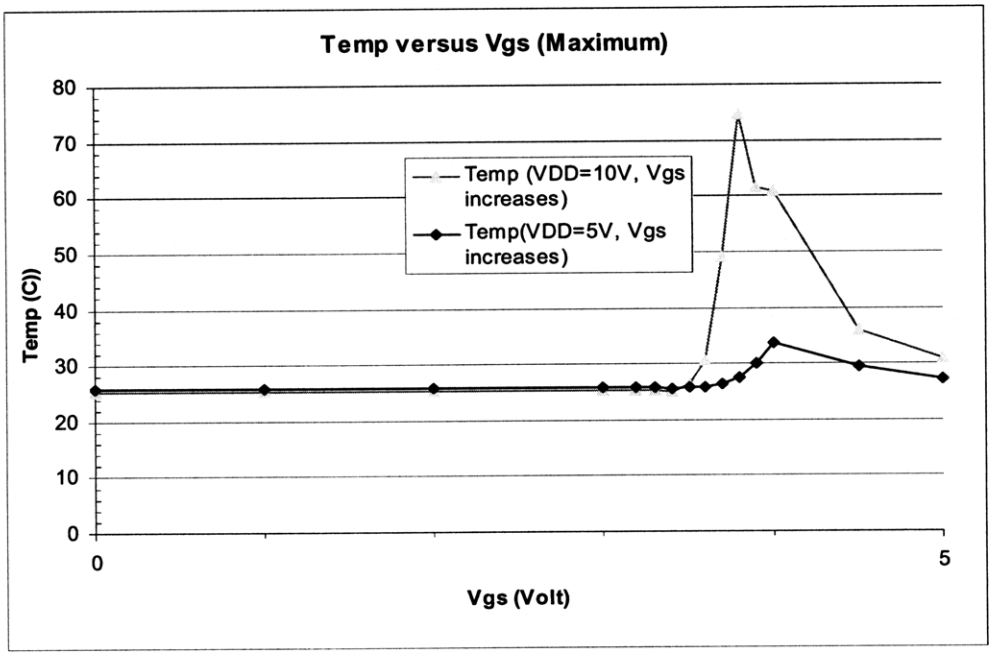


Figure II.3.3 The maximum FITMOS temperature versus gate-source voltage when V_{DD} =5V or 10V.

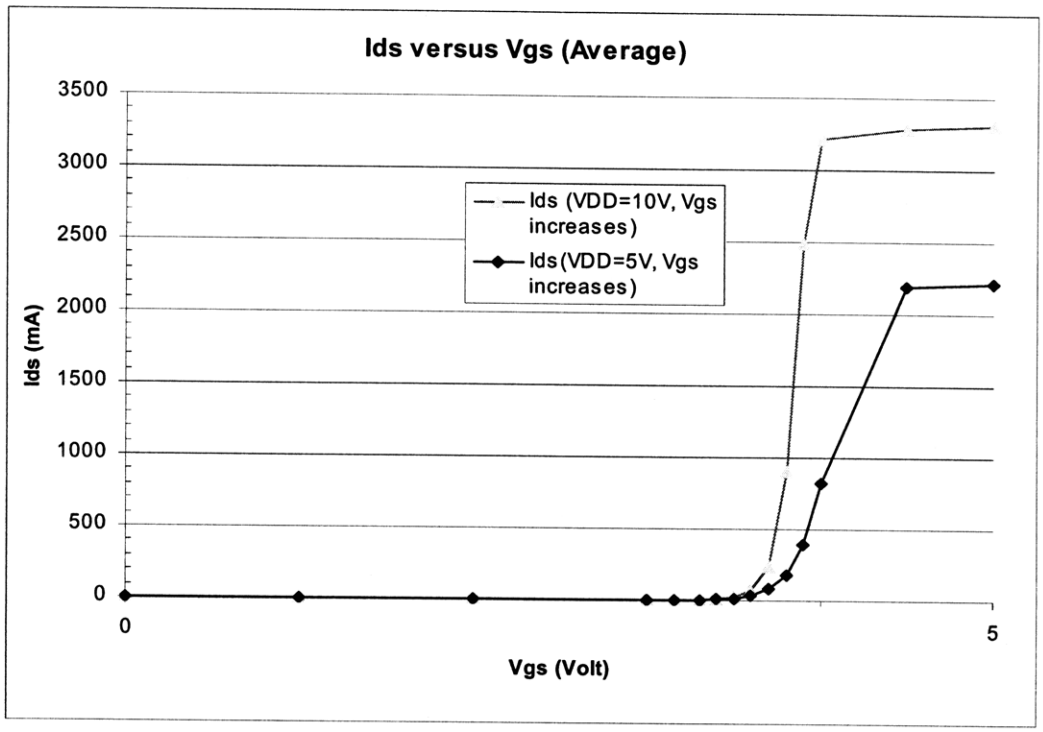


Figure II.3.4 The average FITMOS drain-source current versus gate-source voltage when V_{DD} =5V or 10V

*** (Current is limited by the 2 Ω resistor for high V_{gs}).**

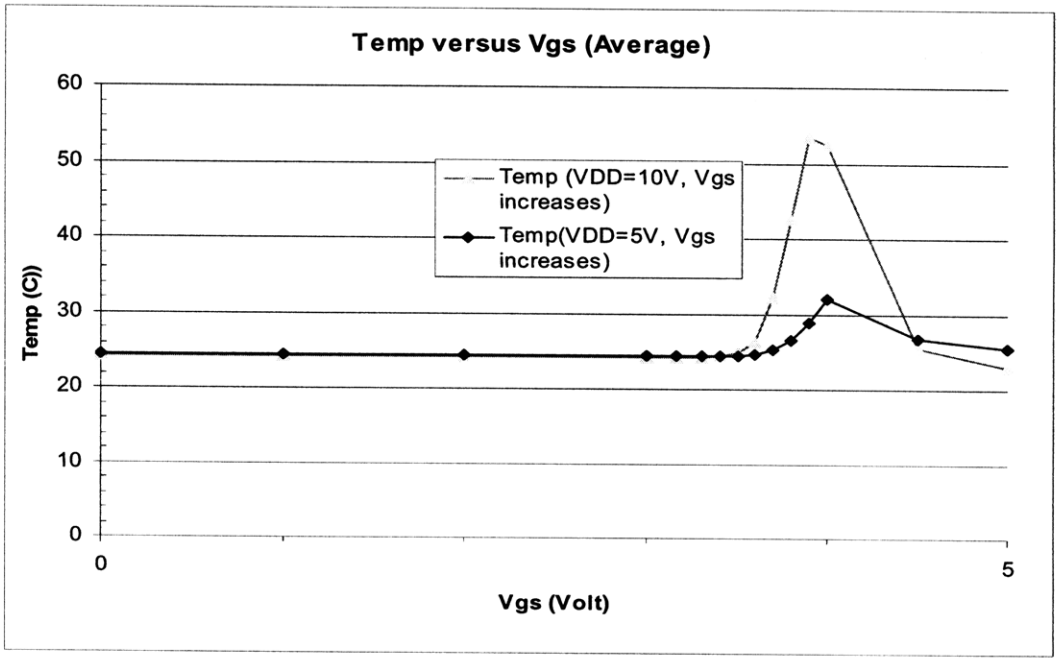


Figure II.3.5 The average FITMOS temperature versus gate-source voltage when V_{DD} =5V or 10V.

II.4 I-V Characteristic Modeling

I_V characteristic is one of the most important characteristics of a device. The I_V characteristic model affects the many loss mechanism in the device, ex conduction loss and switching loss. This section describes the measurement and behavioral modeling for the I_d-V_{ds} characteristics of the Toyota FITMOS device as a function of gate voltage. We do not seek a physical model of device behavior, but rather a simple behavioral model that can be used for rapid simulations and calculation of switching loss.

II.4.1 I-V Characteristic Measurement Methods

In the I-V curve measurement, we used the same circuit as the one we used for threshold measurement in Figure II.3.1. The purpose of this measurement is to model the Drain-Source current in a function of V_{gs} (Gate-Source voltage) and V_{ds} (Drain-Source voltage). The Gate-Source voltage of the MOSFET was set by the DC power supply (Tektronix PS280). In addition, a current-limited DC power supply (HP 6011A) in series with a 2 Ω power resistor was used to apply sweep the supply voltage and hence set the Drain-Source voltage of the MOSFET. The actual Gate-to-Source voltage across the MOSFET was measured by a multimeter (Agilent 34401A). For the drain current measurement, a multimeter (Agilent 34401A) was used to measure the voltage across the 2 Ω resistor. In this way, we were able to calculate the drain current by using the Ohm's Law, $I_{ds} = V_{ds}/R$. Again, the MOSFET was clamped to a hot plate (Omega LHS-720) via an electrically insulating

pad.

II.4.2 Measurement Data

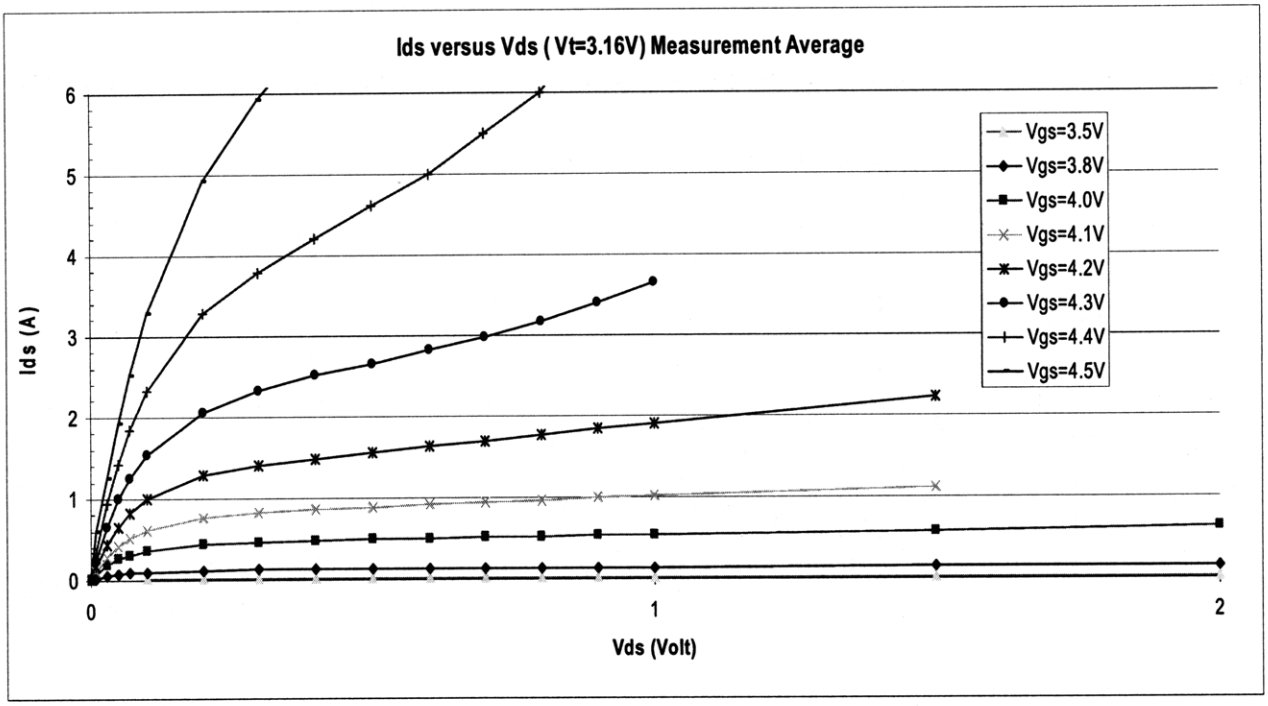


Figure II.4.1 Above curves show the I-V characteristic of the FITMOS. When the V_{gs} is above 4.0V, the MOSFET heats up substantially at high simultaneous V_{ds} and I_d current. In order to get this I-V curve with stable MOSFET temperature, the I_{ds} was only measured up to 1V V_{ds} when the V_{gs} is above 4.0V.

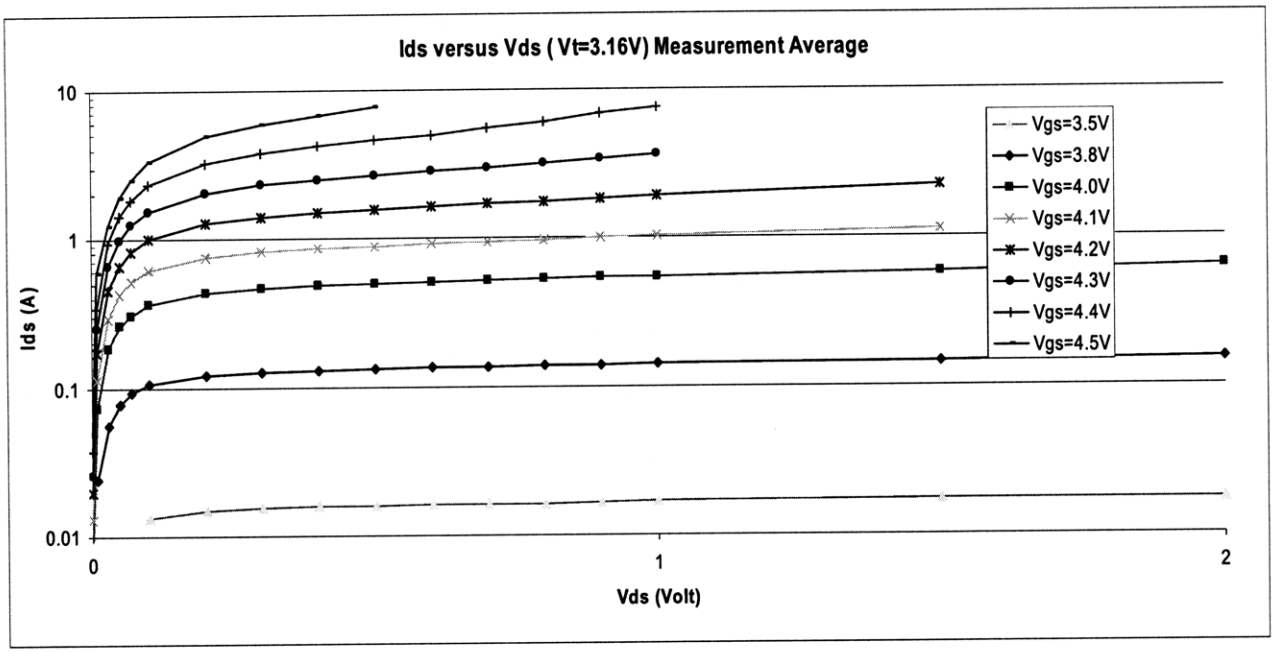


Figure II.4.2 The graph shows the I-V curves of the MOSFET, in which the Y-axis (I_{ds}) is on a Logarithmic scale.

II.4.3 I-V Characteristic Modeling Method

In a previous section, we already described the measurement of the FITMOS I-V curves. In here, we introduce a method to model I-V characteristics of the FITMOS. The Drain-Source current is modeled as a function of V_{gs} (Gate-Source voltage) and V_{ds} (Drain-Source voltage). The purpose of this model is to better capture FITMOS I-V behavior, and hence to provide a more accurate simulation.

Figure II.4.3 shows I_d-V_{ds} curves of the FITMOS parameterized by gate voltage. According to this plot, we can see that FITMOS devices exhibit operation regions consistent with those of conventional MOSFETs, including triode operation (where current rises gradually drain-source voltage), and saturation operation (where current rises more slowly with drain-source voltage). For simplicity, we seek to model behaviors in these two regions as follows: in triode region we model the drain-source

current as linearly proportional to drain-source voltage, with a slope that is $1/R_{on}$ resistance; in the saturation region we model the drain source current as a function of $K(V_{gs}-Vt)^{\wedge}\alpha+\lambda V_{ds}$. So in order to model this I_V curve well, we need to figure out the following relations: 1. the 1/Ron as a function of V_{gs}; 2. the parameters K, V_t and α for $K(V_{gs}-V_t)^{\wedge}\alpha$ in saturation region, and 3.the slope λ as a function of $(V_{gs}-V_t)$.

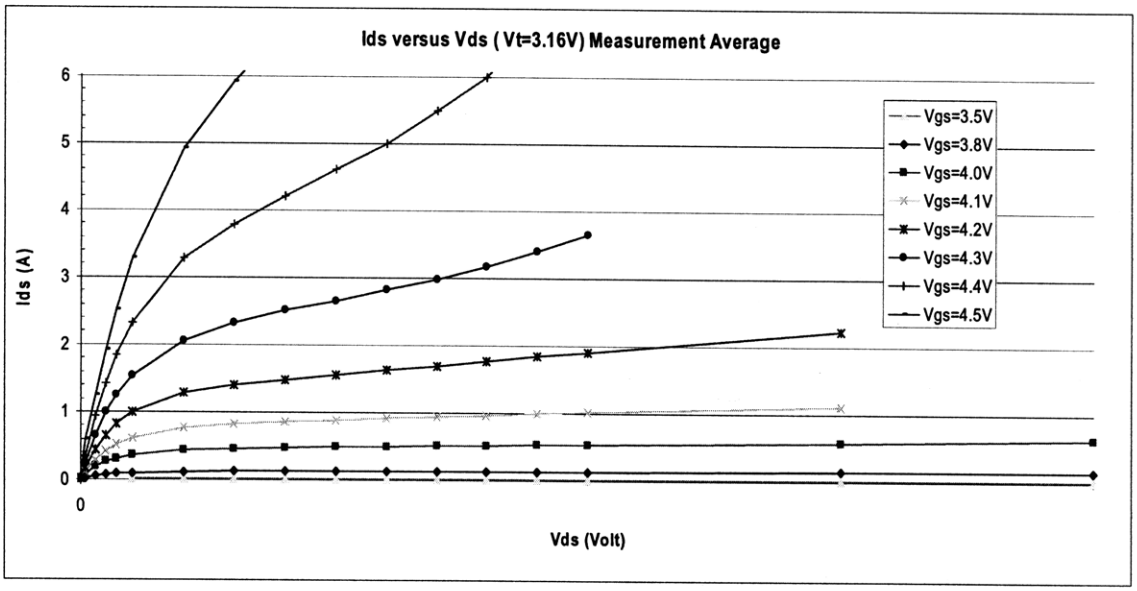


Figure II.4.3 The average I-V curve of the FITMOS.
The average threshold voltage is 3.16V.

II.4.3.1 1/Ron Function

From the I-V curve in Figure II.4.3, we can see that the current I_{ds} is linearly proportional to $1/R_{on}$ when V_{ds} is small. Figure II.4.4 focuses on the triode region of the I-V curve extracted from figure II.4.3. For simplicity and based on empirical observation, we treat the FITMOS device as being in triode region when V_{ds} is less than 0.2 V.

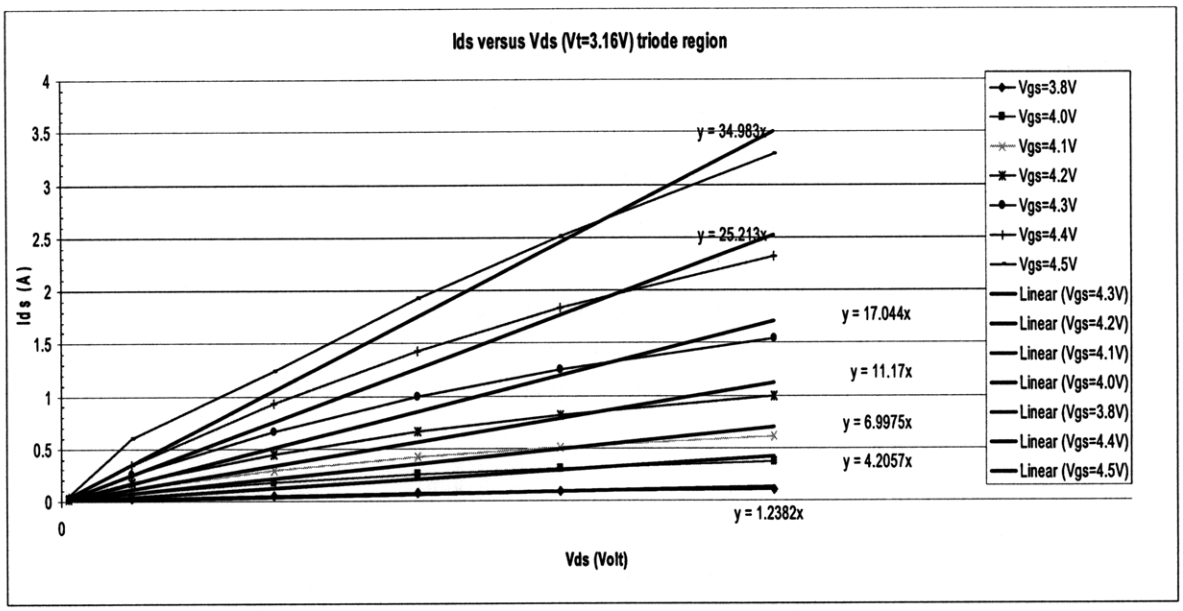


Figure II.4.4 The Triode regions of the FITMOS, linear trendlines are added to model the $1/R_{on}$. From the trendline equations, we can see that $1/R_{on}$ is the slope of each line according to I=V/R.

As a result, from the slope of each line in figure II.4.4, we can find out the $1/R_{on}$ value for each V_{gs}. Figure II.4.5 shows a curve fit the $1/R_{on}$ in a function of V_{gs}-V_t in triode region for low value of V_{gs}-V_t, which is:

$$\frac{1}{R_{on}} = 9.3495*(V_{gs} - V_t)^{4.5431} \qquad (2.4.1)$$

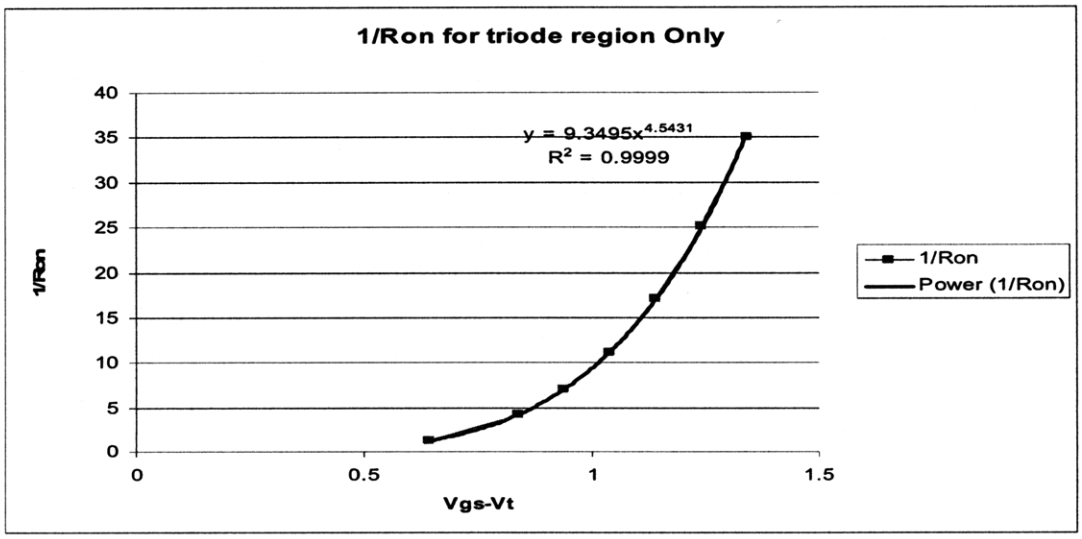


Figure II.4.5 This plot shows the $1/R_{on}$ versus V_{gs}-V_t.
From the power function trendline, we can find out the $1/R_{on}$ in a function of V_{gs}-V_t.

While this curve matches for voltage slightly above threshold, we know that the $1/R_{on}$ will not keep on increasing to infinity as V_{gs}-V_t continues to increase. To account for this, we measured the R_{on} versus V_{gs} for larger value of V_{gs} as well. The measurement setup is the same as the setup we used in a previous section on On-resistance versus temperature. The setup is shown in Figure II.4.6.

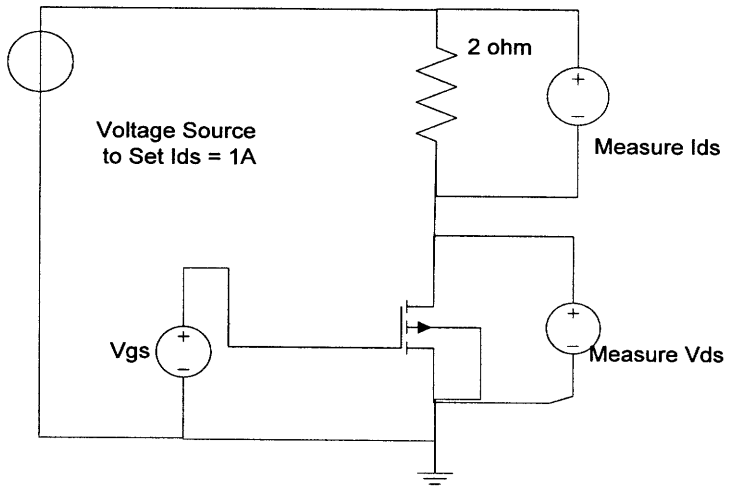


Figure II.4.6 Measurement setup for R_{on} versus V_{gs}.
We set the Ids to 1A and measure the Vds across the FITMOS, then we can calculate the On-resistance from R=V/I. Ron was measured from Vgs = 5V to 10 V with 1v increments.

Figure II.4.7 shows the $1/R_{on}$ versus V_{gs}-V_t for both triode small and large values of V_{gs}. We can see that 1/Ron reaches its maximum when V_{gs} is large. When V_{gs} is equal to 10V, $1/R_{on}$ is about 200 Ω^{-1} and hence R_{on} is about 5mΩ. This is consistent with our previous On-resistance versus temperature measurement results, in which we have the On-resistance as about 5mΩ at room temperature.

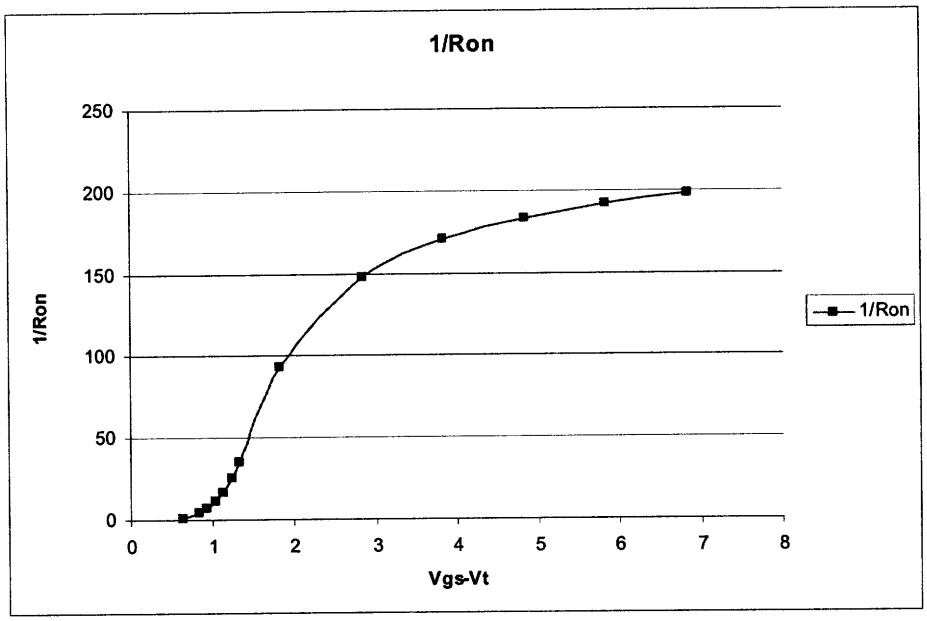


Figure II.4.7 1/Ron versus (Vgs-Vt) for both triode and saturation region (Vt=3.16V).

As a result, we cannot model the $1/R_{on}$ in a power function of V_{gs} when V_{gs} is high, otherwise, it will grow to a very large number which is not consistent with our 5m Ω on-resistance limit. So we model the $1/R_{on}$ in a different function when V_{gs} is large. Figure II.4.8 shows the $1/R_{on}$ curve for large V_{gs}. In this region, a logarithmic function can fit the curve very well:

$$\frac{1}{R_{on}} = 78.053Ln(V_{gs} - V_t) + 56.781 \qquad (2.4.2)$$

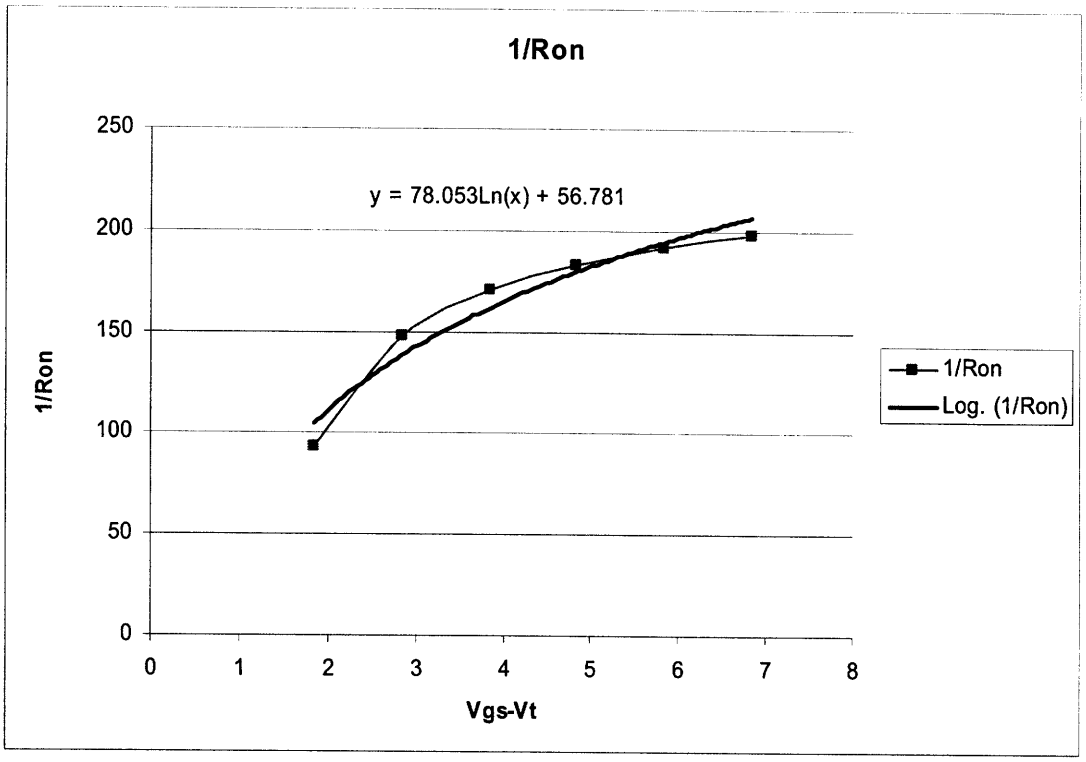


Figure II.4.8 $1/R_{on}$ versus V_{gs}-V_t curve when V_{gs} is large
The Log function trendline shows the function to model the $1/R_{on}$ for large V_{gs}.

In conclusion, we model the $1/R_{on}$ as a conditional function:

$$\frac{1}{R_{on}} = If((V_{gs}-V_t) \le 1.6734,\ 9.3495*(V_{gs}-V_t)^{4.5431}, 78.053Ln(V_{gs}-V_t)+56.781) \tag{2.4.3}$$

Where 1.6734 is the intercept between these two functions, when the If statement is true, function $9.3495*(V_{gs}-V_t)^{4.5431}$ is used, otherwise, $78.053Ln(V_{gs}-V_t)+56.781$ is used.

For small Vgs, when the 1/Ron increases rapidly with V_{gs}, we model it with a power function $9.3495*(V_{gs}-V_t)^{4.5431}$. When Vgs is large, we use the Logarithmic function $78.053Ln(V_{gs}-V_t)+56.781$ to model $1/R_{on}$ to control it within the reasonable physical limit, which is about 200 to 300 Ω^{-1} since on-resistance is about 5m Ω. Figure II.4.9 shows our model curve for the whole range $1/R_{on}$ in comparison

with the measured value. We can see that our model fits the measurement result very well.

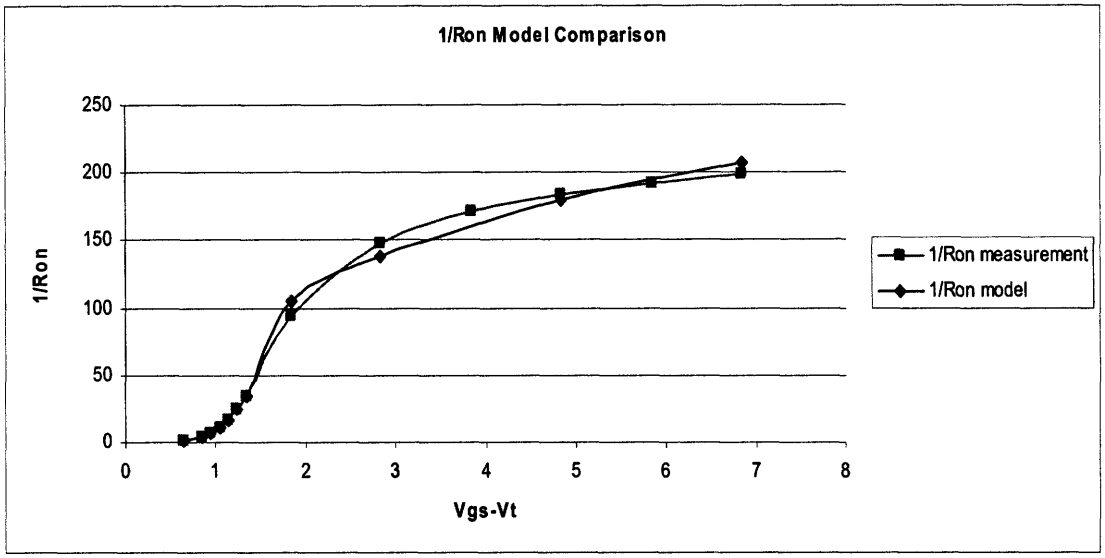


Figure II.4.9 The comparison between our model for 1/Ron and the measurement result. Our model fits quite well with the measurement.

II.4.3.2 $K(V_{gs}-V_t)^{\alpha}$ in saturation region

At high levels of drain-source voltage (e.g., above 0.2V), the FITMOS seems to get into the saturation region and the slope of the I-V curve is reduced. In this case, we try to model the drain-source current with a function $K(V_{gs}-V_t)^{\alpha} + \lambda V_{ds}$. λ is the slope of the I-V curve in saturation region. $K(V_{gs}-V_t)^{\alpha}$ is the intercept of the extended I-V trendline in saturation and the y-axis, which is $V_{ds}=0$. In order to obtain the as $K(V_{gs}-V_t)^{\alpha}$ function in saturation, the I-V curve in saturation was extracted. Figure II.4.10 shows the I-V curve in saturation region.

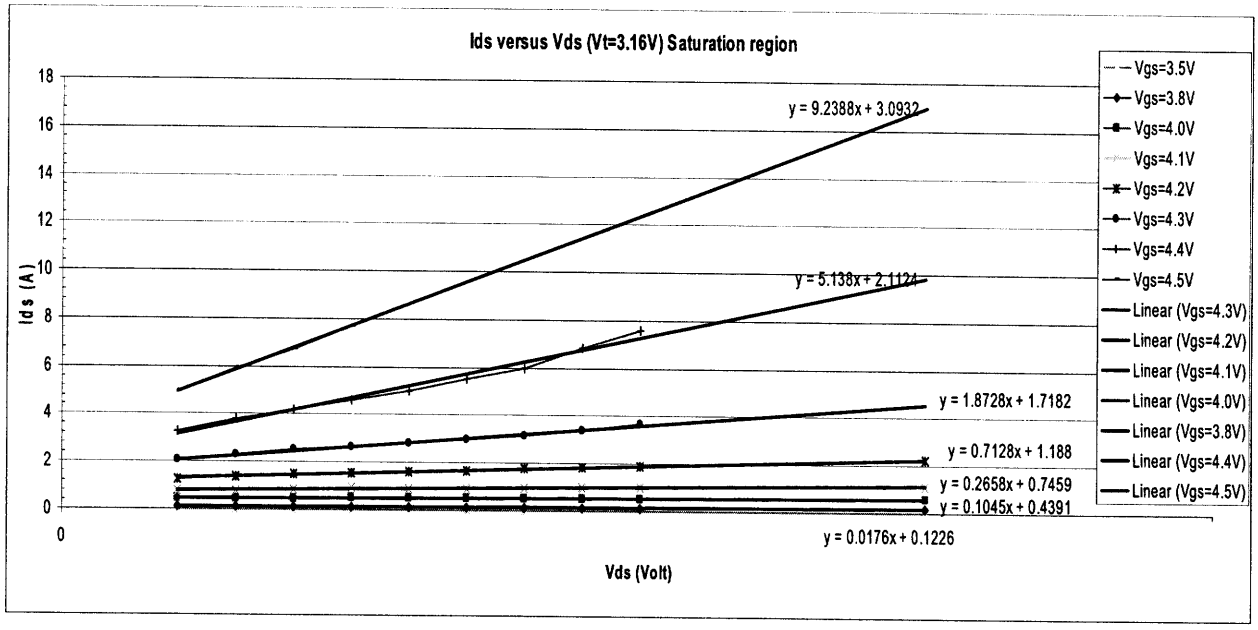


Figure II.4.10 The I-V curve in saturation region only.

From the trendline equations for the drain-source current I_{ds}, when x (V_{ds}) = 0, we have values for $K(V_{gs}-V_t)^{\wedge}\alpha$. Figure II.4.11 shows the $K(V_{gs}-V_t)^{\wedge}\alpha$ versus ($V_{gs}-V_t$) plot. If we model the $K(V_{gs}-V_t)^{\wedge}\alpha$ curve as a power function, we have:

$$K = 0.9172$$
$$\alpha = 4.3406 \qquad (2.4.4)$$
$$K(V_{gs} - V_t)^{\wedge}\alpha = 0.9172 * (V_{gs} - V_t)^{4.3406}$$

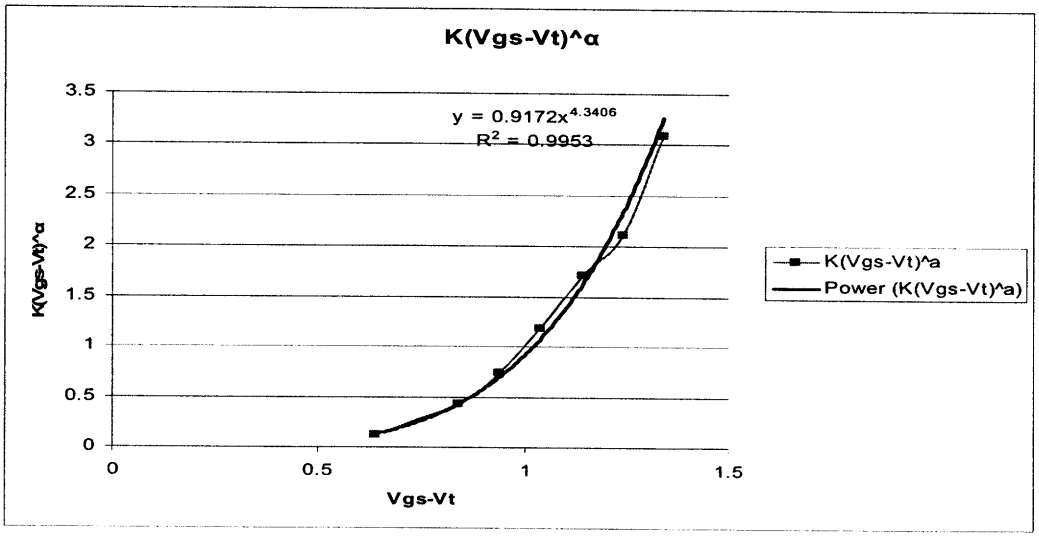


Figure II.4.11 $K(V_{gs}-V_t)^{\wedge}\alpha$ versus ($V_{gs}-V_t$) plot
from the power trendline, we can get the $K(V_{gs}-V_t)^{\wedge}\alpha$ equation in terms of ($V_{gs}-V_t$).

II.4.3.3 slope λ modeling

From the trendline equation in figure II.4.10, we also can obtain the value for the slope of the I-V curve λ in the saturation region. In figure II.4.12, the slope λ versus (V_{gs}-V_t) is plotted. Again, from the power trendline, we can get the slope λ in a function of (V_{gs}-V_t):

$$\lambda = 0.6122 * (V_{gs} - V_t)^{8.7186} \qquad (2.4.5)$$

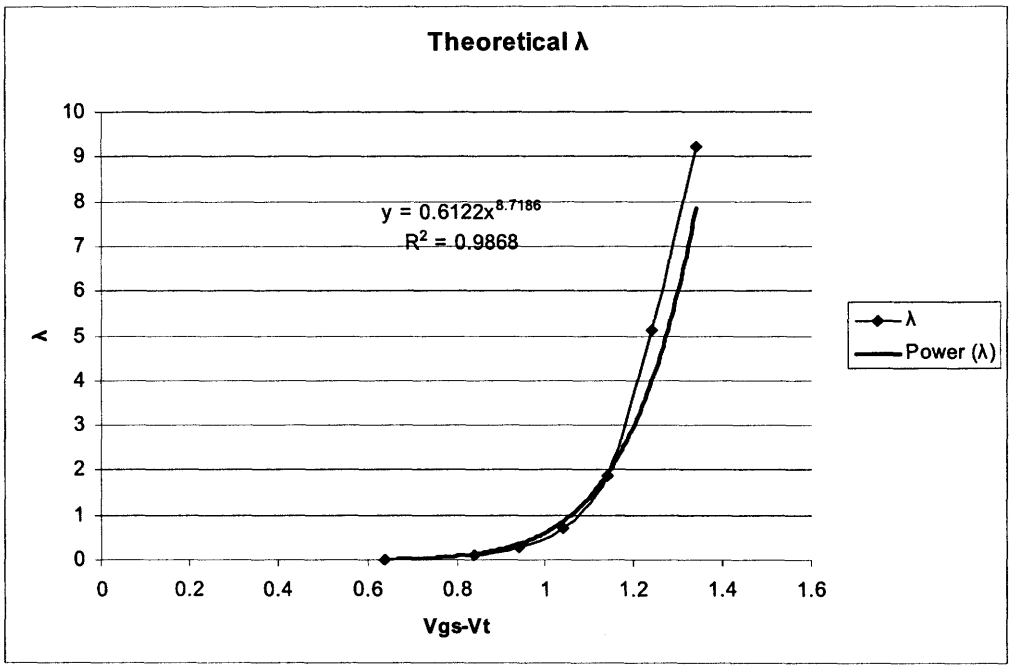


Figure II.4.12 The slope of the I-V curve λ in saturation region versus V_{gs}-V_t. From the power trendline, λ can be expressed as a function a V_{gs}-V_t.

As a result, in the saturation region, we can express the drain-source current Ids in a function of V_{gs}-V_t and V_{ds}:

$$I_{ds} = K(V_{gs} - V_t)^{\alpha} + \lambda * V_{ds}$$
$$= 0.9172 * (V_{gs} - V_t)^{4.3406} + 0.6122 * (V_{gs} - V_t)^{8.7186} * V_{ds} \qquad (2.4.6)$$

II.4.4 FITMOS I-V Model equations and data

From our above analysis, we can express the FITMOS I-V curve as different

equations in triode region and saturation region.

In triode region (modeled as the range $V_{ds} < 0.2V$), the drain source current is modeled as linearly proportional to drain-source voltage, with a slope $1/R_{on}$ that is a function of V_{gs}:

$$I_{ds} = \frac{V_{ds}}{R_{on}} = If((V_{gs} - V_t) \le 1.6734,\ 9.3495 * (V_{gs} - V_t)^{4.5431}, 78.053 Ln(V_{gs} - V_t) + 56.781) * V_{ds} \tag{2.4.7}$$

When the $V_{ds} > 0.2$ V, the FITMOS gets into saturation region:

$$\begin{aligned} I_{ds} &= K(V_{gs} - Vt)^{\alpha} + \lambda * Vds \\ &= 0.9172 * (V_{gs} - V_t)^{4.3406} + 0.6122 * (V_{gs} - V_t)^{8.7186} * V_{ds} \end{aligned} \tag{2.4.8}$$

In the end, we combine these two equations into a conditional function:

$$I_{ds} = MIN(If((V_{gs} - V_t) \le 1.6734,\ 9.3495 * (V_{gs} - V_t)^{4.5431}, 78.053 Ln(V_{gs} - V_t) + 56.781) * V_{ds},\ 0.9172 * (V_{gs} - V_t)^{4.3406} + 0.6122 * (V_{gs} - V_t)^{8.7186} * V_{ds}) \tag{2.4.9}$$

Figure II.4.13 shows the I-V plot from our equation model.

For comparison, the measured I-V curve and our modeled I-V curve are plotted in figure II.4.14; we can see that our behavioral model matches with real FITMOS I-V characteristic very well. In addition, figure II.4.15 shows our model also works for large V_{gs}.

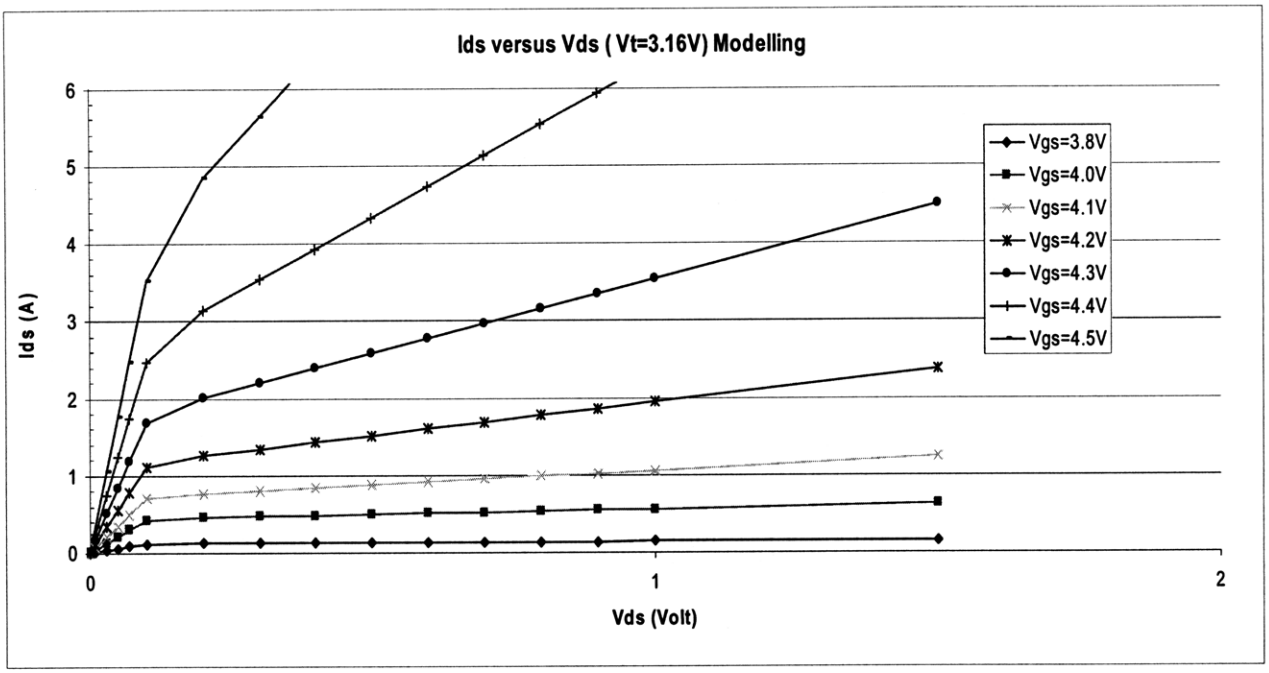


Figure II.4.13 The I-V plot from our equation model.

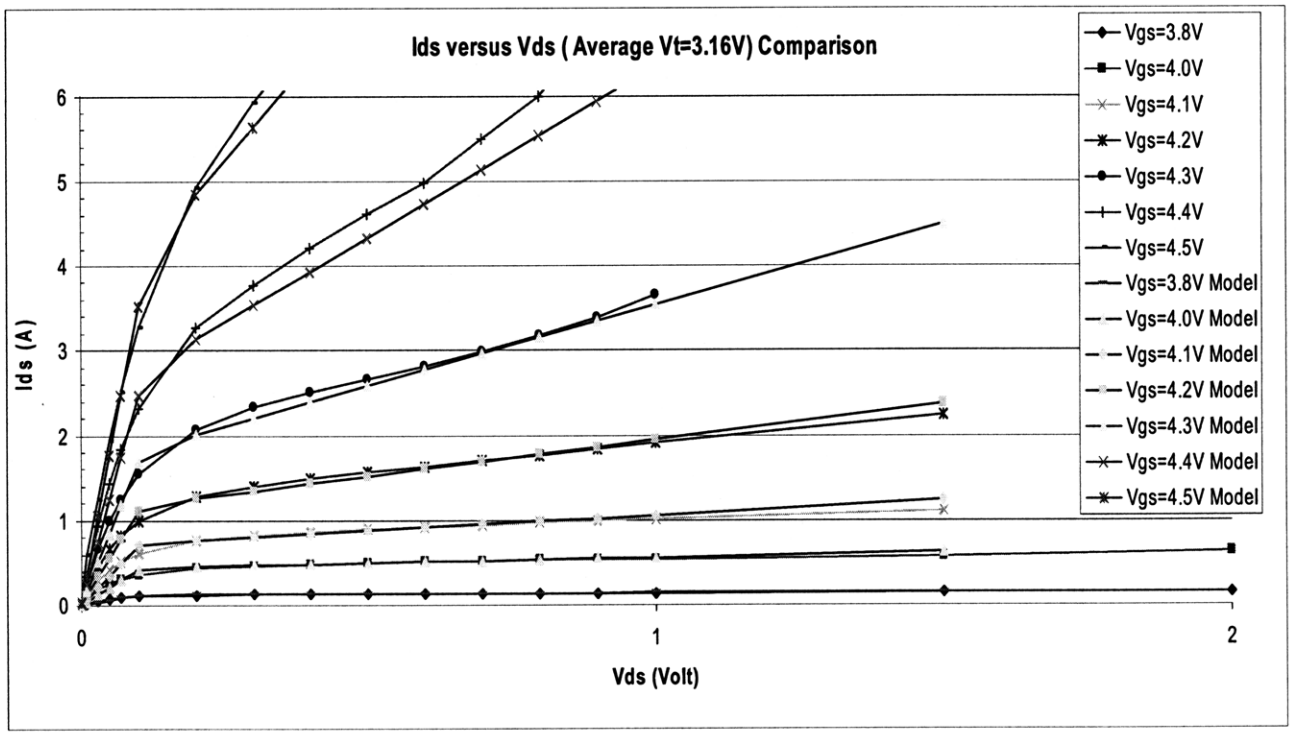


Figure II.4.14 This shows the measured FITMOS I-V characteristic and our behavioral model. Our model matches with the measurement very well.

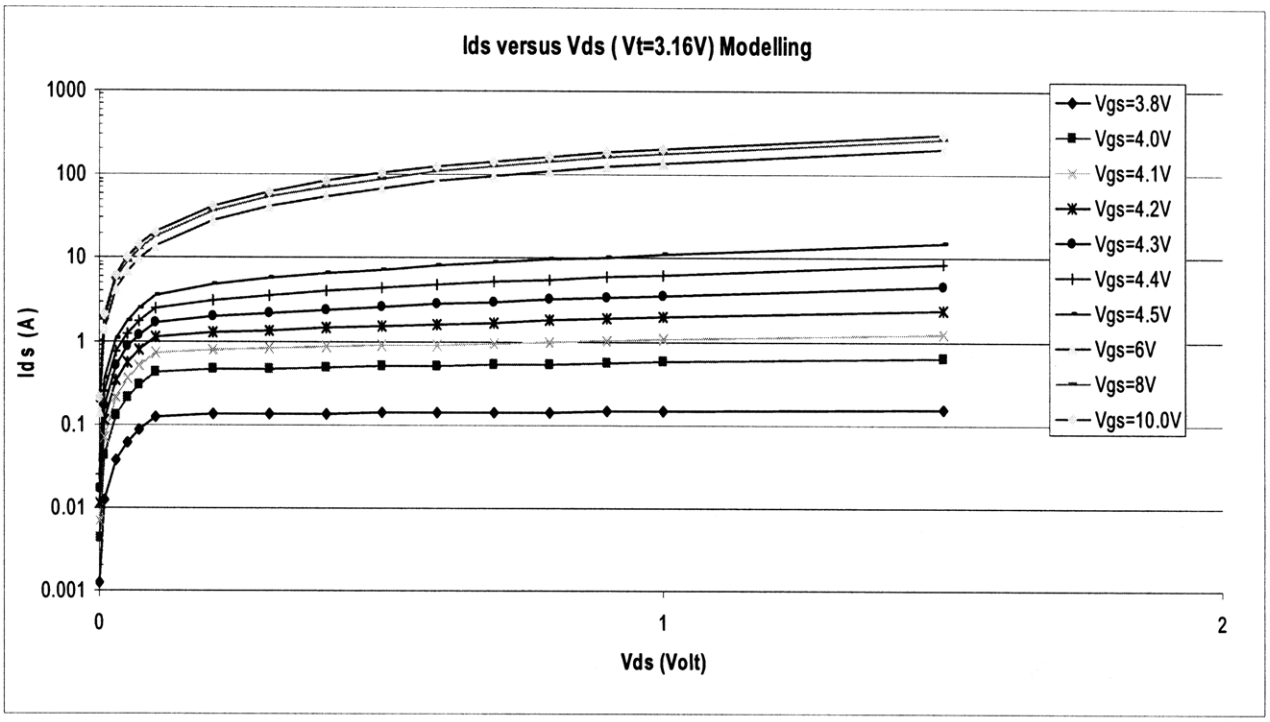


Figure II.4.15 shows the modeled I_d curve versus V_{ds} for large V_{gs}
For large V_{gs} (V_{gs} > 8V), the drain source current I_{ds} is much larger than those of relatively small V_{gs}, so I_{ds} (y-axis) is plotted on a logarithmic scale for clearer comparison.

II.4.5 Difficulties in FITMOS I-V Characteristics Modeling

In the past, the lateral MOSFET had been studied extensively. But the classical model for the current-voltage characteristics of the lateral MOSFET is based on the assumption that between drain and source only the channel resistance exists. This assumption on longer holds for the high voltage power MOS devices. Especially the FITMOS is a vertical floating island trench gate MOSFET, as a result, the conventional MOSFET model does not fit for our FITMOS devices.

In the vertical power MOSFET devices, the source and drain terminals are not only separated by the channel resistance but also all the resistances in the drain current path. Due to the special floating trench gate structure in FITMOS, the

resistances in the drain current path are not well studied. So building an analytical physical model of FITMOS requires more solid-state physics studies and device simulations. In addition, the conventional MOSFET models cannot simulate the unique power device characteristic very accurately such as quasi-saturation. As a result, building an analytical model for FITMOS is not practical in our intense schedule.

Second, since we do not have much experience in building an analytical model for conventional power MOSFETs before, it is hard for us to compare the difficulties in FITMOS modeling and in conventional power MOSFET modeling.

On the other hand, building a behavioral model is relatively simpler and can fulfill our needs for the future design simulation.

II.4.6 FITMOS and Commercial MOSFET I-V Model Simulation Comparison

This section explores the accuracy of SPICE electrical models for conventional power MOSFETs, as provided in manufacturer's datasheets. In addition, we also compare the accuracy of our FITMOS electrical model with this manufacturer model. MOSFET FDP047AN08 is used for the test. The schematic of the test circuit is shown in Figure II.4.16. Voltage source V_1 is used to sweep the drain-source voltage V_{ds} of the MOSFET. Voltage source V_2 is used to control the gate voltage V_{gs}. A small 1m ohm resistor in series with the MOSFET drain is used to monitor the drain current Ids.

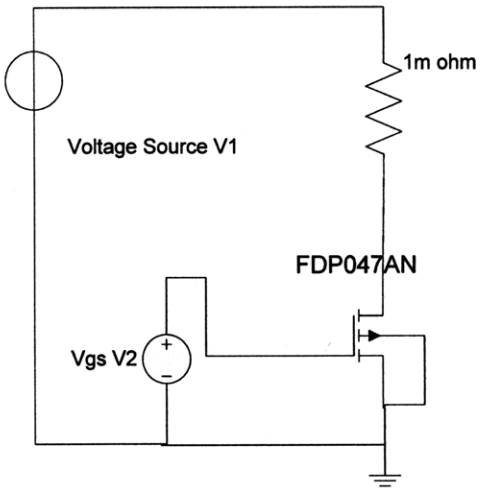


Figure II.4.16 The schematic of the test circuit used in simulation and measurement.

First, the experimental output characteristic of the FDP047AN is shown in figure II.4.17. From the experimental data, the threshold voltage is measured as 2.74 V (Ids = 1mA), which is in the range of the datasheet specified (2V-4V).

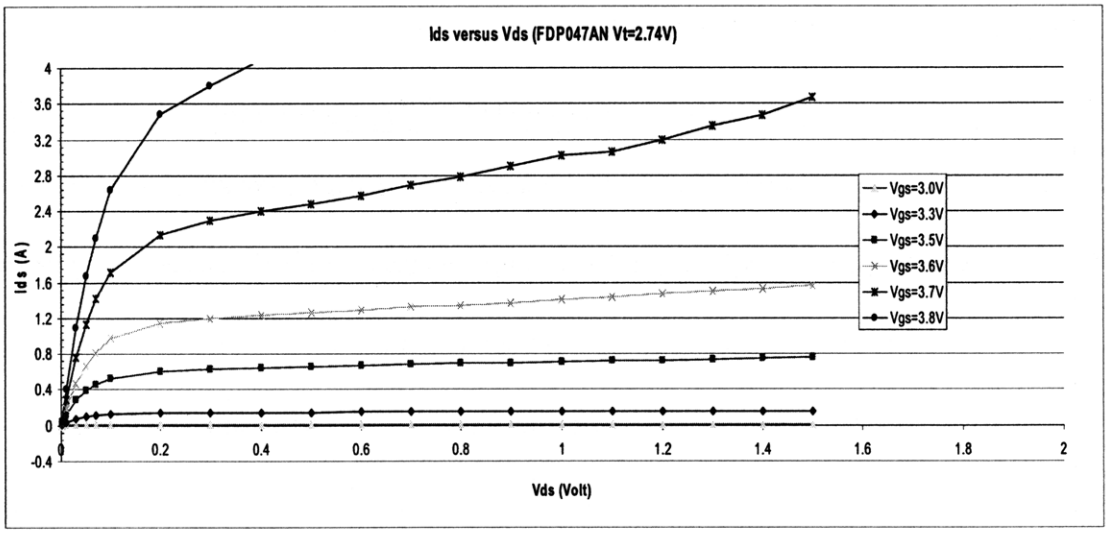


Figure II.4.17 Experimental I-V characteristics of the conventional power MOSFET FDP047AN.

Figure II.4.18 shows the threshold simulation from the manufacturer's datasheet spice model (shown in detail in the appendix). As we can see, the threshold voltage is about 3.3 V for I_{ds}=1mA, which is about 0.6V larger than our experimental

measurement (a wide variation of possible thresholds is allowed in the datasheet). In this case, the simulation of the I-V characteristics of this MOSFET will not match with the experimental data with the same gate voltage.

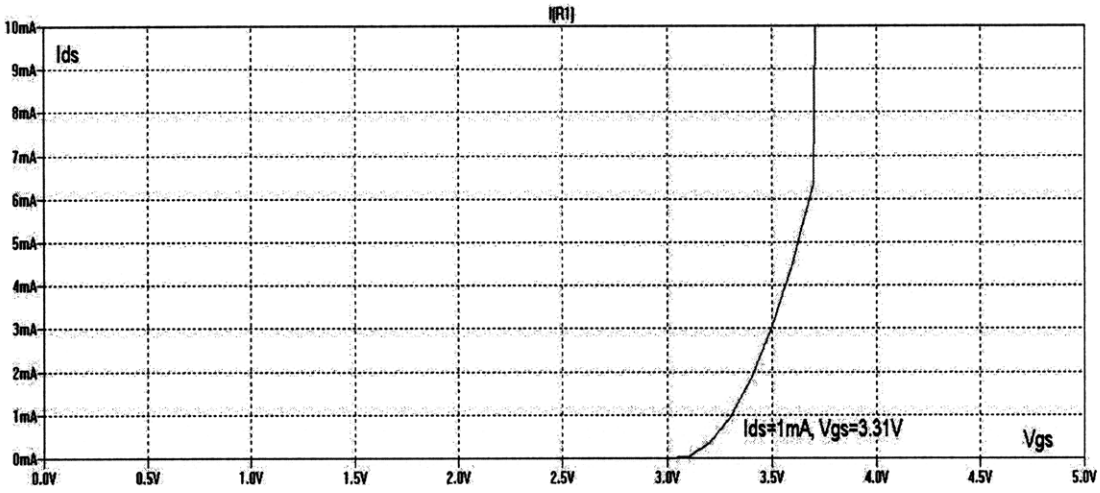


Figure II.4.18 Simulation result for the threshold voltage of the FDP047AN using the manufacturer's Pspice model.
Vt = 3.31V for Ids=1mA and Vds = 10V

Figure II.4.19 shows the simulation of the I-V characteristics of the conventional power MOSFET using the manufacturer's Pspice behavioral model. Since the threshold voltage in the spice model is smaller than the real device, with the same gate voltage, the simulated drain current is much smaller than our experimental data.

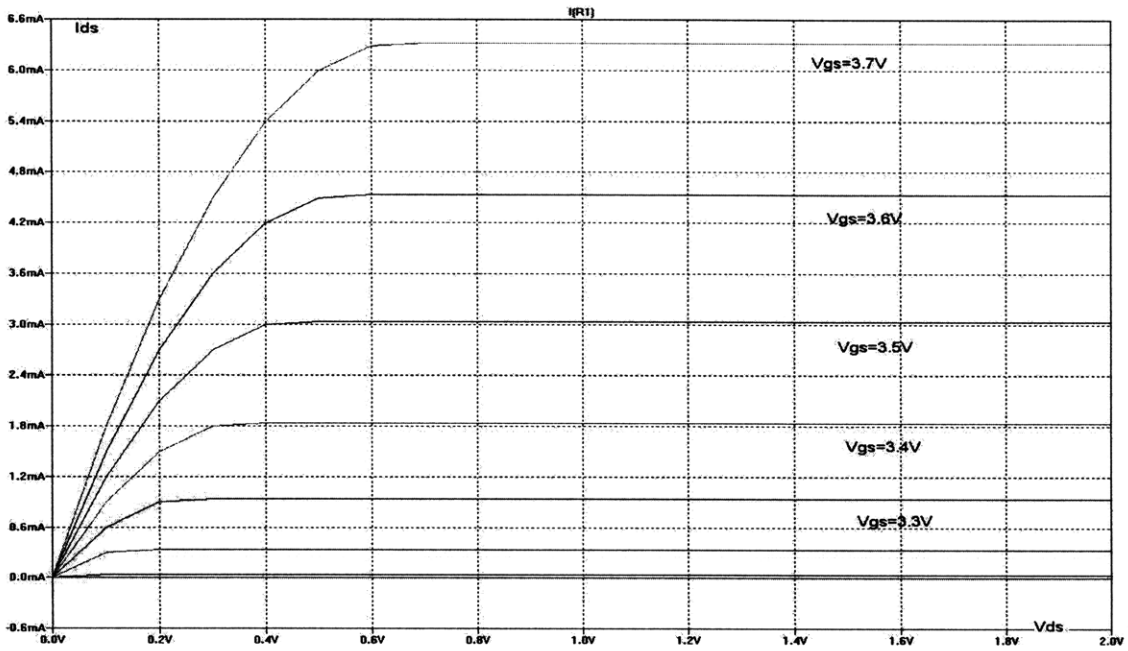


Figure II.4.19 Simulation plot of the I-V characteristics of the conventional power MOSFET FDP047AN.

For a better comparison, the gate voltage level in the simulation was increased to obtain a similar drain current output level as in the measurement. Figure II.4.20 shows the modified simulation of the I-V characteristics curves for the MOSFET FDP047AN. In order to achieve a higher drain current level, the gate voltage is increased 0.7 V higher, which matches with the threshold voltage error (about 0.6V).

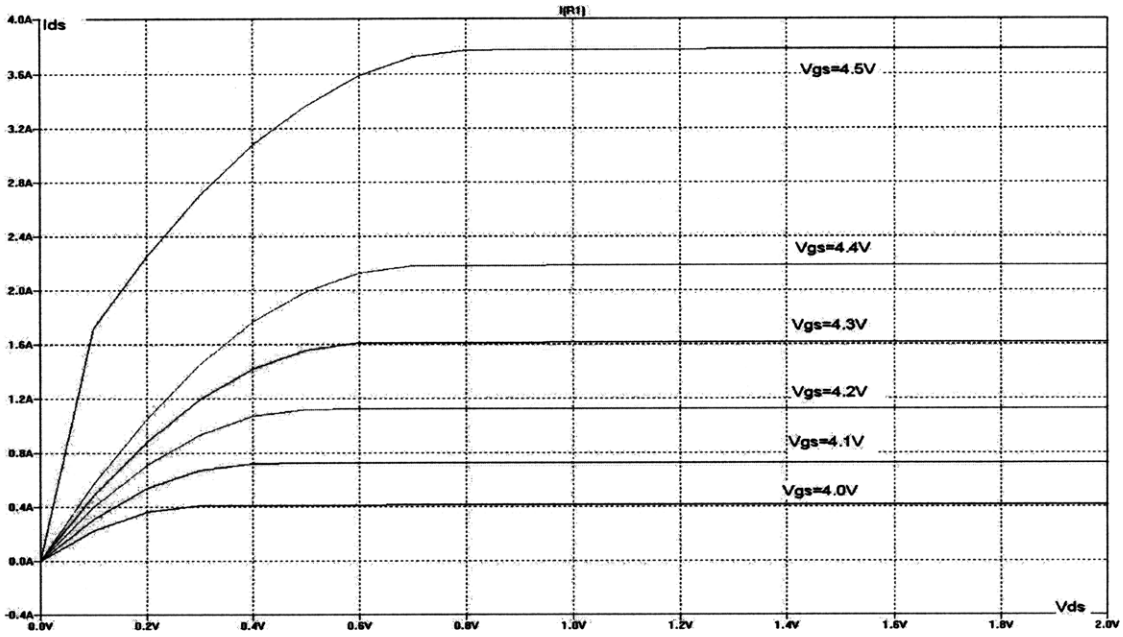


Figure II.4.20 Simulation plot of the I-V characteristics of the conventional power MOSFET FDP047AN with higher gate voltage.

From the above graph, we can see that the simulation result does not match very well with our experimental data for the commercial MOSFET (figure II.4.17). In the simulation, the drain current I_{ds} stays constant for high V_{ds}. But in the experiment, Ids does not stay flat when V_{ds} is high. In addition, the spice model from the datasheet cannot accurately predict the triode region as well. In our measurement, the actual R_{on} in the triode region is significantly smaller than in the simulation. As a result, the spice model for the conventional power MOSFET in the datasheet only give us a very rough approximation to actual device behavior.

Now, we look at our FITMOS model performance. Figure II.4.21 shows that our FITMOS behavioral model in simulation can predict the FITMOS I-V characteristics very well in SPICE.

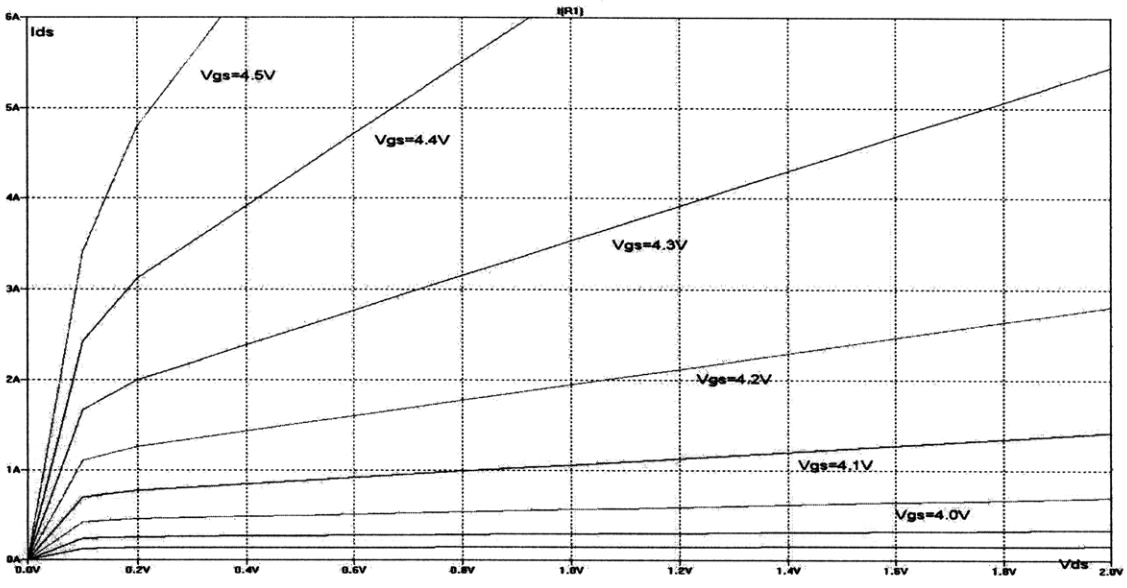


Figure II.4.21 The I-V characteristics simulation of FITMOS with different gate voltages. This simulation was done in Linear Technology LTspice.

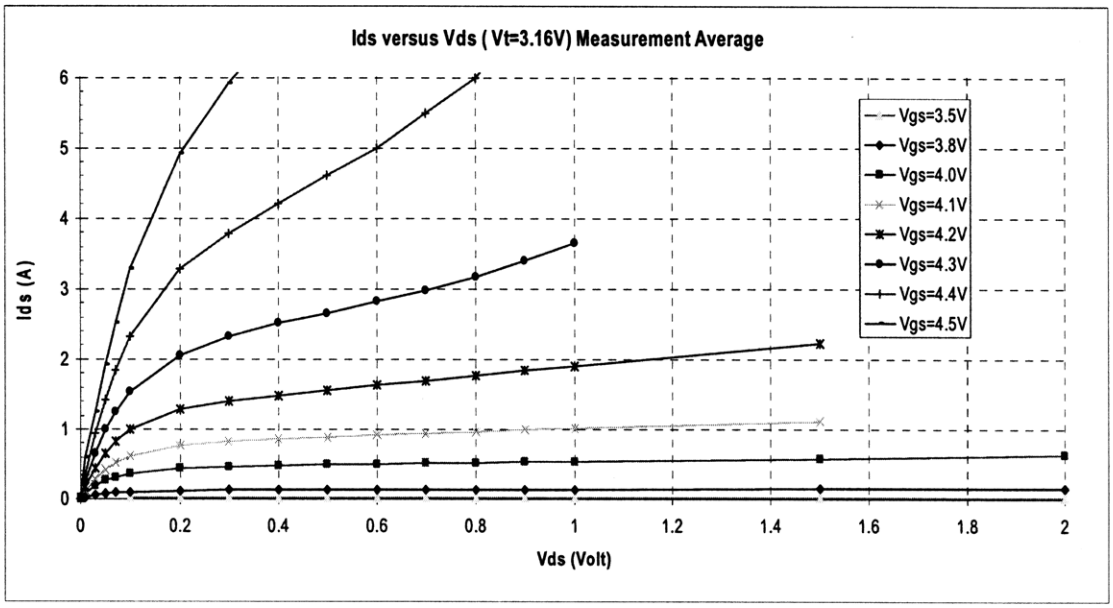


Figure II.4.22 The I-V characteristics measurement plot of FITMOS with different gate voltages.

We can see that the simulation result matches with the experimental data very well. We conclude that even for commercial power MOSFETs, detailed I-V modeling is typically only very approximate. And our FITMOS behavioral model can predict the device electrical behavior within an acceptable accuracy range.

II.5 Gate Charge Measurement

Gate charge is an important factor in determining device loss in switching applications, and is often an element in device figures of merit. From the gate charge, designer can easily calculate the amount of current required from the drive circuit to switch the device on in a desired length of time [3]. This section describes the measurement of Toyota FITMOS device Q-gate. We focus on the "B" series of MOSFETs, using four devices (B_2, B_5, B_{10} and B_{17}) in the measurements.

II.5.1 Measurement Setup

The schematic of the test circuit is shown in figure II.5.1. In order to measure the gate charge, a constant current source is required to supply a stable current for the gate of the FITMOS. As a result, a voltage regulator LM117 is used as a 50mA current source for the MOSFET. In order to measure the actual current flowing into the gate of the MOSFET, a 11 ohm resistor R_2 is connected in series of the gate. By measuring the voltage across R_2, we can calculate the actual current from the ohm's law I=V/R (from the measurement, the actual gate current is about 42.5mA). In addition, a low on-resistance NMOS FDV301N driven by a gate driver UC3710 is used to discharge the gate of the FITMOS periodically. When the NMOS FDV301N is on, the gate current flows into the NMOS and the gate voltage of the FITMOS is discharged to nearly 0V. When the NMOS is off, the current source starts charging the gate of the FITMOS again. By knowing the time it takes to charge up the gate of the FITMOS, we can calculate the gate charge from $Q_{gate} = I_{\_gate}*t$. A

current-limited DC power supply (HP 6012A) in series with a four parallel 43 Ω power resistors was used to apply 40V Drain-Source voltage to the MOSFET. The switching frequency for the MOSFET is 10 kHz. The total Q_{gate} is defined as the total charge needed to charge the gate up to 10V.

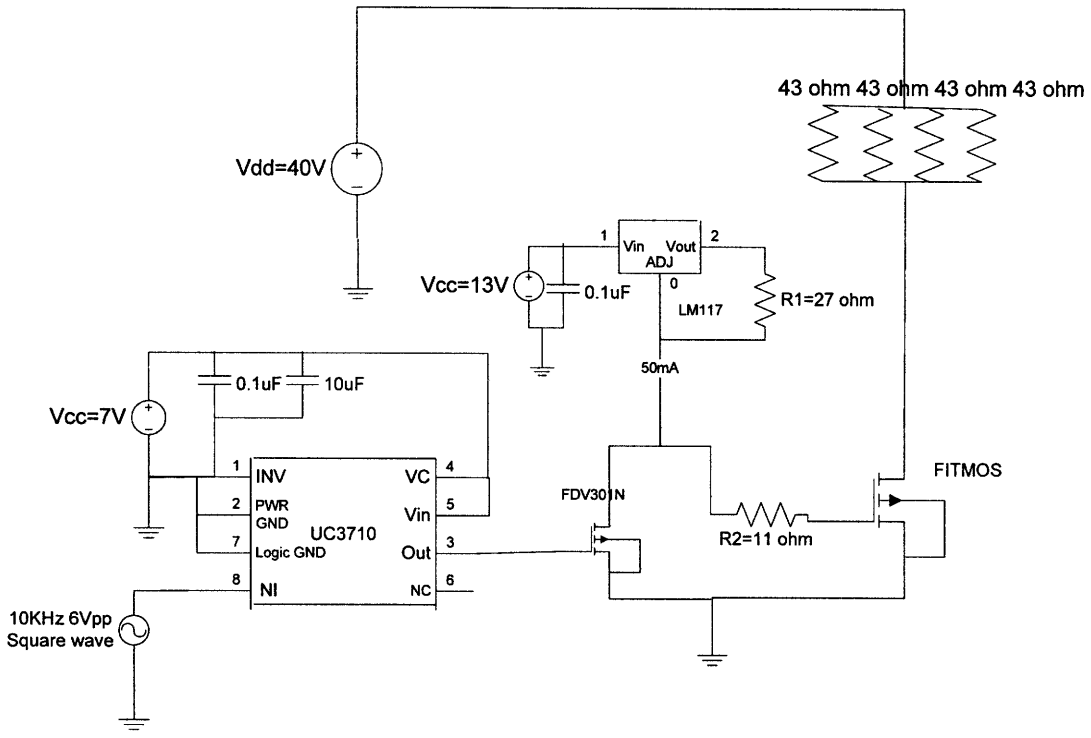


Figure II.5.1 The schematic of the test circuit used in gate charge measurement. A DC power supply (CSI3003XIII) is used to provide the power for the gate driver UC3710 and voltage regulator LM117. A function generator (HP 8111A) is used to provide a 10kHz square wave for the gate driver. The 40V Drain-Source voltage for the FITMOS is provide by a current-limited DC power supply (HP 6012A).

A typical Gate Charge waveform is shown in figure II.5.2. From time t_0, the drive current starts charging the gate source capacitance Cgs and the gate voltage starts increasing. During t_0 to t_1, C_{gs} continues to charge and gate voltage continues to rise. At time t_1, C_{gs} is completely charged. From figure II.5.2, we can see that

V_{gs} becomes constant from time t_1 to t_2 after C_{gs} is fully charged. At this time, the drive current starts to charge the gate-drain capacitance C_{gd} (also called Miller capacitance). This continues until time t_2. Once both of the capacitances C_{gs} and C_{gd} are fully charged at time t_2, gate voltage V_{gs} starts increasing again until it reaches the supply voltage at time t_3. As a result, the total gate charge Q_g is the drive current $I_{\_gate}$ times the total time that takes to charge the gate to 10V (a common datasheet merit), $Q_g = I_{\_gate} * (t_3 - t_0)$. $Q_{gs} = I_{\_gate} e * (t_1 - t_0)$ and $Q_{gd} = I_{\_gate} * (t_2 - t_1)$.

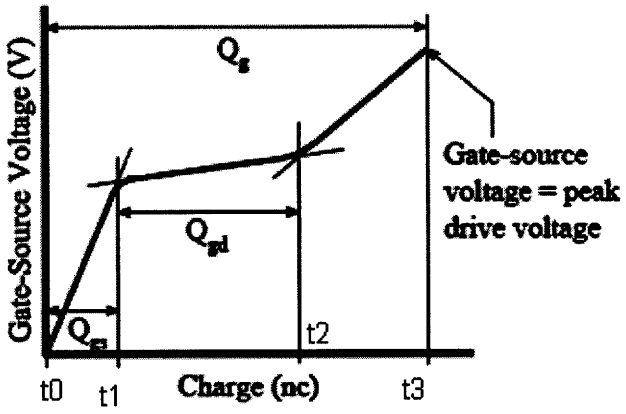


Figure II.5.2 A typical waveform for the Vgs as a function of Gate charge.

II.5.2 Results and Comparison

	B2	B5	B10	B17	Average	Maximum
$Q_{g(TOT)}$	82.4nC	82.3nC	78.2nC	78.6nC	79.6nC	82.7nC
Q_{gs}	19.4nC	20.5nC	20.6nC	19.5nC	20nC	20.6nC
Q_{gd}	26.7nC	22.5nC	21.2nC	22.2nC	23.2nC	26.7nC

Table II.5.1 Q_{gate} total, Q_{gs} and Q_{gd} for each MOSFET we tested.

	FITMOS	IRFB3307ZPbF	IRFB3207ZPbF	IRF1312	SUP90N08	IXTP220N075	IXTP200N085T	FDP047AN08A0	2SK3228	TK60A08J1	2SK3510	2SK3511
Ron (150°C)	8.19 mΩ	9.78 mΩ	6.77 mΩ	20 mΩ	8.64 mΩ	9mΩ	10.5 mΩ	8.46 mΩ	10.6 mΩ	11 mΩ	12.8 mΩ	19.5 mΩ
Qgd	23.2 nC	24nC	33nC	34nC	28nC	50nC	42nC	21nC	30nC	20nC	52nC	35nC
$\sqrt{Ron*Qgd}$	1.38e-5 $(\Omega.C)^{1/2}$	1.53e-5 $(\Omega.C)^{1/2}$	1.49e-5 $(\Omega.C)^{1/2}$	2.61e-5 $(\Omega.C)^{1/2}$	1.56e-5 $(\Omega.C)^{1/2}$	2.12e-5 $(\Omega.C)^{1/2}$	2.1e-5 $(\Omega.C)^{1/2}$	1.33e-5 $(\Omega.C)^{1/2}$	1.78e-5 $(\Omega.C)^{1/2}$	1.48e-5 $(\Omega.C)^{1/2}$	2.58e-5 $(\Omega.C)^{1/2}$	2.61e-5 $(\Omega.C)^{1/2}$
Improvement	0%	9.8%	7.4%	47.1%	11.5%	34.9%	34.3%	-3.8%	22.5%	6.8%	46.5%	47.1%

Table II.5.2 The device Figure of Merit comparisons at 150°C between FITMOS and other 11 commercialized power MOSFETs.

As described above, the time to switch a MOSFET switch in a power application is determined by the required gate charge (along with the current drive capability of the driver). The duration of the switching transition partly determines the amount of overlap between voltage and current during the switching transition, which yields switching loss. (In fact, overlap loss is only one component of the total switching loss.) Moreover, the duration for which the gate-drain (or "Miller") capacitance is charged is often particularly important in determining switching loss. Consequently, the required gate-drain charge sometimes plays a part in switching device figures of merit. For example, to incorporate both switching and conduction loss, a simple figure of merit (or FOM) $=\sqrt{R_{on}*Q_{gd}}$ is defined by Huang [2]. While this figure of merit does not completely capture the loss tradeoffs in MOSFET switches, it is often used as a crude measure when comparing switches.

Here we apply the above-referenced figure of merit $\sqrt{R_{on} * Q_{gd}}$ to both the FITMOS "B-series" devices and several commercial devices. We use the "at temperature" on-state resistance (at 150 °C) and the Q_{gd} value for 40 V drain-source voltage (approximately half of rated V_{ds}, a common datasheet metric). From table II.5.2, we can see that the FITMOS devices provide 7% to 47% improvement in Figure of Merit (very approximately related to dissipation) compared to most of the conventional power MOSFETs, except the FDP047AN08A0, which has a FOM 3.8% better than the FITMOS devices. This suggests that FITMOS devices are highly competitive with (and in many cases substantially better than) available state-of-the art devices in terms of this common FOM. However, as the calculations going into the proposed FOM do not capture all of the important device loss mechanisms, we cannot draw detailed performance conclusions from this comparison. Such conclusions must await a more detailed study which will be performed as part of this research program.

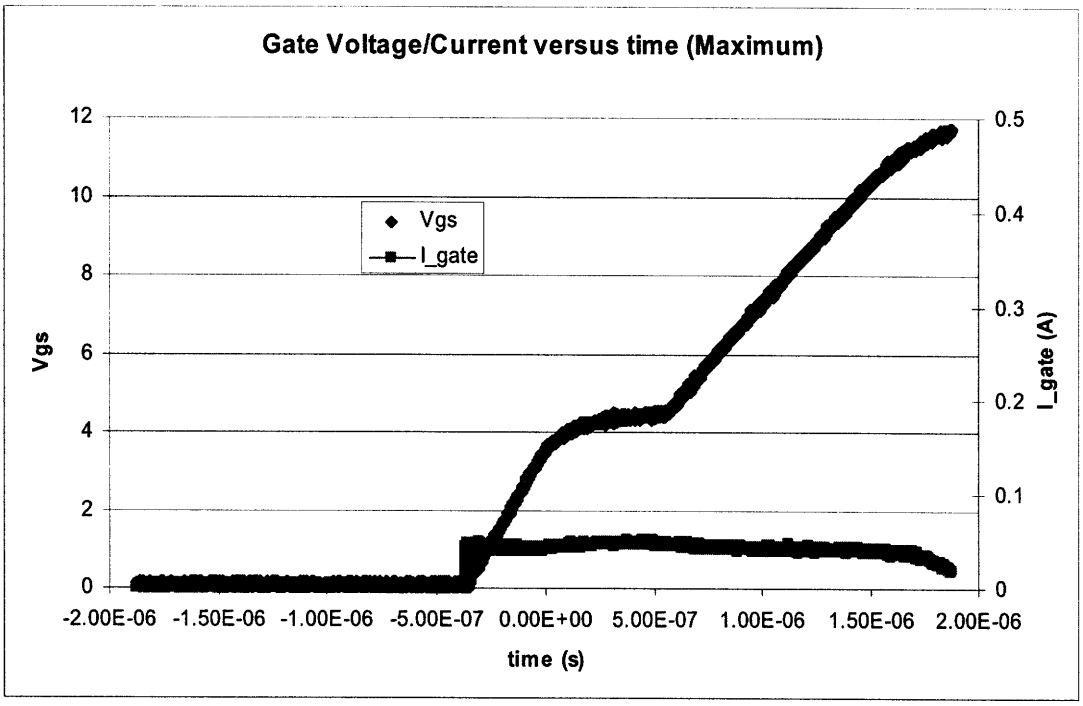


Figure II.5.3 The maximum gate voltage and current versus time.
During the charging time, we can see that the gate current is pretty stable at 42mA.

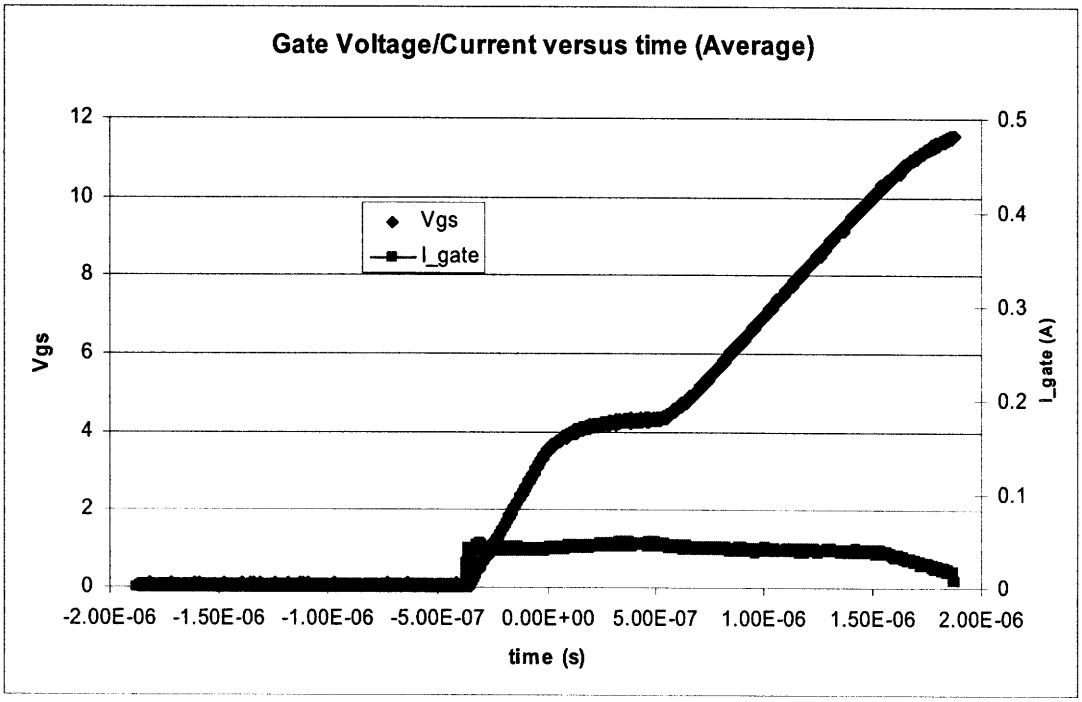


Figure II.5.4 The average gate voltage and current versus time.

II.5.3 Scope Screen Shots for Qgate measurement.

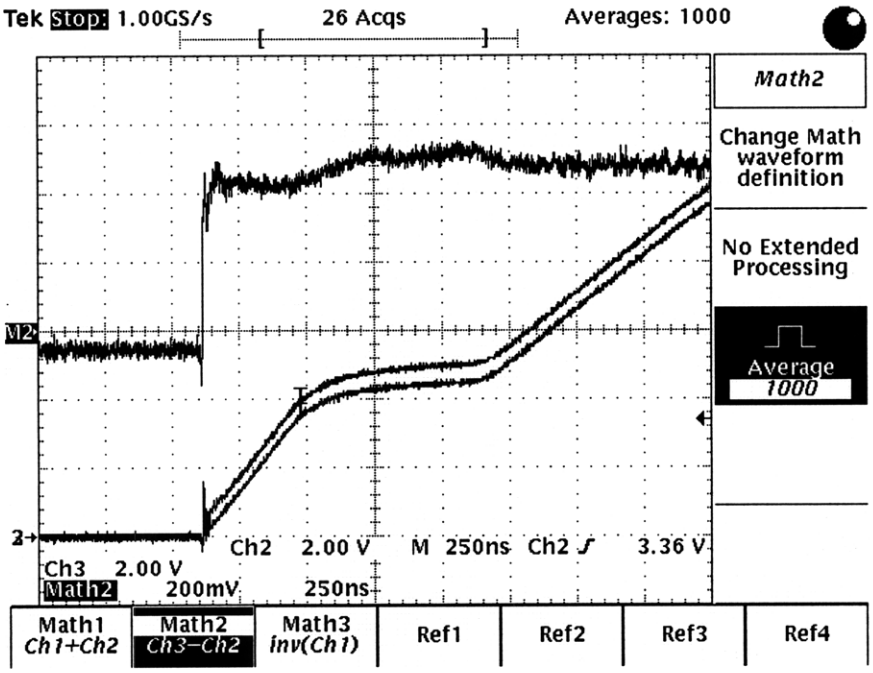


Figure II.5.5 . Scope screen shot for B2 Q_{gate} measurement

Channel2 and channel 3 are measuring the different voltages across the 11 ohm resistor in series with the gate of the MOSFET. The difference between channel2 and channel3 (Math2) shows the voltage across the resistor. From I=V/R, we can calculate the actual gate current for the MOSFET.

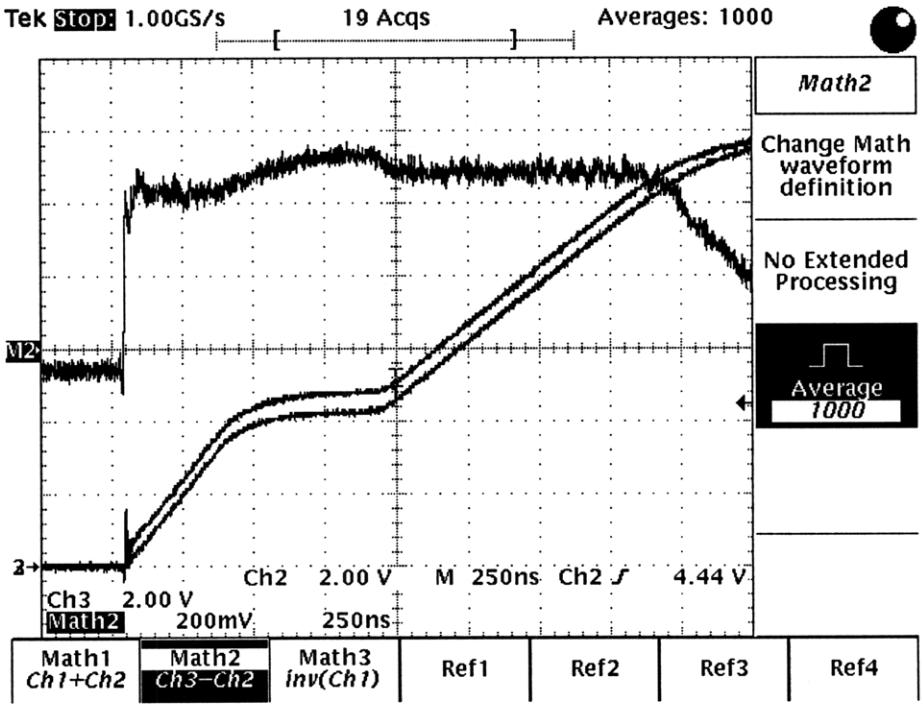


Figure II.5.6 Scope screen shot for B5 Q_{gate} measurement

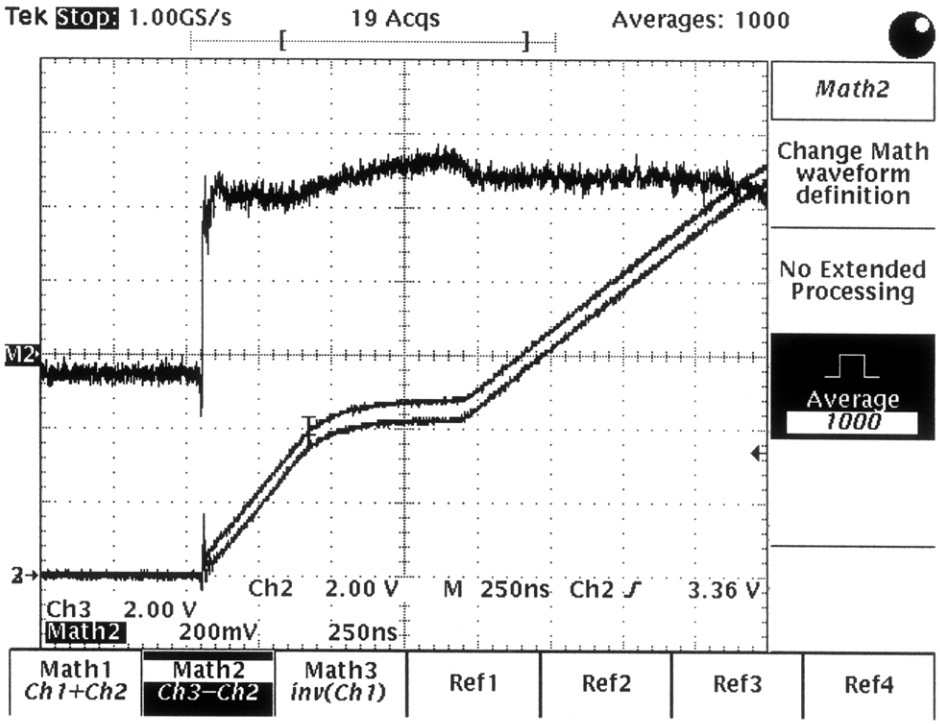


Figure II.5.7 Scope screen shot for B10 Q_{gate} measurement.

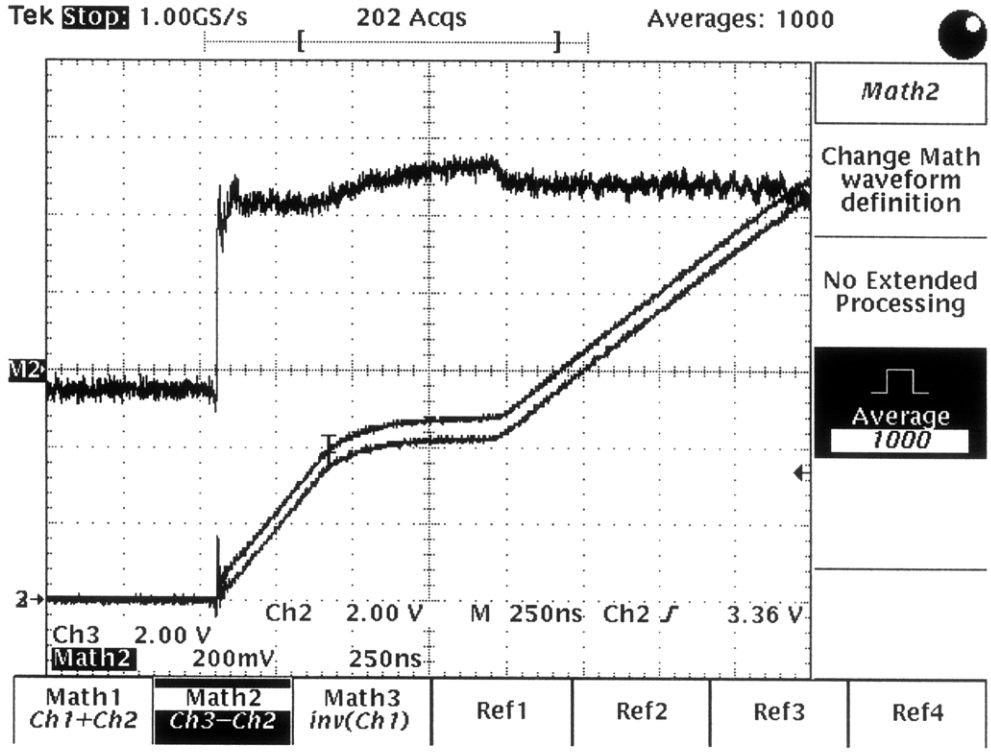


Figure II.5.8 Scope screen shot for B17 Q_{gate} measurement.

II.6 Gate-Drain Capacitance (C_{gd}) Modeling

Gate Drain capacitance is a very important factor in determining device loss in switching applications. In order to have a more accurate simulation and estimation, an accurate C_{gd} model is necessary. This section describes the measurement and modeling of Toyota FITMOS device Gate-Drain capacitance. We focus on the "B" series of MOSFETs, using four devices (B_2, B_5, B_{10} and B_{17}) in the measurements.

II.6.1 Measurement Setup

The schematic of the test circuit is shown in figure II.6.1. The gate-drain capacitance measurement setup is the same as the Q_{gate} measurement setup described in a previous report. A voltage regulator LM117 is used as a 50mA current source for the MOSFET. In order to measure the actual current flowing into the gate of the MOSFET, a 11 ohm resistor R_2 is connected in series with the gate. By measuring the voltage across R_2, we can calculate the actual current from Ohm's law I=V/R (from the measurement, the actual gate current is about 42.5mA). In addition, a low on-resistance NMOS FDV301N driven by a gate driver UC3710 is used to discharge the gate of the FITMOS periodically. When the NMOS FDV301N is on, the gate current flows into the NMOS and the gate voltage of the FITMOS is discharged to nearly 0V. When the NMOS is off, the current source starts charging the gate of the FITMOS again. By knowing the time it takes to charge up the gate-drain capacitor, we can calculate the ΔQ_{gd} from $\Delta Q_{gd} = I_{\_gate}*t$. The incremental gate-drain capacitance C_{gd} is equal to $\Delta Q_{gd}/\Delta V_{gd}$. A current-limited DC power supply (HP 6012A) in series

with a four parallel 43 Ω power resistors was used to apply 40V Drain-Source voltage to the MOSFET. The switching frequency for the MOSFET is 10 kHz.

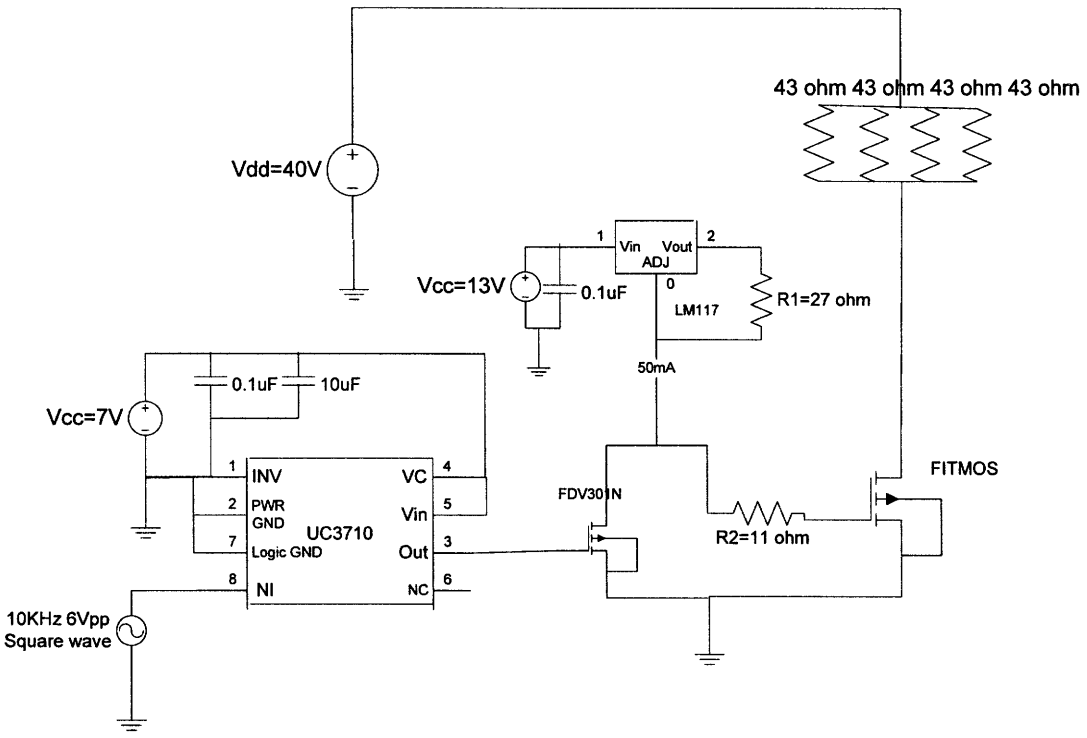


Figure II.6.1 The schematic of the test circuit used in the C_{gd} and Q_{gd} measurements. A DC power supply (CSI3003XIII) is used to provide the power for the gate driver UC3710 and voltage regulator LM117. A function generator (HP 8111A) is used to provide a 10kHz square wave for the gate driver. The 40V Drain-Source voltage for the FITMOS is provide by a current-limited DC power supply (HP 6012A).

A typical Gate Charge waveform is shown in figure II.6.2. From figure II.6.2, we can see that V_{gs} becomes constant from time t_1 to t_2 after C_{gs} is fully charged. At this time, the drive current starts to charge the gate-drain capacitance C_{gd} (also called Miller capacitance). This continues until time t_2. As a result, in this time interval t_1 to t_2, we can extract the C_{gd} accurately by using equation $C_{gd}=\Delta Q_{gd}/\Delta V_{gd}$ and $\Delta Q_{gd}=I\_{gate}*\Delta t$. At the same time, we also measured the drain-source voltage V_{ds}. From all these data, we can plot C_{gd} in a function of V_{dg} ($V_{dg}=V_{ds}-V_{gd}$).

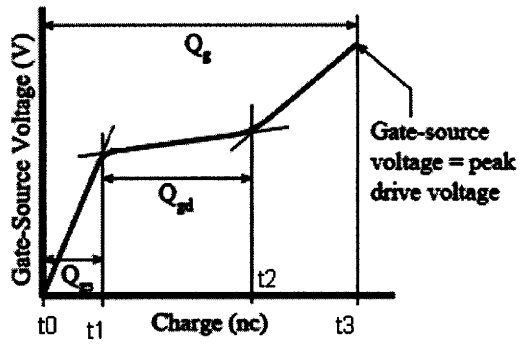


Figure II.6.2 A typical waveform for the Vgs as a function of Gate charge.

Figure II.6.3 shows the actual measurement data plot for the V_{gs} and V_{ds}. There is a good match with the typical Vgs waveform above.

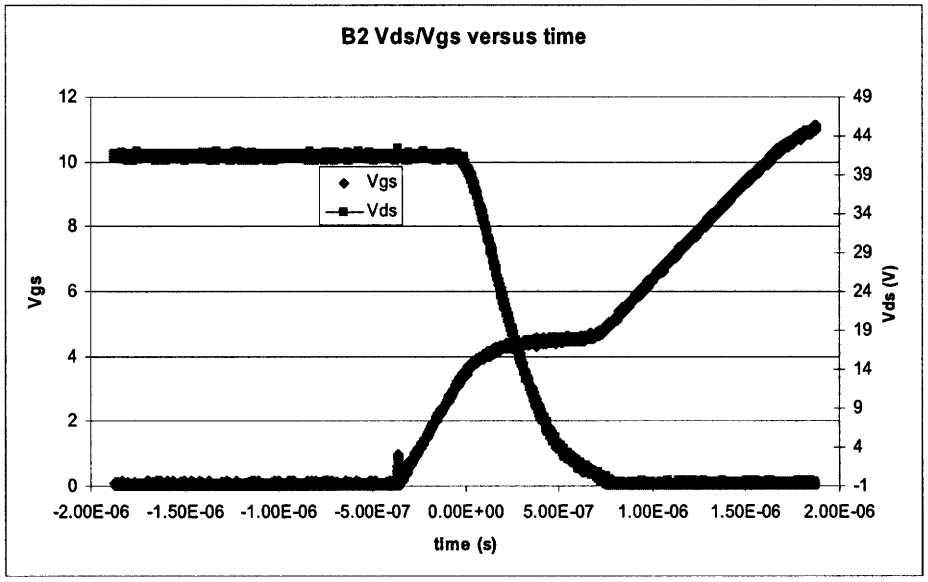


Figure II.6.3 The experimental plot for Vgs and Vds versus time.

II.6.2 Data Analysis

To facilitate simulation, the device capacitances are modeled using appropriate functional forms. These models are intended as simple behavioral models, and do not necessarily reflect physical behavior.

As expected, C_{DG} varies with drain-source bias, decreasing as Drain-Gate bias voltage increases. A simple junction capacitance model was selected to model this

variation, with parameters selected to fit the observed variation. The model used is:

$$C(V) = \frac{C_{j0}}{\left(1 + \frac{V}{\phi}\right)^m} \qquad (2.6.1)$$

With C_{j0}, m, and ϕ selected to fit the data.

Three data points (V_1, C_1, V_2, C_2, V_3, C_3) from the experimental data were chosen fit the curve. The data points were selected to yield a good overall match to the curves. It was found that selecting data points at V=-2, 5, and 15 V yielded a good overall match to the curves.

The value of parameter ϕ was calculated by finding the zero of the function:

$$f(\phi) = \frac{\ln(\phi + V_2) - \ln(\phi + V_1)}{\ln(\phi + V_3) - \ln(\phi + V_1)} - \frac{\ln(C_1/C_2)}{\ln(C_1/C_3)} \qquad (2.6.2)$$

This value of ϕ was calculated numerically in MATLAB as the zero of the function given input values for V_1, C_1, V_2, C_2, V_3, C_3.

Values for m and C_{j0} were then calculated as:

$$m = \frac{\ln(C_1/C_2)}{\ln(\phi + V_2) - \ln(\phi + V_1)} \quad \text{or} \quad m = \frac{\ln(C_1/C_3)}{\ln(\phi + V_3) - \ln(\phi + V_1)} \qquad (2.6.3)$$

and

$$C_{j0} = C_1\left(1 + \frac{V_1}{\phi}\right)^m \text{ or } C_{j0} = C_2\left(1 + \frac{V_2}{\phi}\right)^m \text{ or } C_{j0} = C_3\left(1 + \frac{V_3}{\phi}\right)^m \qquad (2.6.4)$$

After identifying candidate values of ϕ, m, and C_{j0}, using this method for given points (e.g., capacitances at V=-2, 5, and 15 V), the function was plotted on top of the raw data graphs to verify a good fit to the data.

The Parameters of the function that best fit our average data for C_{DG} were:

$$\begin{array}{|l} \phi = 4.3 \\ m = 0.1031 \\ C_{j0} = 0.4472 \end{array} \quad \text{when} \quad \begin{array}{|l} V_1 = -2 \\ V_2 = 5 \\ V_3 = 15 \end{array}$$

giving the function graph:

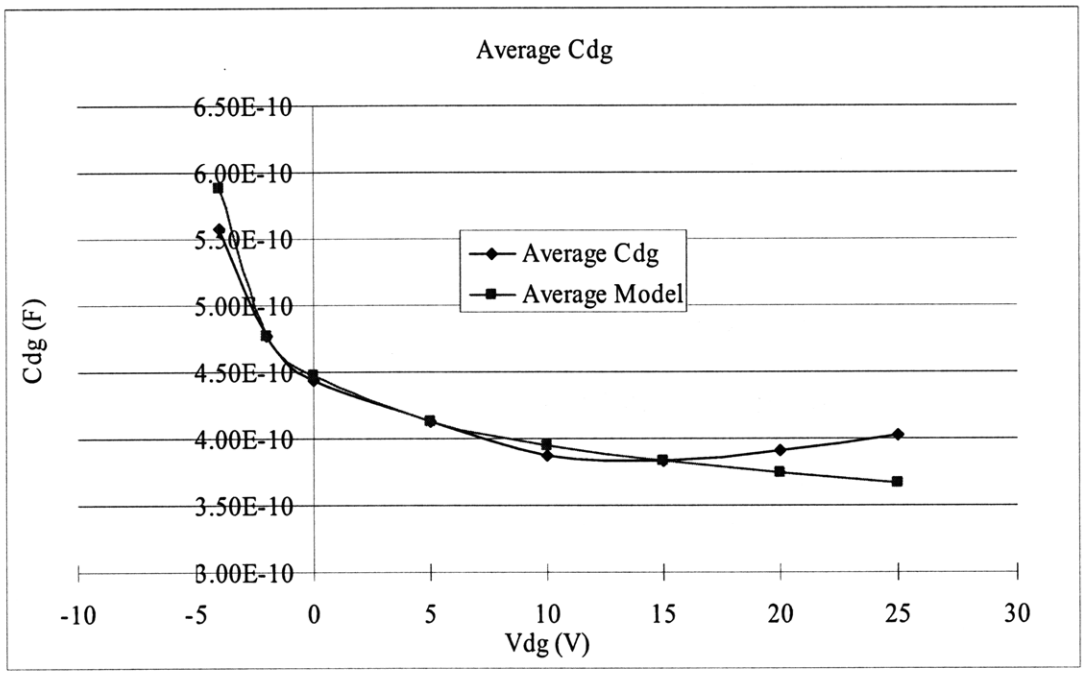


Figure II.6.4 Average Cdg model and measurement data comparison

The Parameters of the functions that best fit our Maximum data for C_{DG} were:

$$\begin{boxed}\begin{aligned}\phi &= 10.11\\ m &= 0.3124\\ C_{j0} &= 0.5918\end{aligned}\end{boxed} \quad \text{when} \quad \begin{boxed}\begin{aligned}V_1 &= -2\\ V_2 &= 5\\ V_3 &= 15\end{aligned}\end{boxed}$$

giving the function graph:

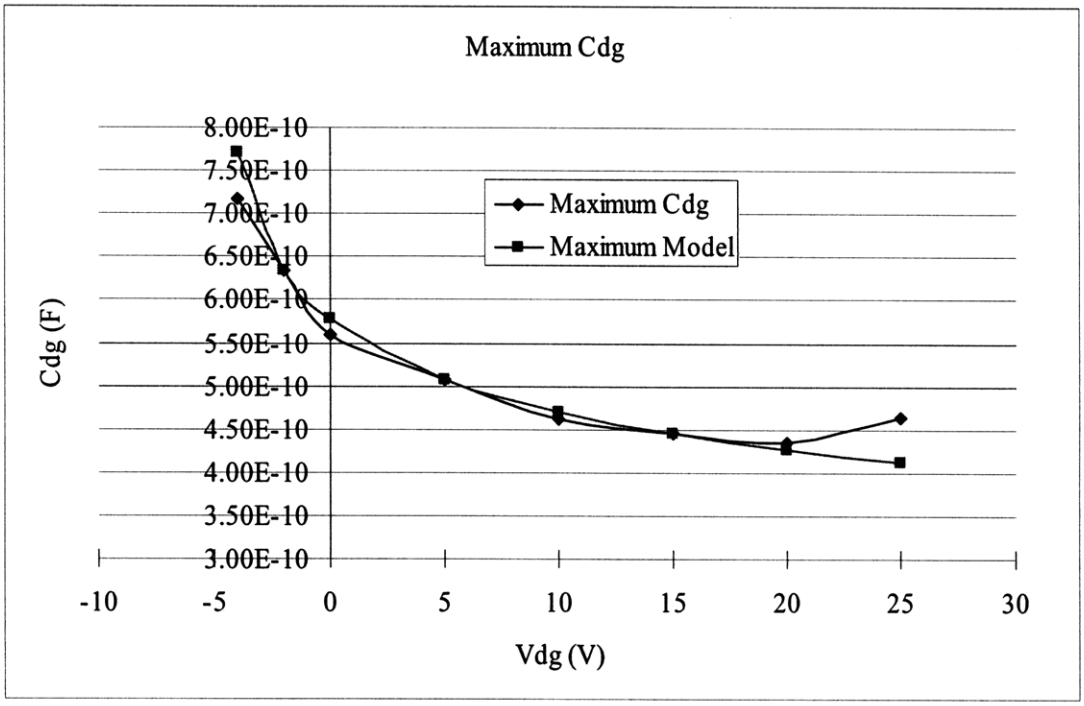


Figure II.6.5 Maximum Cdg model and measurement data comparison

For comparison, an equivalent circuit in figure II.6.6 is used for simulation in LTspice. A 43mA current source is used to provide the gate current for the FITMOS.

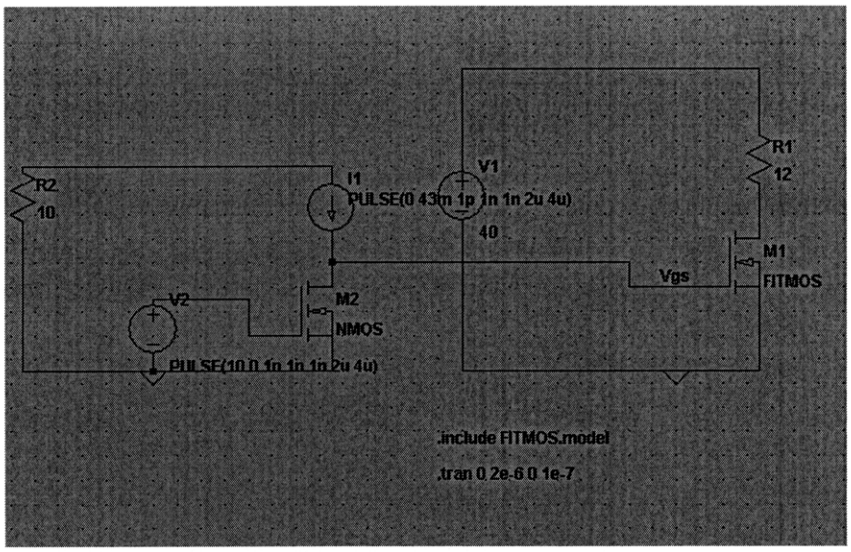


Figure II.6.6 The circuit schematic used in the LTspice
The FITMOS model includes the capacitance model for the gate charge simulation.

From Figure II.6.7, we can see that our FITMOS model can provide a similar gate voltage Vgs waveform as in the experimental measurement.

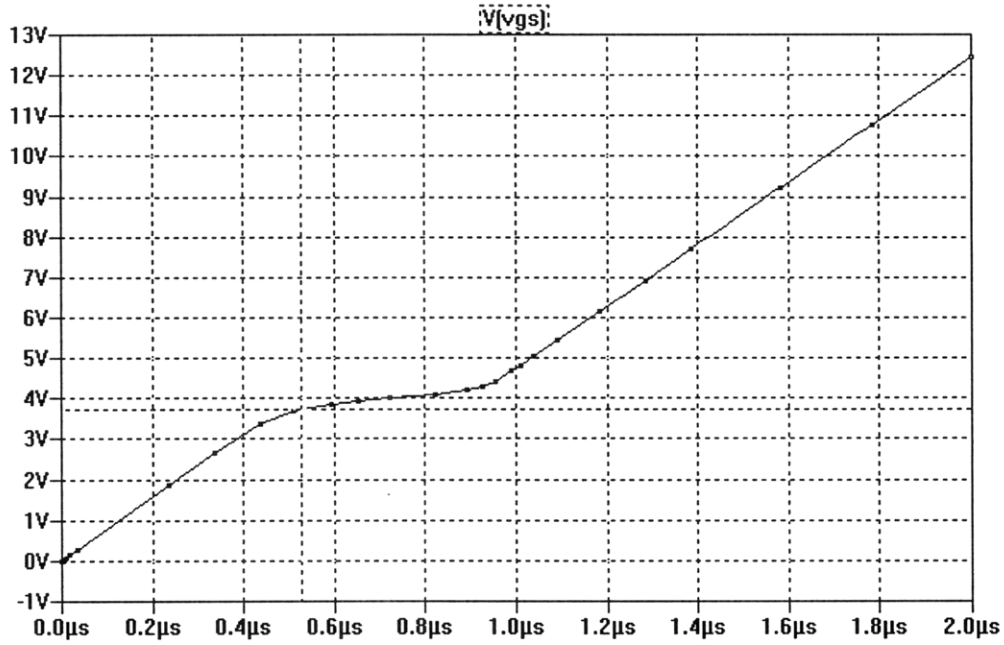


Figure II.6.7 The gate voltage Vgs waveform from the LTspice simulation.

	Measurement	Simulation	error
Q_{gate}	79.6nC	72.24nC	9.24%
Q_{gs}	20nC	21.07nC	5.35%
Q_{gd}	23.2nC	19.4nC	16.4%

Table II.6.1 Simulation and Measurement comparison for Q_{gate}, Q_{gs} and Q_{gd}.

From the above table, we can see that our FITMOS model can give us a quite accurate approximation for the gate charge simulation. As a result, this FITMOS model should be able to provide a good estimation for the switching power loss in the future simulation.

II.6.3 Sample Scope Screen Shots for C_{gd} measurement.

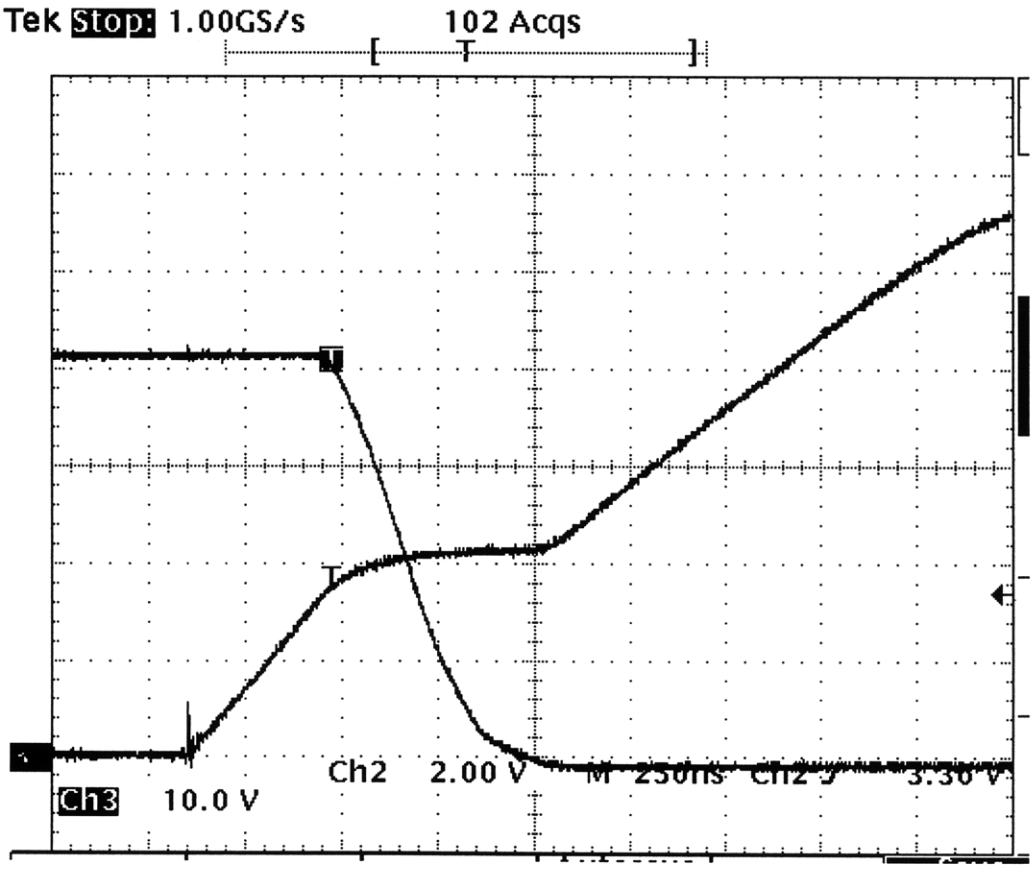


Figure II.6.8 Scope screen shot for B2 C_{gd} measurement
Channel2 is measuring the gate-source voltage V_{gs} and channel3 is measuring the drain-source voltage V_{ds}.

II.7 Reverse Recovery Modeling

Reverse recovery is one of the important loss mechanisms for the power MOSFETs. It happens when the diode is turned from the forward biased to reverse biased. The diode has to sweep out the excessive minor carriers in the junction before it can block the large negative voltage. We believe that the reverse recovery loss can produce noticeable discrepancy between simulation and experimental measurement. In order to obtain an accurate Spice model for our future optimization simulation processes, we need to capture this power and frequency dependent loss well. So in this section, we measured and studied the reverse recovery characteristic for FITMOS and compare it with one of our commercial power MOSFETs FDP047AN.

II.7.1 Measurement Setup

Figure II.7.1 shows the schematic of our reverse recovery measurement [7] [8]. Our proto-type boost DC-DC converter is suitable for this measurement. We first diode connected the top MOSFETs. When we turn off the low-side MOSFET, the body diode of the top MOSFET is forced to turn on and it is forward biased. Once we turn on the low-side MOSFET, it draws out all the current and turns off the high-side body diode. So at this moment, we capture the body diode reverse recovery behavior in the high-side MOSFET. A Tektronix TCP202 current probe is used to measure the current going through the body diode. And the voltage across the diode is measured by the Tektronix P5205 differential voltage probe. For standard comparison, we set the di/dt of the diode falling current to be 100A/us by controlling the gate resistance

of the low-side MOSFET. The diode reverse bias voltage, output voltage of the boost converter is 40V. And we did this measurement for three current settings by controlling the output power to be 200W, 100W and 50W.

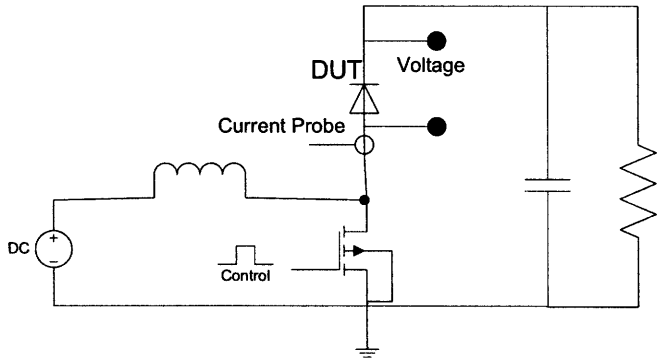


Figure II.7.1 Reverse recovery measurement schematic in our proto-type DC-DC converter.

II.7.2 Experiment Results

We first use the other MOSFETs to test our measurement setup. Figure II.7.2 shows the reverse recovery characteristics for the commercial MOSFET FDP047AN. From the I-V plot, we can observe the reverse recovery behavior clearly. The body diode voltage cannot increase until the diode current reaches the negative peak. Then the diode starts to block the reverse biased voltage rapidly. Also, we can see that the reverse recovery charge, reverse recovery time and the peak negative current all increase as the forward current increases. When forward current is 10A with 100A/us di/dt, the reverse recovery charge for FDP047AN is 512nC. Unfortunately, this number is significantly larger than what stated on the manufacture datasheet. As a result, we need to investigate our experimental setup to make sure the accuracy of our measurement.

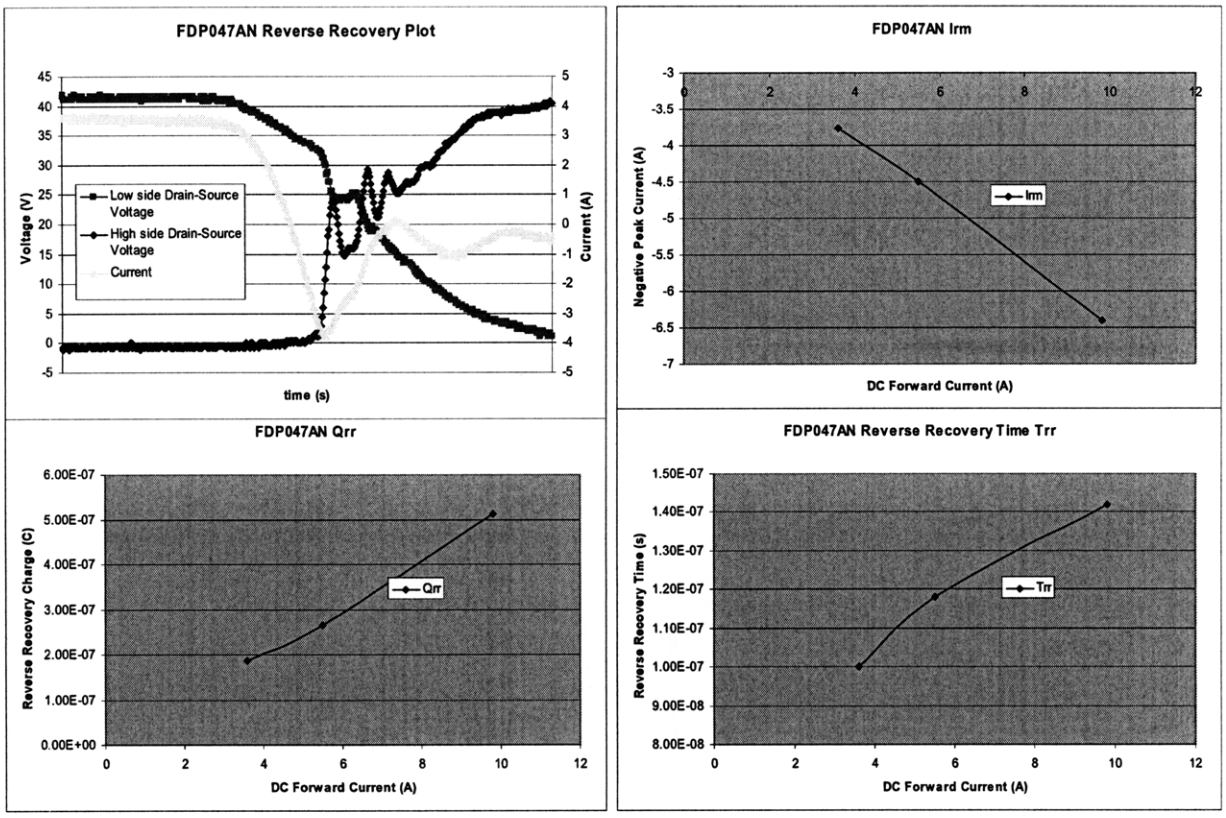


Figure II.7.2 It shows the reverse recovery characteristics for FDP047AN.

In addition, we also measured the reverse recovery characteristics for FITMOS, which is shown in figure II.7.3. With 10A forward current and 100A/us, the reverse recovery charge in FITMOS is only 240nC, which is only half of the commercial power MOSFET FDP047AN. And also, the reverse recovery time and peak negative current in the FITMOS are also significantly smaller than the FDP047AN. But again, these data are much bigger than our theoretical prediction. A experiment setup with better accuracy is preferred for this measurement.

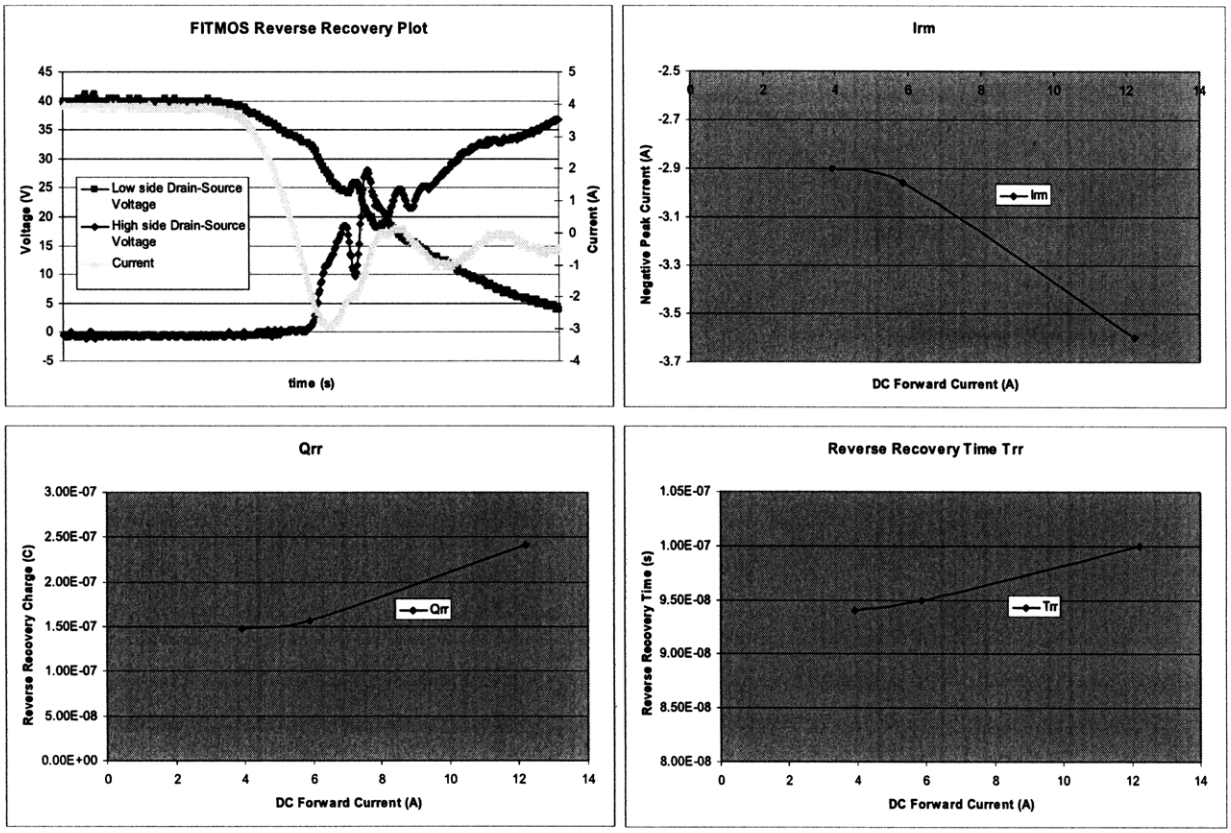


Figure II.7.3 It shows reverse recovery characteristics for FITMOS

II.7.3 Measurement Error Investigation

In the previous section, we use a boost converter to test the reverse recovery characteristics on the body diode of the high-side MOSFET. Unfortunately, the data we measured is off from our expectation. This can be due to the large parasitic inductance in the measurement loop. In order to get a more accurate measurement and eliminate the inductance effect from the current probe, we convert our converter into a DC-DC buck converter and measure the reverse recovery on the body diode of the low-side MOSFET. In stead of using a current probe, we use a current sensing resistor in the source to measure the current. In this setup, we reduce the parasitic

inductance in the circuit loop and will be able to get a more accurate measurement.

II.7.4 Improved Measurement Setup

Figure II.7.4 shows the schematic of our reverse recovery measurement. We used our converter as a DC-DC Buck converter for this measurement. The low-side MOSFET is diode connected. When the control MOSFET is off, all the output current goes through the body diode in the low-side MOSFET. Once we turn on the high-side MOSFET, all the current will be drawn by the high-side MOSFET. The body diode in the low-side MOSFET is forced to turn off. So at this moment, we can measure the reverse recovery behavior of the body diode. For the current sensing, we used four 1.2 ohm surface mount resistor in parallel, which give a very flat resistive response up to 100MHz. Furthermore, in order to eliminate the high frequency ringing for our measurements, an EMI suppression bead was used in the drain of the testing MOSFET. For standard comparison, we set the di/dt of the diode falling current to be 100A/us by controlling the gate resistance of the high-side MOSFET. The diode reverse bias voltage, input voltage of the buck converter is 40V. And we did this measurement for three current settings by controlling the output power to be 400W, 200W and 100W.

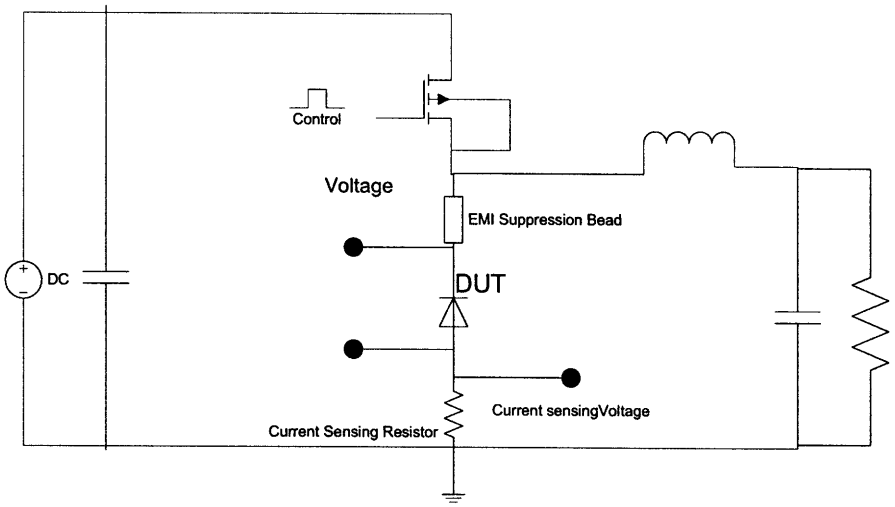


Figure II.7.4 Reverse recovery measurement schematic in our proto-type DC-DC converter.

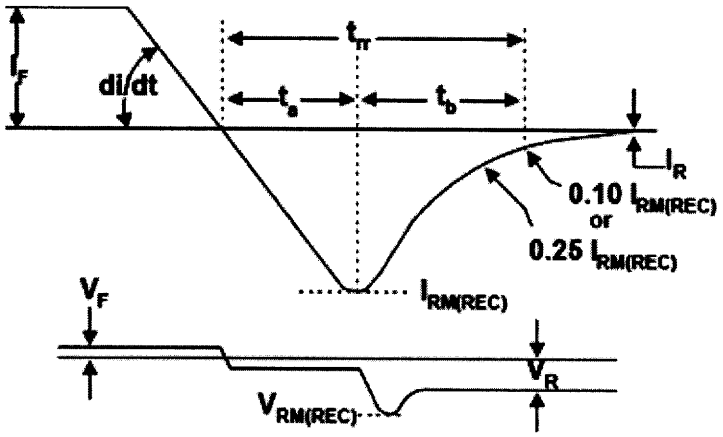


Figure II.7.5 Typical Rectifier Response for Reverse Recovery [6].

Figure II.7.5 shows a typical reverse recovery wave form for a diode. During the T_a period, the diode sweeps out the excessive minor carriers in the junction, and has not yet support the reverse voltage. T_a is controlled by the minority carrier lifetime constant. After the current reaches its negative peak value, the diode is charging the junction capacitance to support the reverse bias voltage. So during the T_b period, the charge is provided for the drain-source capacitance C_{ds}. This charge is affected by the test reverse bias voltage.

II.7.5 Final Reverse Recovery Result and Modeling

We did the reverse recovery measurement for both FITMOS and the commercial MOSFET FDP047AN. And figure II.7.6 shows a sample measurement waveform for FITMOS and FDP047AN. The forward current is 6.7A and di/dt is 100A/us. From the plot, we can see that FITMOS has a shorter T_a, which gives less excessive minority charges. But unfortunately, FITMOS has a larger junction capacitance charge. As a result, FITMOS has a larger overall reverse recovery charge Q_{rr}.

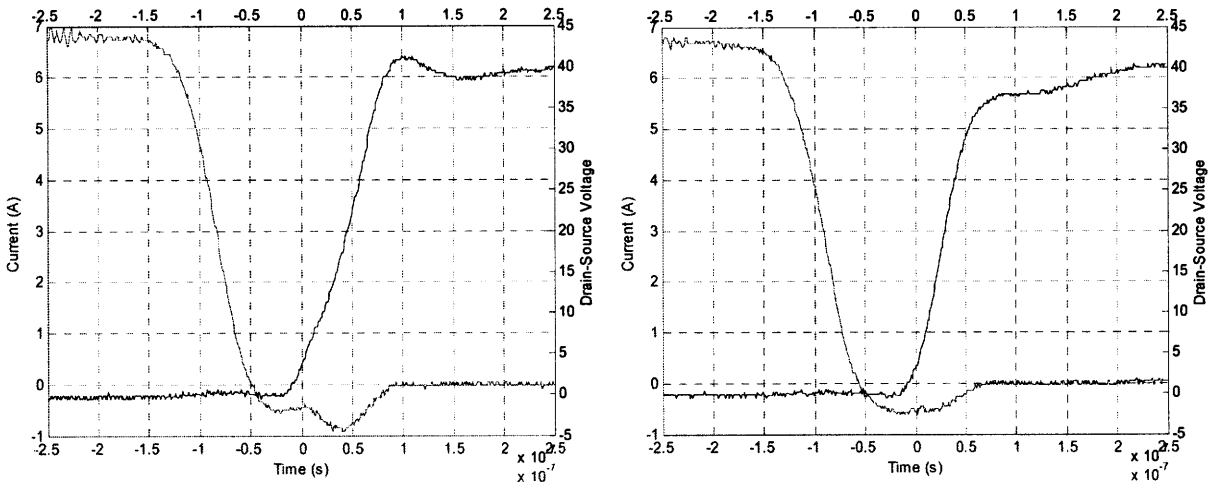


Figure II.7.6 Sample reverse recovery wave form
The left is for FITMOS and the right one is FDP047AN. Forward current is 6.7A and di/dt is 100A/us.

Table II.7.1 shows the detail reverse recovery comparison for FITMOS and FDP047AN. From the table, we further confirm that FITMOS has a shorter T_a across three different forward currents and hence a shorter minority carrier life time constant and less excessive minority carrier charge in the junction. But due to the larger junction capacitance, FITMOS has larger total reverse recovery charge compare to the

FDP047AN.

FDP047AN					
If	Irm	Ta	Trr	Qa*	Qrr
3.4A	-0.8A	32ns	103ns	17nC	52.7nC
6.7A	-0.56A	40ns	126ns	16nC	47.7nC
9.1A	-0.53A	52ns	129ns	20nC	48.3nC

FITMOS					
If	Irm	Ta	Trr	Qa*	Qrr
3.4A	-0.9A	22ns	104ns	12.9nC	78.2nC*
6.7A	-0.56A	31ns	140ns	12nC	69.5nC
9.1A	-0.53A	34ns	167ns	11.1nC	68.5nC

Table II.7.1 The detail reverse recovery characteristics for FITMOS and FDP047AN

***Qa is the charge for excessive minority carrier in T_a period only**

***For FITMOS at If=3.4A, there is an overshoot at drain-source voltage Vds when the diode is turned off. So the effective Vds is 50V instead of 40V for other measurements. As a result, its Qrr is also larger than others.**

Once we collected enough data for the reverse recovery characteristic, we can implement the spice model for the body diode to model the reverse recovery for FITMOS [9] [10]. To model the excessive minority charge in the junction, we extracted the minority carrier life time constant base on our measurement by using equation

$$Tt = \frac{Ta}{Ln(\frac{I_f - I_{rm}}{I_f})}, \qquad (2.7.1)$$

which is 12.4ns. The junction capacitance is modeled by the C_{ds} capacitance.

Figure II.7.7 shows simulated reverse recovery wave form and simulation setup for FITMOS. Since there is no EMI suppression bead in the simulation, there is a high frequency ringing in the wave form. In addition, this also affects the reverse recovery time T_{rr}. But the purpose of the simulation is to capture all the detail loss in the

MOSFET and estimate the performance of the converter. As a result, we only care the reverse recovery charge Q_{rr} in the simulation.

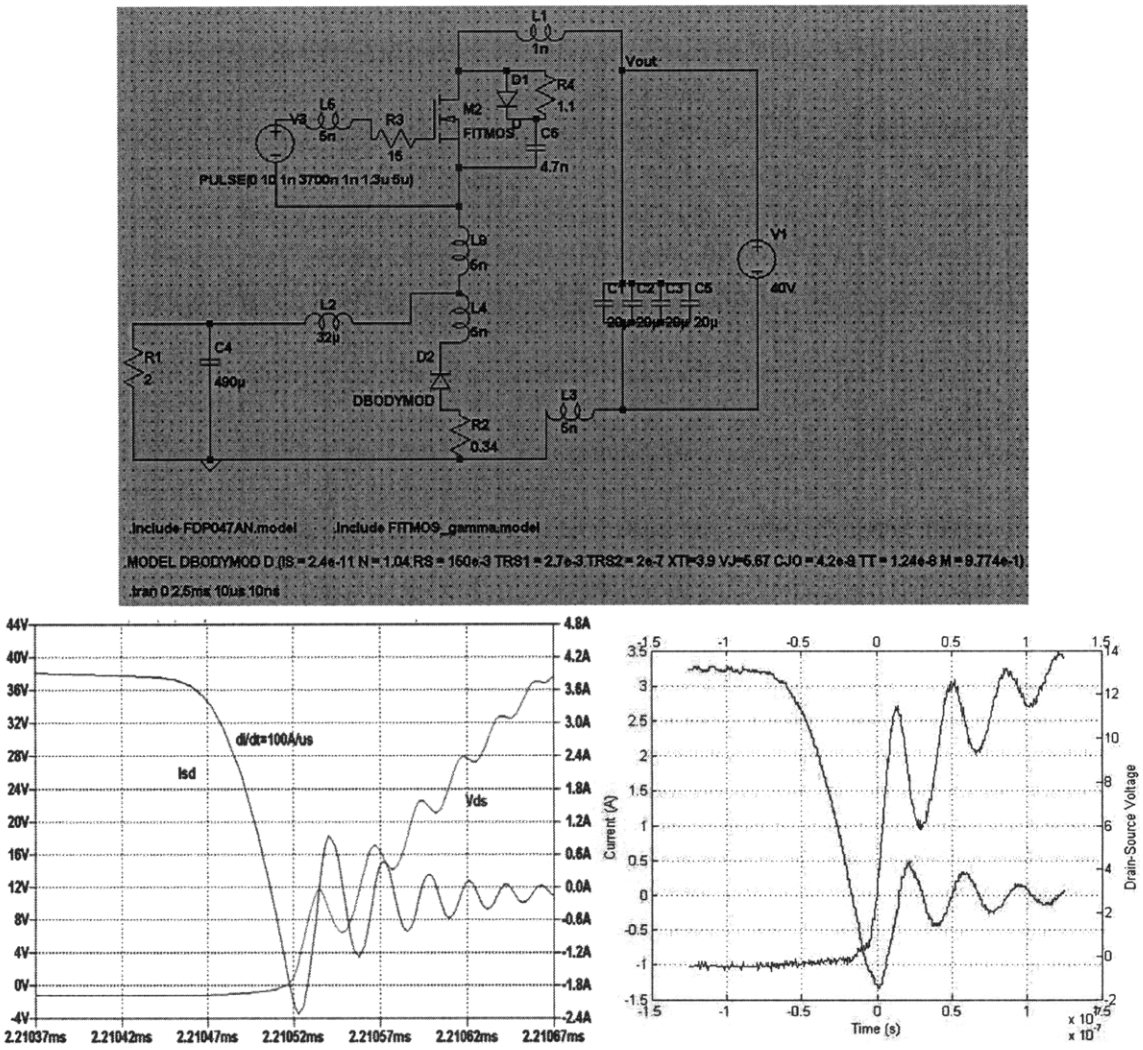


Figure II.7.7 Circuit for the reverse recovery simulation and measurement result comparison. di/dt is controlled to be 100A/us. The bottom left is the simulation waveform. For comparison, the bottom right is the measured waveform. The waveforms are similar. High frequency ringing is presented since here is no high frequency suppression bead in the simulation. But this should not affect capturing the reverse recovery charge.

For further verification, we simulated our model to compare with the reverse recovery waveform we got from Toyota. They both have the same setting: V_{ds}=40V, If=40A and di/dt =100A/us. From the graph, we can see that the simulation matches reasonably with the Toyota measurement. In the simulation, the peak reverse current is -2.2A compare to the -1.6A in the Toyota plot. Also, they both have the same t_{rr}, which is about 30ns.

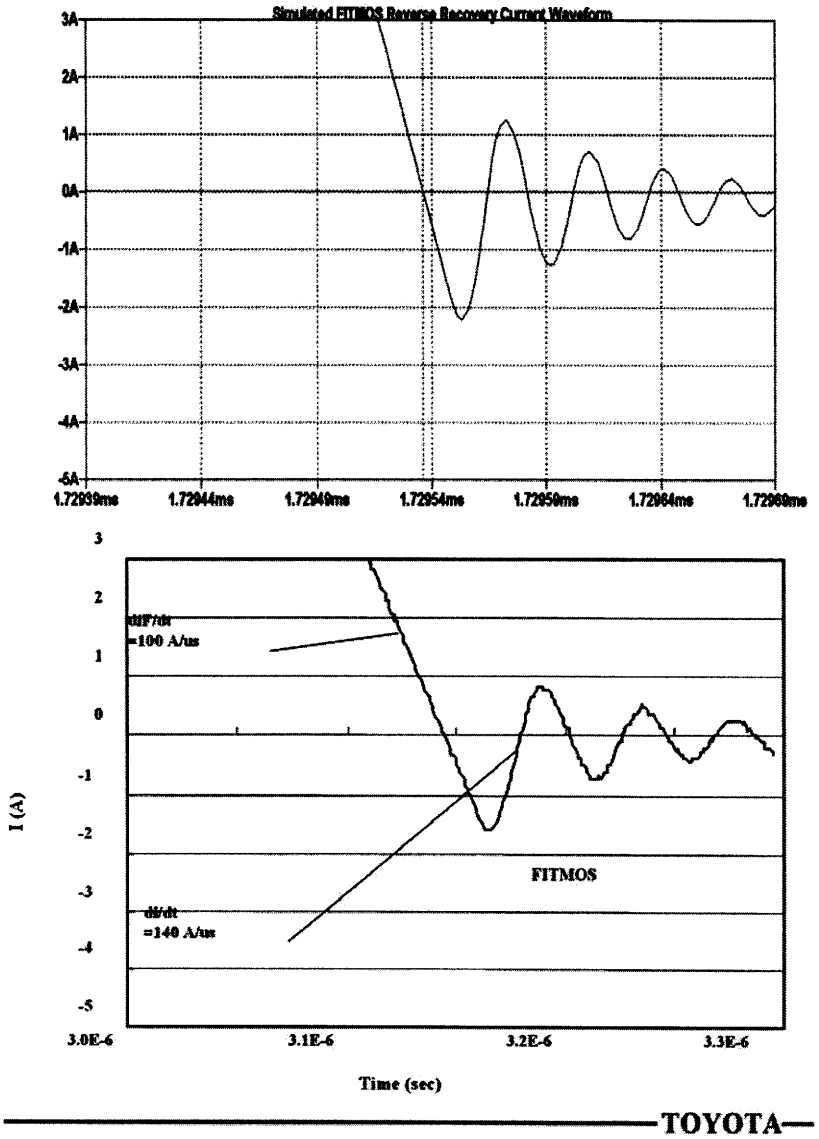


Figure II.7.8 Reverse recovery simulation for FITMOS and Toyota measurement di/dt is controlled to be 100A/us. Vds is 40V and forward current If =40A [4].

Table II.7.2 shows the comparison between the simulation result and the experimental measurement. We can see that the simulation captures the excessive minority carrier charge Q_a well. For the total reverse recovery charge Q_{rr}, the simulation result is also similar to the experimental measurement. We do not compare the T_{rr} in the simulation since the EMI suppression bead changes the current waveform effectively in the experiment but should not affect the reverse recovery charge.

Measurement			Simulation		
If	Qa	Qrr	If	Qa	Qrr
3.4A	12.9nC	78.2nC	3.7A	12.8nC	59.6nC
6.7A	12nC	69.5nC	5.8A	10nC	48.5nC
9.1A	11.1nC	68.5nC	11.8A	11.5nC	52.3nC

Table II.7.2 FITMOS reverse recovery simulation result and experimental data comparison.

As a result, we conclude that the reverse recovery characteristics are measured and implemented in our FITMOS spice model. The FITMOS spice modeling is completed.

II.8 Complete FITMOS Model

After the measurement and modeling of each part of the device parameters is done, we combine all the sub-circuits into a single device model file.

Figure II.8.1 shows the detail FITMOS model schematic we used in our simulations. There are four main parts in this model. The first part is the gate resistance, which was measured to be less than 1.2 ohm. The second part is the parasitic capacitances: C_{gd}, C_{gs} and C_{ds}. The third part is the voltage control current source, which is modeled base on our FITMOS I-V characteristic measurement. In the new model, it can handle both positive and negative drain-source current. The last part is the body diode to model the reverse recovery.

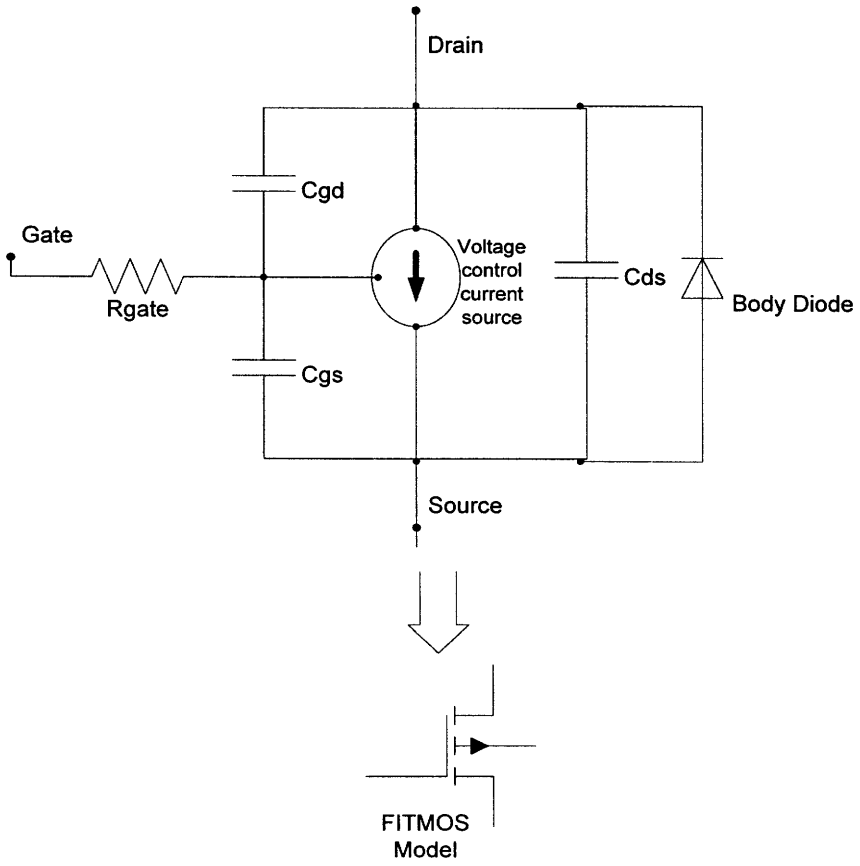


Figure II.8.1 The detail FITMOS model schematics.
The voltage controlled current source is the behavioral model of the FITMOS I-V characteristics

Figure II.8.2 shows the I-V characteristics of the new model. The simulation shows that the model can handle both negative and positive drain-source current well. When the drain-source voltage V_{ds} is less than zero but not negative enough to turn on the body diode, drain-source current follows the MOSFET current model in the linear region. Once the V_{ds} keeps decreasing and becomes negative enough the turn on the body diode, most of the current will go through the body diode and the I-V characteristic of the diode will dominate.

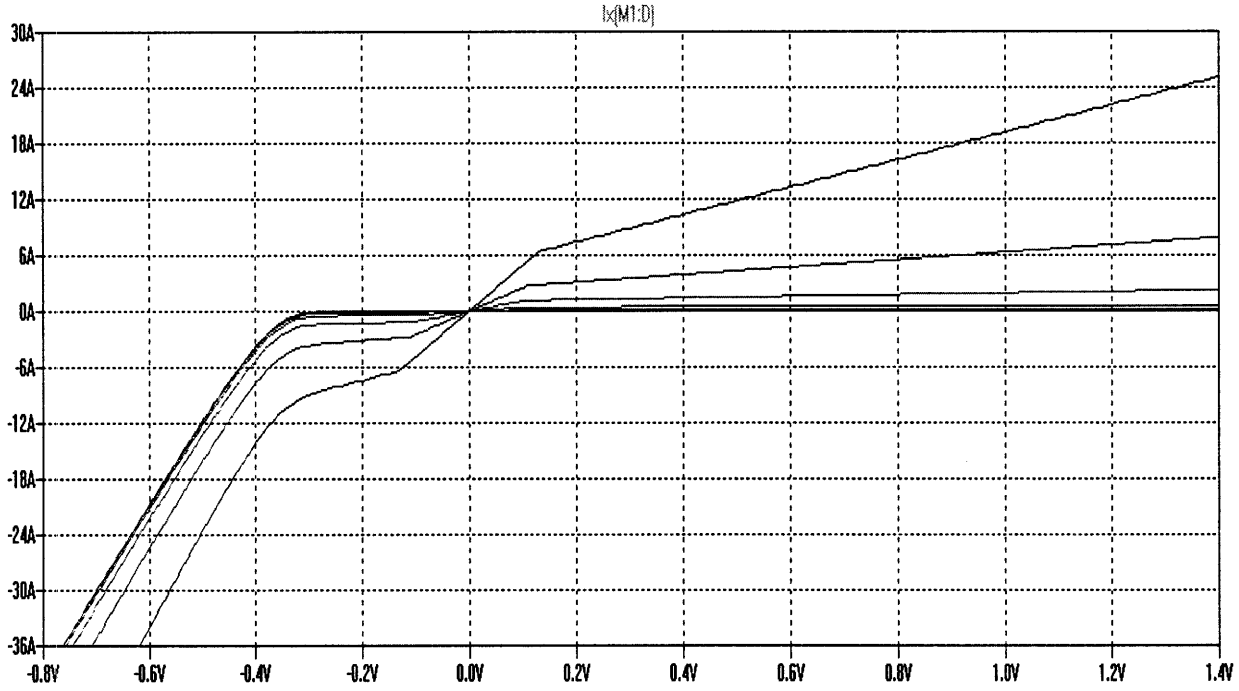


Figure II.8.2 The simulation of the I-V characteristic of the FITMOS model
This new model can handle the full range of the drain-source voltage Vds.

The full Spice model file is in appendix IX.1.

II.9 Converter Simulation Test with FITMOS Model

After finish characterizing FITMOS, a complete SPICE model for FITMOS has built. After the experimental DC-DC Converter is designed, this converter will be used to validate the FITMOS simulation model, collect additional modeling data (such as information about reverse recovery), and experimentally compare FITMOS devices to other MOSFETs under various design points and operating conditions. Once we have a validated SPICE model for the FITMOS, it will be more efficient to optimize the converter performance for the FITMOS.

A DC-DC Converter simulation using our FITMOS model has been done. The purpose of this simulation is to examine the FITMOS SPICE model in the transient simulation. Figure II.9.1 shows the simulation circuit for the converter. This is a synchronous boost converter. For simulation simplicity, 50% duty ratio is used to switch the MOSFETs. As a result, a 28 V output is observed from FigureII.9.2 with a 14 V input, because ideally Vout = Vin / (1-D). The switching frequency is 100 kHz and output power is 80W. Linear Technology LTC4440-5 gate driver is used in the simulated converter circuit. For this simulation, the inductance and capacitance values are not optimized for the system.

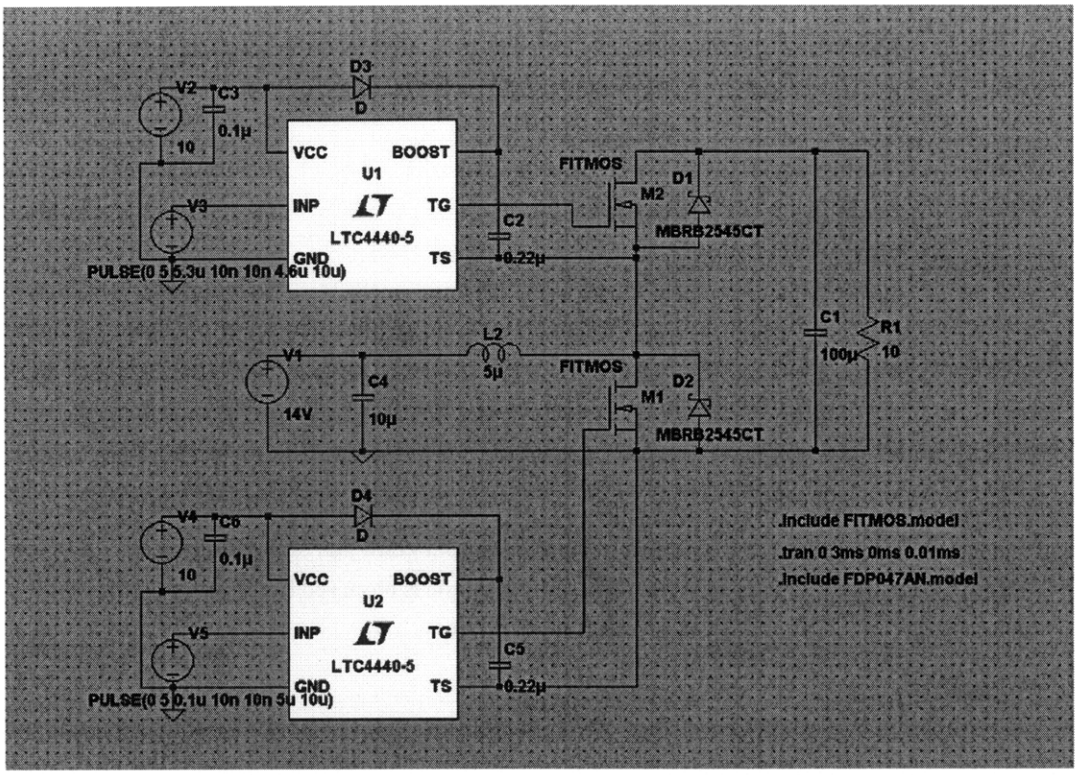


Figure II.9.1 The DC-DC Converter circuit for FITMOS in the Spice simulation
Switching frequency is 100kHz, duty ratio is 50%.

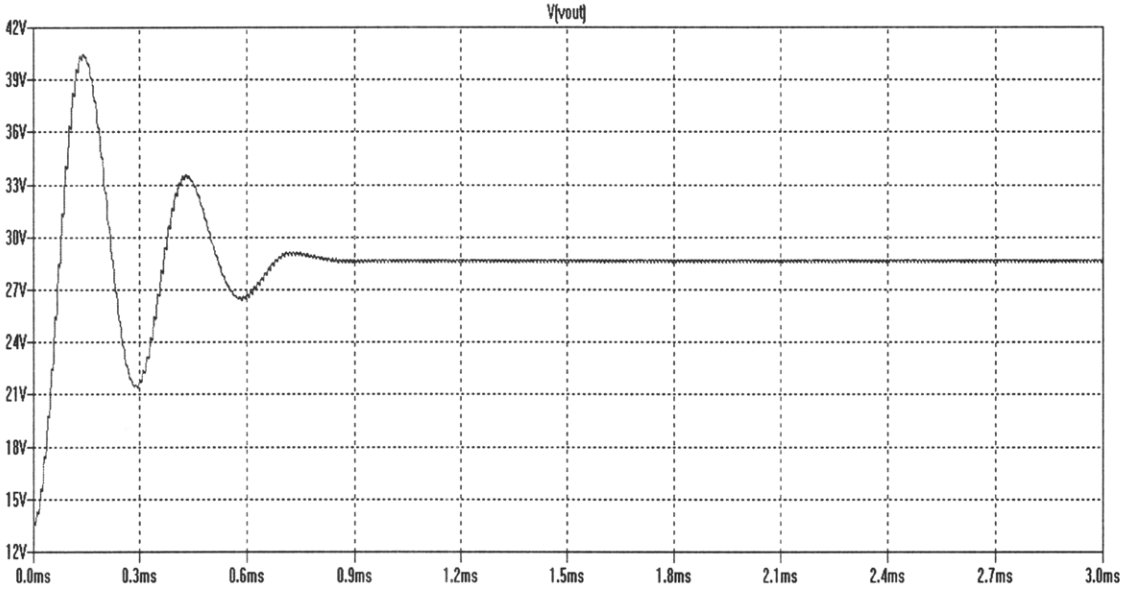


Figure II.9.2 The transient output result for the converter simulation.
In the steady-state, output voltage is 28V as we expected.

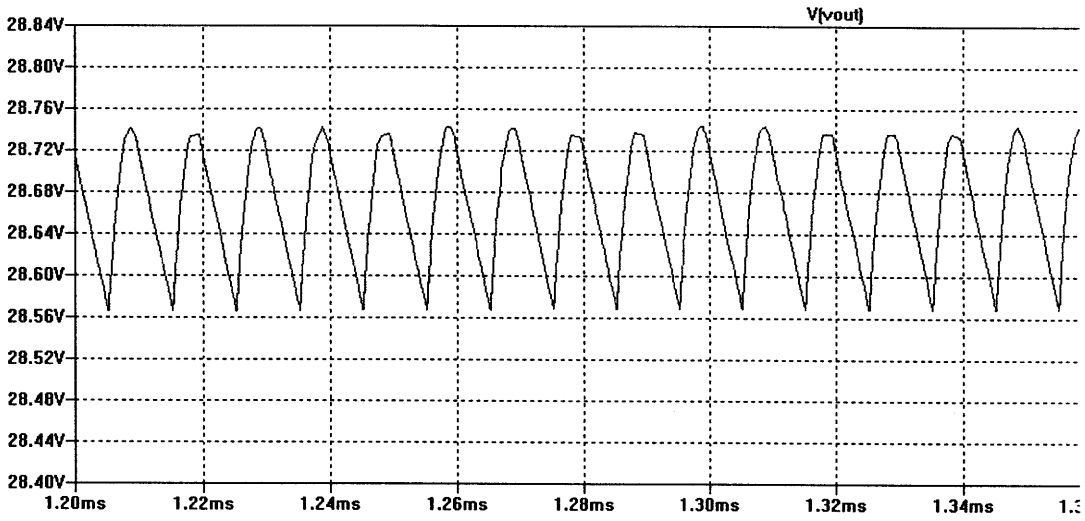


Figure II.9.3 The output rippling for our converter simulation.
At 100kHz switching frequency, 0.16Vpp output ripple is observed in the output with 100uF output capacitor.

The simulation results demonstrate that the FITMOS Spice model is convergent, and its general behavior matches our expectation. Now, we can move on to the prototype DC-DC converter design.

Chapter 3 Converter Prototype

After characterizing the FITMOS, the FITMOS will be used in a bi-directional DC-DC converter (42V/14V) to test its performance, and hence compare it with other conventional power MOSFETs. This bi-directional DC-DC converter can either used as a buck converter for a 42V to 14V down conversion or a boost converter for a 14V to 42V up conversion. In this voltage range, this converter is very suitable for many automobile applications:

1. Dual-Voltage electrical systems (e.g. 42V/14V)
2. Supply higher voltage loads: Audio systems (e.g. 48V); or Power supply for camless engines (e.g. 42V)
3. converter interface to variable-voltage energy storage (e.g. ultra-capacitors for hybrid system)

In the next stage, we need to develop an experimental prototype power converter. From the simulated and experimental converter efficiency and temperature rise, we will have a more accurate basis of comparison of the FITMOS and commercial power MOSFETs.

III.1 Prototype DC-DC Converter Design Summary

The prototype converter is a 14/42V bi-directional DC-DC converter. Note that the circuit board design is flexible enough to permit a wide range of operating conditions and design variations, including switching at up to 500 kHz. The default version of the converter (for initial testing) is designed to output 200W power.

The schematic of the proto-type DC-DC converter, which can be used in either buck or boost mode, is shown in figure III.1.1. A Ti UC3824 PWM chip is used to control the duty ratio for the converter. The operation frequency is up to 500 kHz. The Duty ratio control range is from 7% to 85%. In boost mode, the duty ratio will be 33% in order to provide a 42V output from a 14V input. The high-side driver is based on a Linear Technology LTC4440, which can provide 2.4A driving capability. In order to have a higher drive strength, two LTC4440s are used to provide a total 4.8A driving capability for the high-side FITMOS. For the low side driver, Ti UCC37322 is used, which can provide a 9A driving capability. Timing circuits are provided between the PWM chip and the drivers to control the overlap blanking time between the low-side and high-side driving wave forms. The DC-DC converter is connected as open-loop at this moment.

An AAvid heat sink with 1.78°C/W thermal resistance (length is 3.75in) is used for the FITMOS, which is capable to dissipate more than 35W power from the MOSFETs under natural convection. Four 20uF Capstick capacitors (two on the top and two on the bottom) are used in parallel in the output to give less than 0.5V ripple voltage at 100kHz operating frequency with 200W output power. In order to

minimize the parasitic inductance and prevent the high frequency oscillation, we minimize the output loop between the capacitors and the switches. For the input filter, a 32uH inductor will be made from a RM14/I core with 3F3 material. This input inductor can give less than 5% input ripple current at 100kHz operating frequency with 200W output. And also, a 20uF Capstick capacitor is used to limit the input ripple voltage.

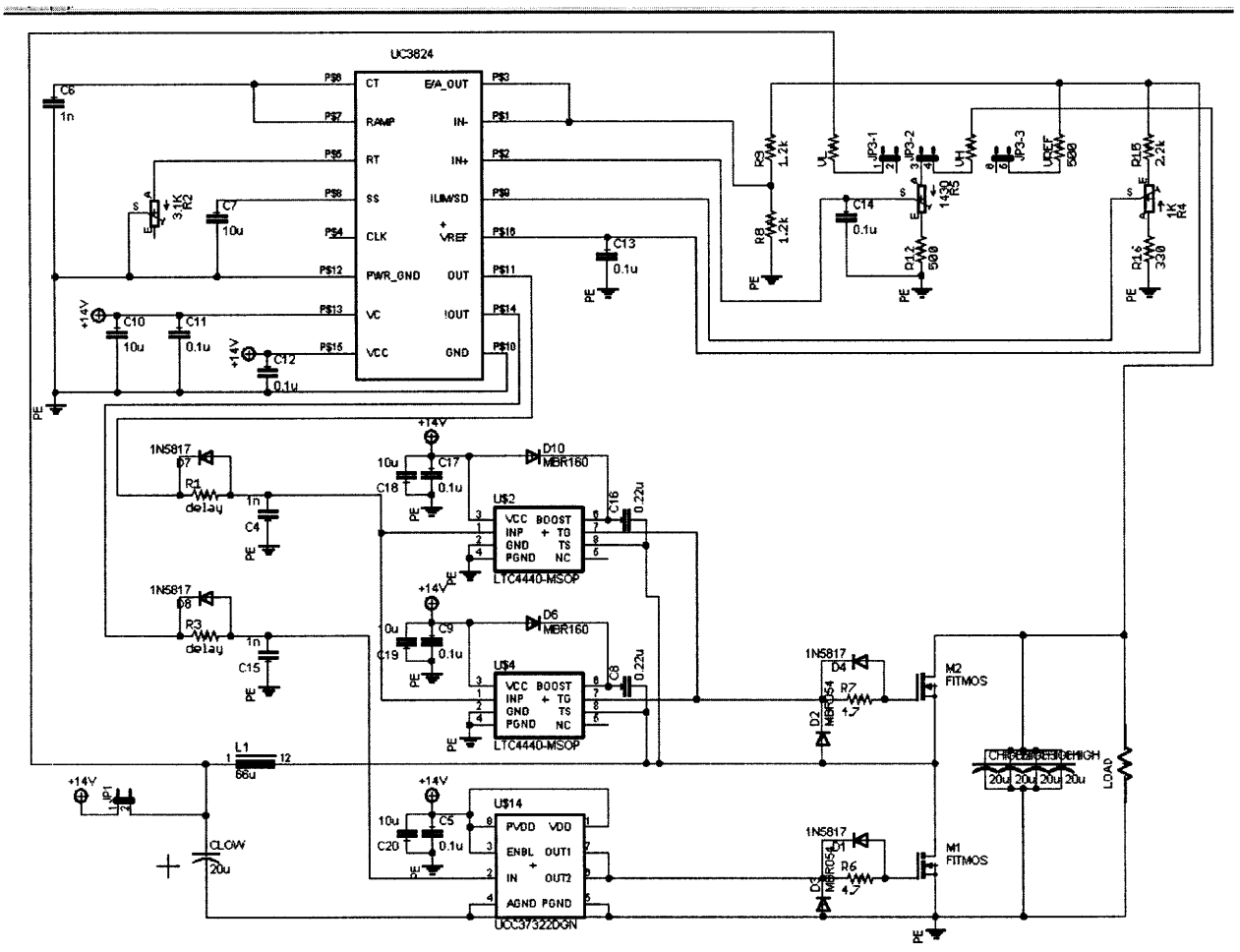


Figure III.1.1 The DC-DC boost Converter schematic drawn in EAGLE.

III.2 Converter PCB Layout

Figure III.2.1 shows the overall layout for the converter, which is implemented in a 4-layer printed circuit board with 2 oz/sq. inch copper. Red is the top plane for ground, and and blue is the bottom layer carrying the power rail. The conductor width is designed to have less than 20 °C temperature rise by using 2oz copper. The PWM and gate drivers can be either powered by the input or from an additional power supply.

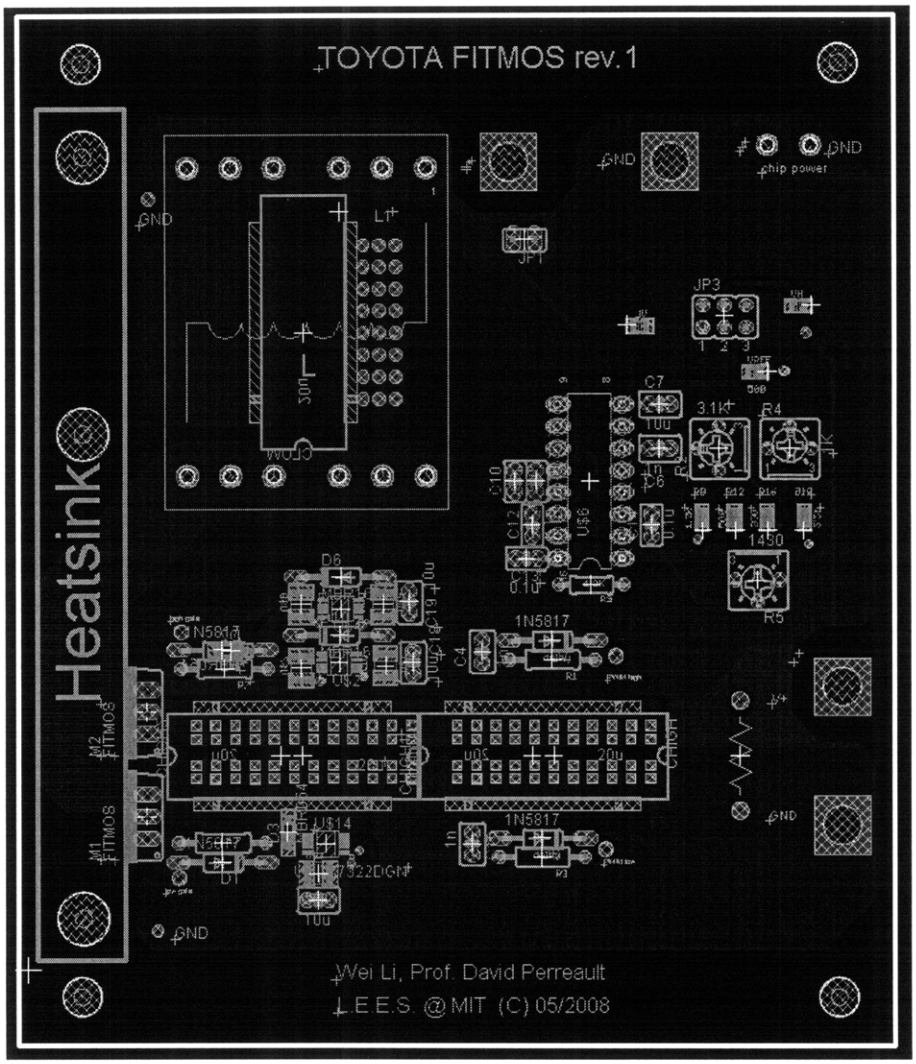


Figure III.2.1 The DC-DC Boost Converter PCB layout drawn in EAGLE

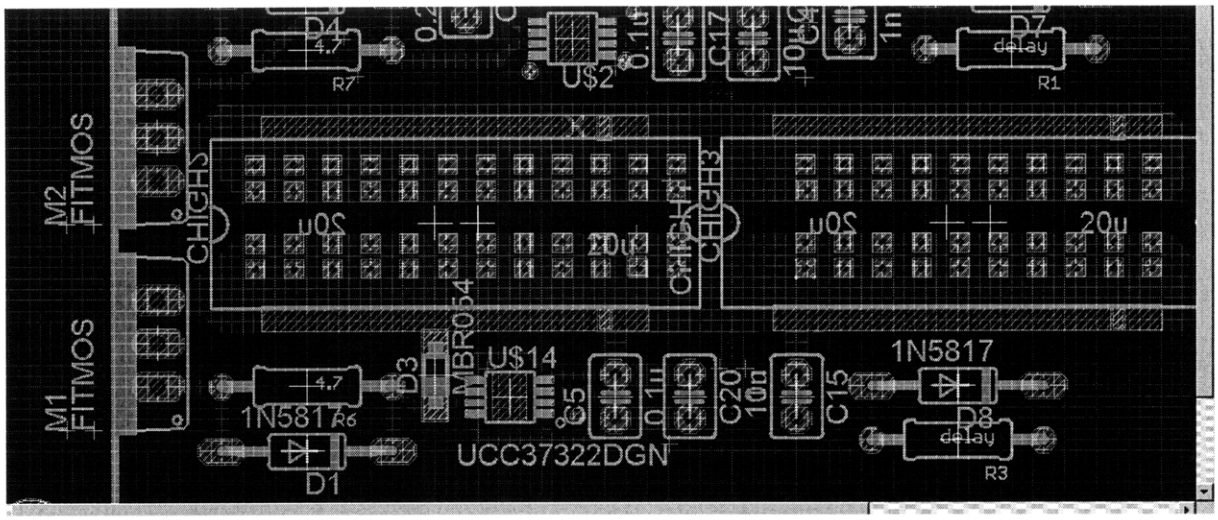


Figure III.2.2 The DC-DC Boost Converter output power stage PCB layout drawn in EAGLE.

Figure III.2.2 shows the power stage in the PCB layout, which includes the MOSFETs and the output filter capacitors. The tide output loop in the layout can help to reduce the parasitic inductance in the PCB and hence reduce the high frequency ringing due to the parasitics.

The details of the PCB layout of the prototype converter are in appendix IX.2.

Chapter 4 Converter Simulation and Measurement

In this chapter, we compare our converter simulation with the prototype converter measurement. In this way, we can test our simulation and try to improve the accuracy of the FITMOS model.

IV.1 Basic Converter Simulation

For the first trial, the DC-DC converter simulation was without any parasitic components. And, the gate driver is ideal in this simulation. In addition, the reverse recovery loss is not included in this model. (The basic FITMOS model is in Appendix VIII.1.2) This simulation only gives us a brief idea of the performance of our converter and shows the convergence of the simulation model.

Figure IV.1.1 shows the DC-DC boost converter schematic we used in LTspice. Input voltage is 14V and output voltage is 42V. The output filter (C_1-C_5) is designed to give less than 0.5V ripple voltage at 100kHz operating frequency with 200W output power. The inductor L_2 will limit the inductor current ripple to be less than 10% at 100kHz operating frequency with 200W output power. In the simulation, the gate drivers are modeled by an ideal voltage sources with selected resistances in series with the gates of the MOSFETs. The resistance values are selected to give 5A peak current for the high-side and 9A peak current for the low-side, values which are similar to the peak current rating for the gate drivers we used in our proto-type DC-DC converter. The internal gate resistance of the "B" series FITMOS devices

has been measured to be less than 1.2 ohm. We simulated the circuit with output power of 100W, 200W and 500W at the operation frequency of 100kHz, 300kHz and 500kHz.

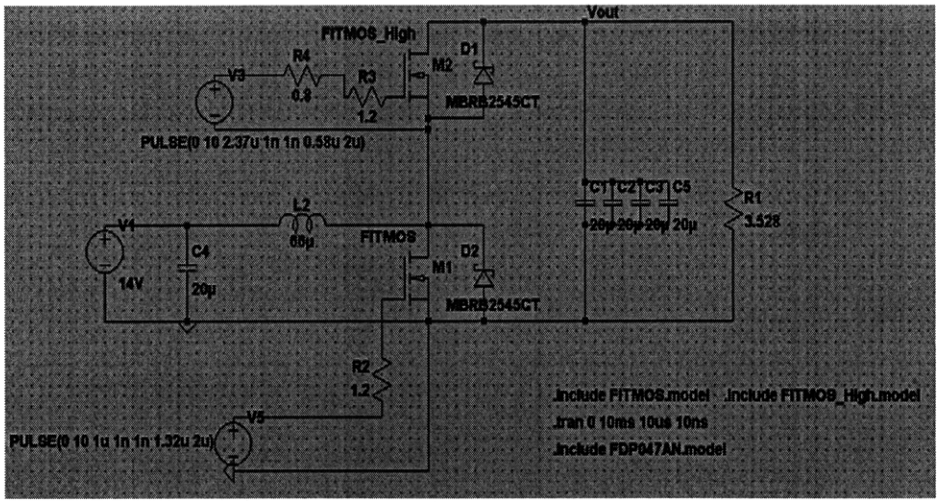


Figure IV.1.1 The DC-DC Boost Converter schematic LTspice.

Figure IV.1.3 and IV.1.4 show the output ripple voltage and input ripple current in the simulation. At 100kHz switching frequency and 200W output power, the calculated output ripple voltage is 0.4V and input ripple current is 1.41A. In the simulation, we got 0.35V output ripple voltage and 1.33A input ripple current, which are very close to our expected values.

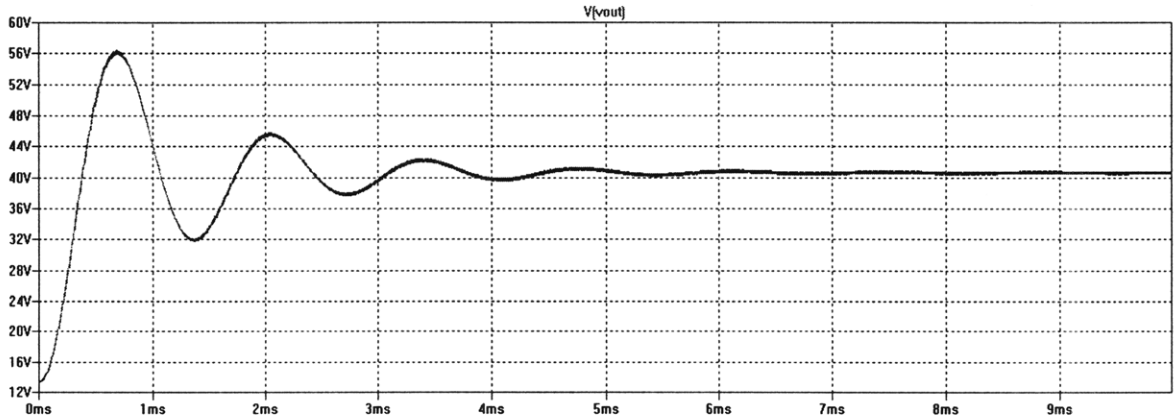


Figure IV.1.2 This plot shows the simulated output voltage for the DC-DC converter Switching frequency is 100kHz and output power is 200W.

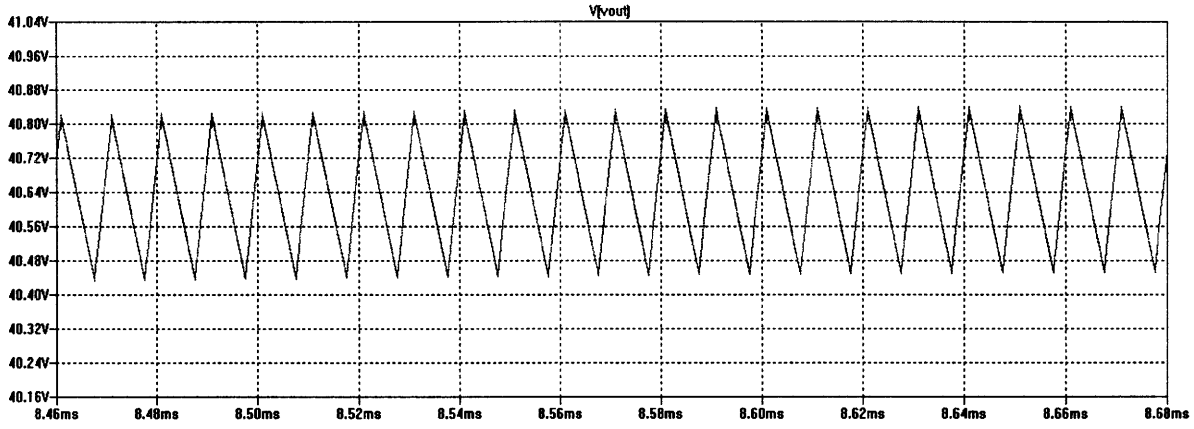


Figure IV.1.3 This plot shows the output voltage ripple in the simulation About 0.4V ripple voltage is observed. This is close to our calculation.

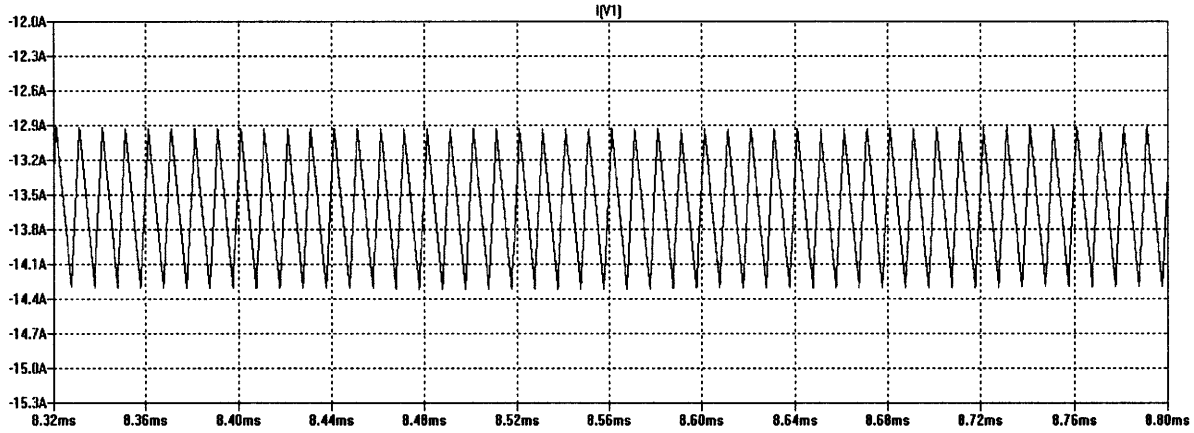


Figure IV.1.4 This plot shows the input ripple current in the simulation The ripple is about 1.33A. It is also very close to the calculated value 1.41A.

For comparison, we also simulate another commercial power MOSFET FDP047AN in the same circuit, which has the best figure of merit of the commercial devices we have studied. Figure IV.1.5 shows the DC-DC converter efficiency in the simulation for both MOSFETs. We got the FDP047AN model from the datasheet, which should be fairly reliable for its accuracy.

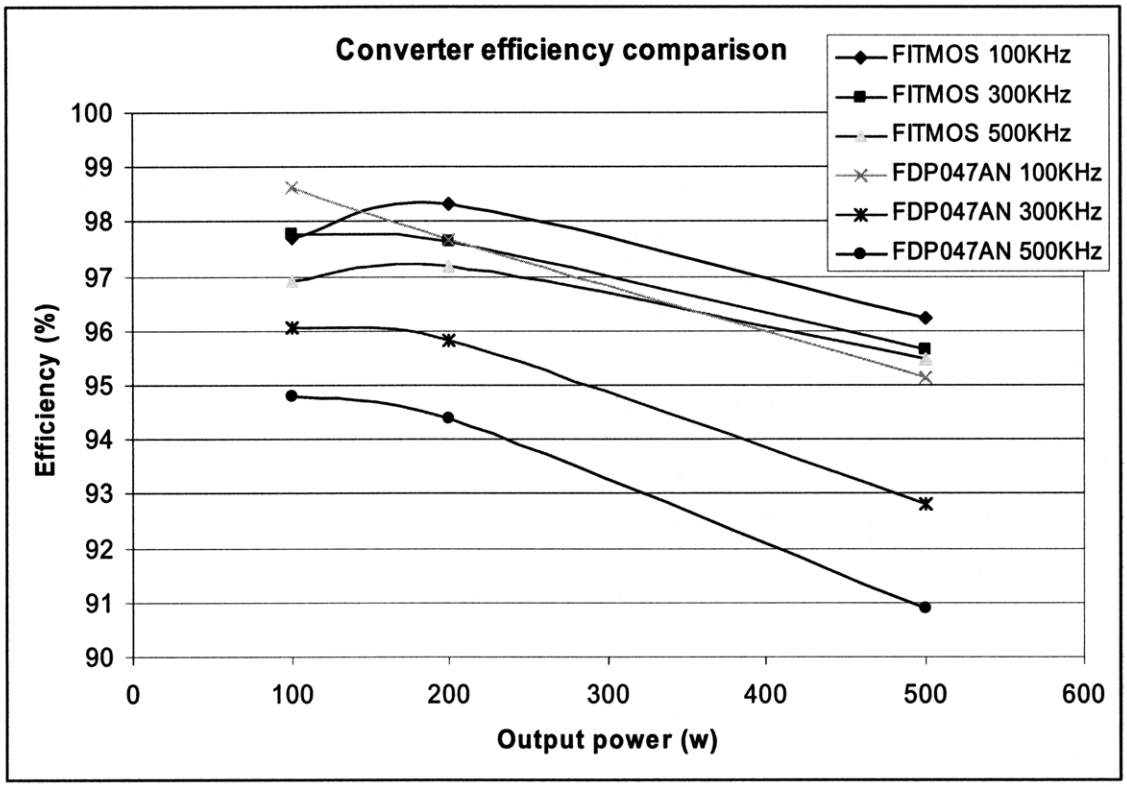


Figure IV.1.5 This plot shows the *simulated* converter efficiency with FITMOS and the commercial power MOSFET FDP047AN.
As we can see, the FITMOS gives 2 % to 5% efficiency improvement over the commercial product under the stated design conditions.

From the graph, we can see that the converter with FITMOS gives an overall better performance. When the operation frequency increases, the converter efficiency does not drop as much as the commercial power MOSFET FDP047AN. So in higher operation frequency, FITMOS potentially provides a significant efficiency improvement. When the switching frequency is above 300kHz, the converter with FITMOS has overall larger than 2% efficiency improvement. At 500W high power output, the converter with FITMOS is more than 4% better at 500kHz operation frequency. Only at low output power and low operation frequency (100W@100kHz), does the FDP047AN excel, where it is less than 1% better. In the

next section, we will compare this simulation data with the experimental measurement to confirm these improvements and the accuracy of our FITMOS spice model.

Detail simulation data:

Output Voltage (V)	42	42	42
Input Voltage (V)	14	14	14
Duty Ratio	0.666666667	0.666666667	0.666666667
Power (W)	100	200	500
Ouput Resistance	17.64	8.82	3.528
Freq (kHz)	100	100	100
Output Voltage (V)	40.925	40.627	39.752
Output Current (A)	2.32	4.61	11.268
Input Voltage (V)	14	14	14
Input Current (A)	6.932	13.6	33.234
Efficiency %	97.71173053	98.30682676	96.24706328
Calculated Input Current Ripple (A)	1.414141414	1.414141414	1.414141414
Simulated Current Ripple (A)	1.4	1.33	1.3
Calculated Ouput Voltage Ripple (V)	0.198412698	0.396825397	0.992063492
Simulated Voltage Ripple (V)	0.18	0.35	0.9
Overlap Loss & Conduction Loss (W)	2.102	3.10953	17.350464
Gating Loss (W)	0.1215	0.11624	0.11538

Freq (kHz)	300	300	300
Output Voltage (V)	41.95	41.54	40.572
Output Current (A)	2.38	4.71	11.5
Input Voltage (V)	14	14	14
Input Current (A)	7.27	14.29	34.81
Efficiency %	97.76296718	97.62601021	95.63770545
Calculated Input Current Ripple (A)	0.471380471	0.471380471	0.471380471
Simulated Current Ripple (A)	0.45	0.46	0.45
Calculated Ouput Voltage Ripple (V)	0.066137566	0.132275132	0.330687831
Simulated Voltage Ripple (V)	0.07	0.14	0.34
Overlap Loss & Conduction Loss (W)	1.939	4.4066	20.762
Gating Loss (W)	0.3455828	0.35114	0.5198852

Freq (kHz)	500	500	500
Output Voltage (V)	41.35	40.876	39.92
Output Current (A)	2.34	4.63	11.32
Input Voltage (V)	14	14	14
Input Current (A)	7.09	13.865	33.76
Efficiency %	96.9192657	97.20794681	95.49424352
Calculated Input Current Ripple (A)	0.282828283	0.282828283	0.282828283
Simulated Current Ripple (A)	0.26	0.264	0.26
Calculated Ouput Voltage Ripple (V)	0.03968254	0.079365079	0.198412698
Simulated Voltage Ripple (V)	0.04	0.083	0.201
Overlap Loss & Conduction Loss (W)	2.501	4.85412	20.7456
Gating Loss (W)	0.57464	0.581778	0.5763776

Table IV.1.1 Detail simulation result for the converter with FITMOS

Output Voltage (V)	42	42	42
Input Voltage (V)	14	14	14
Duty Ratio	0.666666667	0.666666667	0.666666667
Power (W)	100	200	500
Ouput Resistance	17.64	8.82	3.528
Freq (kHz)	100	100	100
Output Voltage (V)	40.91	40.484	39.35
Output Current (A)	2.32	4.59	11.154
Input Voltage (V)	14	14	14
Input Current (A)	6.86	13.574	32.94
Efficiency %	98.63273861	97.6821428	95.1333389
Calculated Input Current Ripple (A)	1.414141414	1.414141414	1.414141414
Simulated Current Ripple (A)	1.34	1.23	1.32
Calculated Ouput Voltage Ripple (V)	0.198412698	0.396825397	0.992063492
Simulated Voltage Ripple (V)	0.19	0.37	0.9
Overlap Loss (W)	1.1288	4.21444	22.2501
Gating Loss (W)	0.18687288	0.1948392	0.2028672

Freq (kHz)	300	300	300
Output Voltage (V)	41.76	41.115	39.49
Output Current (A)	2.37	4.66	11.2
Input Voltage (V)	14	14	14
Input Current (A)	7.32	14.238	34
Efficiency %	96.04976987	95.83584131	92.80036378

Calculated Input Current Ripple (A)	0.471380471	0.471380471	0.471380471
Simulated Current Ripple (A)	0.45	0.45	0.42
Calculated Ouput Voltage Ripple (V)	0.066137566	0.132275132	0.330687831
Simulated Voltage Ripple (V)	0.06	0.14	0.3
Overlap Loss (W)	3.5088	7.7361	33.712
Gating Loss (W)	0.56157952	0.58892456	0.60158

Freq (kHz)	500	500	500
Output Voltage (V)	41.1	40.248	38.321
Output Current (A)	2.33	4.56	10.862
Input Voltage (V)	14	14	14
Input Current (A)	7.15	13.82	32.637
Efficiency %	94.78387176	94.3814682	90.90019766
Calculated Input Current Ripple (A)	0.282828283	0.282828283	0.282828283
Simulated Current Ripple (A)	0.27	0.25	0.26
Calculated Ouput Voltage Ripple (V)	0.03968254	0.079365079	0.198412698
Simulated Voltage Ripple (V)	0.04	0.077	0.188
Overlap Loss (W)	4.337	9.94912	40.675298
Gating Loss (W)	0.93301144	0.97647912	0.99376776

Table IV.1.2 Detail simulation data for converter with commercial power MOSFET FDP047AN.

IV.2 Simulation and Measurement w/o Reverse Recovery

So far, our proto-type DC-DC converter has been built and is working properly. The purpose of this proto-type DC-DC converter is to verify the accuracy of our FITMOS spice model. As a result, we compare our Spice simulation with the proto-type DC-DC converter in the following aspects: Efficiency, Gate source signal, Drain source signal and Output Voltage wave form. The FITMOS model used in this simulation has included the parasitic inductance in the circuit to improve the simulation accuracy. In addition, external gate resistance is added to match with the prototype converter board. But reverse recovery characteristic is not included in this simulation. (The improved FITMOS model is in Appendix IX.1.3)

IV.2.1 Simulation and Measurement Comparison for FITMOS

Figure IV.2.1 shows the picture of our proto-type DC-DC converter. Input voltage is 14V and output voltage is 42V. The output 80uF capacitor is designed to give less than 0.5V ripple voltage at 100kHz operating frequency with 200W output power. The 30uH inductor will limit the inductor current ripple to be less than 10% at 200kHz operating frequency with 200W output power. In addition, a 2.7 Ω resistor is connected in series with the gate of the high-side MOSFET and a 1.2 Ω resistor is connected in series with the gate of the low-side MOSFET. These resistors are chosen based on the observation of the gate-source signal. These gate resistors are big enough to limit the dv/dt and prevent high frequency oscillations, but also maintain a fast enough turn-on transition. Furthermore, the main purpose of this board is to test our simulation model, in order to improve the performance of the DC-DC converter, those

resistor values will be optimized in the future.

Figure IV.2.2 shows the schematic of the DC-DC converter we used in the Spice simulation. For the low-side MOSFET, we added a snubber circuit (diode D1, 1.2 Ω resistor R4 and 4.7nF capacitor C6) to slow down the MOSFET turn off transition to reduce the parasitic oscillation at the drain. However according to $P = \frac{1}{2} C * V^2 * f$, this snubber circuit will give 1.13W more loss to the converter at 300kHz operation frequency, which is less than 1% efficiency loss.

For comparison, we measured the efficiency of this converter for 100W and 200W output load at 200kHz, 300kHz and 500kHz operation frequency.

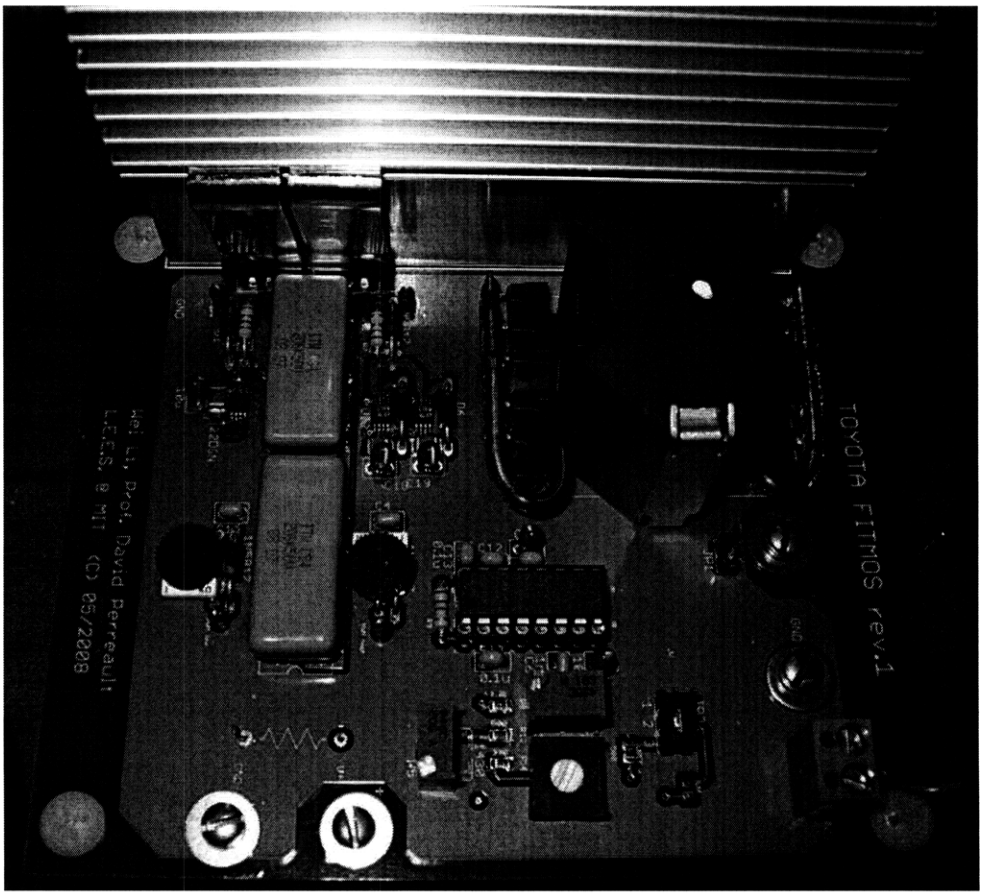


Figure IV.2.1 The picture of our proto-type DC-DC converter

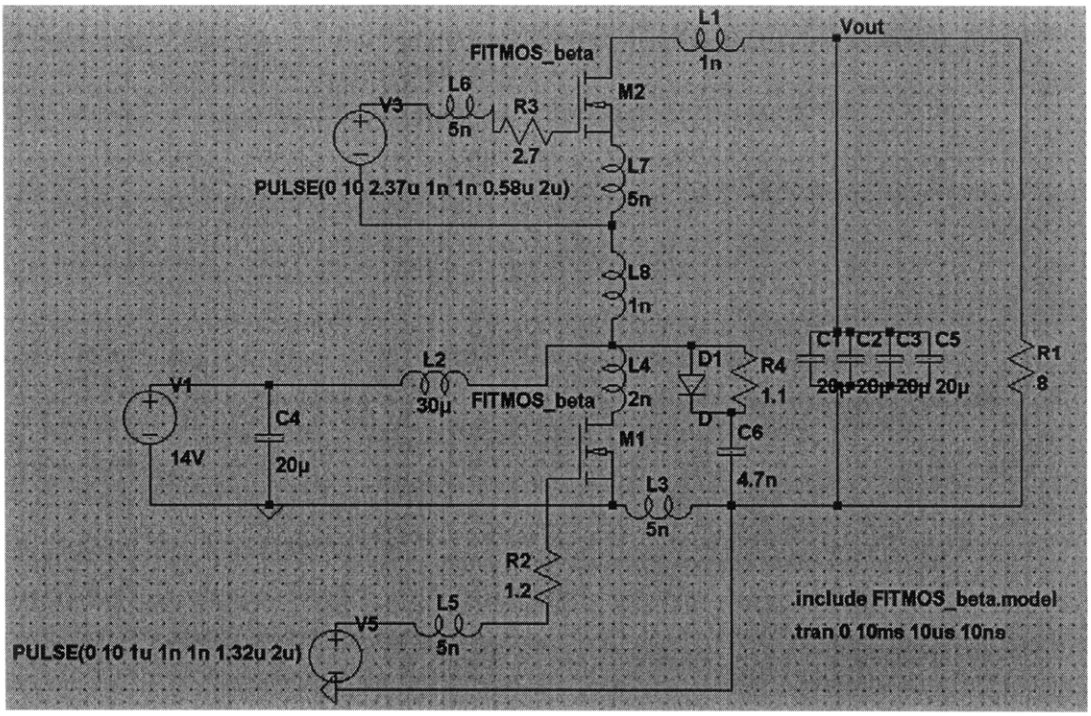


Figure IV.2.2 The schematic of the DC-DC converter in LTspice. Parasitic inductances are added to the schematic to further improve the accuracy of the simulation.

Figure IV.2.3 show the efficiency comparison chart between the simulation and proto-type converter experimental result. As we can see, the simulation result is very close to the measurement, which is just a couple percent higher than the experimental data. In the simulation, we did not count the power consumption in the logic control circuitry. And the parasitic elements in the PCB board may also give us some errors. As a result, a few percent differences in the simulation are within the acceptable range.

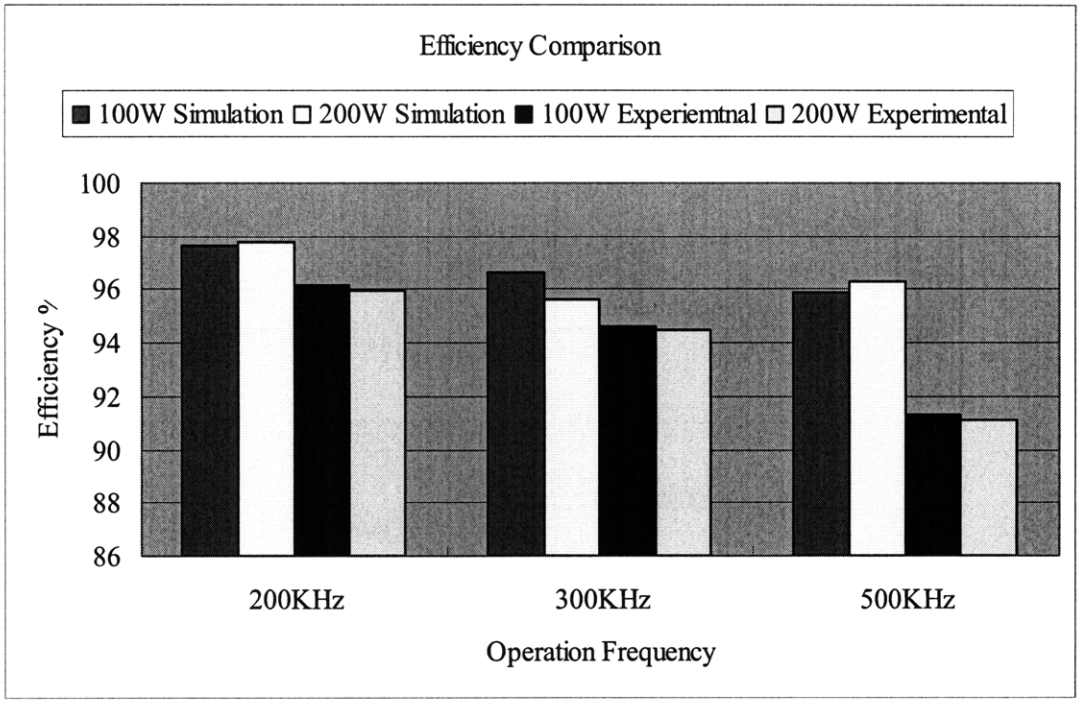


Figure IV.2.3 It shows the converter efficiency between the Spice simulation and the proto-type converter measurement.

Furthermore, we compare the gate and drain signals in the converter. Due to the parasitic components, we have high frequency oscillations in both gate and drain. These oscillations can be observed in both simulation and proto-type board. In the proto-type converter, we measured the oscillation frequency is about 55MHz, which is 18ns in period. The scope waveform for the gate and drain signals are shown in figure IV.2.4.

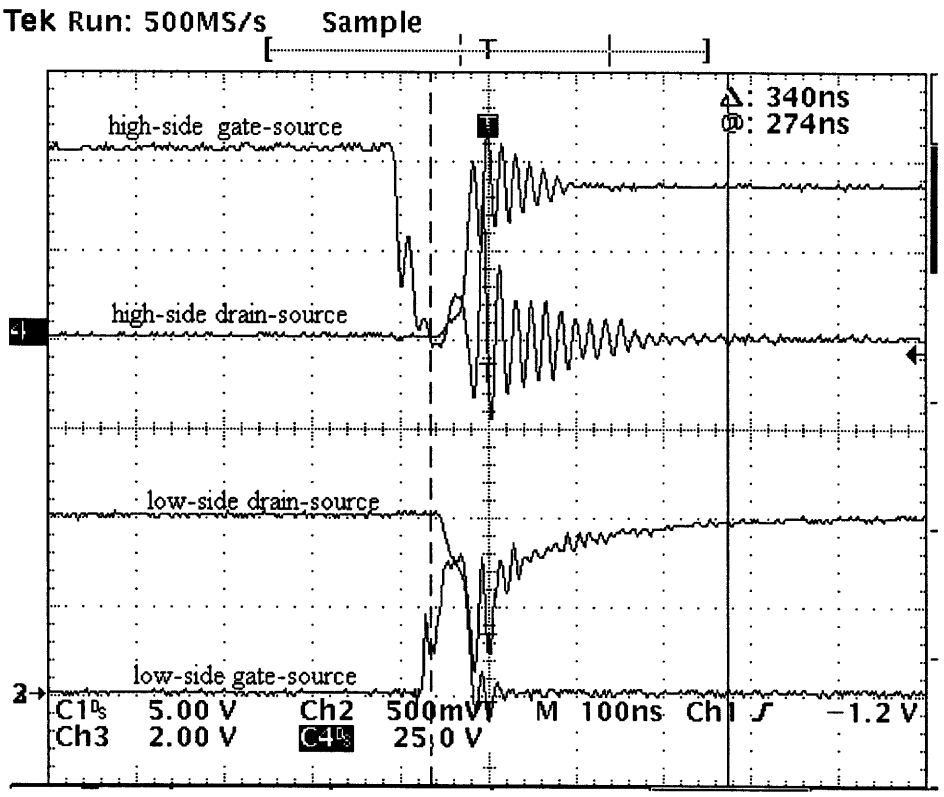


Figure IV.2.4 Scope waveforms for the gate-source and drain-source signals on the proto-type converter.

****Ch2 and Ch3 are 10x probes. So the scale is 5V and 20V.**

From Figure IV.2.4, we also can see the body diode reverse recovery behavior in the higher side drain-source waveform. After the high side MOSFET is turned off, the drain source voltage can not rise up immediately. It takes about 50-60ns for the diode to recover and starts blocking the reverse voltage.

Now, we compare the proto-type converter behavior with our simulation model. Figure IV.2.5 shows the gate-source and drain-source wave forms from the simulation. In the high-side gate-source and drain-source wave form, we also can observe the high frequency oscillation in the simulation. The oscillation frequency is about 65MHz, which is 15.4ns in period. This is close to our measurement, which is 18ns in period. In addition, the simulation also shows the reverse recovery behavior in the

high-side MOSFET. Since it is very hard for us to model the gate driver current, in the simulation, the gate of the MOSFET will be turned on about twice faster than our measurement. But overall, our model can predict the converter behavior pretty accurately.

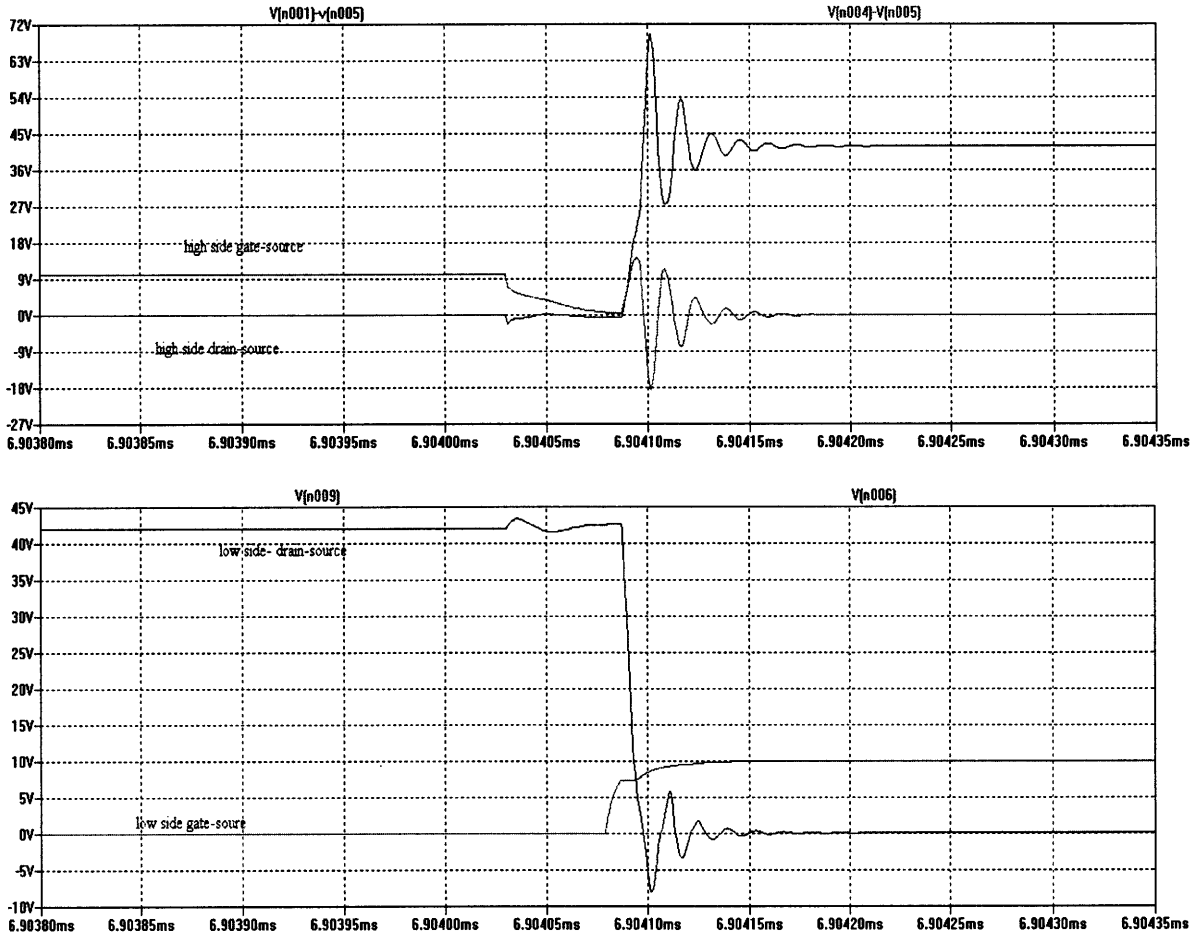


Figure IV.2.5 Gate-source and drain-source wave forms in simulation
The top graph is the high-side gate-source and drain-source wave forms and the bottom graph is the low-side gate-source and drain-source wave forms. The time scale is 50ns/div.

In the end, we compare the output waveform between our measurement and simulation result. Due to the parasitic oscillation in the drain, our output voltage has some high frequency ringing also. In figure IV.2.6 and 7, they show the output voltage ringing for both experimental measurement and simulation. For the experimental

measurement, there is 2-2.5V peak to peak ringing. Unfortunately, the peak to peak ringing in the simulation is about 5 times larger, which is over 10V. But we will study this mismatch more in the future.

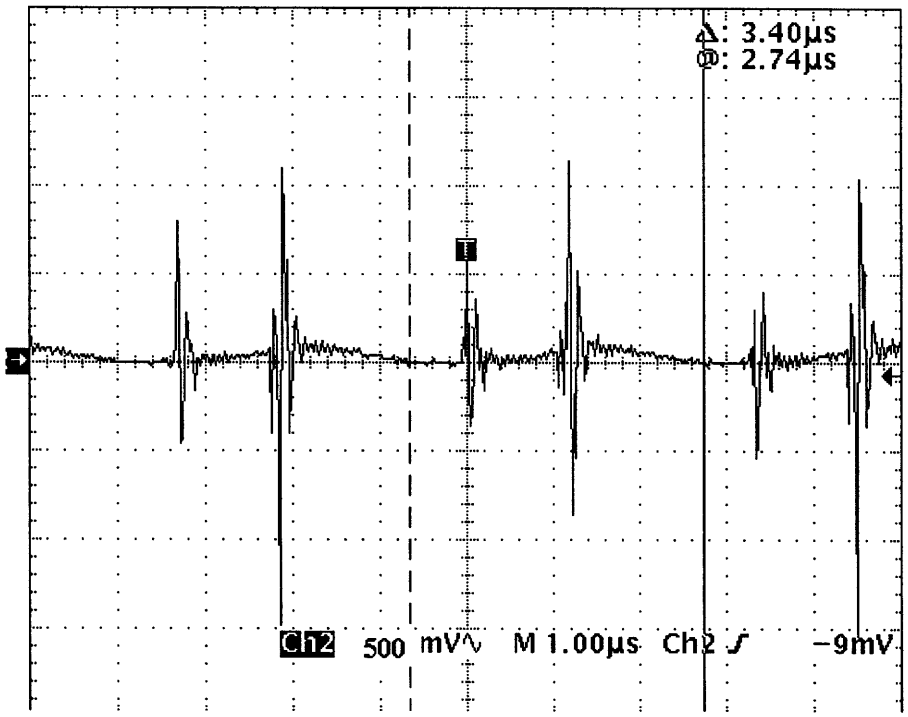


Figure IV.2.6 The output voltage ringing measured on the proto-type DC-DC converter

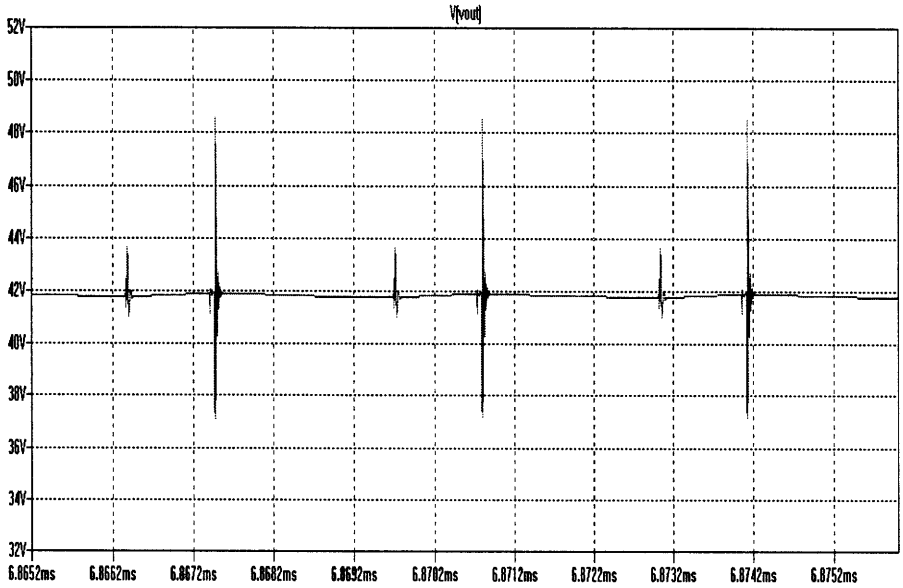


Figure IV.2.7 The output voltage waveform from our Spice simulation.

In conclusion, from our measurement, the Spice model can model the FITMOS pretty well and be able to predict the behavior of our proto-type converter accurately. For the future study, we will further understand the high frequency parasitic ringing more. If necessary, there are still several techniques that we can apply to reduce those ringing.

IV.2.2 Comparison between FITMOS and FDP047AN

As a quick comparison, we also built an identical copy of the same DC-DC converter except for using the most competitive commercial MOSFET FDP047AN. In this section, we will compare the performance of the converter with commercial MOSFET with the one with FITMOS under hard-switching conditions.

For comparison, we measured the efficiency of the converter with commercial MOSFET FDP047AN for 100W and 200W output load at 200kHz, 300kHz and 500kHz operation frequency. According to our section II.5, MOSFET FDP047AN has the best Figure of Merit [2] on the market. While this figure of merit does not completely capture the loss tradeoffs in MOSFET switches, it is often used as a crude measure when comparing switches. As a result, we used FITMOS to compete with the commercialized power MOSFET with the best FOM, which is FDP047AN.

Figure IV.2.8 shows the converter efficiency comparison between FITMOS and commercial MOSFET FDP047AN. It can be seen that the efficiency of the converter with FDP047AN is between 0.25% and 1% better than the one with FITMOS for the design and operating conditions tested. We should emphasize that this converter is just a prototype, and is not optimized for the FITMOS yet. This

rough comparison just gives us a quick look of the FITMOS performance. After we have a deeper study of FITMOS, we will have an idea which area (in terms of operation mode, switching frequency and output power) is more suitable for FITMOS.

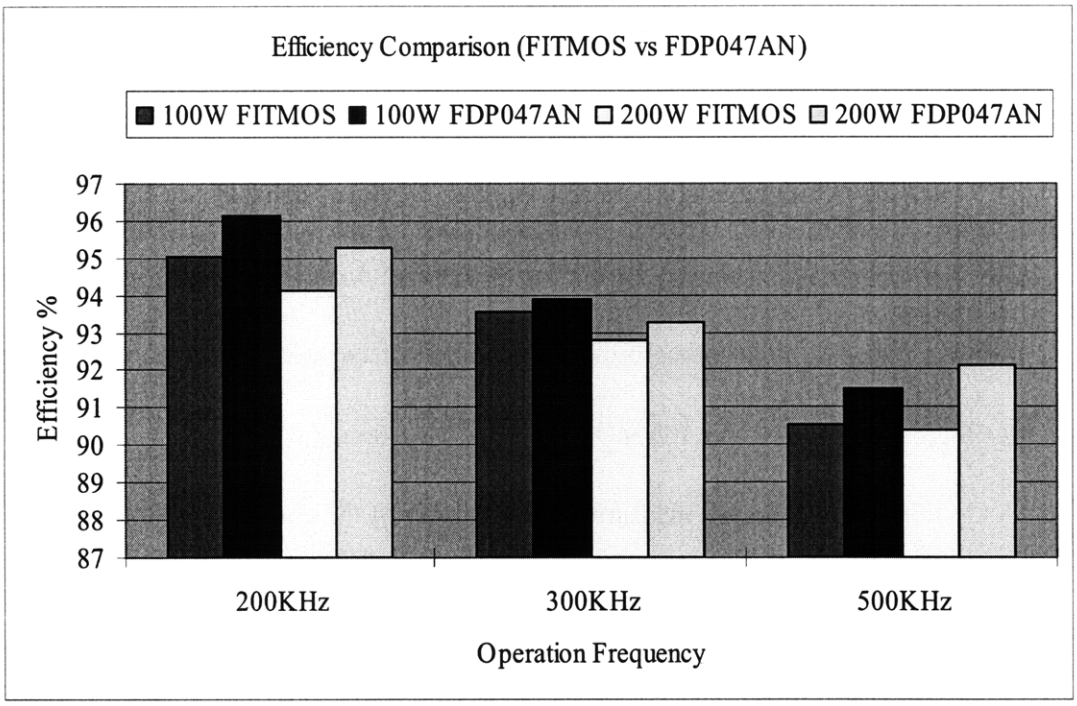


Figure IV.2.8 It shows the converter efficiency comparison between FITMOS and FDP047AN

In addition, we also compare the gating power loss between FITMOS and FDP047AN. Gating power was as measured from the dc power supply feeding the gate drive circuits. Since FITMOS has smaller Q_{gs} and Q_{gate} than FDP047AN, we believed that FITMOS will have less gating power loss over FDP047AN. This is also shown in the experimental measurement. As we can see in figure IV.2.9, in overall operation frequencies, FITMOS has less gating loss than FDP047AN.

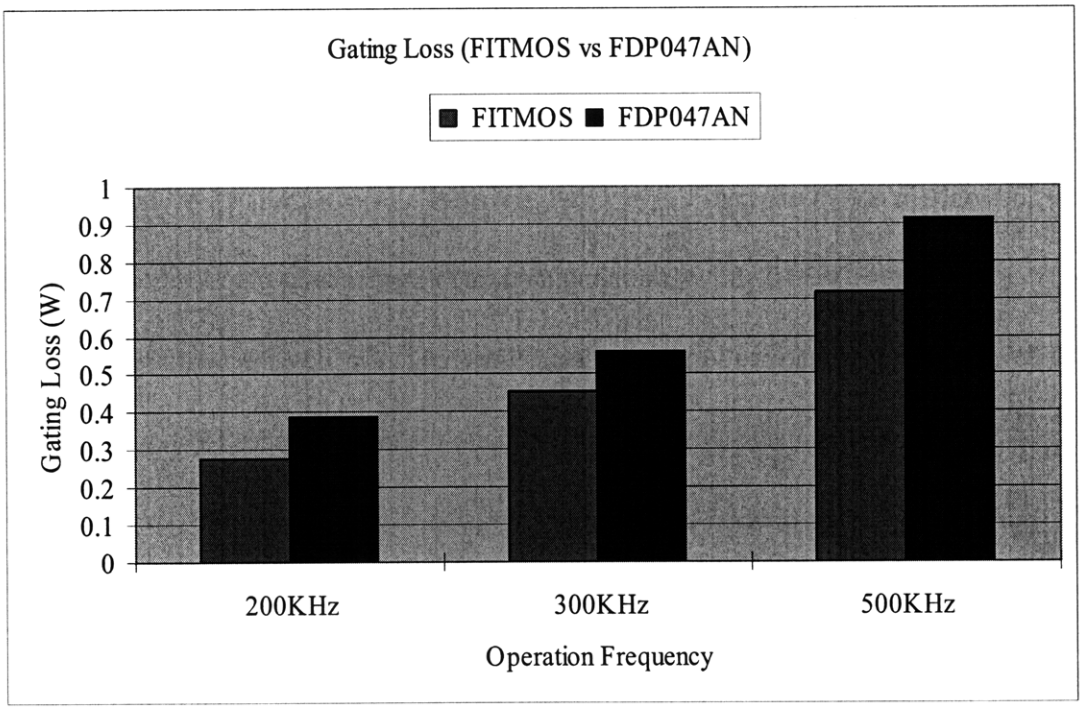


Figure IV.2.9 It shows the gating loss comparison between FITMOS and FDP047AN.

Overall, we can see that FITMOS has a highly competitive performance over most of the commercial power MOSFETs in the market. In the future, after a deeper study, we will have a more detailed performance comparison for FITMOS and other commercialized power MOSFETs.

An additional area of study has been to compare our simulation models for the FITMOS devices with the performance measured in our experimental prototype. We will use these measurements to validate and refine our simulation models for the FITMOS devices. A good model will be necessary to use simulation tools and closed-loop optimization methods to explore the design space.

In our simulation, we did not model the loss for the inductor and gate drivers. In order to have a more accurate comparison between our simulation models to the experimental data, we measured the inductor loss and logic and gate driver power consumption in our converter separately. In this way, we can focus on the switch loss only in our simulation.

Figure IV.2.10 shows the simulated and experimental gate loss for FITMOS. We can see that the gate loss increases as the frequency increases. And the simulated loss has a good match to the experimental data; the error is under 15% of gate power, and is a very small fraction of overall power.

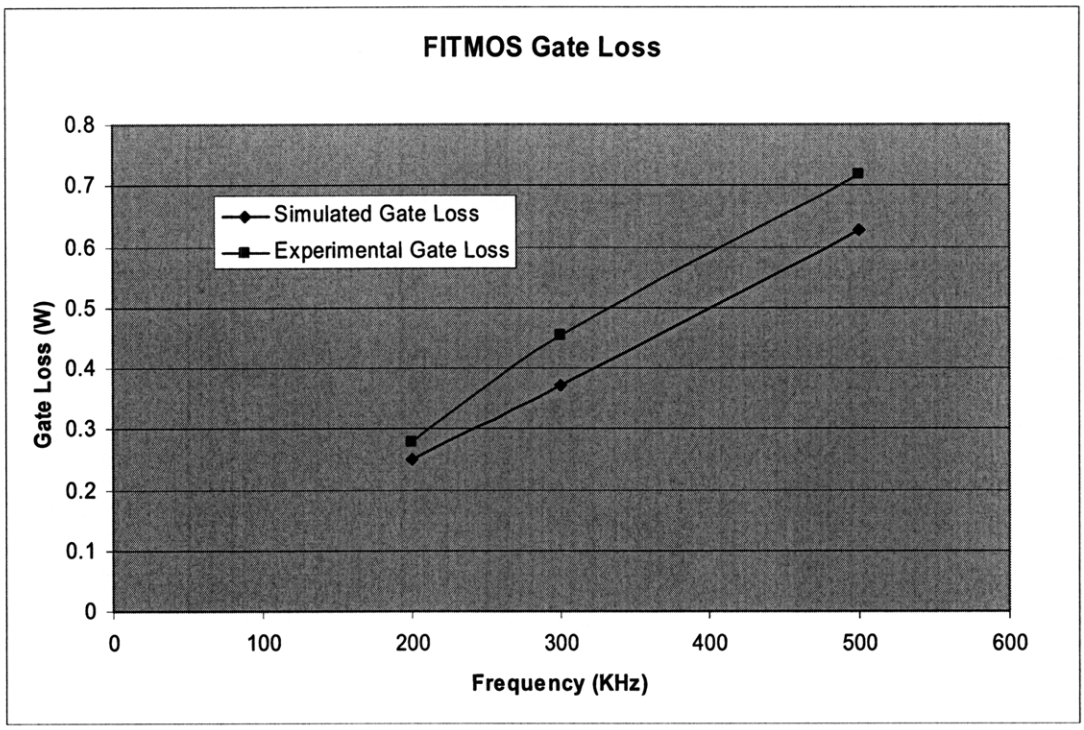


Figure IV.2.10 The comparison between simulated gate loss and experimental gate loss for FITMOS.

Figure IV.2.10. Data is taken at 200kHz, 300kHz and 500kHz.

Figure IV.2.10 shows the converter efficiency comparison between simulation and experimental data. Unfortunately, there are quite large discrepancies between the simulation and measurement. As we can see, this discrepancy increases as the operation frequency increases. The simulation is off by 3% of input power at 200kHz while it is off by 5.5% at 500kHz. Also, when the output power is lower, the simulation error is also lower. So from this graph, we can notice that there are some other frequency related losses we missed or did not adequately capture in our spice model. One possibility could be the reverse-recovery loss from the body diode in the switch, which we did not include in our spice model yet. As a result, in the next step, we will measure the reverse-recovery behavior for the FITMOS and try to figure

out other possible losses we missed in our model. We believe we can obtain a more accurate model after our study.

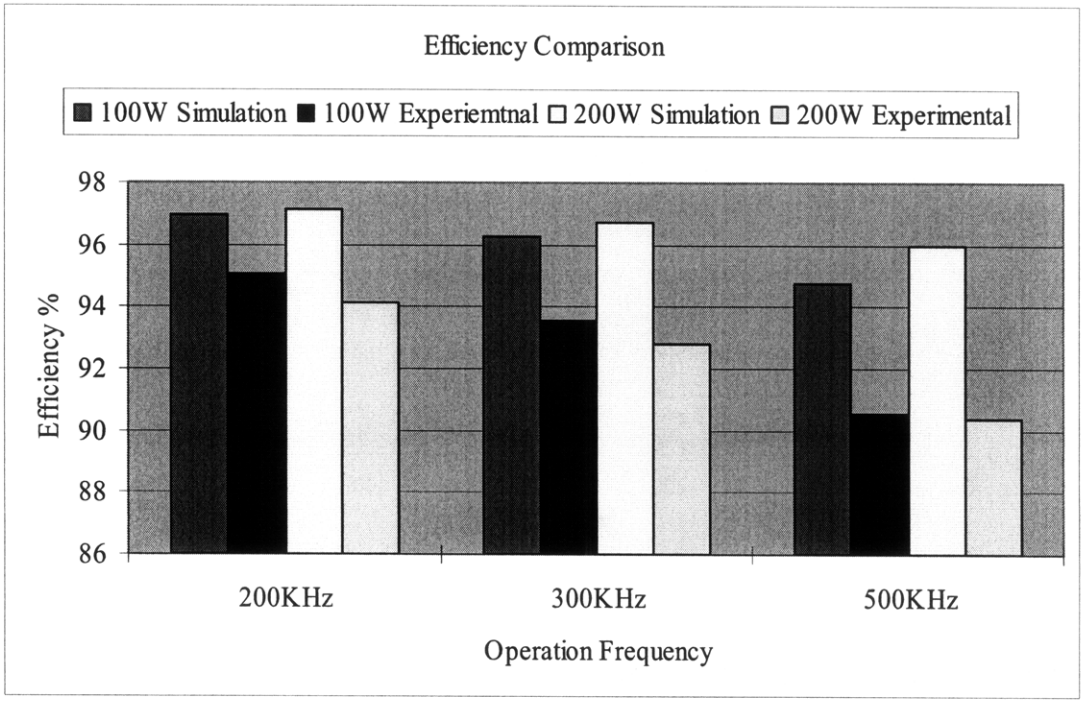


Figure IV.2.11 Converter efficiency comparison between FITMOS simulation and measurement.

IV.3 Simulation and Measurement with Complete Model

From the previous measurement and comparison, it seems that the reverse recovery characteristic is important to our simulation performance. As a result, we include the body diode model in our simulation to obtain a more accurate result. In this section, we will compare the improved FITMOS SPICE simulation and the experimental data under hard-switching conditions. (Up to this stage, the FITMOS Spice model is fully completed, and gives the best accuracy. The improved completed FITMOS model is in Appendix IX.1.4)

Figure IV.3.1 shows efficiency comparison between the simulation and the experimental measurements over different operating frequencies. The input voltage is 14V and the output voltage is 42V. For comparison, we measured the efficiency of the converter with FITMOS for 100W and 200W loads at operating frequencies of 100kHz, 200kHz, 300kHz and 500kHz. As the operational frequency increases, the switching loss increases, and hence the converter efficiency drops. From the plot, we can see that our FITMOS model shows reasonable results compared to the experimental data. At the highest operating frequency, 500kHz, our model only shows 2% deviation compared to the measurement. This result shows that our simulation can predict the trend of the converter performance under different operating frequencies reasonably well.

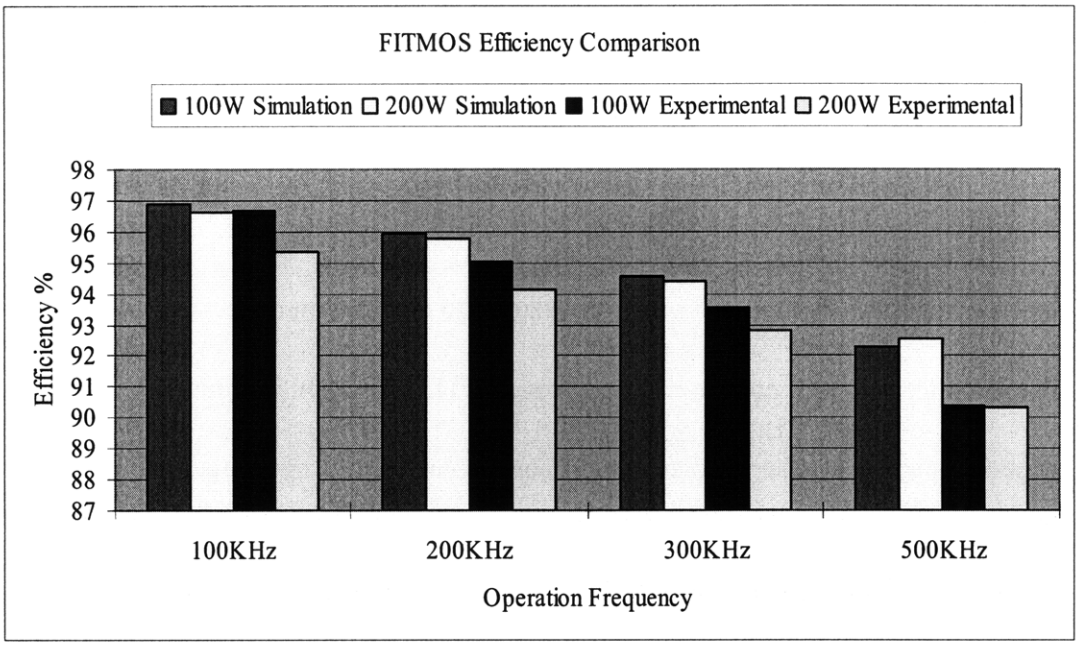


Figure IV.3.1 Converter efficiency comparison between FITMOS model simulation and experimental measurement.

In the next step, we test our simulation accuracy under different loadings at fixed operating frequency. We did the comparison under two different switching frequencies: 200kHz and 500kHz. For each operating frequency, we tested five different loadings: 50W, 100W, 200W, 300W and 400W. In order to further test the performance of our simulation model, we also compare our result to the commercial MOSFET FDP047AN model, which is included in the manufacturer's datasheet. Figure IV.3.2 and 3 show the efficiency comparison between the commercial FDP047AN model with the experimental data.

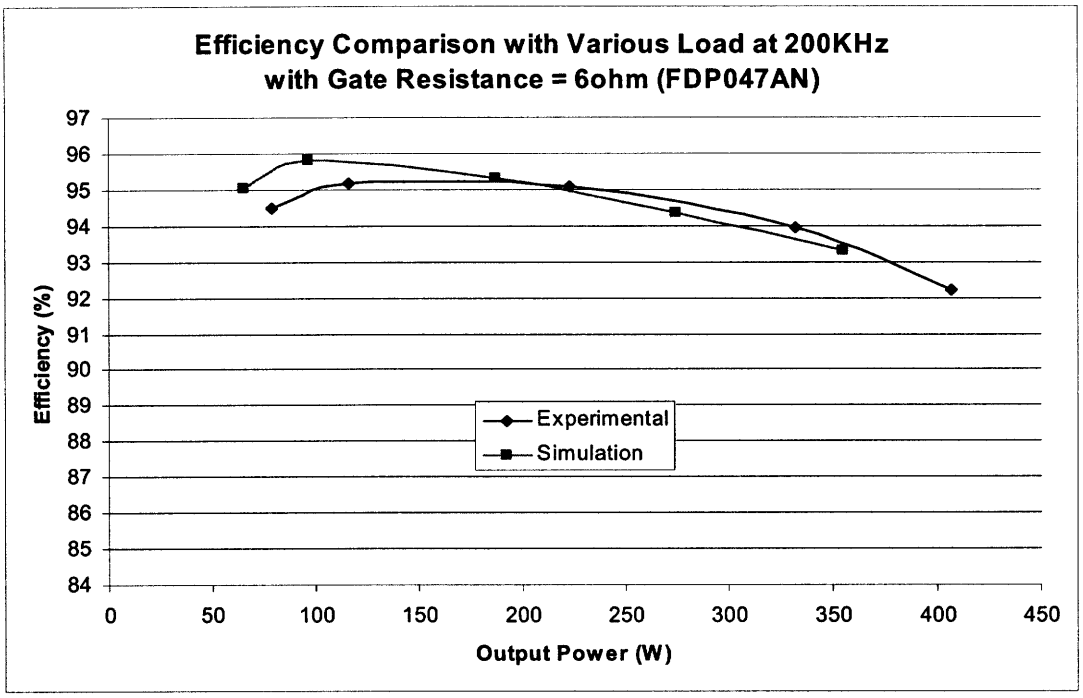


Figure IV.3.2 Efficiency comparison between the commercial MOSFET FDP047AN model with the experiment at operation frequency 200kHz

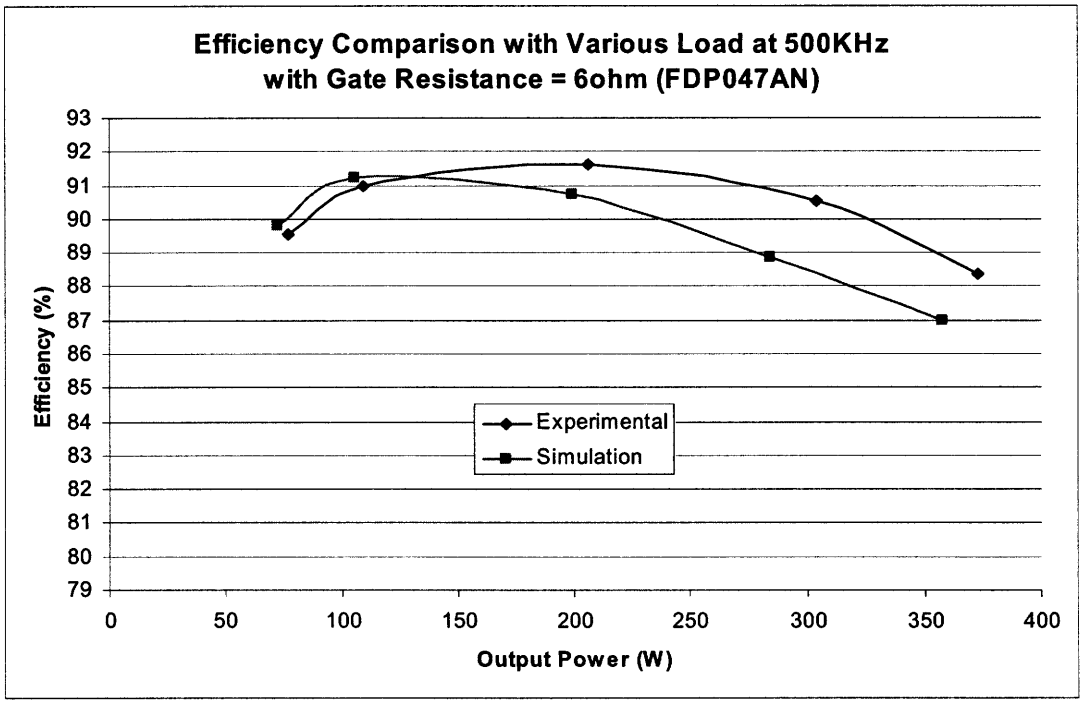


Figure IV.3.3 efficiency comparison between the commercial MOSFET FDP047AN model with the experiment at operation frequency 500kHz.

From the above graphs, we can see that the FDP047AN SPICE model from the manufacturer's datasheet can model the performance of the DC-DC converter quite well. The biggest deviation between the simulation and experimental data is 2%. The simulation model shows a bigger error in higher frequency and higher power.

Now, we consider our FITMOS modeling in the simulation. For the MOSFET turn-on/off transient behavior, we focus on the miller effect in the gate-source voltage and di/dt of the drain-source voltage, since they mainly affect the overlap loss in the switch for the hard switch converter. And we believe that the overlap loss dominates in the total loss of the converter. Figure IV.3.4 and 5 show the detail comparison between the FTIMOS simulation and the experimental measurement for 500kHz operating frequency and 200W output power. By tuning the external gate resistance to 6 Ω to model the gate driver behavior, we can get a very good match for the Miller effect in the simulation. The charging time due to the Miller effect is about 47ns at 200W. From the high-frequency ringing in the drain-source voltage, we can predict the parasitic inductance in the loop from the LC time constant. In addition, from the voltage drop induced by the parasitic inductance in the drain-source voltage, we can extract the di/dt of the drain-source current Ids in the MOSFET by V=L*di/dt. In our simulation, we got a similar voltage drop in the drain source voltage of the MOSFET by comparing to the experimental data. Hence, we believe that our simulation can model the turn on/off transient for the FITMOS accurately.

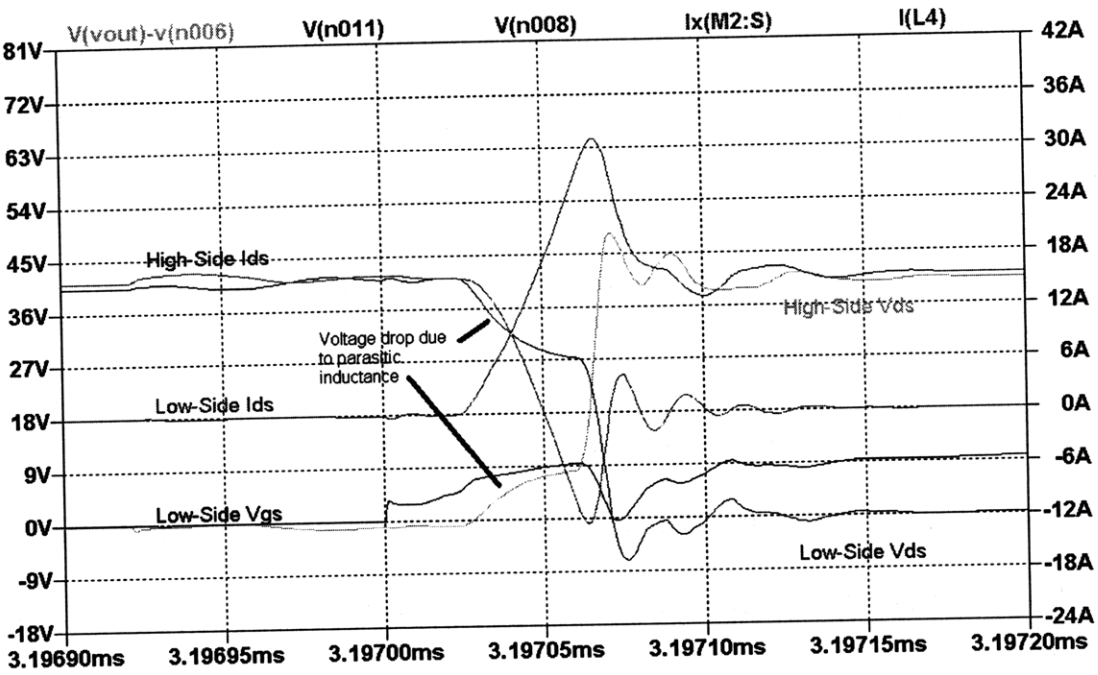


Figure IV.3.4 Turn on transient simulation plot for the low side FITMOS at 500kHz operation frequency and 200W output power.

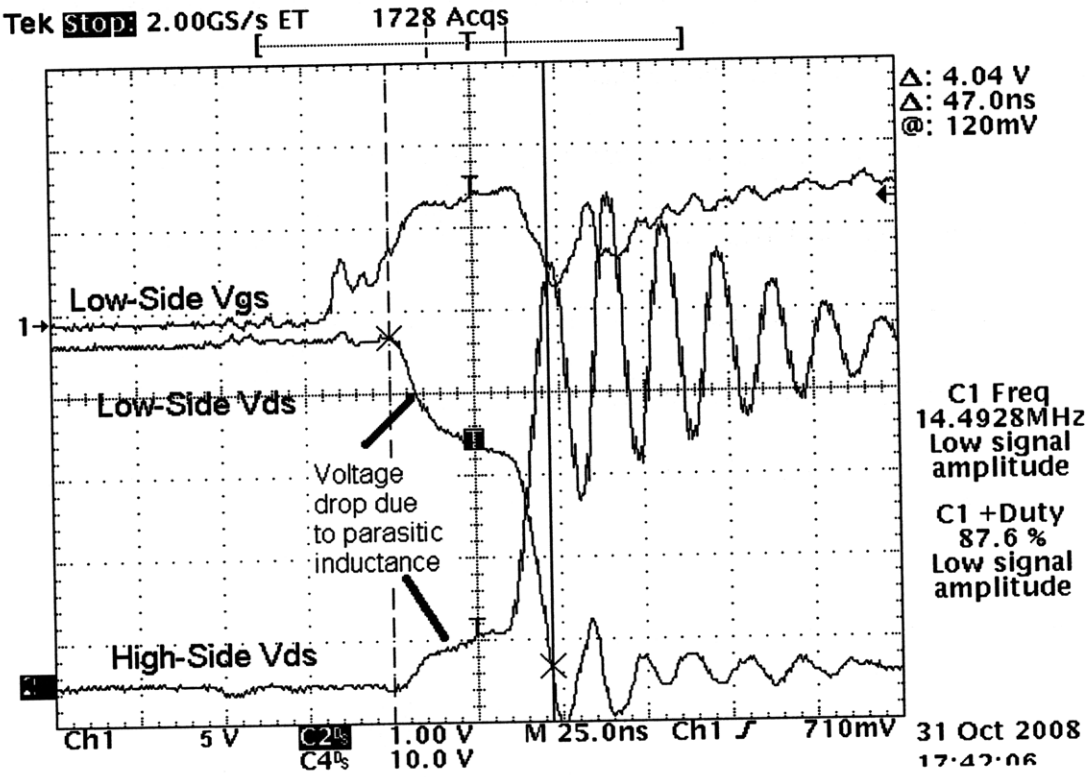


Figure IV.3.5 Experimental measurement for the turn on transient of low side FITMOS at 500kHz operation frequency and 200W output power

Figure IV.3.6 and 7 show the efficiency comparison between our FITMOS model and the experimental data for fixed frequency and various output power. We can also see that our model can predict the performance of the converter reasonable in a wide range, from 50W to 400W. Except at the 400W high output power range, our model only has no more than 2% error than the measurement. But in the 400W high output power range, the thermal factor becomes significant. The device gets hot and produces more and more loss. Since we do not have an accurate thermal model under this extreme high temperature, our simulation gives higher error for larger output power. But overall, our simulation model can predict the trend of the performance of our converter under different loading with fixed operating frequency. And this is very important for our future computer-aid optimization process.

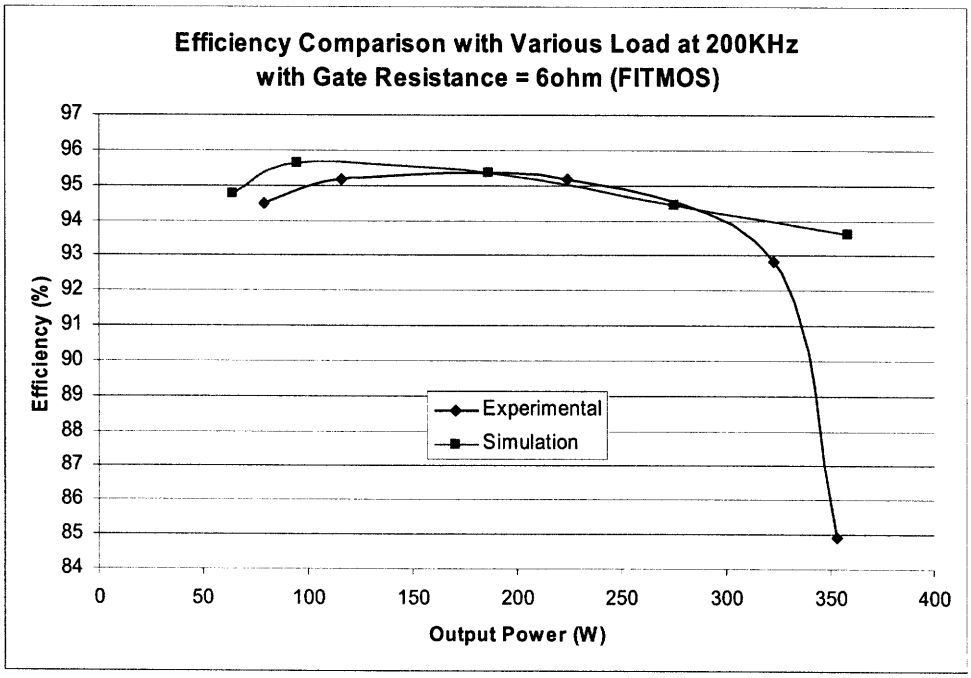


Figure IV.3.6 The efficiency comparison between our FITMOS model with the experimental data at operation frequency 500kHz.

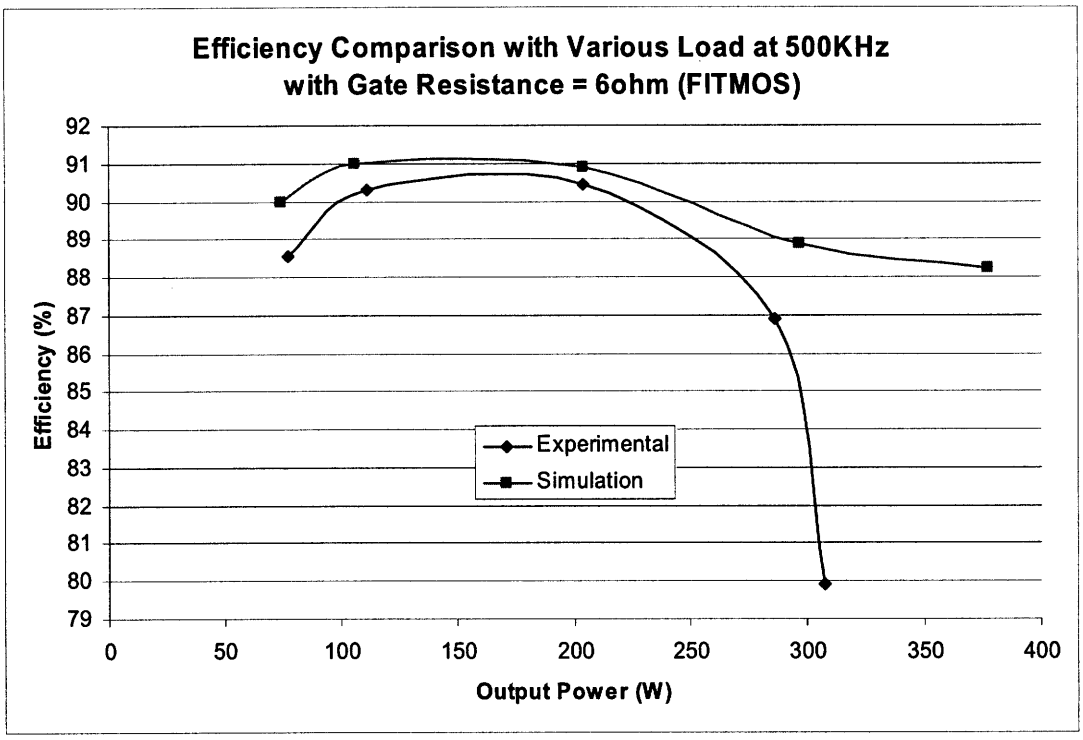


Figure IV.3.7 It shows the efficiency comparison between our FITMOS model with the experimental data at operation frequency 500kHz.

In the end, we conclude that we have obtained a relative accurate spice mode for the FITMOS, even compared to the commercialized power MOSFET FDP047AN model on the manufacturer's datasheet. And our spice model can predict the behavior and performance of converter reasonably well. But in high power output, there is an unreasonable high offset between out simulation and measurement. A deeper study about this behavior will be discussed in the next chapter.

Chapter 5 V_{DS} Saturation Problem in FITMOS

In our last chapter, we measured the efficiency of the test converter (Figure V.1.1 shows the measurement setup) with FITMOS devices under different conditions. We found out that the converter efficiency drops significantly at higher output power (greater than 200W for 14V to 42V conversion). After carefully studying the circuit behavior, a strange phenomenon was observed in the drain-source voltage V_{ds} for the low side MOSFET for a time period after the device is turned on. This chapter documents this behavior, as it is perceived to be of significant importance in application of the FITMOS device.

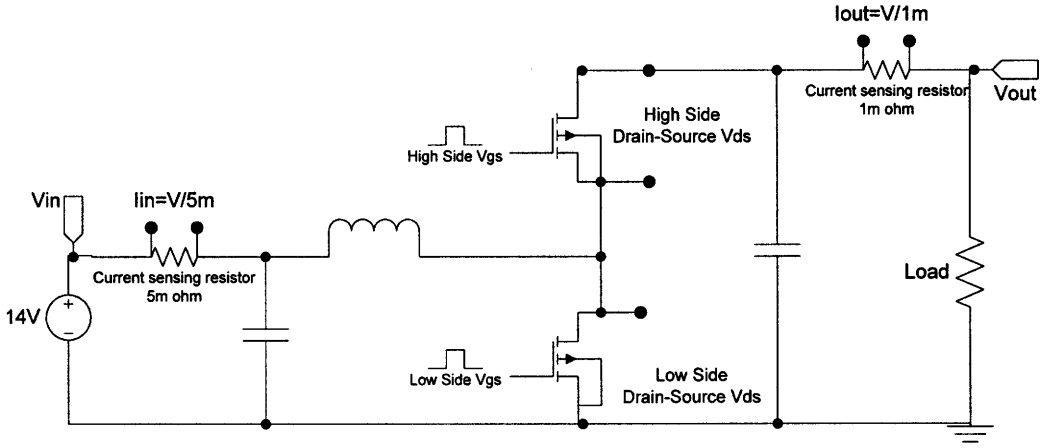


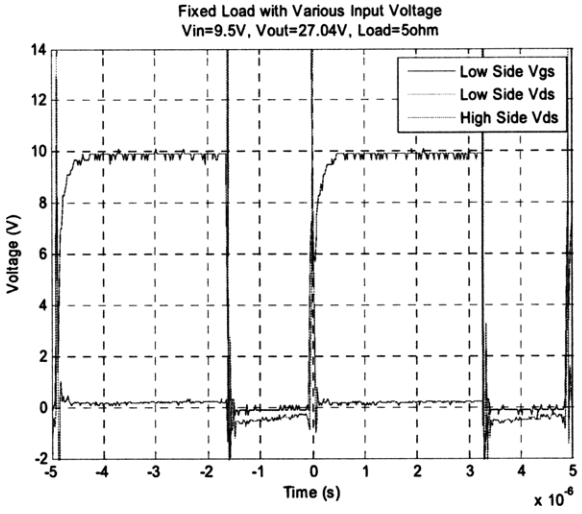
Figure IV.3.1 This graph shows the voltage and current measurement setup. Input current is measured with a 5m ohm current sensing resistor. Output current is measured with a 1m ohm current sensing resistor. High side drain-source voltage V_{ds} is measured with a differential probe. When the MOSFET is off, the drain-source voltage V_{ds} is equal to the output voltage. When the MOSFET is on, the drain-source current I_{ds} in the device is equal to the input current I_{in}.

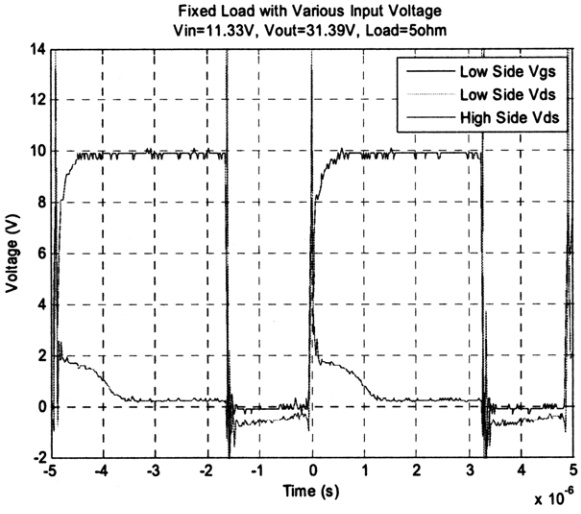
When the bottom transistor is turned on, it carries the inductor current, where the current level (referred to here as I_{ds}) depends on the input and output voltages (and consequently on duty ratio) and the load resistance. As the drain-source current I_{ds} that is carried is increased to certain level (e.g., by adjusting load resistance or input voltage at constant duty ratio), the drain-source voltage of FITMOS does not drop quickly to the normal low level ($R_{ds\text{-}on}$* I_{ds}) that is expected. Instead, it temporarily drops to a 2-3V saturation level (or voltage step level) when the switch is turned on, and only drops to a low level as expected after a long delay time that depends on operating point. When I_{ds} is increased sufficiently, this voltage step can extend across the whole on period for the switch. This situation significantly increases the loss in the device, and hence lowers the efficiency of the converter. To enable this phenomenon to be studied, we captured this behavior under three conditions: 1.fixed load with various input voltages; 2.fixed input voltage and output voltage with various loads; 3.fixed input current with various output voltages.

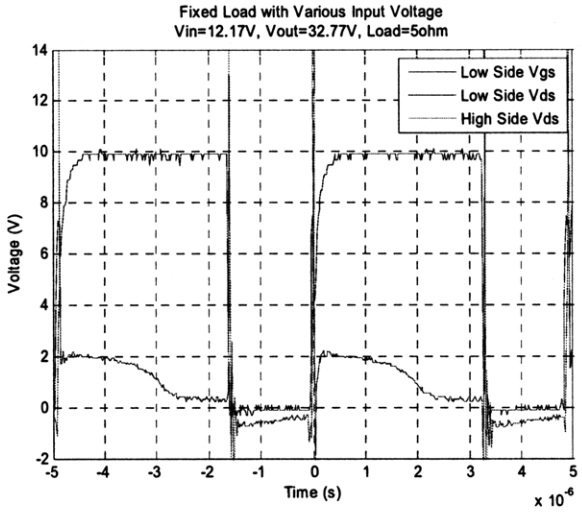
V.4 Fixed Load with Various Input Voltage

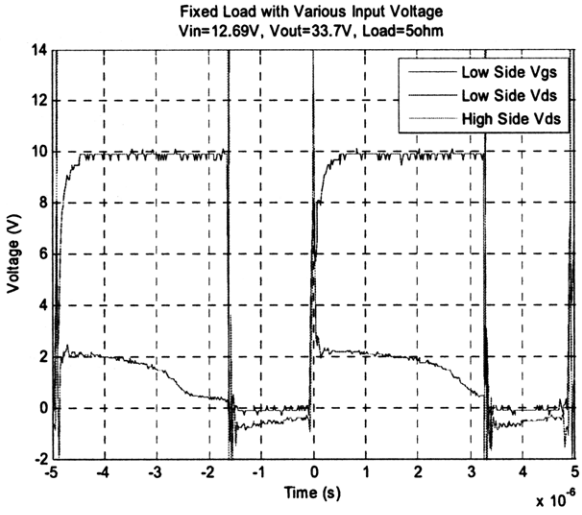
As the input voltage is increased at constant duty ratio, the input current and output voltage both increase. For an on-state duty ratio of 66.6% at a switching frequency of 200kHz and load resistance of 5 ohm, the voltage saturation in V_{ds} starts to happen as V_{out} exceeds 31V and I_{in} reaches 20A. As illustrated below, it becomes quite pronounced for V_{out} =31.39 with I_{in} =19A, and its amplitude and duration increases

with increasing input voltage and current.









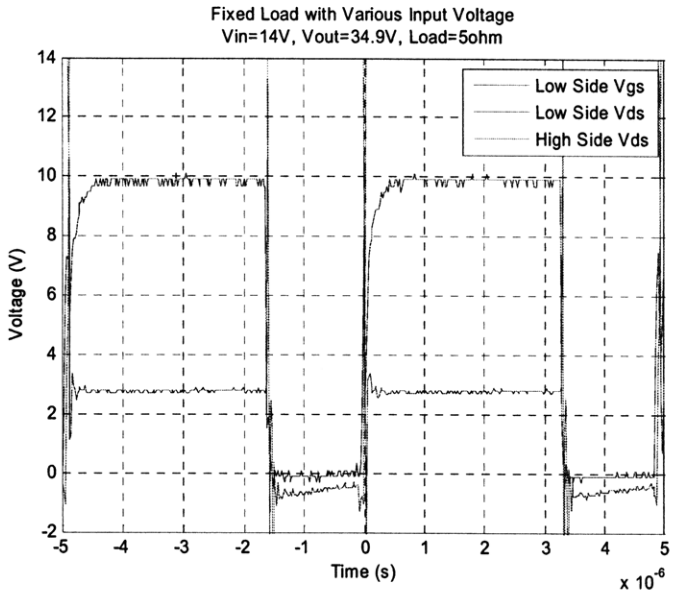
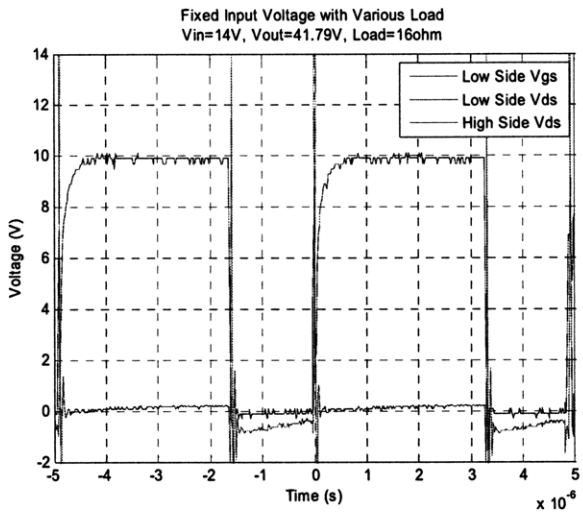


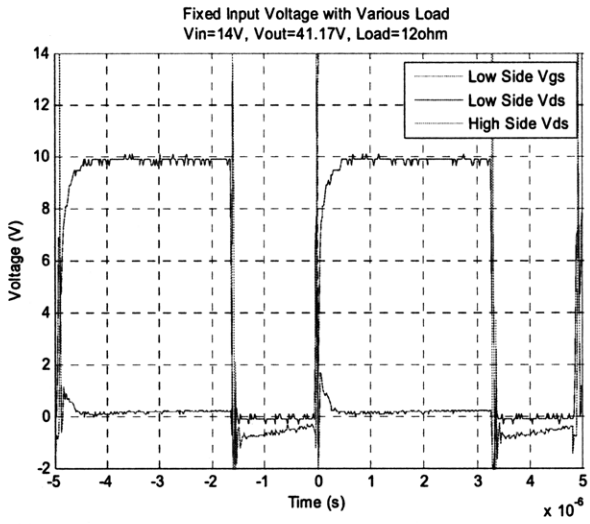
Figure V.4.1 Switching waveform for FITMOS with Fixed load and various input voltage.

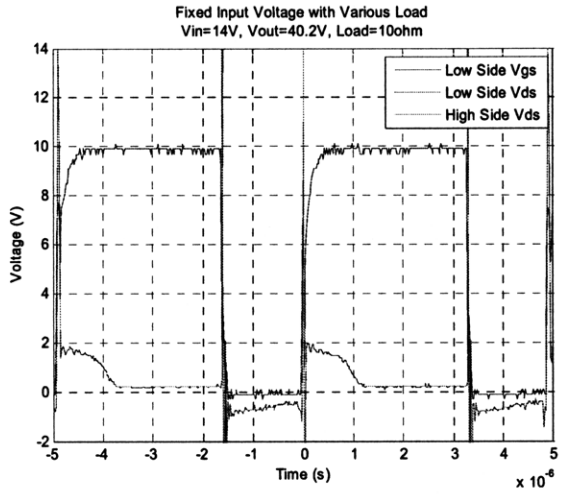
When the V_{out} is 34.9V and I_{in} =22.6A, the voltage saturation step in V_{ds} extended to the whole on period.

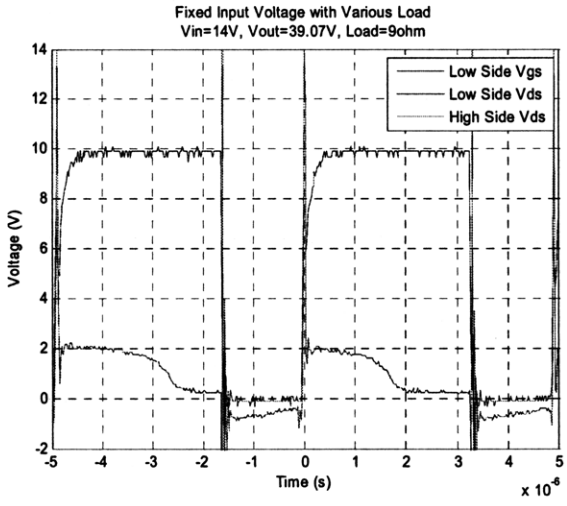
V.5 Fixed Input Voltage with Various Load

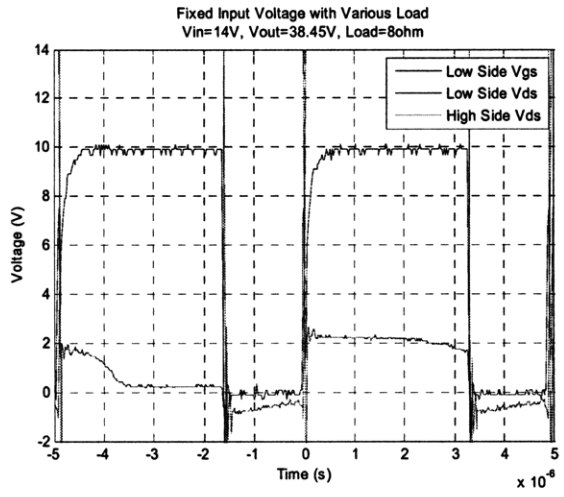
To further observe this behavior, we kept the switching frequency at 200kHz, fixed the input voltage 14V and duty ratio to 66.6%, and hence fixed the output voltage to 42V, but changed the loading to change the input and output current. With V_{out} =41.17V and I_{in} =10.3A, we started seeing the voltage saturation in the drain-source voltage.

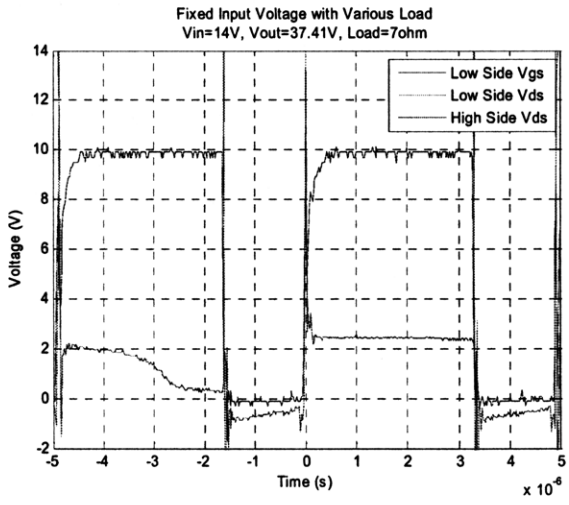

Fixed Input Voltage with Various Load
Vin=14V, Vout=41.79V, Load=16ohm
Low Side Vgs
Low Side Vds
High Side Vds
Voltage (V)
Time (s)
x 10^-6


Fixed Input Voltage with Various Load
Vin=14V, Vout=41.17V, Load=12ohm
Low Side Vgs
Low Side Vds
High Side Vds
Voltage (V)
Time (s)
x 10^-6


Fixed Input Voltage with Various Load
Vin=14V, Vout=40.2V, Load=10ohm
Low Side Vgs
Low Side Vds
High Side Vds
Voltage (V)
Time (s)
x 10^-6


Fixed Input Voltage with Various Load
Vin=14V, Vout=39.07V, Load=9ohm
Low Side Vgs
Low Side Vds
High Side Vds
Voltage (V)
Time (s)
x 10^-6


Fixed Input Voltage with Various Load
Vin=14V, Vout=38.45V, Load=8ohm
Low Side Vgs
Low Side Vds
High Side Vds
Voltage (V)
Time (s)
x 10^-6


Fixed Input Voltage with Various Load
Vin=14V, Vout=37.41V, Load=7ohm
Low Side Vgs
Low Side Vds
High Side Vds
Voltage (V)
Time (s)
x 10^-6

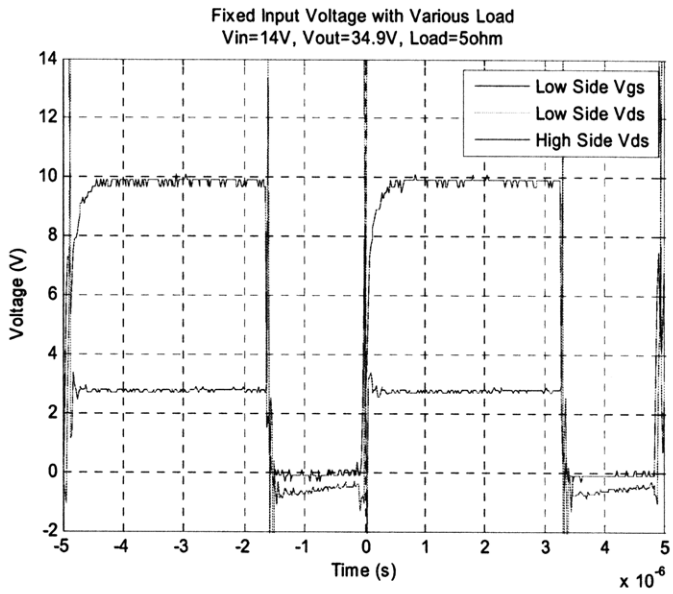


Figure V.5.1 Switching waveform for FITMOS with Fixed input and various load.

As the I_{in} increased to 22.6A and V_{out} =34.9V, the voltage saturation step in V_{ds} extended to the whole on period.

V.6 Fixed Input Current with Various Output Voltage

As a final means of observing this behavior, we fixed the switching frequency and duty ratio as before, but varied the input voltage and load resistance to hold input current and hence I_{ds} constant with varying output voltage. When the V_{out} =28.8V and I_{in} =23.33A, the voltage saturation in V_{ds} starts to happen, as illustrated below.

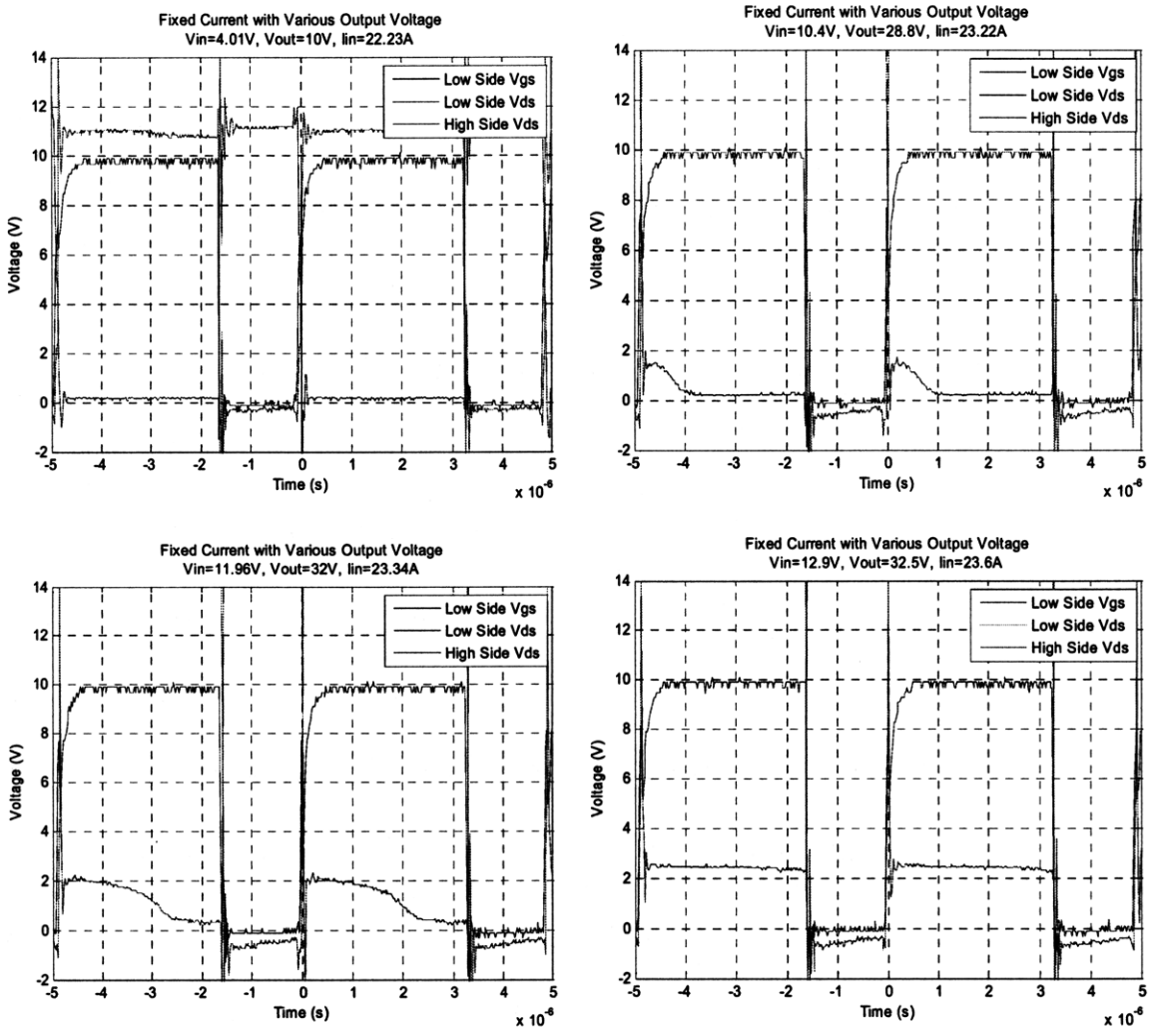


Figure V.6.1 Switching waveform for FITMOS with Fixed current and various output voltage.

When V_{out} is 32.5V and I_{in} =23.6A, the voltage saturation step in V_{ds} extended to the whole on period.

In figure V.3.2, we illustrate the boundary of the region for which the saturation step in on state voltage was observed in terms of drain-source off-state voltage V_{ds} and drain-source on-state current Ids. If the FITMOS is operating under the conditions below the line, the saturation step in voltage V_{ds} (and its associated loss) is not observed.

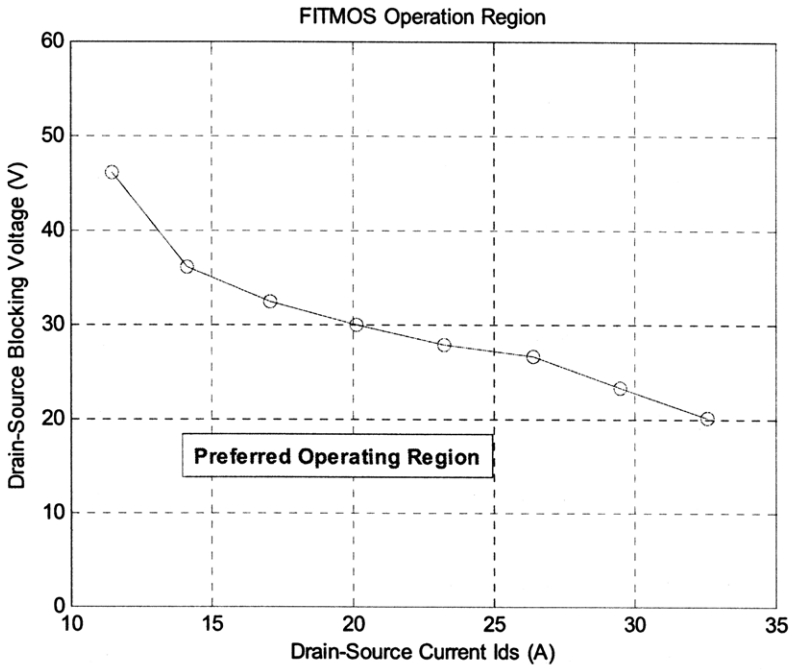


Figure V.6.2 It shows the preferred operating region for FITMOS to avoid the high loss induced by the V_{ds} voltage saturation.

This V_{ds} saturation problem only happens in the old FITMOS. The latest version improved FITMOS has corrected this problem and has a much better performance in the high power region. When the V_{ds} saturation problem does not occur in low device stress region, the old FITMOS and improved FITMOS have very similar performance.

Chapter 6 Optimization

After we completed the FITMOS modeling, we have compared the simulation result with the experimental data under different conditions (different output powers with fixed operation frequency and fixed output power with different operation frequencies). The result shows that our model can match with the measurement within an acceptable range. From now on, we will focus on the converter design optimization for FITMOS. At first, we will use our simulation model to find out the optimal converter design for taking advantage of FITMOS devices. We will then build and test the optimized converter to verify the simulation and fine tune it to the ultimate design.

VI.7 Simulation Optimization Process

Due to the complexity of our FITMOS model, a full design scan for FITMOS in the computer-aided design tool would require a tremendous amount of computing time and this is inefficient. In order to optimize the performance of the FITMOS sufficiently, we will focus on studying the use of FITMOS in certain regimes and on certain aspects of the design tradeoffs (e.g., DCM, CCM and size efficiency trade-off). First of all, we will investigate the performance of FITMOS under soft-switching in this report. Figure VI.1.1 shows the converter circuit for soft-switching in simulation. The input voltage of the converter is 14V and the output voltage is about 42V. Based on earlier results, output power of 100W and 200W were tested. To achieve

soft-switching, an external capacitor $C_{\_extra}$ was added in parallel with the drain and source of the low-side MOSFET. A small input inductance (0.7uH) was also chosen to obtain a slightly over 200% peak to peak ripple current. This is useful in realizing zero-voltage soft switching. For example, consider the "top to bottom" switch transition. When the inductor current goes negative, it discharges the capacitor $C_{\_extra}$ and hence lowers the drain-source voltage V_{ds} of the low-side device. When the V_{ds} of the low-side device becomes zero, we turn the MOSFET on to achieve the ZVS (zero voltage switching) to reduce overlap loss on the device. In addition, by controlling the dead time between two devices, we also can obtain a ZVS for the high-side device. The soft-switching waveforms are shown in figure VI.1.2. We can see that we can achieve ZVS when the low-side device is turned on or the high-side device is turned on and off. A nearly ZVS is also achieved for the low-side device turn off transition due to the large external capacitance between the drain and source. In this situation, we can eliminate the overlap loss in the devices. The trade-off is that we have a large ripple current and hence larger conduction loss in the circuit and larger core and winding loss in the inductor.

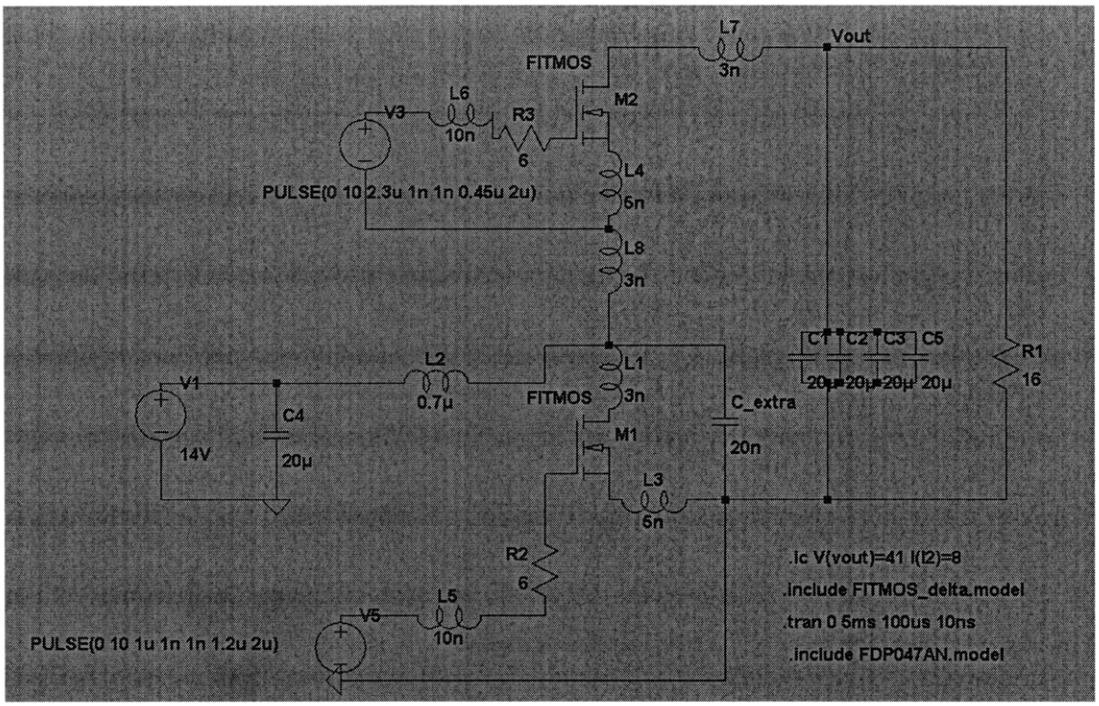


Figure VI.7.1 It shows converter circuit for soft-switching in Spice simulation. $C_{\_extra}$ is added in parallel with the drain and source to achieve ZVS.

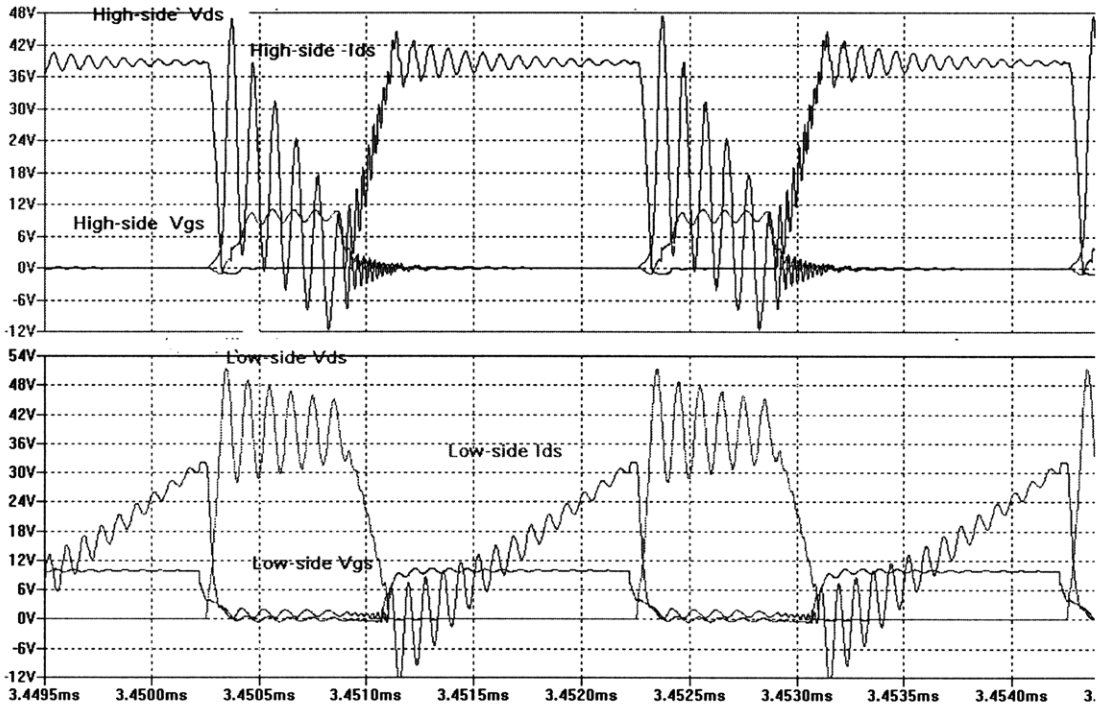


Figure VI.7.2 It shows the switching waveforms of the low-side and high-side devices under ZVS. ZVS is achieved in the turn on and off period of both devices.

Figure VI.1.3 shows the converter performance under soft-switching with 500kHz operation frequency. (Note: The following efficiency calculation based on simulation models does not include inductor loss; we will calculate inductor loss separately. The calculation does include logic and gate driver loss.) When the $C_{\_extra}$ is 20nF, the converter reaches its peak efficiency 95% at 100W output power, which is more than 3% higher than predicted for hard switching (91.4%). For 200W output power, the converter reaches its peak efficiency 93.2% when $C_{\_extra}$ is 50nF. In hard switching, the converter only has 91.2% efficiency in simulation. This suggests that soft-switching can reduce certain amount of device overlap loss and hence reduce device stress and improve converter efficiency for FITMOS.

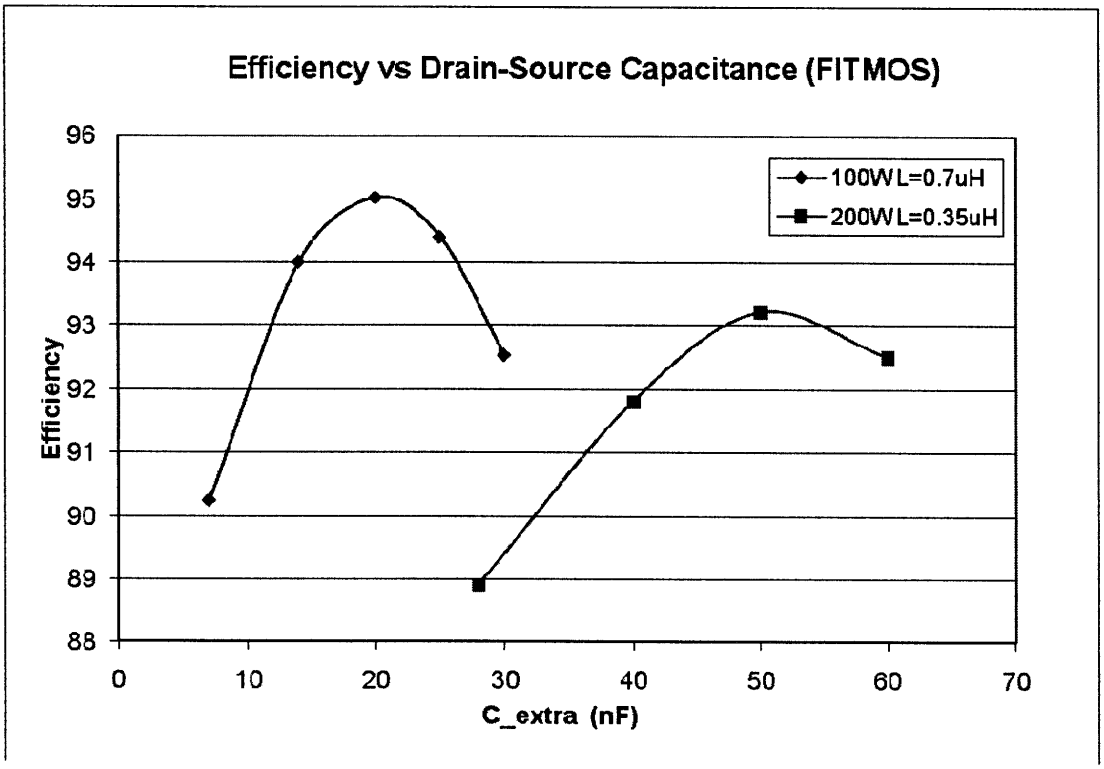


Figure VI.7.3 It shows the converter efficiency versus $C_{\_extra}$ under soft-switching. Efficiency calculation based on the simulation model of appendix IX.1.4. This efficiency includes all the losses except inductor loss. We will optimize the inductor design separately.

For comparison, we also simulated the converter performance with the commercial device FDP047AN under soft-switching. FigureVI.1.4 shows the converter performance with FDP047AN under soft-switching with 500kHz operation frequency. Since FDP047AN has very similar characteristics as FITMOS, the converter reaches its peak efficiency under almost the same settings. In 100W output power, simulation suggests that soft-switching will improve the efficiency of FDP047AN converter from 91.6% in hard switching to 93.6%. But in 200W output power, the converter has worse performance. The efficiency drops from 91.1% in hard switching to 90%. On the other hand, the simulation results suggest that FITMOS has a better performance than FDP047AN under soft-switching. Especially in higher output power 200W, the converter with FITMOS has more than 3% improvement in simulation. This may be beneficial from the lower $R_{ds\text{-}on}$ in FITMOS since soft-switching eliminates the overlap loss but increases the conduction loss.

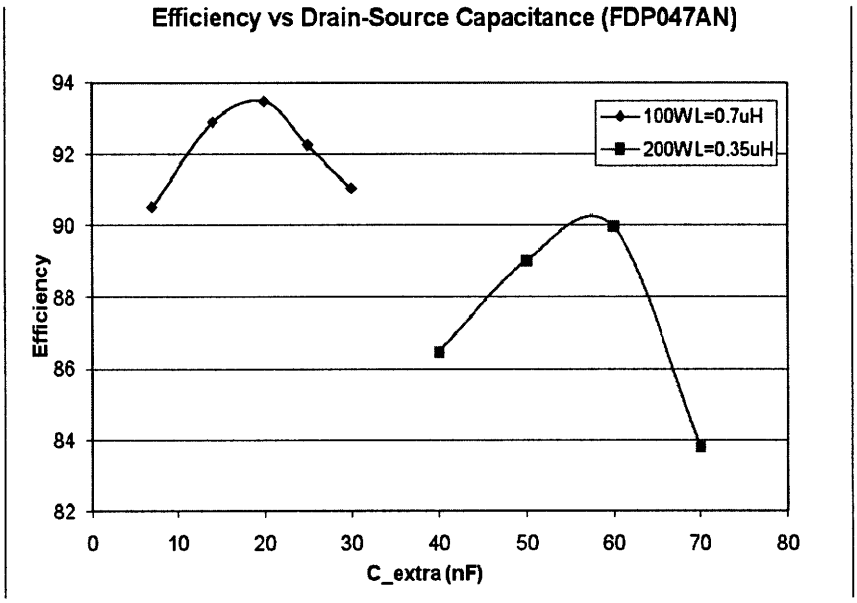


Figure VI.7.4 It shows the converter efficiency versus C_extra under soft-switching for FDP047AN Again, this efficiency includes all the losses except inductor loss.

For the input inductor, we use a MATLAB script [12] (Appendix IX.3) to find out the best design for the converter. The MATLAB script first will simulate the current waveform in the inductor. Then based on the giving inductance and current waveform, the script tries to design an inductor based on each core in the data set and retains those which are feasible [11]. For each design the script calculates core losses and winding losses (including losses due to skin and proximity effect) based on fitted empirical data and theoretical models. The loss data (and expected core temperature rise) are retained with the design parameters for all feasible designs. From the data result, we can choose the best inductor design for our converter. For 100W output power, the inductance is 0.7uH, the best inductor design using RM cores of Ferroxcube 3F3 material is:

RM10PA315 :
N = 1 of guage 10
Bpk 776.6024
Jwire = 1288.056 A/in^2
Pcore = 0.75864 Watts
Pwind = 0.062141 Watts
Ptot = 0.82078 Watts
delta T = 24.6235deg C

For 200W output power, the inductance is 0.35uH, the best inductor design is:

RM10PA160 :
N = 1 of guage 10
Bpk 788.9294
Jwire = 2576.112 A/in^2
Pcore = 0.78911 Watts
Pwind = 0.24856 Watts
Ptot = 1.0377 Watts
delta T = 31.13 deg C

As a result, accounting the inductor loss only drops the converter efficiency by

0.5%.

(The optimum inductor is not the one with the lowest loss; we also consider other factors, like size and temperature rise. In here, we picked the one with the best balance between our considerations.)

So far, based on the simulation, we can see that FITMOS is expected to have better performance in soft-switching. Since the converter with FDP047AN has better efficiency in hard switching during the experiment, we may assume that the FITMOS has more overlap loss in hard switching. And because FITMOS has a lower Rds-on, it has a better performance for soft switching while ZVS can eliminate the overlap loss. In the next step, we implement the soft-switched converter to test this conclusion experimentally.

VI.8 Optimization Experimental Result

After we finished simulation optimization for the FITMOS, we modified our converter to operate in soft-switching mode at 500kHz switching frequency to verify our simulation result.

Figure VI.2.1 shows the converter efficiency plot of our soft-switching mode DC-DC converter. The input voltage of the converter is 14V and the output voltage is 42V. The switching frequency is 500kHz and the output power is 100W. In order to achieve soft-switching mode, we need over 200% peak to peak ripple ratio. As a result, a 0.7uH inductance is chosen. From our MATLAB inductor optimization script, RM10PA160 core is picked to compromise both size and loss. From our calculation, the inductor loss is 1.13watt. In the efficiency plot, the inductor loss is excluded since there are many ways to implement this inductor and the inductor loss can vary.

First of all, we can see that the improved FITMOS has a slightly performance improvement than the old FITMOS. And we believe that this improvement can become larger under the higher current stress due to the V_{ds} voltage saturation step problem of the old FITMOS. But unfortunately, we can see that there is a significant offset between our simulation and measurement data. Other than that, the converter efficiency remains constant over a wide drain-source capacitance range, which does not follow the simulation prediction. In the simulation, we can see that the converter efficiency peaks at $C_{\_extra}$ =22nF and drops at both ends of the capacitance range.

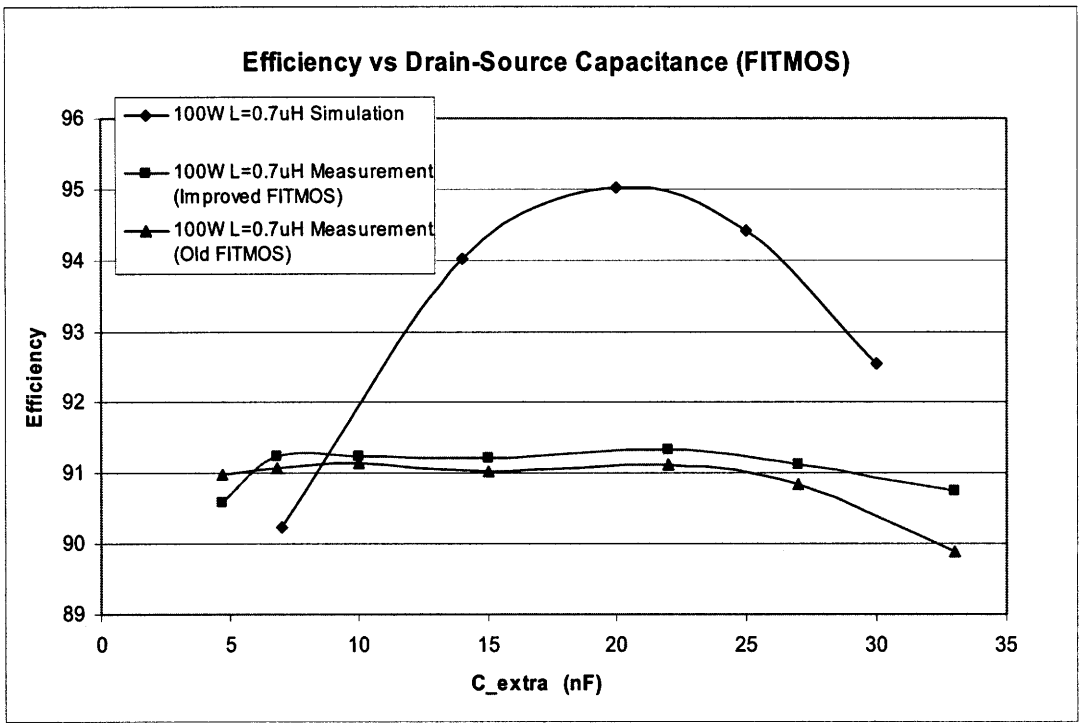


Figure VI.8.1 It shows converter efficiency comparison between simulation and measurement under soft-switching mode at 500kHz switching frequency. $C_{\_extra}$ is added in parallel with the drain and source to achieve ZVS. In the plot, the inductor losses are excluded. But all other losses are taken into account including the power loss in the control and gate driver circuitry.

For comparison, we also plot the converter efficiency in soft-switching mode with the other competitive commercial power MOSFET FDP047AN. Figure VI.2.2 shows the efficiency plot for FDP047AN versus external drain-source capacitance. In simulation, the converter efficiency with FDP047AN is relative lower than the one with FITMOS. But in experimental measurement, the converter with FDP047AN behaves similarly to the simulation prediction. It has the better performance when the external drain-source capacitance is at the 20nF range and the efficiency drops to both ends. And under the peak performance condition, the FDP047AN is about 1% better than the FITMOS.

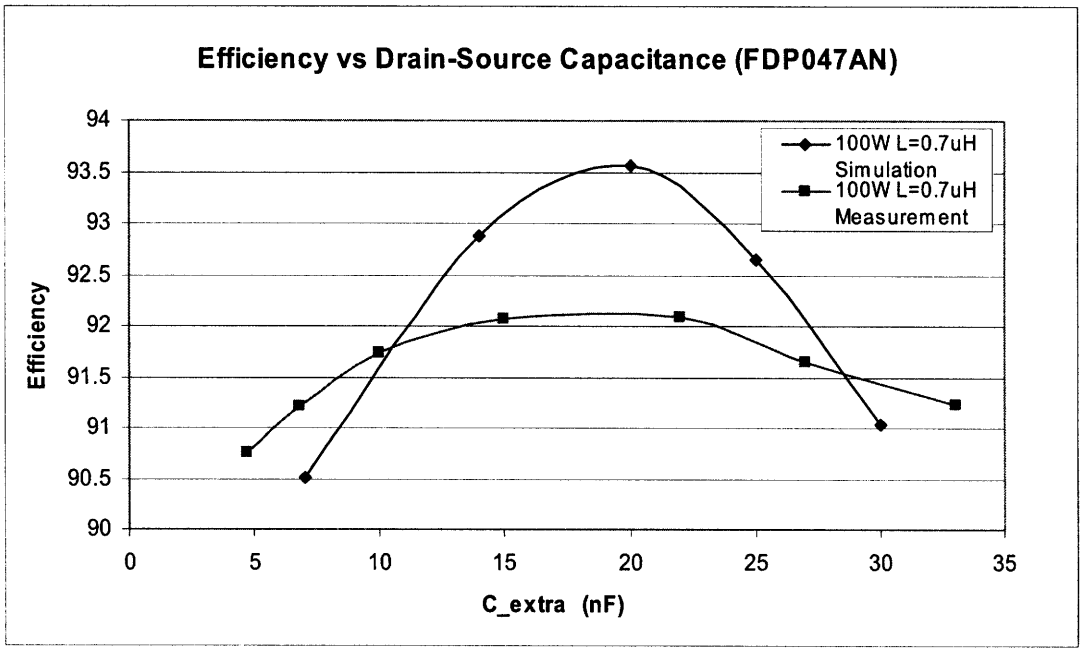


Figure VI.8.2 It shows efficiency of the converter with FDP047AN under soft-switching mode at 500kHz switching frequency.
C_{extra} is added in parallel with the drain and source to achieve ZVS. Again, the inductor losses are excluded. But all other losses are taken into account including the power loss in the control and gate driver circuitry.

Now we want to study the mismatch between simulation and measurement for FITMOS. In the soft-switching, we are achieving ZVS for switches and hence we minimize the overlap loss in the MOSFET. As a result, we suspect there is a dynamic conduction loss element we did not catch in our model since the simulation only models the conduction loss due to the static on-resistance. To further examine our prediction, we carefully measured the switching waveform for the improved FITMOS in the soft-switching converter at 500kHz and compared it with the commercial MOSFET FDP047AN. Figure VI.2.3 shows the switching waveform for the FDP047AN, while figure VI.2.4 shows the switching waveform for Improved FITMOS under different Ids.

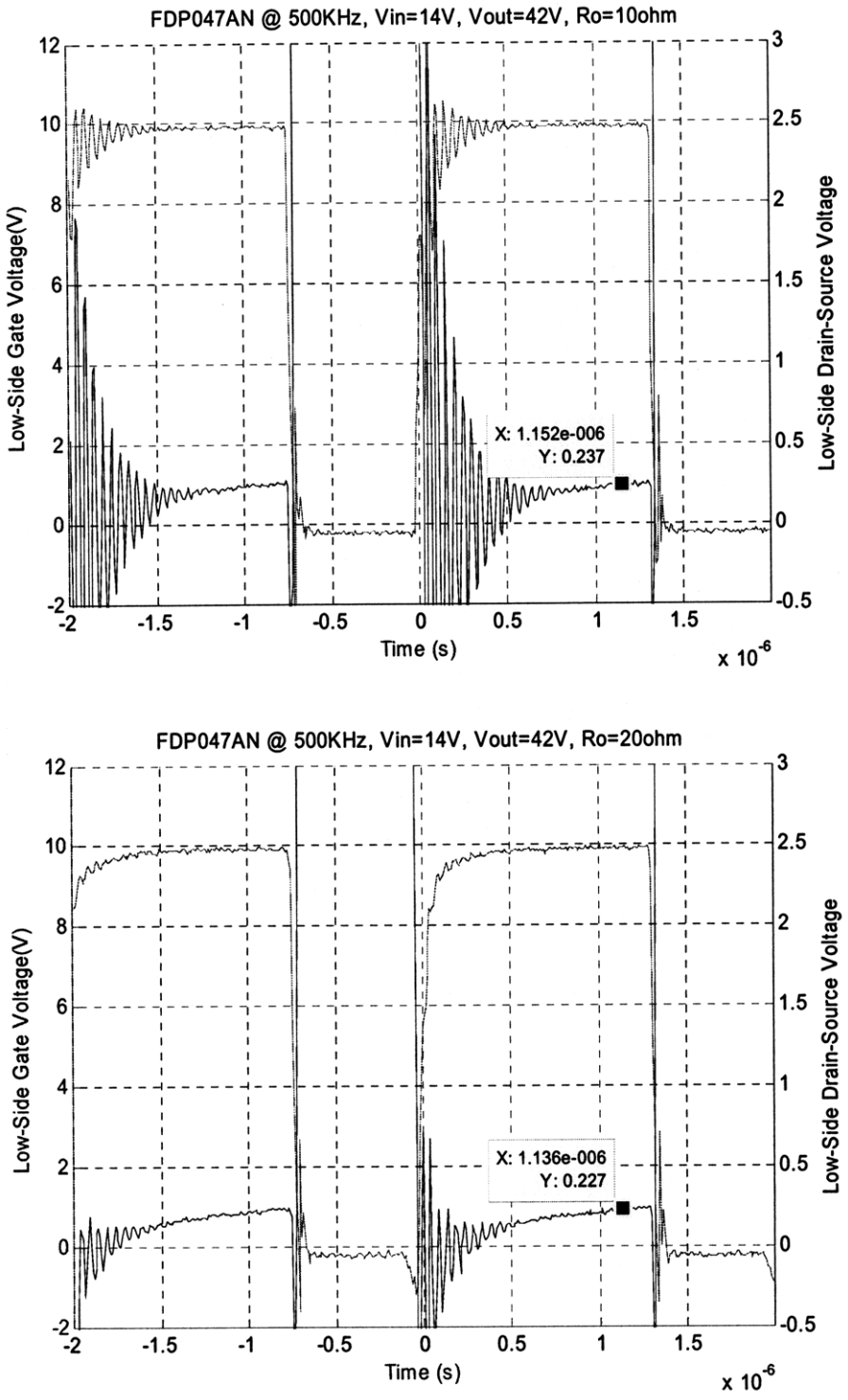


Figure VI.8.3 It shows switching waveform for the FDP047AN at 500kHz in the soft-switching converter.

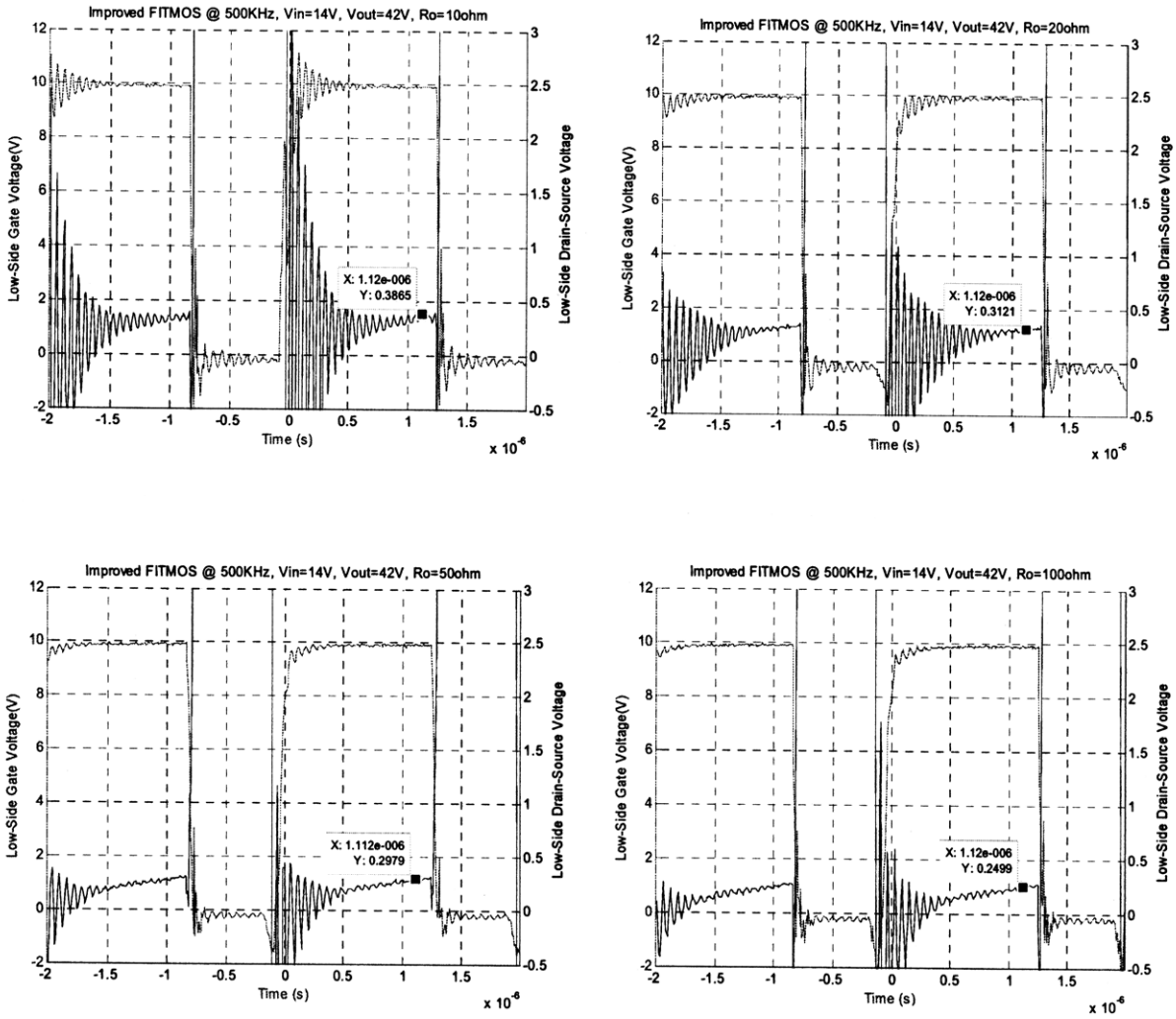


Figure VI.8.4 It shows switching waveform for the Improved FITMOS at 500kHz in the soft-switching converter with different load.
We change the current Ids level by change the load resistance from 10 ohm to 100ohm.

Both FITMOS and FDP047AN have the similar on-resistance under the static drain-source current Ids. But when they are switching at 500kHz and experiencing a large Ids current ripple (in soft-switching mode), the FITMOS has a much higher dynamic on-resistance. When output power is about 200W, the $V_{ds\text{-}on}$ is only 0.237V in FDP047AN compared to 0.387V in Improved FITMOS. So the on-resistance of FITMOS is 63.3% higher under the large dynamic current. Due to this dynamic change in on-resistance, we are experiencing a much higher conduction loss in

soft-switching. This also explains the large offset between our simulation and measurement. In soft-switching, the large current ripple and large dynamic on-resistance make the conduction loss majorly affect the overall converter performance. While the conduction loss dominates the overlap loss, we cannot see the relatively small performance variation of the converter with different external drain-source capacitance. As a result, the converter efficiency is flat under the wide external drain-source capacitance range.

In order to further confirm that the large on-resistance is caused by the large dynamic drain-source current change. We also test the switching waveform of the FITMOS (both old and improved FITMOS) under hard-switching mode, in which the FITMOS experiences much smaller current ripple. The result is shown in figure VI.2.5. First of all, we can see that Improved FITMOS has a much better ac-characteristic than the old FITMOS. The V_{ds} saturation step problem is solved in the Improved FITMOS. So I predict that the improved FITMOS should have a much better performance when the output power is greater than 200W. In addition, the Improved FITMOS shows a much lower $V_{ds\text{-}on}$ in hard-switching mode (0.31V in soft-switching and about 0.1V in hard-switching with the similar current amplitude). Also, the measurement shows that the $V_{ds\text{-}on}$ increases when we scale up the switching frequency from 200kHz to 500kHz. This further proves that the dynamic current change can affect the $R_{ds\text{-}on}$ under switching.

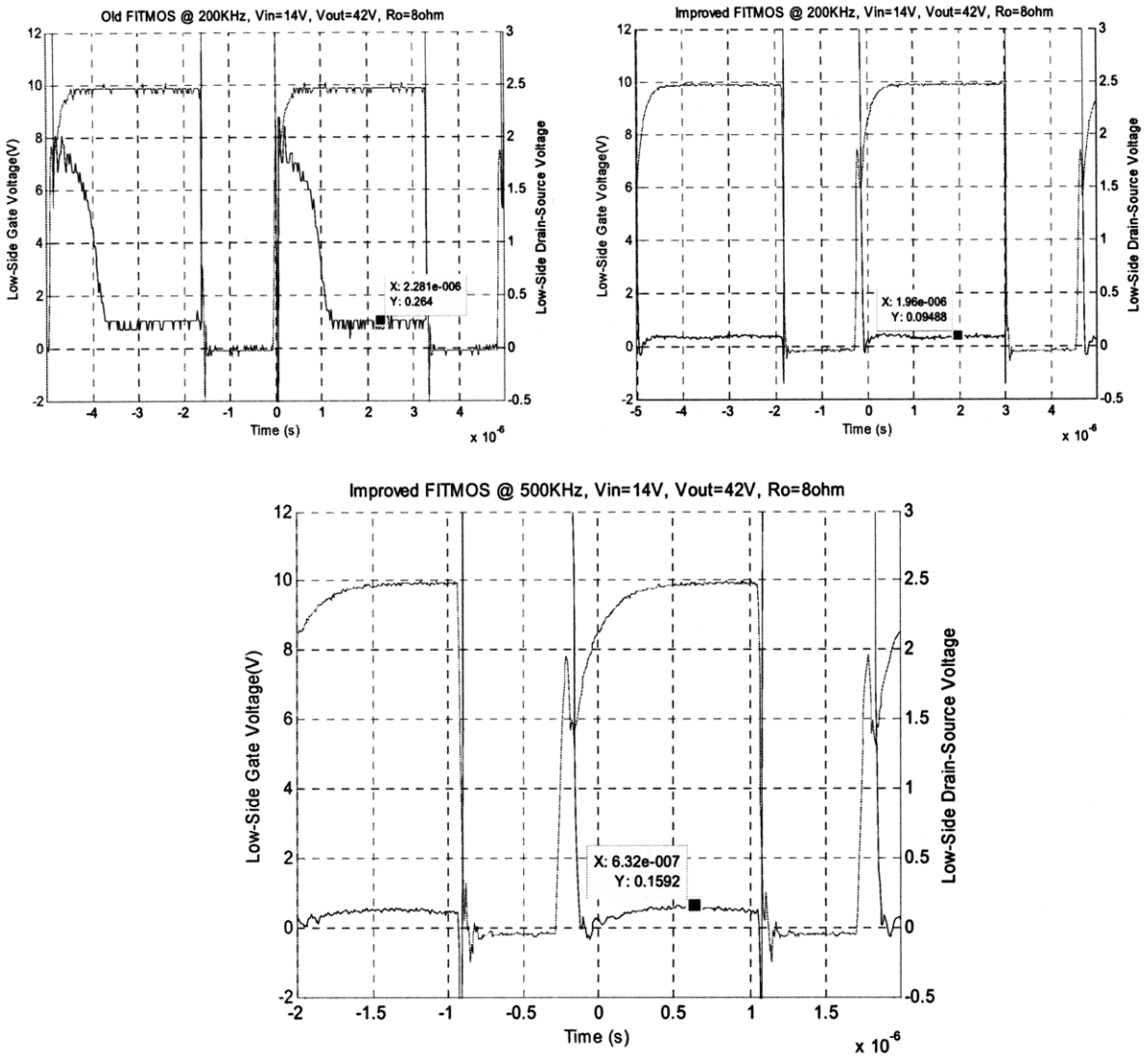


Figure VI.8.5 The switching waveform for both Improved FITMOS and old FITMOS in the hard-switching converter

The top graphs are the switching waveform for both Improved FITMOS and old FITMOS at 200kHz in the hard-switching converter. The bottom graph is the switching waveform for the Improve FITMOS at 500kHz in the hard-switching converter

In soft-switching, due to the high di/dt, small packaging parasitic inductance change can affect our drain-source voltage V_{ds} measurement. In order to study the forward voltage drop in the FITMOS carefully, we would like the extract the parasitic inductance in the device. From our switching wave VI.2.3 and 4, the FDP047AN and FITMOS have ringing frequencies of 25MHz and 17.86MHz respectively when the device is turned on. Since we have a 10nF external capacitance across the drain and source of the device for soft-switching, we can extract the parasitic inductance in the package from the ringing frequency by $f_{ring} = \frac{1}{2*\pi*\sqrt{L*C}}$.

$$L_{FITMOS} = \frac{1}{C}*(\frac{1}{2*\pi*f_{ring}})^2 = 7.94nH$$
$$L_{FDP047AN} = \frac{1}{C}*(\frac{1}{2*\pi*f_{ring}})^2 = 4.05nH \qquad (6.2.1)$$

The additional parasitic inductance in the FITMOS package can provide certain voltage offset during the high di/dt period due to $V = L\frac{di}{dt} = 59mV$. But the forward voltage drop difference in V_{ds} between FITMOS and FDP047AN is over 90mV. This shows that we might have an extra dynamic on-resistance increase in the high di/dt period.

In addition, we also study this phenomenon from the power loss aspect. From the inductor power loss at turnoff $P = \frac{1}{2}*L*i_{peak}{}^2*f$, the extra 3.9nH parasitic inductance only gives additional 0.39W loss in the converter while the output power is 100W. This only contributes 0.39% efficiency drop in converter. But from both our efficiency measurement and simulation, we all experienced over 1% efficiency drop from our expectation. After considering the V_{ds} offset and loss contributed from the

extra parasitic inductance, we still suspect that there is a dynamic change for on-resistance with the large dynamic drain-source current change.

Chapter 7 Dynamic On-resistance Study

From the experiment and simulation mismatch and MOSFET switching waveforms we observed in the chapter 6, we suspect that the FITMOS on-resistance is dependent on the dynamics of the drain-source current. An increased V_{ds} is observed during the on period when the device is experiencing high di/dt in the drain-source current. After we extract out the parasitic inductance effect, the result still makes us suspect that effective on-resistance increases under the high dynamic current di/dt change environment. In this chapter, we investigate the dynamic behavior of the on-resistance in the MOSFETs.

VII.9 Dynamic On-resistance

We study the on-resistance behavior in two aspects: one is the on-resistance dependence on current frequency (e.g. at constant di/dt); the other is the on-resistance dependence on dynamic current change di/dt (e.g. at constant drive frequency). Figure VII.1.1 shows the equipment setup for this experiment. A 10V V_{gs} is continuously applied to the device to maintain the MOSFET on during the whole experiment. In this way, we can prevent the parasitic ringing from affecting our measurement during the switching transition of the device. A sinusoidal current is applied through the device. By measurement the drain-source voltage V_{ds}, drain-source current I_{ds} and the phase between the V_{ds} and I_{ds}, we can extract the real on-resistance in the MOSFET

from $\frac{V_{ds}}{I_{ds}} * \cos(\theta)$, if the voltage and current waveform are purely sinusoidal with negligible distortion. The sinusoid signal is applied by the Agilent 33250A function generator. This sinusoidal signal is amplified by the power amplifier ENI 3100LA to drive current into the drain-source port of the MOSFET. A 50 Ω load is connected in series with the MOSFET to match the output impedance of the power amplifier. A common mode choke, realized as turns of 50 Ω coaxial cable interconnect through a ferrite core, is used to eliminate common-mode currents.

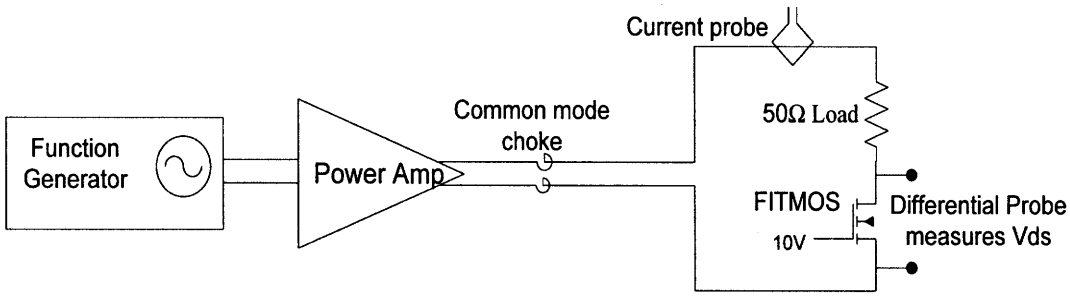


Figure VII.9.1 The equipment setup for the dynamic on-resistance measurement. A Tektronix TDS7254B scope is used for the measurement. V_{ds} is measured by the Tektronix differential probe P7330 and the drain-source current I_{ds} is measured by the Tektronix current probe TCP202. An Agilent 33250A function generator and an RF power amplifier ENI 3100LA are used to drive the MOSFET

For comparison, a 5mΩ current sensing resistor and commercial power MOSFET FDP047AN are also tested in this experiment. Figure VII.1.2 shows the measurement result of MOSFET on-resistance response respect to different current frequencies at constant current amplitude (thus peak di/dt increases proportionally to frequency). The sinusoidal current frequency is increased from 100kHz to 1MHz

while the amplitude is held constant at 1.2A. Over the whole frequency range, the current sensing resistor maintains the same resistance, which is about 4.6mΩ. When the current is above 500kHz, the on-resistances of both FITMOS and FDP047AN have substantial increment. This shows that the on-resistances of both MOSFETs are frequency dependent. But overall, the FITMOS on-resistance is about 30% higher than the FDP047AN. As a result, the FITMOS has higher conduction loss than the FDP047AN. As the frequency goes higher, the loss caused by the on-resistance will also increase.

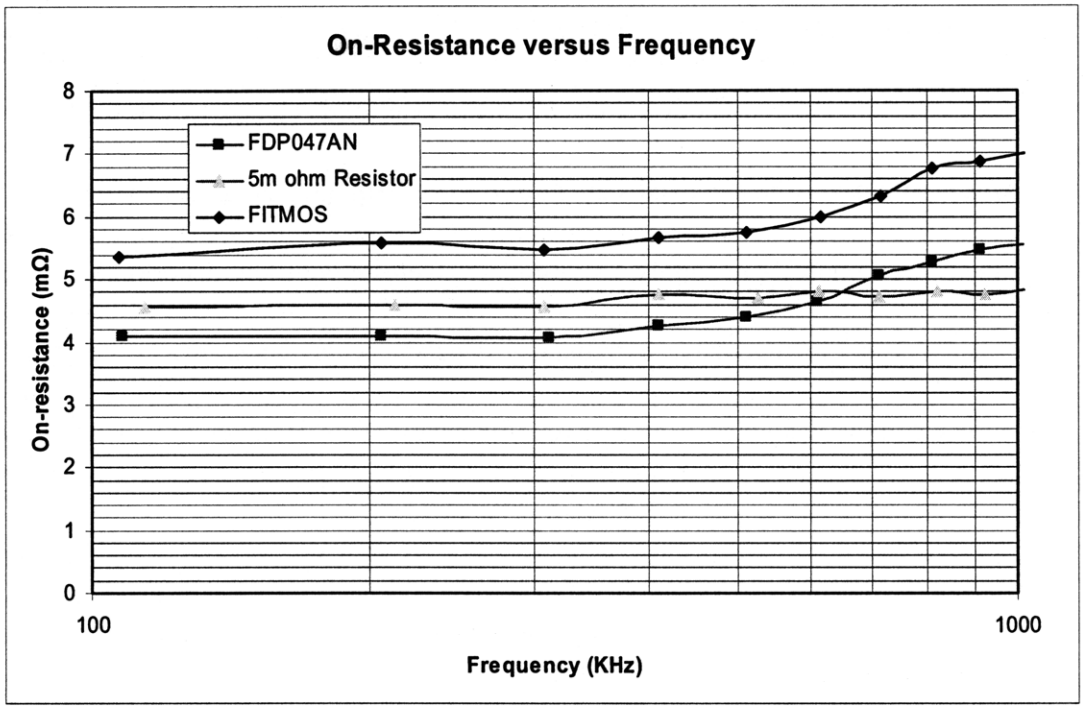


Figure VII.9.2 This plot shows the on-resistance dynamic behavior respect to switching frequency. Both FITMOS and FDP047AN have noticeable on-resistance increment when switching frequency is above 500KHz. measurements are made for sinusoidal current drive of 1.2A peak

Figure VII.1.3-5 below show the measurement result of MOSFET on-resistance with respect to different peak dynamic peak current change di/dt at constant drive frequency. A sinusoidal wave voltage was used to drive the current through the MOSFET. The frequencies of the sinusoidal voltage are 300kHz, 500kHz and 800kHz. di/dt is controlled by the amplitude of the sinusoidal voltage. The resistance of the current sensing resistor should be independent of di/dt and frequency. The measurement result also matches our prediction. From the graphs, it also observes that the on-resistance of FDP047AN remains approximately constant across peak di/dt conditions at a given drive frequency. As observed before in Figure VII.1.2, the resistance does increase somewhat as frequency increases. By contrast, the FITMOS on-resistance increases about 8.8% when the peak di/dt changes from 0.2A/us to 1.6A/us at 300kHz and about 12.5% when the peak di/dt changes from 0.6A/us to 4A/us at 800kHz. (The achieved slew rate at given frequency is limited by the ability of the power amplifier to supply a sinusoidal waveform with low distortion). Thus, not only does FITMOS have a frequency dependence in the on-resistance, it also exhibits a di/dt dependence at a given frequency. This is inherently a nonlinear phenomenon, as the resistance is drive-level dependent.

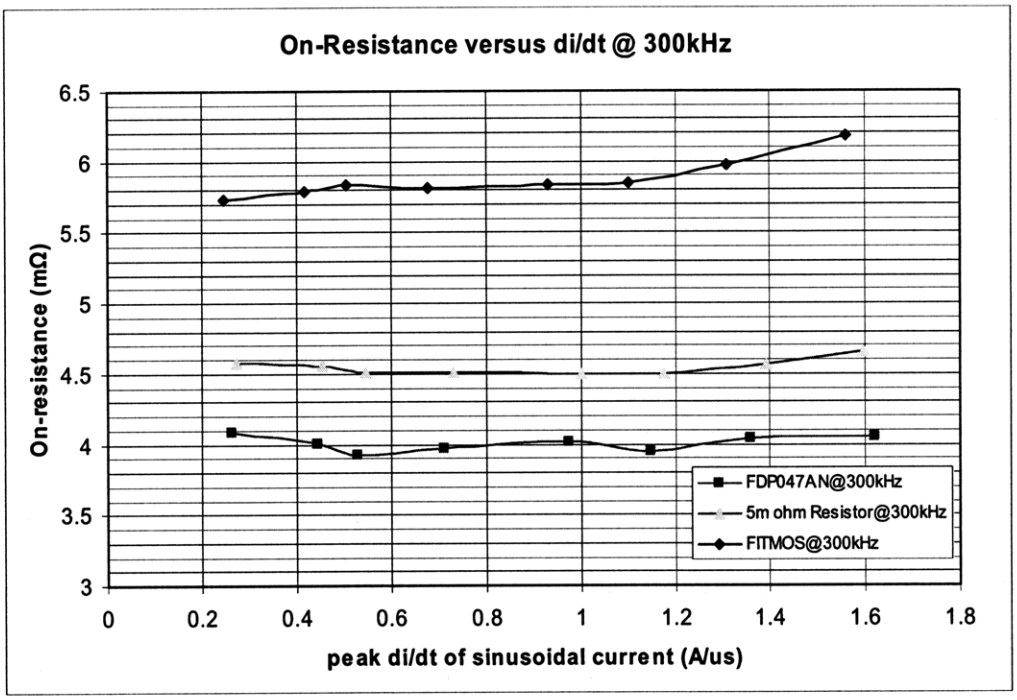


Figure VII.9.3 On-resistance dynamic behavior respect to di/dt at 300kHz.
The on-resistance in FITMOS increases 8.8% when peak di/dt is changed from 0.2A/us to 1.6A/us for sinusoidal drain-source currents at 300kHz.

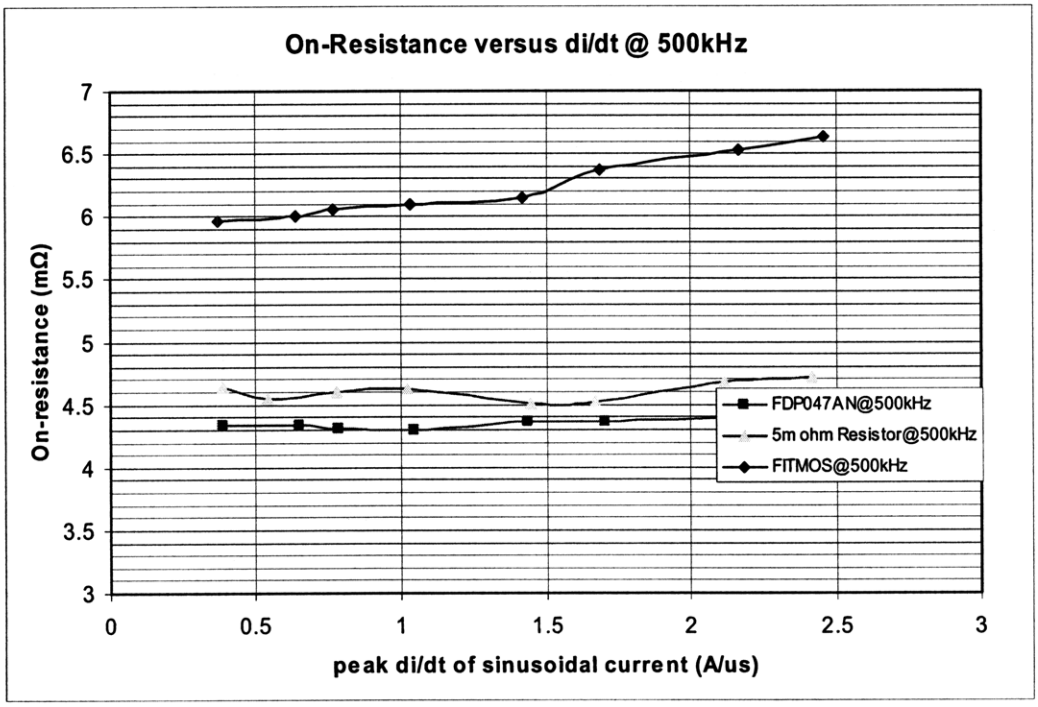


Figure VII.9.4 On-resistance dynamic behavior respect to di/dt at 500kHz.
The on-resistance in FITMOS increases 10% when peak di/dt is changed from 0.4A/us to 2.5A/us for sinusoidal drain-source currents at 500kHz.

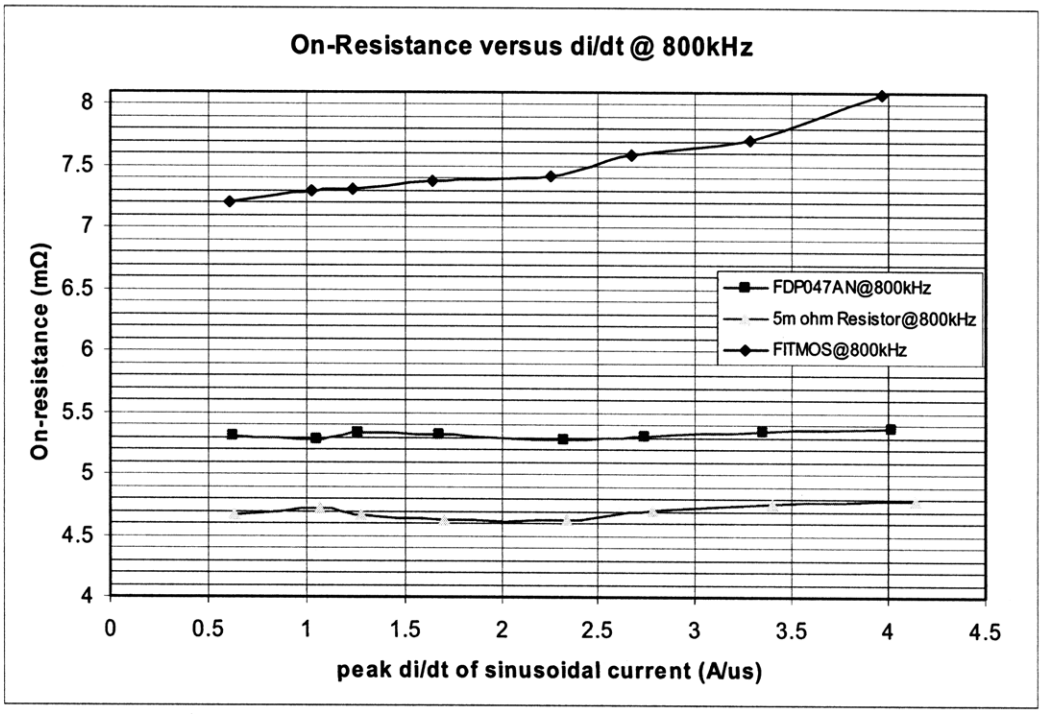


Figure VII.9.5 On-resistance dynamic behavior respect to di/dt at 800kHz. The on-resistance in FITMOS increases 12.5% when peak di/dt is changed from 0.6A/us to 4 A/us for sinusoidal drain-source currents at 800kHz.

Figure VII.1.6-8 below show the measurement results of MOSFET on-resistance response respect to different frequencies with the peak dynamic current change di/dt held constant. As expected, the resistance of a 5m Ω current sensing resistor holds approximately constant with different peak di/dt and frequencies. The on-resistance of FDP047AN increases as the frequency increases at constant peak di/dt, but its on-resistance remains the same with different peak di/dt. This result shows that the on-resistance of FDP047AN has frequency dependence, but its on-resistance is independent of peak di/dt. The on-resistance of FITMOS also increases as the current frequency increases at constant peak di/dt. But the result also illustrates an offset between different peak di/dt plots. This shows that the on-resistance of FITMOS is

not only frequency dependent, but also di/dt dependent.

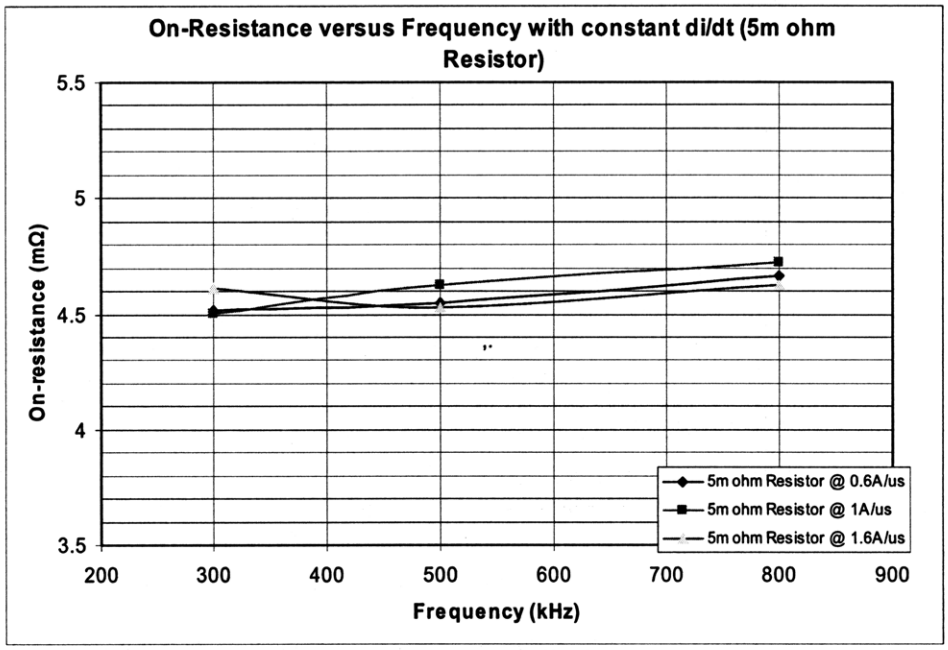


Figure VII.9.6 5m Ω resistance versus frequency with the peak di/dt held constant. Resistance of 5m Ω current sensing resistor is approximately constant with different frequencies and peak di/dt.

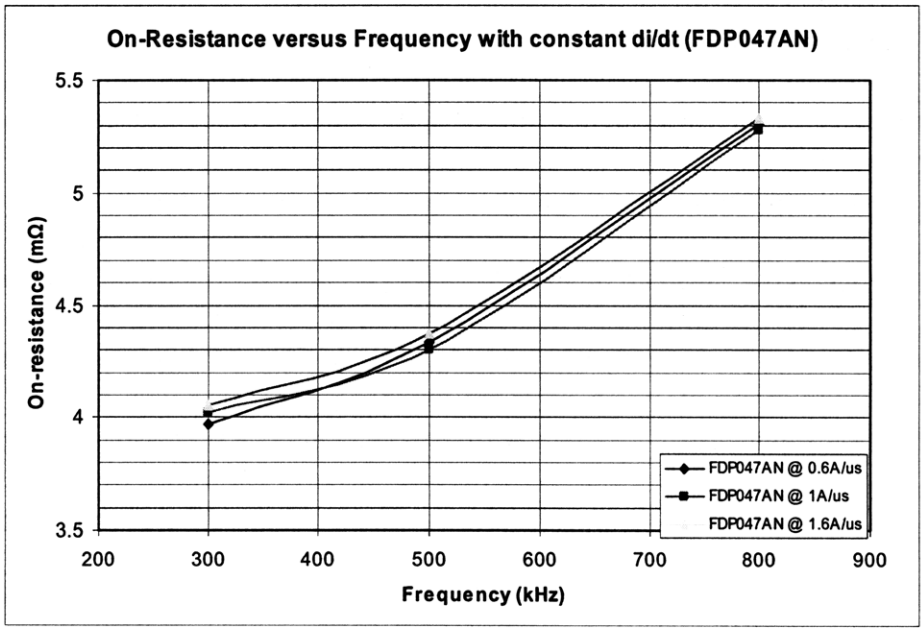


Figure VII.9.7 FDP047AN on-resistance versus frequency with the peak di/dt held constant. The on-resistance of FDP047AN increases as the frequency increases. But it is approximately the same with the same peak di/dt

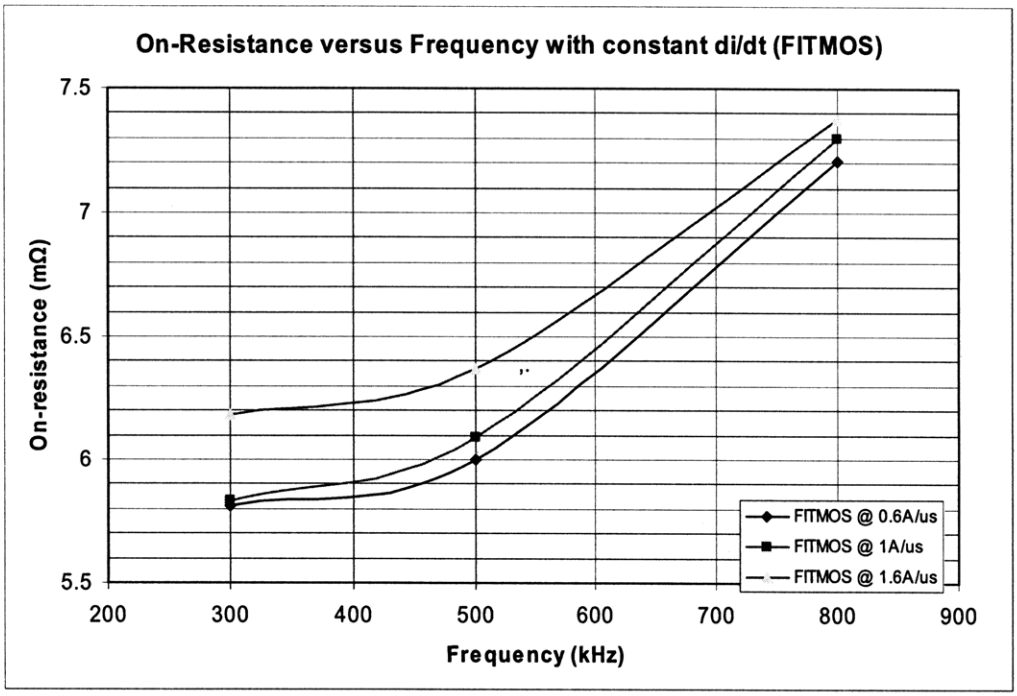


Figure VII.9.8 FITMOS on-resistance versus frequency with the peak di/dt held constant. The on-resistance of FITMOS increases as the frequency increases. But it also increases as the peak di/dt increases.

These results further verified our suspicion about the dynamic behavior of the on-resistance described in the previous chapter. The frequency and di/dt dependent on-resistance explains the performance degradation in the soft-switching mode converter due to the higher di/dt in the MOSFETs. Furthermore, this also explains the mismatch between the simulation and measurement since our SPICE model did not capture the dynamic behavior of the on-resistance. In the end, this experiment result draws out the conclusion in two major aspects: first of all, the DC on-resistance of FITMOS is about 20%-30% larger than FDP047AN; second, the on-resistance of FITMOS has a dependence on di/dt that is not apparent in the commercial MOSFET FDP047AN.

Chapter 8 Conclusions

In conclusion, we have characterized the FITMOS carefully and built a complete SPICE model for FITMOS. In the simulation, we are able to model the static on-resistance, I-V characteristics, parasitic capacitance and reverse recovery characteristic in the body diode accurately. Our SPICE model can predict the behavior and performance of the FITMOS in hard switching mode with good accuracy.

The distinctive feature of the FITMOS is the use of floating islands and trench gates with a thick oxide layer on the bottom. By spreading out the field intensity in the junction, this feature can increase the breakdown voltage, maintain low on-resistance and also reduce the gate capacitance. During our characterization, the FITMOS parameters show that FITMOS is one of the most competitive power MOSFETs in the 60 – 100V breakdown range. It also has very close performance to the best commercial power MOSFET we can find on the market.

From the mismatch between simulation and measurement, we are led to investigate the dynamic on-resistance of the FITMOS. Our experimental result shows the on-resistance dependence on peak current slew rate (di/dt) at constant drive frequency. This dynamic on-resistance behavior in FITMOS can be a source of degradation of the performance of the converter, which explains the missing loss mechanism in the simulation. As a result, the dynamic on-resistance characteristic should be considered while choosing the converter design.

Appendix

IX.10 Spice Model

IX.10.1 Spice model for the conventional power MOSFET FDP047AN08

*from the manufacture data sheet

PSPICE Electrical Model

.SUBCKT FDP047AN08A0 2 1 3 ; rev March 2002
CA 12 8 1.5e-9
CB 15 14 1.5e-9
CIN 6 8 6.4e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 82.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.81e-9
LSOURCE 3 7 4.63e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 9e-4
RGATE 9 20 1.36
RLDRAIN 2 5 10
RLGATE 1 9 48.1
RLSOURCE 3 7 46.3
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 2.3e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

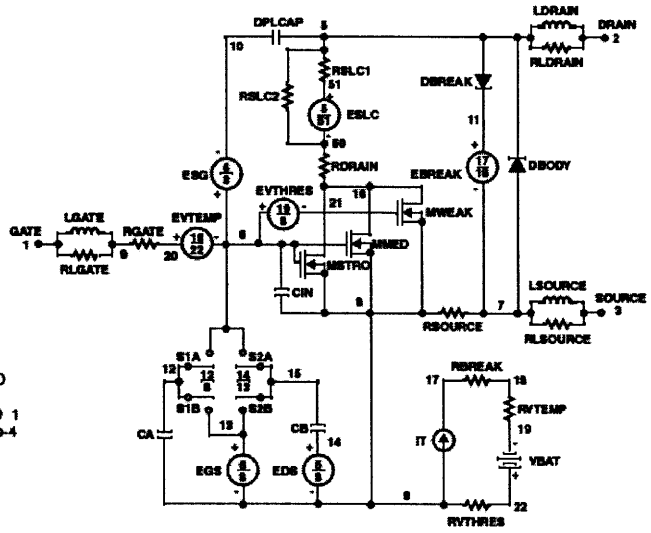
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*250),10))}

.MODEL DBODYMOD D (IS = 2.4e-11 N = 1.04 RS = 1.76e-3 TRS1 = 2.7e-3 TRS2 = 2e-7 XTI=3.9 CJO = 4.35e-9 TT = 1e-8 M = 5.4e-1)
.MODEL DBREAKMOD D (RS = 1.5e-1 TRS1 = 1e-3 TRS2 = -8.9e-6)
.MODEL DPLCAPMOD D (CJO = 1.35e-9 IS = 1e-30 N = 10 M = 0.53)
.MODEL MMEDMOD NMOS (VTO = 3.7 KP = 9 IS =1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.36)
.MODEL MSTROMOD NMOS (VTO = 4.4 KP = 250 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 3.05 KP = 0.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.36e1 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = -9e-7)
.MODEL RDRAINMOD RES (TC1 = 1.9e-2 TC2 = 4e-5)
.MODEL RSLCMOD RES (TC1 = 1.3e-3 TC2 = 1e-5)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -6e-3 TC2 = -1.9e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.4e-3 TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.0 VOFF= -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF= -4.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.0 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF= -1.0)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



FDP047AN08A0 / FDI047AN08A0 / FDH047AN08A0

IX.10.2 First Basic SPICE model for FITMOS

***This is our first basic Spice model for FITMOS. It does not include the gate resistance and has a**
***poor modeling for junction capacitance. In addition, this FITMOS model only can carry**
***positive Drain-Source current.**

```
.SUBCKT FITMOS 2 1 3
* 2 1 3 : Drain Gate Source
* Vgs = V(1, 3)
* Vds = V(2, 3)
.param Vt = '3.16'


*Voltage dependent current source
Gds 2 3 VALUE={If(V(1, 3)<=3.16, 0, MIN(If((V(1,3)-Vt)<=1.6734, 9.3495*PWR((V(1,3)-Vt),
4.5431), 78.053*Ln(V(1,3)-Vt)+56.781)*V(2,3),
+ 0.9172*PWR((V(1,3)-Vt), 4.3406)+0.6122*PWR((V(1,3)-Vt), 8.7186)*V(2,3)))}

*Gate Charge Components
Cgs 1 3 5n
Cdg 2 1 Q=IF(x<-9, 1.2n*x, MAX(0.35n, 0.5918n/PWR((1+x/10.11), 0.3124))*x)

Cds 2 3 Q=2.143n/PWR((1+x/5.67), 0.9774)*x

.ENDS
```

IX.10.3 Improved SPICE model for FITMOS

***This is our beta version of the FITMOS model. It includes the gate resistance in the model. And *the model also can carry both positive and negative current. In additional, a schottky diode is *added to the drain and source to reduce the reverse recovery effect.**

```
.SUBCKT FITMOS_beta 2 G 3
* 2 1 3 : Drain Gate Source
* Vgs = V(1, 3)
* Vds = V(2, 3)
* Gate resistance is from 1.05 to 1.6 ohm
.param Vt = '3.16' Rgate = '1.2'


*Gate Resistance
Rgate G 1 'Rgate'

*Body Drain Diode
Diode_body 3 2 Body_Diode


*Voltage dependent current source
Gds 2 3 VALUE={IF(V(2,3)<0, 0, If(V(1, 3)<=3.16, 0, MIN(If((V(1,3)-Vt)<=1.6734,
9.3495*PWR((V(1,3)-Vt), 4.5431), 78.053*Ln(V(1,3)-Vt)+56.781)*V(2,3),
+ 0.9172*PWR((V(1,3)-Vt), 4.3406)+0.6122*PWR((V(1,3)-Vt), 8.7186)*V(2,3)))))}


*Inverted Voltage dependent current source
Gds_inv 3 2 VALUE={IF(V(2,3)>0, 0, If(V(1, 3)<=3.16, 0, MIN(If((V(1,3)-Vt)<=1.6734,
9.3495*PWR((V(1,3)-Vt), 4.5431), 78.053*Ln(V(1,3)-Vt)+56.781)*V(3,2),
+ 0.9172*PWR((V(1,3)-Vt), 4.3406)+0.6122*PWR((V(1,3)-Vt), 8.7186)*V(3,2)))))}


*Gate Charge Components
Cgs 1 3 5n
Cdg 2 1 Q=IF(x<-9, 1.2n*x, MAX(0.35n, 0.5918n/PWR((1+x/10.11), 0.3124))*x)

Cds 2 3 Q=2.143n/PWR((1+x/5.67), 0.9774)*x

.ENDS

.model Body_Diode D(Is=19.4n Rs=.01 N=.733 Eg=.718 Xti=.535 Cjo=2.05n Vj=.4 M=.41 Iave=25
Vpk=45 type=Schottky)
```

IX.10.4 Improved completed SPICE model for FITMOS

***This is the improved completed Spice for FITMOS, which includes the parasitic inductance in**
***the drain, gate and source. It also includes the body diode model for the reverse recovery**
***characteristics. In additional, Cds and Cgd are modeled by the junction capacitance of a diode.**
***This can help the convergence of the simulation and improve the simulation speed.**

```
.SUBCKT FITMOS D G S
* 2 1 3 : Drain Gate Source
* Vgs = V(1, 3)
* Vds = V(2, 3)
* Gate resistance is from 0.7 to 1.5 ohm
.param Vt = '3.16' Rgate = '1.5' Kthermal = '0.85'
*Room Temp @ 25 degree C, Rgate=0.81 ohm
*                50W            100W          200W    400W
*Kthermal:    1.0-0.95       0.9-0.85      0.85    0.75

*Drain Source Inductance
Ldrain D 2 2n
Rldrain D 2 20

Lsource S 3 5.5n
Rlsource S 3 55

*Gate Resistance
Lgate G 4 4.8n
Rlgate G 4 48
Rgate 4 1 'Rgate'

*Body Drain Diode
Diode_body 3 2 Body_Diode

*Voltage dependent current source
Gds 2 3 VALUE={IF(V(2,3)<0, 0, If(V(1, 3)<=3.16, 0, MIN(If((V(1,3)-Vt)<=1.6734,
9.3495*PWR((V(1,3)-Vt), 4.5431), 78.053*Ln(V(1,3)-Vt)+56.781)*V(2,3)*Kthermal,
+ 0.9172*PWR((V(1,3)-Vt), 4.3406)+0.6122*PWR((V(1,3)-Vt), 8.7186)*V(2,3)*Kthermal))))}

*Inverted Voltage dependent current source
Gds_inv 3 2 VALUE={IF(V(2,3)>0, 0, If(V(1, 3)<=3.16, 0, MIN(If((V(1,3)-Vt)<=1.6734,
9.3495*PWR((V(1,3)-Vt), 4.5431), 78.053*Ln(V(1,3)-Vt)+56.781)*V(3,2)*Kthermal,
+ 0.9172*PWR((V(1,3)-Vt), 4.3406)+0.6122*PWR((V(1,3)-Vt), 8.7186)*V(3,2)*Kthermal))))}

*Gate Charge Components
```

```
Cgs 1 3 5n

Dcap 1 2 Dcap

.ENDS

.model Body_Diode D(IS = 2.4e-11 N = 1.0 RS = 15e-3 VJ = 5.67 CJO = 4.2e-9 TT = 1.24e-8 M =
9.774e-1)
.model Dcap D(IS = 1e-30 N = 10    VJ = 10.11 CJO = 0.5918e-9 M = 3.124e-1)
*TT=Ta/(ln(If-Ir)/-Ir)
```

IX.11 PCB Layout Masks and Schematics

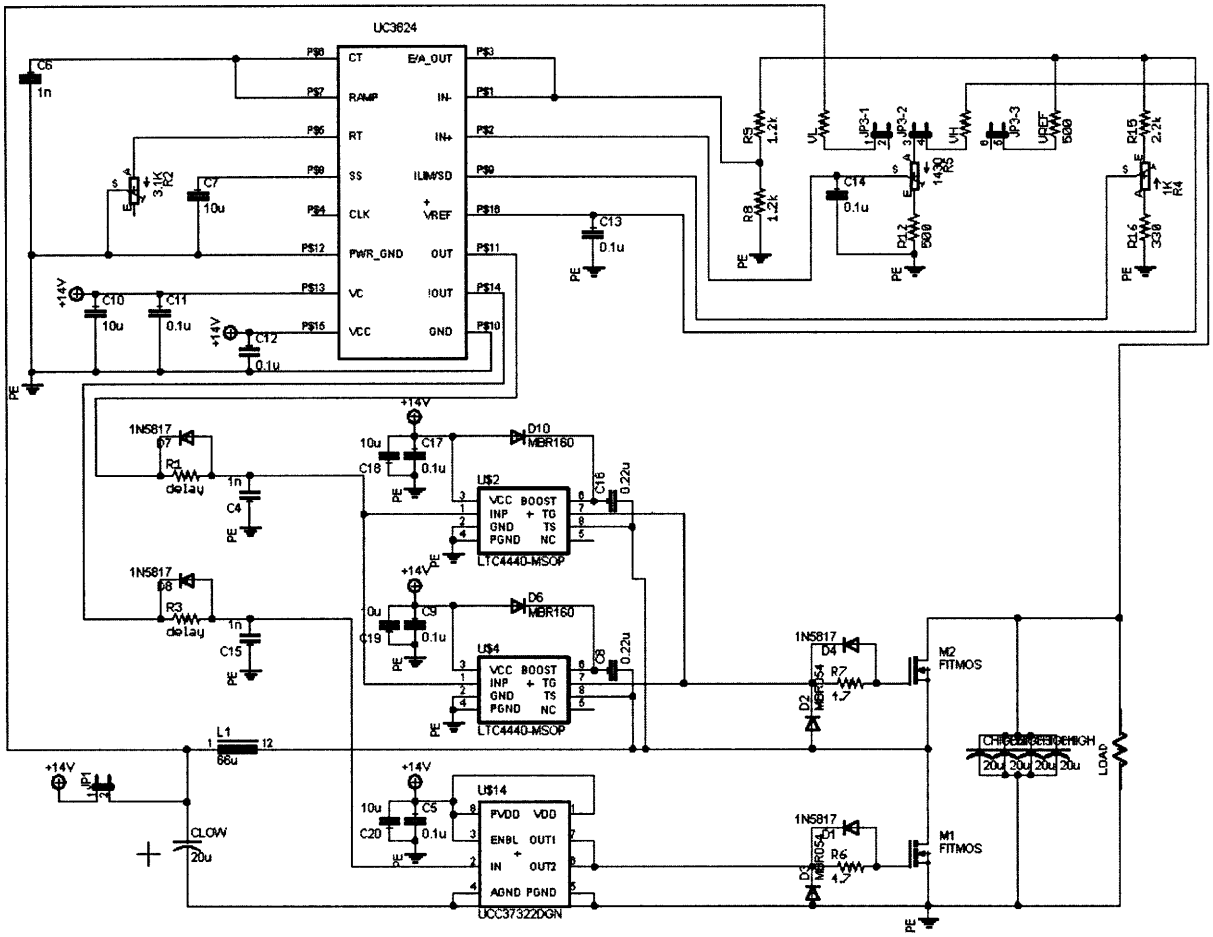


Figure IX.11.1 The DC-DC boost Converter schematic drawn in EAGLE.

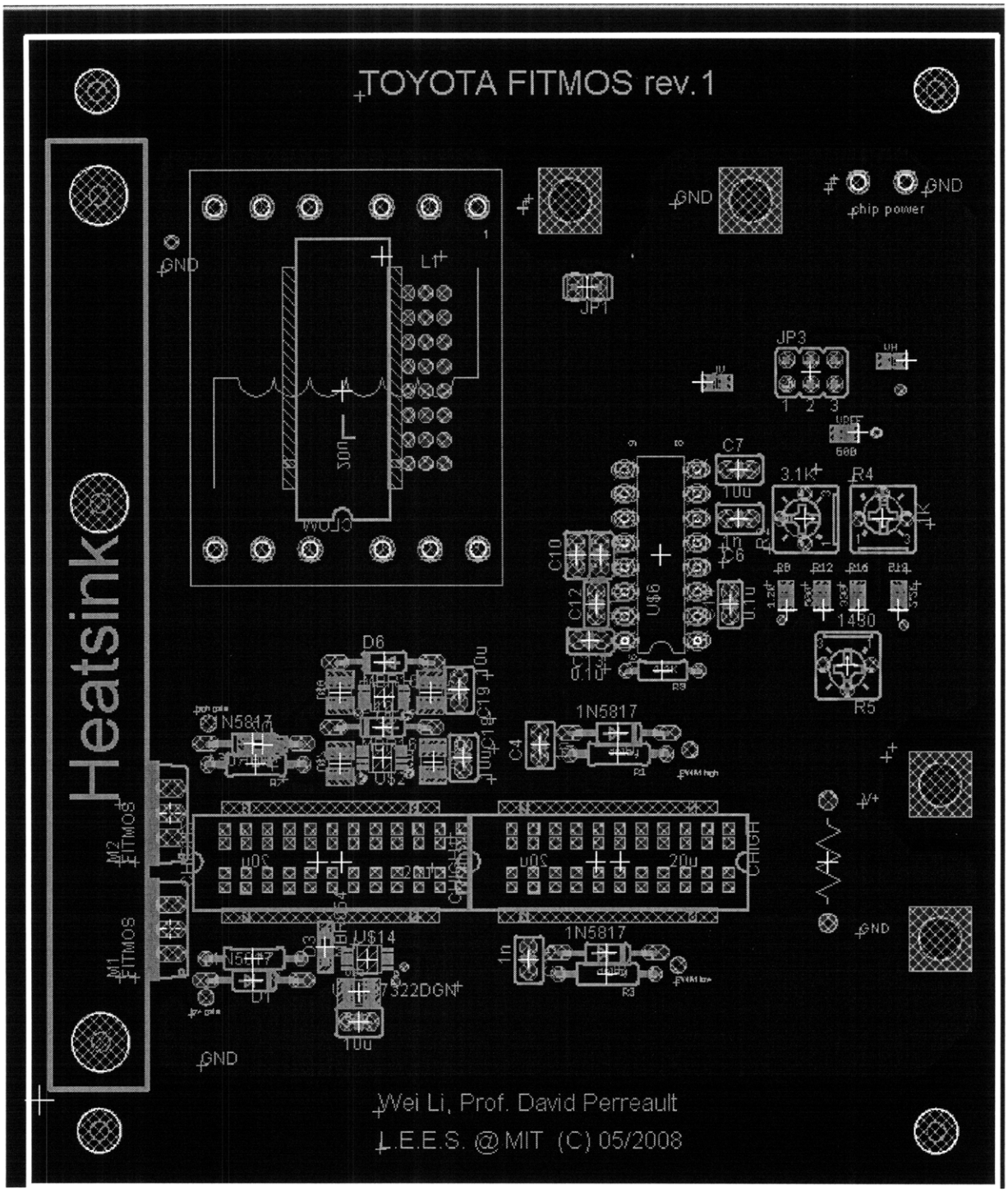


Figure IX.11.2 The first layer PCB layout drawn in EAGLE.

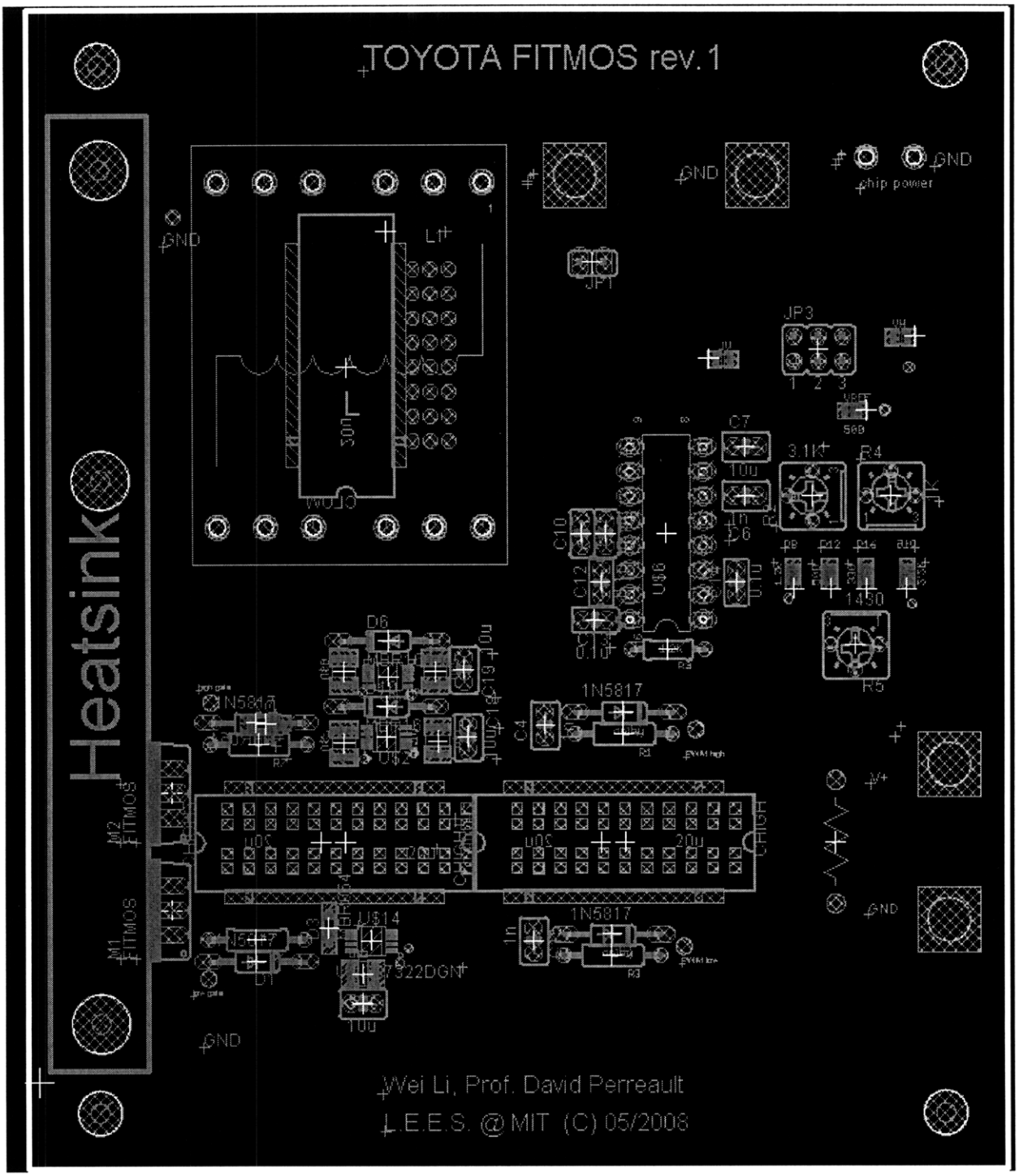


Figure IX.11.3 The second layer PCB layout drawn in EAGLE

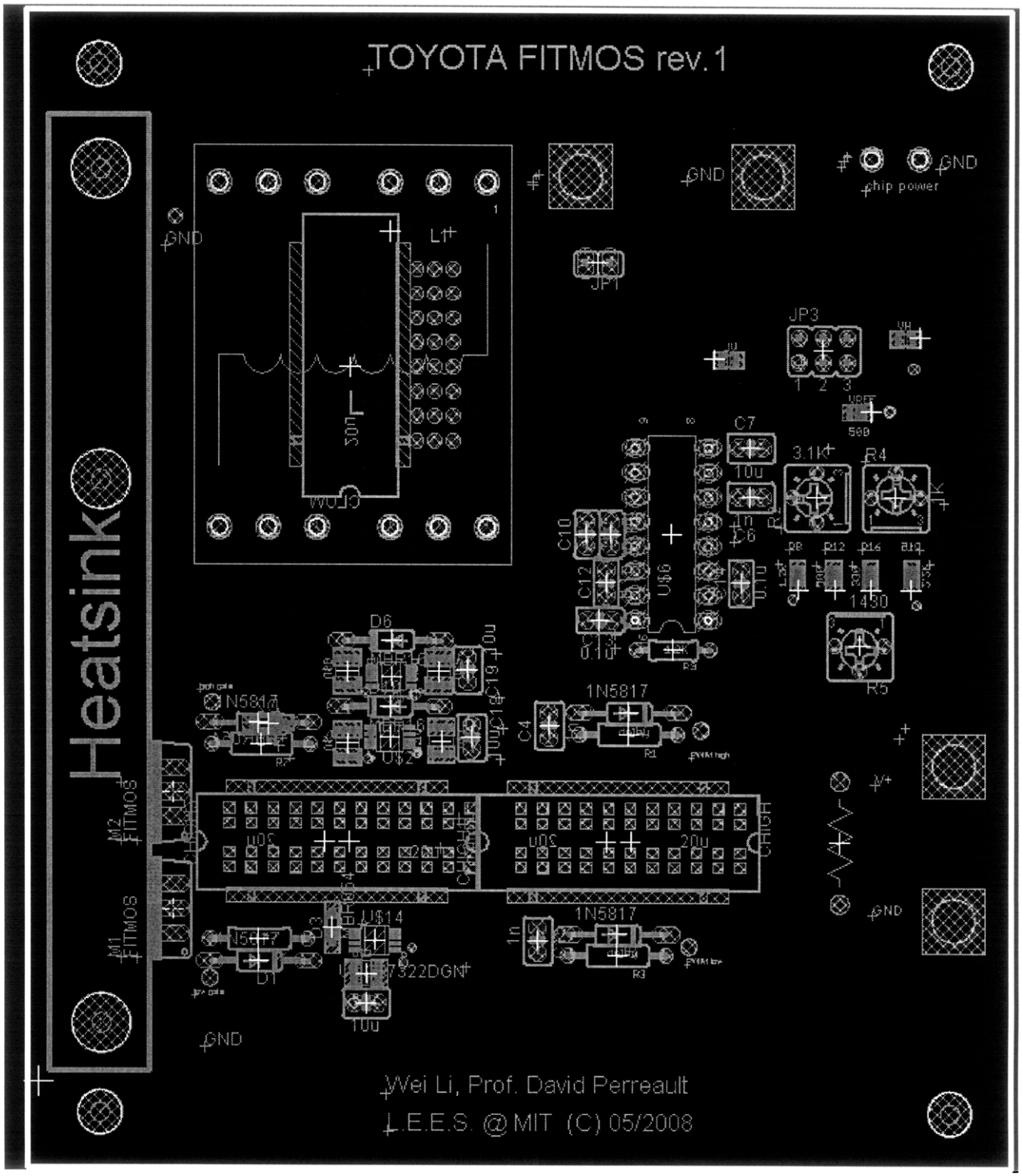


Figure IX.11.4 The third layer PCB layout drawn in EAGLE.

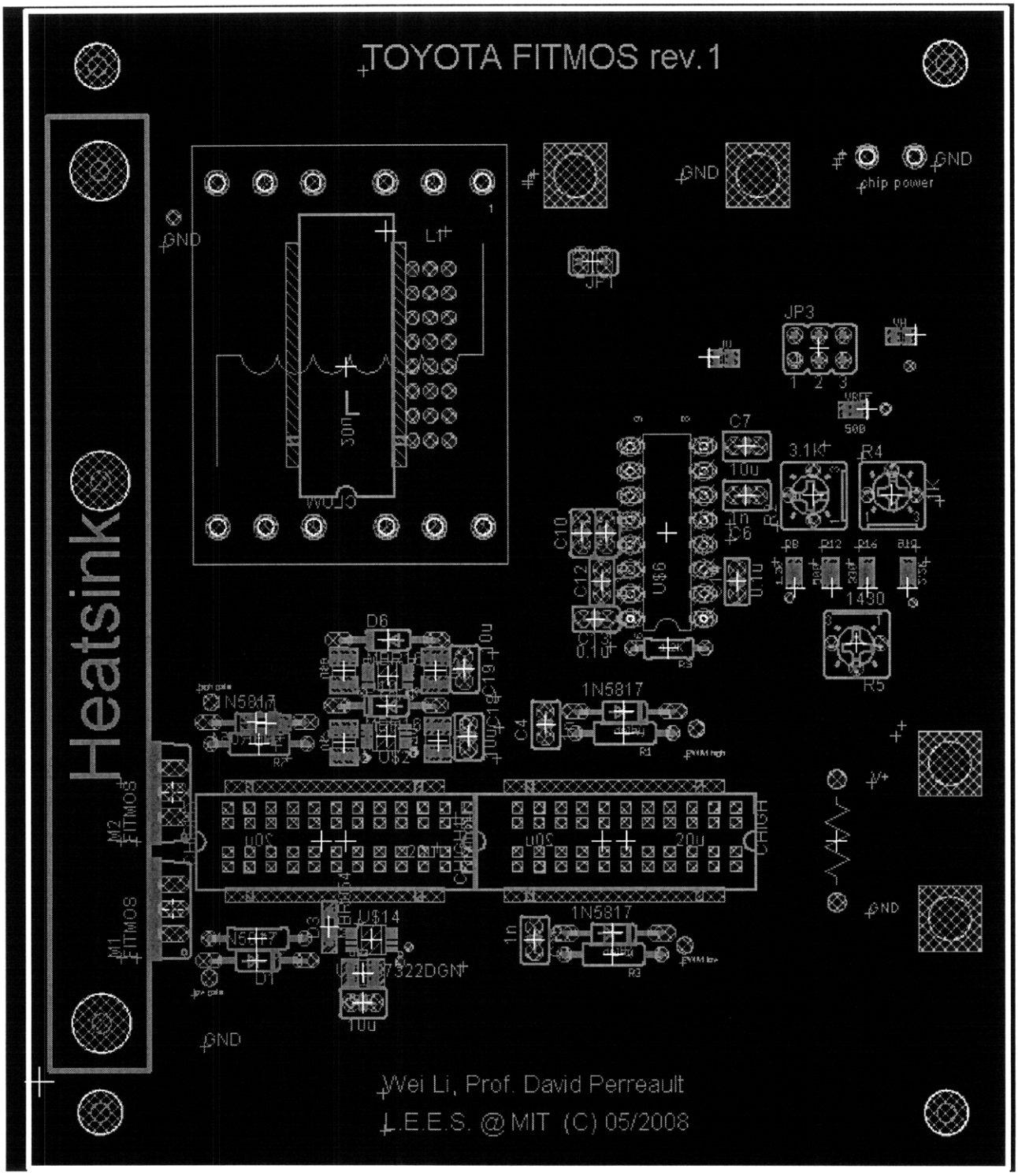


Figure IX.11.5 The fourth layer PCB layout drawn in EAGLE.

IX.12 Inductor Optimization Scripts

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%


% This script is used to design the input inductors
% for the boost rectifier.   Given the operational
% parameters of the boost inductor, the script generates
% feasible designs for the inductor based on core and
% wire data in the script BRLDAT.   The script tries to
% design an inductor based on each core in the data set
% and retains those which are feasible.   For each design
% the script calculates core losses and winding losses
% ( including losses due to skin and proximity effect)
% based on fitted empirical data and theoretical models.
% The loss data ( and expected core temperature rise)
% are retained with the design parameters for all
% feasible designs, and are stored in the specified
% diary file.

% Set up parameters for this test
% Input voltage for the boost converter is 14V, and output is 42V.
vo = 42;
Vin = 14;
maxdfrac = 0.9; % fraction of max theoretical duty cycle
outfname = 'ldes100.asc'; % output file name
Freq = 500e3;
Tsw = 1/Freq;      % fsw about 500 kHz
L = 0.7e-06;         % L is specified in Henries
ppc = 1000;          % many points per cycle for accuracy
dt = Tsw/ppc;
Pomax = 100; % command duty cycle for this power

   % we want to specify the proper d to achieve Vout for the specified
   % Vin.
d = (vo-Vin)/vo;
ton = d*Tsw
if d > 1.001*maxdfrac,
   error(' Duty cycle commanded exceeds maximum specified value.');
end;
```

```
% Simulate the converter and calculate the inductor current.
% The result is then used to calculate the core and winding losses,
% as well as the energy storage required.

[i_lcyc, issmag, issphi, ipk_AC] = brsiss(L,vo,Vin,Tsw,ton,ppc,Pomax);
%%%%%%save 'ilwave2.mat' i_lcyc issmag issphi
%%%%%%load 'ilwave2.mat';
i_lrms = sqrt(i_lcyc*i_lcyc'/length(i_lcyc));
ipk = max(i_lcyc);

% Run the script which sets up core and wire data
brldat;

% Save program responses to the output file.
diary(outfname);
disp(['L = ',num2str(L)]);
% Loop through available cores and synthesize
% inductor designs.
for core = 1:numcores,
  designok = 1; % assume this core design works
                % Calc number of turns needed on this
                % core to get desired L value.
  N = round(1000*sqrt(1000*L/AL(core)));
                % Calculate B at peak current in gauss
                % for this N.
  Bpk = 0.1*AL(core)*N*ipk/Ac(core);
                % If required peak B is more than 3000
                % gauss, then we are too close to the
                % Bsat = 3300 gauss, and the design is
                % not acceptable
  if Bpk > 3000,
    designok = 0;   % design is not ok
    disp([corename(core,:),' rejected: Bpk = ',num2str(Bpk),' gauss.']);
  end;
                % If design is still ok, try to find a
                % wire size which fits on the core.
                % Select largest wire which fits.
                % This may not be at all optimal.
  guage = minguage-1;
  while designok == 1,
    guage = guage + 1; % check next guage
    if guage > maxguage,
      designok = 0 % acceptable wire guage not found,
```

```
                    % this design is not acceptable
    disp([corename(core,:),' rejected: no wire fits.']);
  end;
  winarea = N/tpsqin(guage);
  if winarea < wa(core),
    break; % This wire guage is ok,
            % break out of loop
  end;
end; % while designok == 1;

            % If design is still ok, check to make
            % sure that current in wire is at an
            % acceptable level.  Reject the design
            % if not.  We require the rms current
            % density to be less than 3000 A/in^2.
if designok == 1,
  Jwire = i_lrms/(pi*(dwire(guage)/2)^2);
  if Jwire >= 3000,
    designok = 0;
    disp([corename(core,:),' rejected: Jwire = ',num2str(Jwire),' A/in^2.']);
  end; % if Jwire
end; % if designok

            % If the design is still ok, calculate
            % the inductor losses.  These losses
            % include the core losses and the
            % winding losses.
if designok == 1,
            % Calculate core losses.  This eqn. is
            % a fit of empirical data.  Pcore is in
            % watts, fsw is in kHz, B is in gauss,
            % Vc is in cm^3.  This is a conservative
            % estimate based on the peak flux swing
            % encountered in the cycle.
 % Pcore = 9.16e-13*(1e-03/Tsw)^1.231*(Bpk/2)^2.793*Vc(core);
 Bpk_AC = AL(core)*N*ipk_AC/Ac(core)*1e-5; % in Tesla
  Pcore = 2.1e-5*(Freq)^1.8*(Bpk_AC/2)^2.5*Vc(core)*1e-3;
            % Calculate winding losses using the approach
            % of Carsten (PCIM Nov. 1986, pp 34 - 46).  We
            % calculate an equivalent resistance at each freq
            % which accounts for both skin & proxim effect.
            % This is used to calc total winding loss from
            % the spectrum of the inductor current.
```

```
            % dc resistance of the winding = resistance per
            % inch x inches per turn x # of turns
  Rdc = Rperl(guage)*lpt(core)*N;
            % equiv square-wire thickness of conductor (Carsten)
  heff = (pi/4)^0.75*dwire(guage)^1.5/sqrt(dinsu(guage));
            % approx number of wiring layers needed
            % assume 90% horizontal packing
  m = round(N/(0.9*ww(core)/dinsu(guage)));
            % each frequency component in the inductor current is
            % a multiple of the line frequency.  We will calculate
            % loss components at each multiple of the line freq:
            % i(t) = sum over k of {issmag(k)*cos((k-1)*w*t+issphi(k))}.
            % we have data for 1 <= k <= ppc.  We will
            % calculate Rmult, which is the ratio of the effective
            % ac resistance to the dc resistance at each k value
            % up to a predefined switching frequency multiple fswmult.
  fswmult = 50;
  k = 1:fswmult-1;
            % Calc skin depth at each frequency.
            % This actually varies vs. T, wire
            % composition, etc.
  skind = 2.6*ones(size(k))./sqrt((k)*Freq);
            % Using Carsten's calculations:
  Xk = heff*ones(size(skind))./skind; % eff. wire thickness in skin depths
  Xcplx = Xk + i*Xk;
  M1 = real(Xcplx.*(cosh(Xcplx)./sinh(Xcplx)));
  D1 = real(2*Xcplx.*(sinh(0.5*Xcplx)./cosh(0.5*Xcplx)));
  Rmult = M1 + (m^2-1)*D1/3;
  Rmult = [1,Rmult]; % include dc term
  Pwind = sum(issmag(1:fswmult) .* issmag(1:fswmult) .* ...
          (Rdc*Rmult));
end; % if designok = 1 calc inductor losses

            % if design is ok, calculate core temperature
            % rise, and reject design if it is too high.
            % we define too high as >= 50 deg Celcius.
if designok == 1,
  deltaT = Rth(core)*(Pwind+Pcore);
  if deltaT > 80,
    designok = 0;
    disp([corename(core,:),' rejected: delta T = ',num2str(deltaT),' deg C.']);
  end;
end;
```

```
        % If the design is ok, display the data
  if designok == 1,
     disp('                    ');
     disp([corename(core,:),' :']);
     disp(['N = ',num2str(N),' of guage ',num2str(guage)]);
     disp(['Bpk ',num2str(Bpk)]);
     disp(['Jwire = ',num2str(Jwire),' A/in^2']);
     disp(['Pcore = ',num2str(Pcore),' Watts']);
     disp(['Pwind = ',num2str(Pwind),' Watts']);
     disp(['Ptot = ',num2str(Pcore+Pwind),' Watts']);
     disp(['delta T = ',num2str(deltaT),' deg C']);
     disp('----------------------------');
  end; % if designok = 1
end; % for core
diary off;
% we are finished.



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%


function [i_lcyc, issmag, issphi, ipk_AC] = brsiss(L,vo,Vin,Tsw,ton,ppc,Pomax);
%
% BRSISS       Simulation-based calculation of the input switching spectrum
%              The magnitudes and phases of the harmonics of the periodic
%              waveform are calculated using an fft approach.   i(t) = sum over k of
%              {issmag(k)*cos((k-1)*w*t+issphi(k))}.   The program calculates
%              for 1<= k <= ppc*pi/(w*Tsw)
%
%    [i_lcyc, issmag, issphi] = brsiss(L,vo,Vin,Tsw,ton,ppc,Pomax);
%       i_lcyc       input current (time) waveform of boost
%                    converters over a full cycle .
%       issmag       Vector of magnitudes of the specified freqs., in amps.
%                    The kth element is for frequency (k-1)*w/(2*pi) and
%                    there are N=ppc*pi/(w*Tsw) points.
%       issphi       Vector of phases of the specified frequencies, in rad/sec.
%                    The kth element is for frequency (k-1)*w/(2*pi), and
%                    there are N=ppc*pi/(w*Tsw) points.
%       L            Input boost inductor value, Henries.
%       vo           Output voltage, Volts.
%       Vin          Input voltage, Volts.
%       Tsw          Switching period, sec.   The switching period should be
```

```
%                    chosen so there is an integral number of cycles in pi/6
%                    of the line period.
%       ton          Switch on time, sec.
%       ppc          Number of points to use per switching cycle.   This number
%                    must be large enough to allow accurate DFT calculation of
%                    the desired switching harmonics (say a factor of 10 over
%                    the maximum switching harmonic number to compute).   Also,
%                    ppc must be an integer multiple of Nint.
%       harmnums     Vector containing list of harmonic numbers to compute.


Idc = Pomax / Vin
 % Assume the low side device turned on first.
di_on = Vin / L   % when the low side device is on, the voltage across the
                  % inductor is Vin
di_off = (Vin-vo) / L   % when then high side device is on, the voltage
                        % across the inductor is Vin-Vout
dt = Tsw/ppc;    % time step between points

for index = 1:ppc,
    if (index*dt < ton)
        ir_lcyc(index) = index*dt*di_on;
        ipk_AC = ir_lcyc(index);
    else
        ir_lcyc(index) = ipk_AC+(index*dt-ton)*di_off;
    end;
end;
%i_lcyc = ones(1,ppc)*Idc;
i_lcyc = ir_lcyc+(Idc-ipk_AC/2);

                          % generate time vector over a switching cycle
t_lcyc = 0:(Tsw/ppc):Tsw;
                          % calculate inductor current harmonics
                          % component magnitudes using an FFT approach
IL = fft(i_lcyc);
issmag = abs(IL(1:ppc/2))/ppc;
                      % include time shift to get correct phase
issphi = angle(IL(1:ppc/2));
                       % we are done



%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%

% This script BRLdat.m defines variables containing data
% for boost-rectifer inductor design.  Params for Phillips
% (Ferroxcube) 3F3 material ferrite square cores are
% defined, as is some wire table data for various guages.
%
% The core data is for Phillips ferrite square cores, sizes
% RM8 to RM14.  These cores seem to be a good choice for the
% application.  The 3F3 material is specified for its low
% loss characteristics.  The data sets are as follows:
%    Quantity                  Var name          units
%    Number of cores           numcores          numerical
%    Core name                 corename          text
%    AL (mH@1000 turns)        AL                numerical
%    eff. core area            Ac                cm^2
%    eff. core volume          Vc                cm^3
%    core thermal Resist.      Rth               deg C / W
%    core winding area         wa                in^2
%    core winding width        ww                in
%    avg. length per turn      lpt               in
%
% The wire data is taken directly from the phillips ferrite
% components data book and the New England Wire Co. data
% book.  The data for a given guage is
% indexed by the guage number, so dwire(12) is the diameter
% of 12 guage wire.  The wire data specified is as follows:
%    Quantity                  Var name          units
%    min wire guage            minguage          numeric
%    max wire guage            maxguage          numeric
%    bare wire diameter        dwire             in
%    insulated diameter        dinsu             in
%    Turns / in^2              tpsqin            numeric
%    Resistance / length       Rperl             Ohms / in.
%

%%%%%%%%%%%%%%%%%%%% Core data, Phillips 3F3 square cores RM6 - RM14

% Core names
corename = [...
'RM6SPA63   '; 'RM6SPA100 '; 'RM6SPA160 '; 'RM6SPA250 '; 'RM6SPA315 '; ...
'RM8PA160   '; 'RM8PA250   '; 'RM8PA315   '; 'RM8PA400   '; ...
'RM10PA160 '; 'RM10PA250 '; 'RM10PA315 '; 'RM10PA400 '; 'RM10PA630 '; ...
'RM12PA160 '; 'RM12PA250 '; 'RM12PA315 '; 'RM12PA400 '; ...
```

```
'RM14PA250 ' ; 'RM14PA315 ' ; 'RM14PA400 ' ; 'RM14PA630 ' ; 'RM14PA1000' ];

numcores = length(corename);

% AL is mH for 1000 Turns
AL = [   63 ; 100 ; 160 ; 250 ; 315 ; ...
         160 ; 250 ; 315 ; 400 ; ...
         160 ; 250 ; 315 ; 400 ; 630 ; ...
         160 ; 250 ; 315 ; 400 ; ...
         250 ; 315 ; 400 ; 630 ; 1000 ];

% Ac is effective core area in cm^2
Ac = [ 0.37 ; 0.37 ; 0.37 ; 0.37 ; 0.37 ; ...
       0.52 ; 0.52 ; 0.52 ; 0.52 ; ...
       0.83 ; 0.83 ; 0.83 ; 0.83 ; 0.83 ; ...
       1.46 ; 1.46 ; 1.46 ; 1.46 ; ...
       1.98 ; 1.98 ; 1.98 ; 1.98 ; 1.98 ];

% Vc is effective core volume in cm^3
Vc = [   1.09 ;   1.09 ;   1.09 ;   1.09 ;   1.09 ; ...
         1.85 ;   1.85 ;   1.85 ;   1.85 ; ...
         3.47 ;   3.47 ;   3.47 ;   3.47 ;   3.47 ; ...
         8.34 ;   8.34 ;   8.34 ;   8.34 ; ...
        13.90 ; 13.90 ; 13.90 ; 13.90 ; 13.90 ];

% Rth is core thermal resistance in deg. C / W
Rth = [ 60 ; 60 ; 60 ; 60 ; 60; ...
         38 ; 38 ; 38 ; 38 ; ...
         30 ; 30 ; 30 ; 30 ; 30 ; ...
         23 ; 23 ; 23 ; 23 ; ...
         19 ; 19 ; 19 ; 19 ; 19 ];

% wa is core (bobbin) winding area in square inches
wa = [ 0.024 ; 0.024 ; 0.024 ; 0.024 ; 0.024 ; ...
       0.048 ; 0.048 ; 0.048 ; 0.048 ; ...
       0.066 ; 0.066 ; 0.066 ; 0.066 ; 0.066 ; ...
       0.120 ; 0.120 ; 0.120 ; 0.120 ; ...
       0.170 ; 0.170 ; 0.170 ; 0.170 ; 0.170 ];

% ww is core (bobbin) winding width in inches
ww = [ 0.254 ; 0.254 ; 0.254 ; 0.254 ; 0.254 ; ...
       0.365 ; 0.365 ; 0.365 ; 0.365 ; ...
       0.409 ; 0.409 ; 0.409 ; 0.409 ; 0.409 ; ...
       0.567 ; 0.567 ; 0.567 ; 0.567 ; ...
```

```
        0.726 ; 0.726 ; 0.726 ; 0.726 ; 0.726 ];

% lpt is average wire length per turn in inches
lpt = [ 1.18 ; 1.18 ; 1.18 ; 1.18 ; 1.18 ; ...
          1.65 ; 1.65 ; 1.65 ; 1.65 ; ...
          2.00 ; 2.00 ; 2.00 ; 2.00 ; 2.00 ; ...
          2.40 ; 2.40 ; 2.40 ; 2.40 ; ...
          2.80 ; 2.80 ; 2.80 ; 2.80 ; 2.80 ];

%%%%%%%%%%%%%% Wire Data, vectors indexed by guage number (10-30 ga);

% no data for guages 1 - 10;
gablank = [NaN ; NaN ; NaN ; NaN ; NaN ; NaN ; NaN ; NaN ; NaN ];
maxguage = 30;
minguage = 10;

% bare wire diameter in inches
dwire = [ gablank ; ...
            0.1019 ; 0.0907 ; 0.0808 ; 0.0719 ; 0.0641 ; 0.0571 ; ...
            0.0508 ; 0.0453 ; 0.0403 ; 0.0359 ; 0.0320 ; 0.0285 ; ...
            0.0254 ; 0.0226 ; 0.0201 ; 0.0179 ; 0.0159 ; 0.0142 ; ...
            0.0126 ; 0.0113 ; 0.0100 ];

% (Nominal) heavy film insulated wire diameter in inches.
% Taken from New England Wire Co. Data book.
dinsu = [ gablank ; ...
            0.1056 ; 0.0938 ; 0.0837 ; 0.0749 ; 0.0675 ; 0.0602 ; ...
            0.0539 ; 0.0482 ; 0.0431 ; 0.0386 ; 0.0346 ; 0.0309 ; ...
            0.0276 ; 0.0249 ; 0.0223 ; 0.0199 ; 0.0178 ; 0.0161 ; ...
            0.0144 ; 0.0130 ; 0.0116 ];

% turns per square inch (heavy film insulated wire, machine wound)
% Taken from Phillips ferrite core data book.   This is more
% conservative than the New England Wire Co. data book estimate.
tpsqin = [ gablank ; ...
             89 ;   112 ;   140 ;   176 ;   221 ;   259 ;   327 ; ...
            407 ;   509 ;   634 ;   794 ;   989 ; 1238 ; 1532 ; ...
           1893 ; 2351 ; 2932 ; 3711 ; 4581 ; 5621 ; 7060 ];

% resistance per length in Ohms / inch (from Phillips data book)
Rperl = 1.0e-05 * [ gablank ; ...
                        8.333 ;   10.500 ;   13.167 ;   16.667 ; ...
                       21.083 ;   26.500 ;   33.500 ;   42.167 ; ...
                       53.250 ;   67.083 ;   84.167 ; 106.667 ; ...
```

```
                    135.000 ; 169.167 ; 214.167 ; 270.000 ; ...
                    341.667 ; 428.333 ; 544.167 ; 676.667 ; ...
                    866.667 ];
% The previous values are at 20 deg C.    We should scale them
% for operation at 100 deg C.
Rperl = Rperl*(1 + 0.004*(100-20));
```

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