n-XYTER - A CMOS Read-Out ASIC for a new Generation of High Rate Multichannel Counting Mode Neutron Detectors

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Abstract

For a new generation of 2-D neutron detectors developed in the framework of the EU NMI3 project DETNI [1], the 128-channel frontend chip n-XYTER has been designed. To facilitate the reconstruction of single neutron incidence points, the chip has to provide a spatial coordinate (represented by the channel number), as well as time stamp and amplitude information to match the data of x- and y-coordinates. While the random nature of the input signals calls for self-triggered operation of the chip, on-chip derandomisation and sparsification is required to exploit the enormous rate capability of these detectors ($\geq 4 \times 10^6 \mathrm{cm}^{-2}\mathrm{s}^{-1}$). The chosen architecture implements a preamplifier driving two shapers with different time constants per channel. The faster shaper drives a single-pulse discriminator with subsequent time-walk compensation. The output of this circuit is used to latch a 14-bit time stamp with a ≤ 2 ns resolution and to enable a peak detector circuit fed by the slower shaper branch. The analogue output of the peak detector as well as the time stamp are stored in a 4-stage FIFO for derandomisation. The readout of these FIFOs is accomplished by a token-ring based multiplexer working at 32 MHz, which accounts for further derandomisation, sparsification and dynamic bandwidth distribution. The chip was submitted for manufacturing in AMS's C35B4M3 0.35µm CMOS technology in June 2006.

I. Neutron Physics' Experiments

High energy physics usually relies on accelerators as particle sources. These machines also provide a suitable time reference (the so-called bunch clock) which is used to disentangle the signals resulting from different particle collisions. Thus position reconstruction can be easily realised by deriving a coincidence period from the accelerator's timing.

In contrast, neutron physics' experiments, as sketched in fig. 1, use (at least on the time scale of interest) continuous sources like nuclear reactors. In turn the appearance of scattered neutrons is Poissonian distributed and not related to any external signal. As a consequence, the synchronous readout of such a detector with an external clock would require an enormous readout bandwidth. Alternatively a self-triggered system can be employed, which would allow for derandomisation and sparsification already in the front-end electronics.

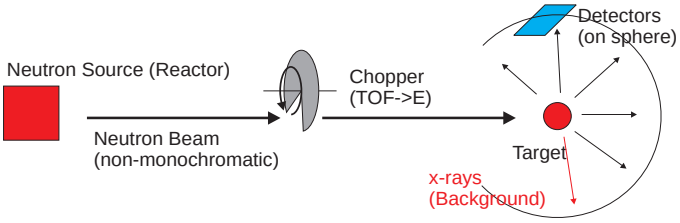

Figure 1: Strongly simplified layout of a typical neutron scattering experiment. The chopper wheel is used for energy determination, based on a slow (µs) TOF measurement.

II. The DETNI Detectors

Targeted for the next generation of neutron sources, in the framework of the EU FP-6 NMI3 project DETNI a new generation of neutron detectors for imaging and time-of-flight applications is being developed. In particular these detectors are:

- Gd-Si-MSD, a double-sided Silicon-Microstrip detector with a solid ^{157}Gadolinium converter.
- CASCADE, a gaseous detector using multiple GEM[1] foils coated with a ^{10}Boron converter.
- Gd/CsI MSGC, a hybrid MSGC employing a solid ^{157}Gadolinium converter.

Any of these detectors is characterised by a high number of readout channels per coordinate (up to 640 × 640 for the Si-MSD) and a very high event rate, unprecedented in single-event counting 2-D neutron detectors [2].

[1] Gas Electron Multiplier

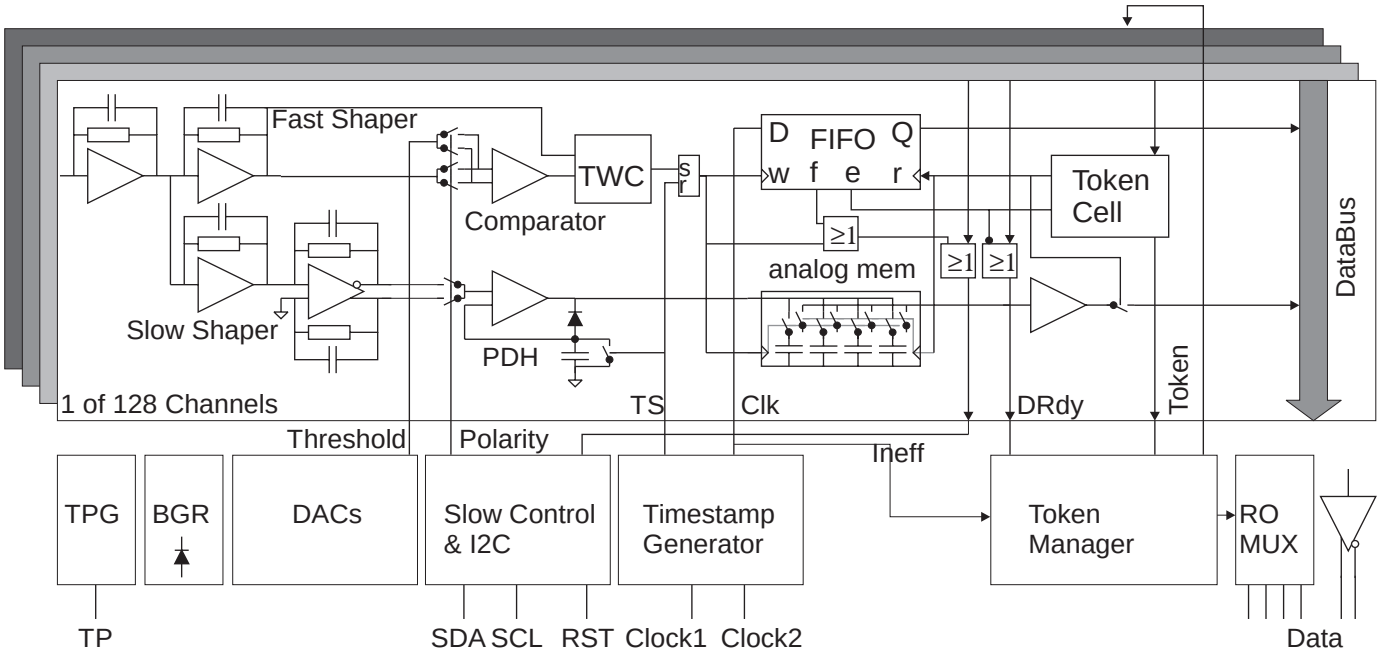

Figure 2: Block schematic of the n-XYTER 1.0 chip. The top part shows one of the 128 channels.

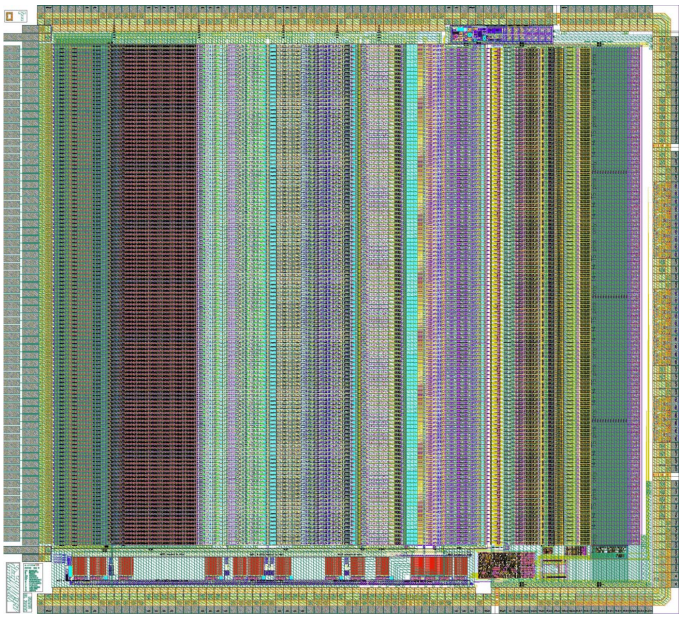

Figure 3: Layout of the 8.0 mm × 8.8 mm n-XYTER 1.0 chip.

III. The n-XYTER 1.0 Chip

To read out the CASCADE and Si-MSD detectors with event rates up to 100 MHz at a 10 % dead time loss, the n-XYTER[2] 1.0 chip has been developed. It integrates 128 channels. To cope with the high-rate statistical input signals, the front-end part of the chip uses an asynchronous, data-driven architecture, which relies on time stamp latching triggered by a time-walk compensated discriminator. The back-end part of the chip is clock-synchronous and accomplishes the derandomisation, sparsification and bandwidth-distribution tasks to limit the dead-time loss. A simplified schematic is shown in fig. 2. After a front-end only test chip[3], the full-scale 128 channel n-XYTER 1.0 chip has been submitted in June 2006. The chosen process, AMS C35B4M3 (0.35 µm) CMOS, includes linear polysilicon capacitors, 4 metal layers, a thick, low impedance top metal layer and MIMCAPs[4]. The latter two features have been extensively used for power supply filtering, implemented via low-impedance connections and local blocking capacitors. The layout of the 8.0 mm × 8.8 mm chip is shown in fig. 3. The following description will follow the chip's signal path:

A. Front End

A charge sensitive preamplifier, constructed around a folded cascode circuit forms the input stage. For its superior noise performance, an NMOS input transistor has been chosen. Unlike conventional readout chips, the signal path is split into two branches after the preamplifier:

- A fast CR – RC shaper, driving the timing-critical path performing the time measurement.
- A slow CR – $(RC)^2$ shaper driving the more noise-critical measurement of the deposited energy.

While the fast branch relies on a single-ended topology for the shaper, the slow branch implements a fully differential second shaper stage. This allows the selection of the correct signal polarity for the subsequent peak detector and hold circuit for either polarity of the input signal. The schematic of the front-end is shown in fig. 4, while figs. 5,

[2] neutron physics X Y T and Energy deposition Readout chip
[3] DETNI_FE10, submitted in 2005 [3]
[4] Metal InterMetal CAPapacitors - Capacitors between two metal layers

6 and tab. 1 detail the performance of this circuit, which had been previously submitted on the DETNI_FE10 chip [3].

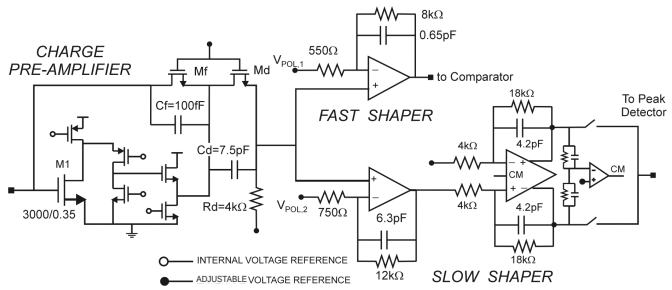

Figure 4: Schematic of the front-end, including the FAST and SLOW shaper branches.

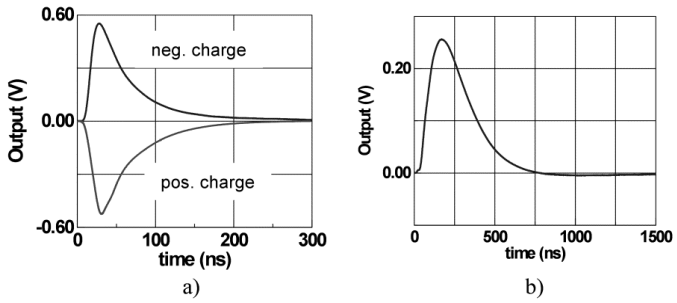

Figure 5: Measured pulse shape of the front-end (from the DETNI_FE10 chip [3]). a) FAST channel b) SLOW channel

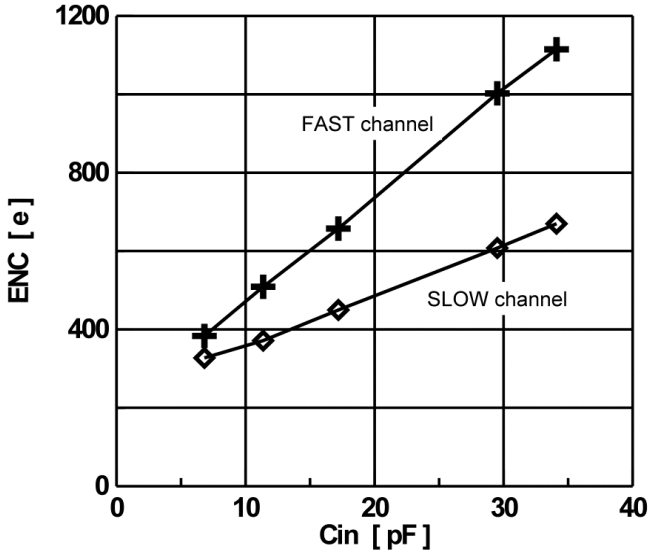

Figure 6: Measured noise performance of the two branches of the front-end, measured on the DETNI_FE10 chip [3].

Table 1: Performance of n-XYTER 1.0's front-end. The measurements were performed with the DETNI_FE10 test chip [3].

	FAST channel	SLOW channel
ENC	$200\,e^- + 26.9\,e^-/pF$	$233\,e^- + 12.7\,e^-/pF$
Rise Time[a] (1 . . . 99 %)	18.5 ns (measured) 20.8 ns (simulated)	139 ns (measured) 138 ns (simulated)

[a] Measured with 30 pF input capacitance

B. Discriminator and Time-Walk Compensation

To correlate the signals on the x- and y-plane of a detector by means of a time stamp, a discriminator has to detect these signals without any dependency on the signal amplitude. The standard approach to accomplish this is the use of a constant-fraction discriminator, which uses a delay line to generate a bipolar pulse. However, delay lines are not available in CMOS technology and a different solution has been chosen [4]: As shown in figure 7, a single pulse discriminator is followed by a voltage controlled delay circuit, which is used to compensate the time walk. With this circuit a reduction of the comparator's time dependency to less than 2 ns has been achieved, as shown in fig. 8. Further results from this circuit are shown in figs. 9 and 10.

The output of the time walk compensation circuit is not only used to latch a 14 bit timestamp, but also to arm the peak detector and hold circuit connected to the slow channel.

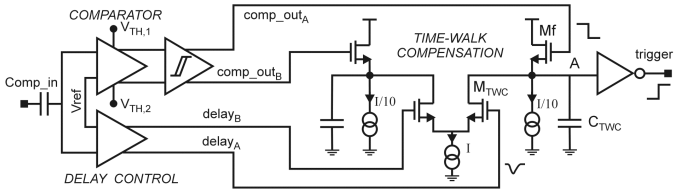

Figure 7: Schematic of the discriminator and time walk compensation circuit. The signals on the delay_a and delay_b inputs control the delay of the circuit by modifying the discharge current of C_{TWC}.

C. Peak-Detector and Hold Circuit

To detect and hold the peak amplitude of the slow channel, the classical peak detector and hold circuit proposed in [5] was adopted. It is depicted in fig 11.

D. Channel FIFO

The slow timing of the peak detector and hold circuit (≈ 150 ns peaking time) permits the synchronisation of the front-end's data with the 32 MHz readout clock already at this stage, without any possibility to introduce additional dead time. The channel FIFO features four stages of analogue and 14-bit wide digital memory. It is used to buffer the data until the channel is granted the multiplexer bus

for a readout cycle.

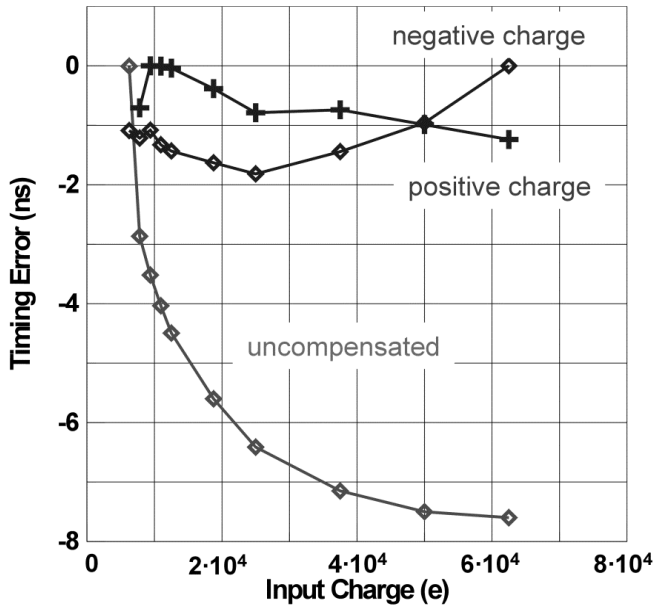

Figure 8: Measured time walk after the discriminator and time walk compensation circuits: The timing error is reduced to ≤ 2 ns (results from the DETNI_FE10 test chip [3]).

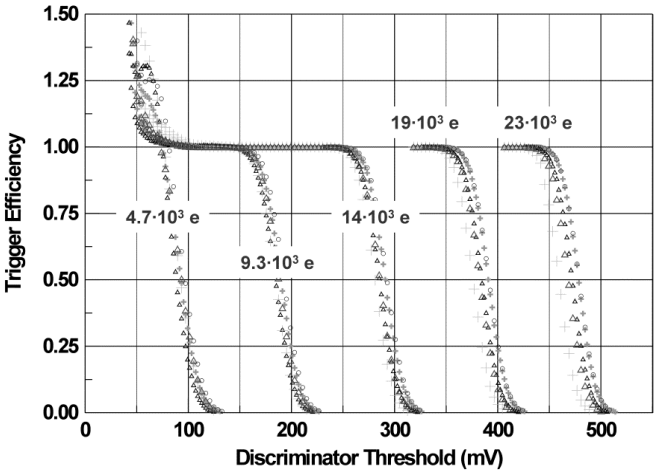

Figure 9: Measured trigger efficiency for different input charges (results from the DETNI_FE10 test chip [3]).

E. Multiplexer

The readout multiplexer is actually implemented as a bus, featuring a token-ring based arbitration schema. It is depicted in fig. 12. This way the readout bandwidth is equally distributed among all channels in case of saturation, while a single channel can still exploit the complete bandwidth, if there are no concurrent requests. Besides the analogue amplitude information and the time stamp, each channel also transmits its ID to provide a spatial coordinate.

The token is injected into the token ring on the rising edge of the 32 MHz readout clock and latched on the falling edge by the token cell of the first non-empty channel. This channel is granted the readout bus for the next clock cycle, while the token is passed on to the next non-empty channel on the next rising edge of the clock. The token manager itself works like a token cell, driven by the logical AND of all channels' empty signals, i.e it will only latch the token, if there is no readout data available.

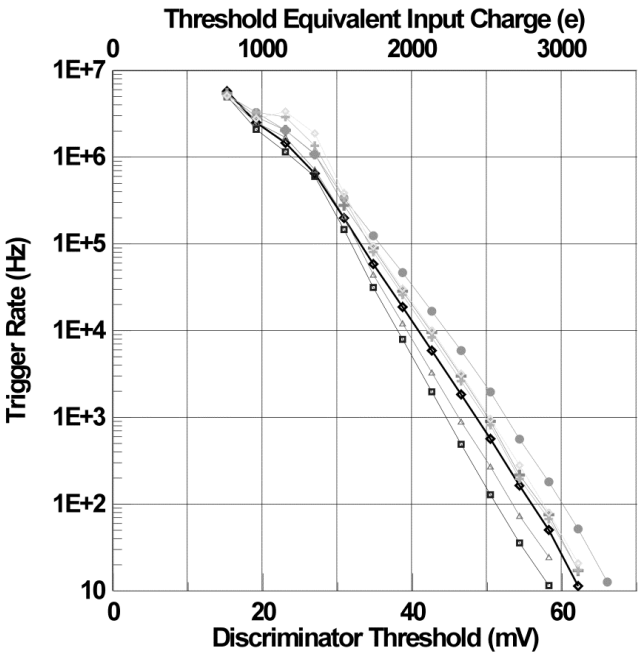

Figure 10: Trigger rate with no signal applied to the input (measured with 28 pF total input capacitance on the DETNI_FE10[3] test chip).

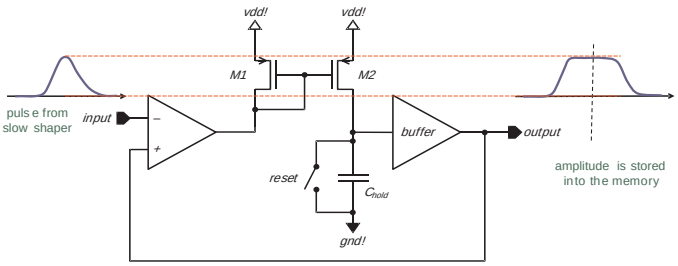

Figure 11: Block schematic of the peak-detector and hold circuit.

Looking at this scenario, the worst case is to have data only in the last channel. Then the token has to pass 127 channels in half a clock cycle, which is not possible for higher temperatures and/or slower corners of the manufacturing process. To overcome this, a token bypass is activated for a group of 16 channels if these are empty, which shorts the token's delay by a factor of 16. In the worst case, the token now has to pass 7 bypasses and 15 token cells to reach the last channel, which ensures the chip's operation even under the worst manufacturing and

temperature conditions.

While the analogue data is driven off-chip via a differential buffer synchronous to the 32 MHz readout clock, time stamp, channel number and other digital data are multiplexed to 128 MHz and driven off-chip via 8 LVDS lines.

While the front end parts of the chip have been tested on the DETNI_FE10 [3] chip, the channel FIFO and readout multiplexer have been evaluated together as an FPGA implementation before the components were implemented on the n-XYTER 1.0 ASIC.

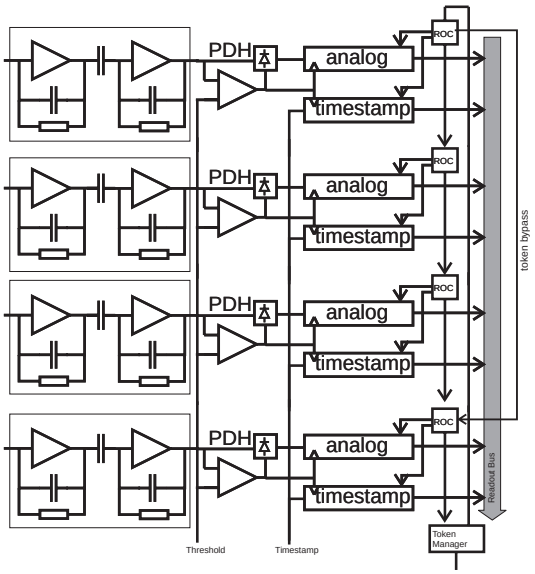

Figure 12: Simplified block schematic showing the readout structure of the n-XYTER 1.0 chip. The token cell is part of each channel's readout cotroller (ROC).

F. Time-Stamp Generator

The time stamp is derived from a 256 MHz clock fed to the chip. A delayed copy of this clock is generated via an adjustable delay line. A logic OR of these two clocks results in a 512 MHz signal used as the time stamp's LSB, fixing the time resolution to ≤ 2 ns. The 13 MSBs are the Gray-encoded output of a counter, derived from the original 256 MHz clock. A global reset signal zeroes this counter and empties all channel FIFOs.

G. Slow Control and Monitoring

A standard I^2C-interface provides access to the control and monitoring functions of the n-XYTER 1.0 chip. It controls the DACs to set e.g. the bias currents of the analogue stages and the discriminator threshold. The latter features circuitry for correction on a per-channel basis to account for interchannel variations. Furthermore, a sophisticated test signal generator featuring programmable amplitudes channel masks and injection points has been included. As an additional feature, counters for latched and rejected events allow an experimental evaluation of the system's efficiency.

IV. Summary

For the new generation of neutron detectors of the EU NMI3 project DETNI [1] a 128 channel readout chip has been developed. It was submitted for manufacturing in June 2006. Its architecture has been taylored to fit the statistical nature and rate of the signals expected from future neutron sources. Thus each channel's charge sensitive preamplifier drives two shapers:

1. A fast one facilitating a time measurement via a time-walk compensated discriminator latching a time stamp.

2. A slow one for energy measurement via a peak detector and hold circuit.

The further signal path includes a 4-stage FIFO per channel for derandomisation and a token-ring based readout multiplexer for sparsification and dynamic bandwidth distribution. While the front-end was was tested on the DETNI_FE10 [3] test chip, the back-end signal path was successfully tested with Monte Carlo data on an FPGA prior to the ASIC implementation.

Due to the unique properties of this architecture an implementation with a lower number of channels (MSGCROC), targeted for applications with even higher rates, has been developed.

The future plans, besides the test of n-XYTER 1.0, include also radiation hard versions of the n-XYTER, intended for future heavy ion experiments.

V. Acknowledgments

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