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Threshold calibration and threshold finding procedure in various LHCb muon MWPC

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Abstract

Threshold calibration and threshold finding procedure in the LHCb muon MWPCs are discussed in this note. Two thresholds in units of charge [fC] are needed in principle: one for the anodes, e.g. 12fC, and one for the cathodes, e.g. 6fC. In reality 120,000 individual thresholds due to variations in offset in CARIOCA chip, different detector capacitances of pads with different size resulting variations in sensitivity from chamber to chamber have to be calculated in register units [r.u.] and move to the threshold registers located in DIALOG chip. The general formula for thresholds in [r.u.] for a given charge unit [fC] is presented. A list of detector capacitance and the averaged sensitivity needed for threshold calculations are given for the inner-most LHCb muon MWPCs in Appendix.

Contents

Introduction

The problem considered below is related to the LHCb Muon system which consists of 1368 Multi-wire Proportional Chambers (MWPC) with about 120,000 physical channels [1, 2]. In order to make offset correction the individual thresholds are calculated for the same charge and move to the internal registers. The technique presented in this note was discussed on LHCb week in March 2006 [3].

Various readout schemes are used in the LHCb muon MWPC:

1) Wire Pad Chamber (WPC) in which the pad is a wire strip of a certain width along X-axis in a bending plane and a certain length along Y-axis;
2) Cathode Pad Chamber (CPC) in which one cathode has been segmented into pads of various sizes (Single Cathode Readout, SCRO) or both cathodes segmented (Double Cathode Readout, DCRO) depending on region around beam line and muon station number;
3) In the inner-most regions R1 and R2 of stations M2 and M3 the chambers have combined readout of both wire strips and cathode pads (CWPC);
4) The chambers CWPC have been made as DCRO in region R1 of stations M2 and M3, and as SCRO in regions R2 and R3. Station M1 of region R2 is built on CPC-DCRO scheme, region R3 on CPC-SCRO whilst region R4 on WPC scheme.
5) Station M1 of region R1 has been built on GEM technology [2].

Front-end electronics (FEE) of the LHCb Muon system is based on 2 dedicated chips: CARIOCA and DIALOG [4, 5]. The chambers are equipped with the front-end boards (FEB) built on these chips and called CARDIAC positive and CARDIAC negative for cathode readout and for wire readout, respectively [6].

The first goal of this note is to propose the general threshold finding procedure and the second one to provide calibration of the register units *[r.u.]* with collected charge units *[fC]* by using the external charge injector. Parameters such as channel sensitivity and detector capacitance related to a choice of the thresholds in *[r.u.]* for the inner-most LHCb muon MWPC are presented in Appendix.

1. Requirements to thresholds

As known from measurements and simulation [7, 8], in order to get 95% efficiency for bi-gap which, in turns, gives 99% efficiency in *20ns* time window for 4-gap MWPC of the certain LHCb muon station, the threshold must be installed in a range of *10-20%* of mean signal deposited in the bi-gap. Such high threshold will also reduce cross-talks to be within 10% limit. Such characteristics are achieved approximately at the threshold of about*12fC* for WPC and *6fC* for CPC-SCRO assuming a mean signal *100fC* developed during rather short current integration time $T_{peak}=10ns$.

As one can see from Fig.1, it is achieved for the gas mixture *Ar(40%)CO2(55%)CF4(5%)* of the final MWPC with 2mm wire pitch and 2.5mm anode-cathode gap at the operational voltage *HV=2.45kV* for bi-gap at low and intermediate rates (muon stations M2-M5). Reduced threshold, e.g. *6fC* or even smaller, has to be used in case of muon station M1 (CPC-DCRO). It can be also achieved at *HV=2.45kV* due to double signal w.r.t. CPC-SCRO. In order to compensate dead time losses at high rates the operational voltage can to be increased to *HV=2.55-2.65kV*.

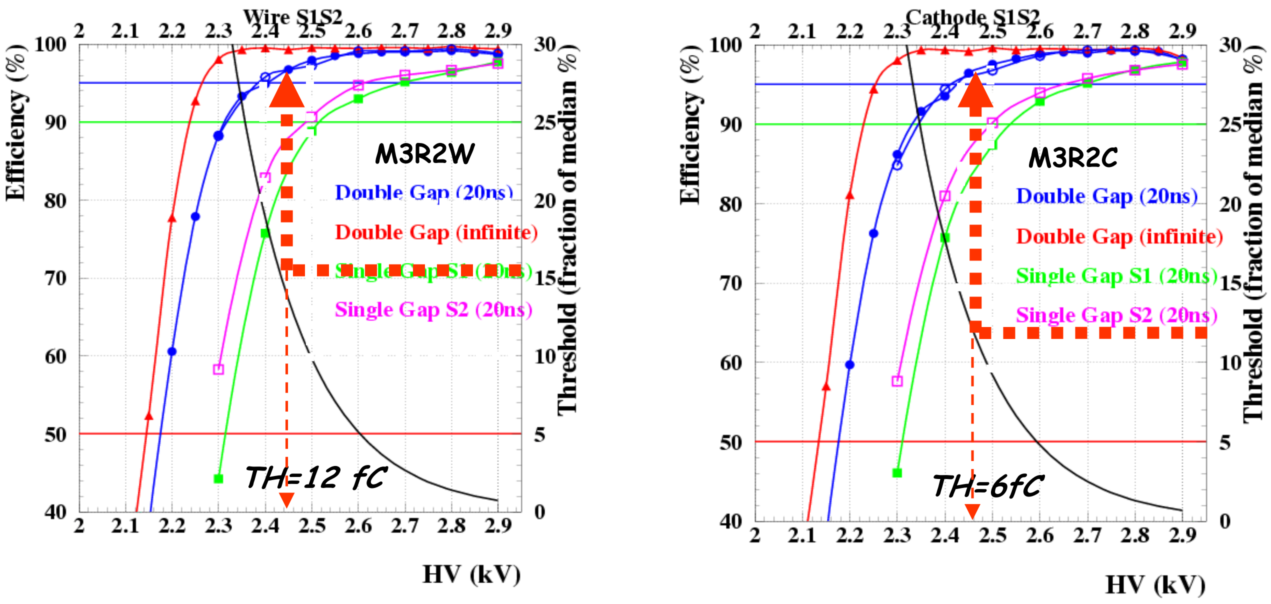

Fig.1. Thresholds 12fC and 6fC as fractions of mean signal (simulation) to obtain efficiency above 95% in 20 ns time window (measurements) for bi-gap MWPC with wire readout and cathode readout, respectively.

2. Threshold calibration

2.1. Internal and external charge injectors

There is an ***internal injector*** built-in CARIOCA chip in each channel. However this feature can not be used for threshold calibration due to mismatch in chip design in both CARIOCA and DIALOG. CARIOCA can inject very large signal of about 100fC, while the maximum threshold produced by DIALOG is equal to 30fC. With such limitations the only digital test can be done to check that the channel alive. Therefore, for threshold calibration the ***external injector*** has to be used. However, it can not be done for all 120,000 channels, but for only a few channels. So, the threshold calibration will be done in average for various MWPC design configurations.

2.2. Register calibration made with precise external charge injector

The ***external injector*** consists of the capacitor which creates the delta-like current pulse from the applied voltage step. To terminate coaxial cable the resistor 50 Ohm is mounted there. Both elements, resistor and capacitor, are carefully shielded. In order to measure or verify precisely the capacitor value the following technique was used. In Fig.2 the voltage $V_{in}(t)$ applied to the injector is shown, as well as the current $I_{in}(t)$ through the capacitor which is connected in series to *50 Ohm* input impedance of the scope. The area of the signal $I_{in}(t)$ measured by scope vs. $V_{in}(t)$ is shown in Fig.2*b*. The linear fit of measured data presented in Fig.2*b* gives capacitor *4.76pF* for voltage in *mV* and pulse area in *fC (pVs measured by scope are multiplied by the ratio 1000/50)*. It has to be noted, the input impedance 50 Ohm used in these measurements is similar to the input impedance of the front-end CARIOCA amplifier. Precision with which the capacitor has been measured with this method is rather high.

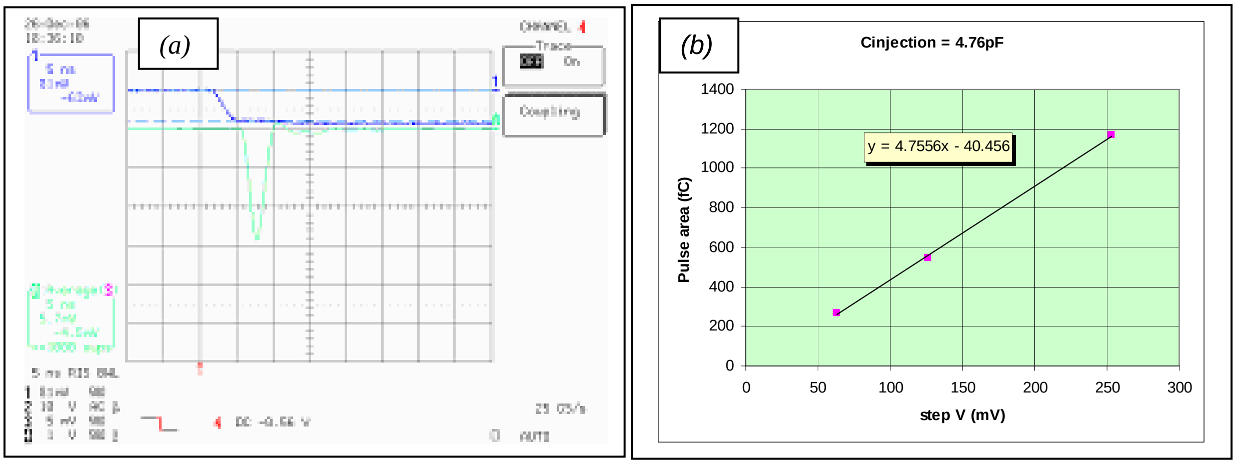

Fig.2. Precise measurement of the capacitor in the external charge injector: *(a)* applied voltage step and current pulse, *5ns/div*; *(b)* capacitor value *4.76pF* is found as the slope of line.

Using the external charge injector with well known capacitor, one can calibrate in charge units *[fC]* the device which controls the threshold - register within DIALOG in our case.

DIALOG chip produces DC voltage and applies it to the discriminator input in CARIOCA chip. While the register number is changed in range of 8 bits (0-255), the DC voltage is ranged from 625 to 1250mV at well known step 2.35mV per bit *[r.u.]*. The discriminator in CARIOCA is a differential one. Above and below offset it changes polarity to the opposite one. In order to maximize dynamic range for a given signal polarity two versions of schematics have been designed: CARIOCA negative and CARIOCA positive optimal for anode and cathode signals, respectively.

In Fig.3 results of register calibration have been shown (minimum two points are needed). It has been done by sending a known charge $Q_{in}\,[fC]$ by the ***external injector*** at known frequency and finding at which register unit $[r.u.]$ the signal is detected at 50%-efficiency (in practice, we do not measure efficiency, but rate). Maximum accuracy of measurement is achieved in this way. A linear fit of measured data for this particular case defines two parameters: $y = Ax + B$, where parameter $A = 5.1\left[\frac{r.u}{fC}\right]$ for a given channel is the slope of line and $B = 57\,[r.u.]$ the intercept. If both parameters are multiplied by $2.35\left[\frac{mV}{r.u.}\right]$ which is the constant scale factor of 8-bit DAC within DIALOG, the sensitivity is defined in *mV/fC* and the intercept or offset in *mV* (625mV has to be added to find the voltage applied from DAC to discriminator). The sensitivity corresponds to $S = 11\left[\frac{mV}{fC}\right]$ for chamber M3R2C with C_{det} *=130pF*. The sensitivity depends on C_{det}, because a part of the current $I_{in}(t)$ from detector returns back through the detector capacitance C_{det} which shunts the amplifier and the remaining part is only amplified. The sensitivity as well as the intercept can be found for other channels in a similar manner.

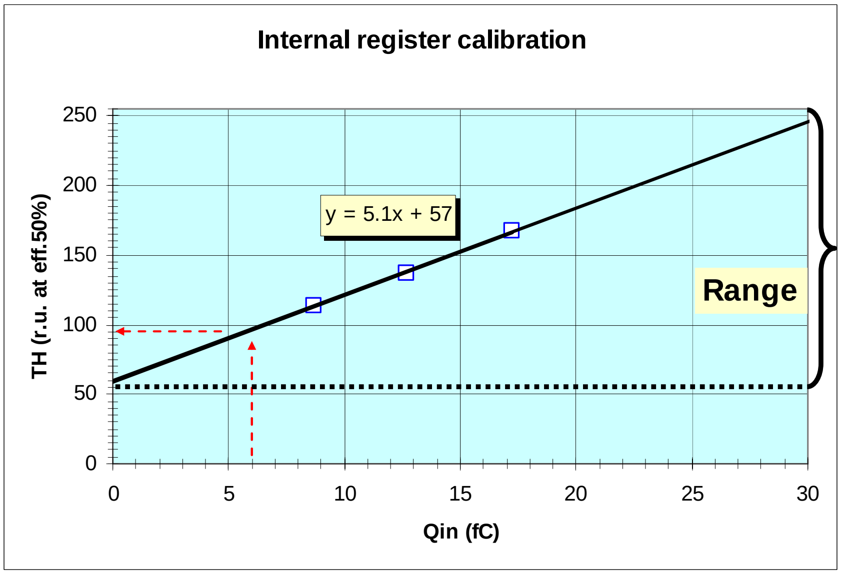

Fig.3. Threshold calibration parameters: slope 5.1r.u./*fC* and intercept 57r.u. for the *i-th* channel of chamber M3R2C (CARIOCA positive) at C_{det} *=130pF*.

This is enough information to calibrate the internal register in DIALOG chip in *[fC]* for a given C_{det}. It has to be noted, however, it is not the threshold finding procedure, but one step.

As shown in section 1, only two thresholds in units of charge are needed in principle for the LHCb muon system: one for the anode channels, e.g.*12fC*, and one for the cathode channels, e.g. *6fC*. In reality 120,000 of individual thresholds due to variations in offset of CARIOCA chip, different detector capacitances of pads with different size, resulting sensitivity variations from channel to channel have to be calculated in register units *[r.u.]* and move to the threshold registers located in DIALOG.

3. Threshold finding procedure

3.1. Baseline position (zero-threshold) on register scale

The operational threshold is defined here as the content of threshold register at which noise count becomes acceptable with respect to one at zero-threshold. Let's specify where the baseline position corresponding to zero-threshold on a register scale is located. As it has been shown in ref. [9], so called ***vertex frequency*** indicates the position of zero-threshold. In turns, the vertex frequency is related to the bandwidth of the amplifier-shaper located in front of the discriminator. According to Rice's theory [10], for white noise power spectrum *w(f*) and ideal band-pass filter whose band extends from f_a to f_b the ***expected number of zeros per second*** is equal:

$$f_0 = 2\sqrt{\left[\frac{\int_0^{\infty} f^2 w(f)df}{\int_0^{\infty} w(f)df}\right]} = 2\sqrt{\frac{1}{3}\cdot\frac{\left(f_b^3 - f_a^3\right)}{\left(f_b - f_a\right)}} \qquad (1).$$

The number of transitions of the noise signal via zero-threshold for a given polarity is half of this number:

$$f_{n0} = \frac{1}{2} f_0 \qquad (2).$$

Thus, f_{n0} is the average rate which could be detected by an ideal discriminator, i.e. discriminator without dead time, without hysteresis, and other imperfections, with unlimited dynamic range, etc. The author of this note in ref. [9] has introduced for this feature a new term 'vertex' frequency and show how it can be measured.

Unfortunately, the cut-off frequencies f_a and f_b are unknown for CARIOCA chip. However, as shown in [9], the vertex frequency is a well-measured parameter, it is enough to make threshold scan, i.e. to measure noise count vs. threshold for two cases, e.g. at one capacitor, then at another one connected to the input of amplifier. In order to simplify the task of zero-threshold finding and make it automatically, the 24-bit counters for rate measurements have been introduced in DIALOG chip (one counter per channel). So, 16-channel CARDIAC board has 16 rate-meters. One can provide accurate measurements of rate versus threshold (called threshold scan) in each individual channel while maximum threshold installed in all other channels in order to prevent a parasitic interference on board.

Results of zero-threshold finding for one channel are shown in Fig.4 for illustration.

The x-axis here is presented in *register units squared* and the y-axis in a count per second in *log*$_{10}$ *scale*. The relation is presented by a straight line in such scale, if one excludes very low and very high rates.

In Fig.4 the vertex frequency has been defined for one channel of CARIOCA positive *(a)* and CARIOCA negative *(b)*. Two different capacitors, first C_{det} and then C_{det} plus additional capacitor connected in parallel to C_{det} were used in order to define two straight lines by linear fit and to find crossing point by following extrapolation.

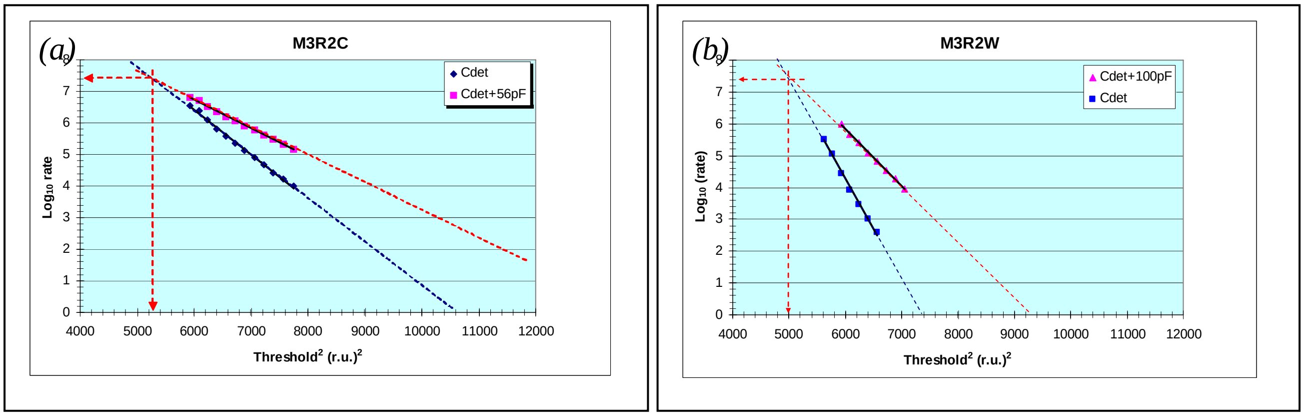

Fig.4. Zero-threshold corresponds to the vertex frequency of 25MHz:
(a) CARIOCA positive; (b) CARIOCA negative.

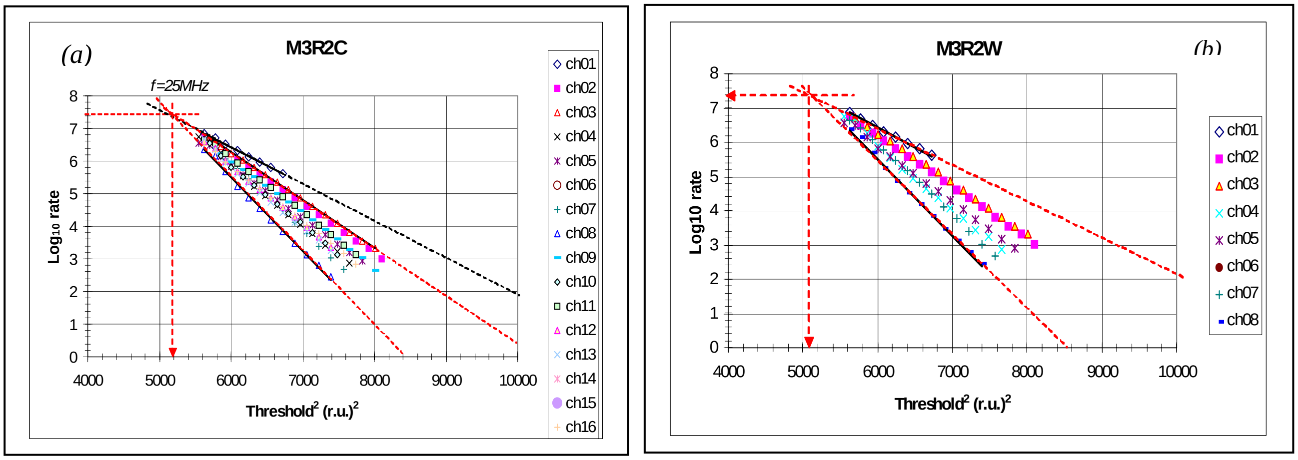

Fig.5. Vertex and zero-threshold finding via cone of crossing lines within one 16-channel CARDIAC board connected to the chamber: M3R2C *(a)* and M3R2W *(b)*.

Zero finding can be done also by another way using a spread from channel to channel of the real C_{det} and a natural spread of noise characteristics within one CARDIAC board, see Fig.5 for illustration. In this way the offset has to be ignored, i.e. any but common offset has to be used.

As one can see in Fig.4 and Fig.5, the vertex frequency is equal approximately to 25 MHz for both CARIOCA positive and CARIOCA negative[1]. The precision of measurements of the vertex frequency is not high but good enough for our purpose. With the measured (or once defined) vertex frequency for CARIOCA chip the zero-threshold can be found, as a crossing point of two lines: the common horizontal line $y = 7.4$ corresponding to the vertex frequency of *25 MHz* and inclined one $y = a_i x + b_i$ for *i-th* channel which has a specific slope for each individual channel at a certain noise level. This measurement can be done 'in situ' automatically by computer during threshold scan.

3.2. General formula for thresholds calculation

Let's take for illustration one channel of CARDIAC-board connected to M3R2C, e.g. channel 1 as most noisy one in Fig.7, and calculate threshold in register units *[r.u.]* as well as in units of charge *[fC]*. Two characteristic points will be used: *X1* is considered as the baseline position (zero-threshold) and *X2* specifies the upper limit of noise rate. Two noise parameters a_i, b_i in a given channel are found from linear fit, see Fig.8.

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[1] Accurate measurements show, that CARIOCA negative have lower vertex frequency due to additional inverter.

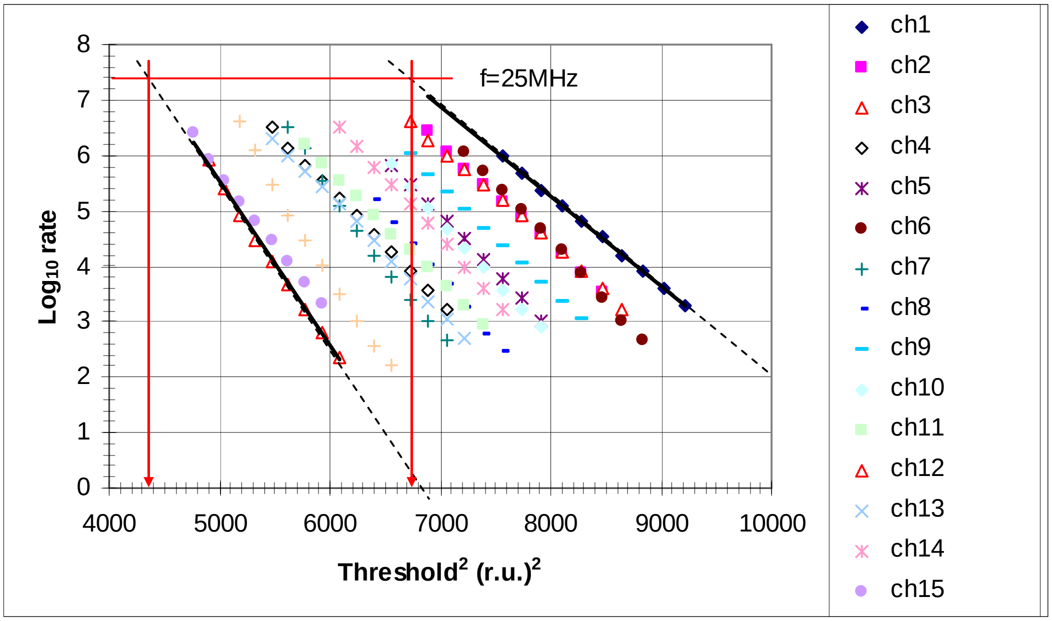

Fig.7. Zero-threshold spread within one 16-channel CARDIAC board.

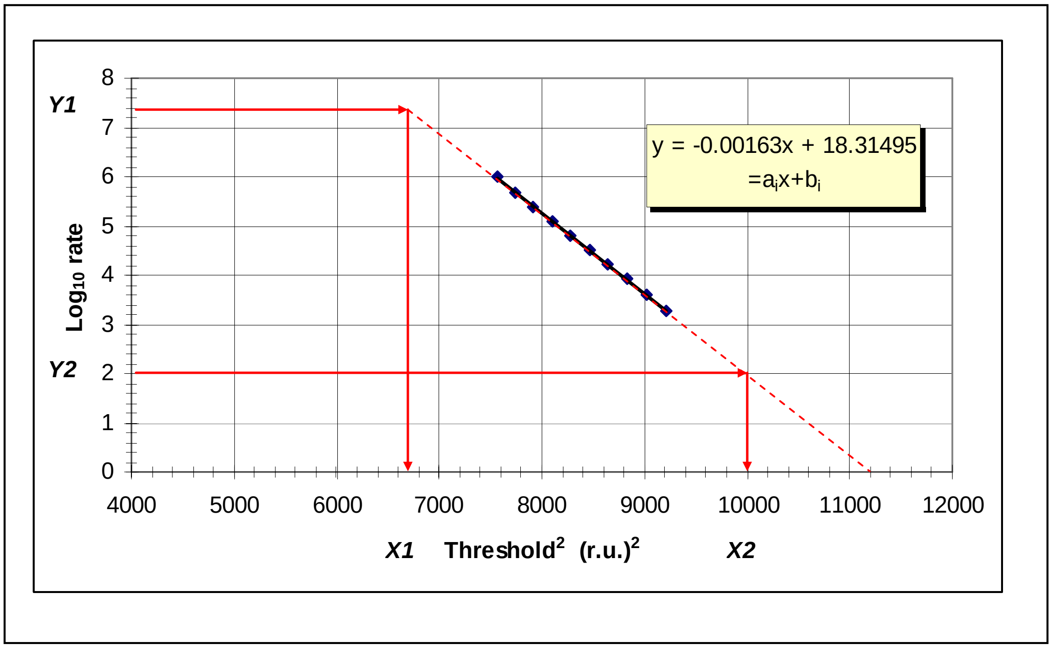

Fig.8. Noise fit-parameters a_i, b_i for channel 1 (see Fig.8) and corresponding characteristic points *X1, Y1* and *X2, Y2*.

The threshold in *[fC]* for particle detection is the level above the baseline on register scale:

$$\left\langle Q^{th}{}_i \right\rangle = \frac{\sqrt{X2_i} - \sqrt{X1_i}}{\langle A \rangle} = \left(\sqrt{\frac{2-b_i}{a_i}} - \sqrt{\frac{7.4-b_i}{a_i}} \right) \times \frac{2.35\left[\frac{mV}{r.u.}\right]}{\langle S \rangle \left[\frac{mV}{fC}\right]} \quad [fC] \qquad (3)$$

Here a_i and b_i are specified by threshold scan for each *i-th* channel, offset B is cancelled as equal for both points *X1* and *X2*, sensitivity A and S are known from measurements in average. Result shown in brackets $\langle \mid \rangle$ means here either the average value or the worst case defined by user.

Back solution now:

What the threshold in *[r.u.]* has to be installed for a given threshold in units of charge *[fC],* i.e. Q^{th}_{given} ?

$$\sqrt{X2_i} = \sqrt{X1_i} + \frac{Q^{th}_{given}}{\langle A \rangle} = \left(\sqrt{\frac{7.4-b_i}{a_i}} \right) + Q^{th}_{given} \times \frac{\langle S \rangle \left[\frac{mV}{fC}\right]}{2.35\left[\frac{mV}{r.u.}\right]} \quad [r.u.] \qquad (4)$$

Let’s consider the numerical example.

For channel 1 (shown in Fig.8 and taken from Fig.7 as the worst case) of chamber M3R2C: $a_i = -0.00163$, $b_i = 18.31$, $Y1 = 7.4$, $Y2 = 2$ one can find the threshold to be installed into DIALOG according to Eq.4:

$$\sqrt{X2_i} = \left(\sqrt{\frac{7.4-18.31}{-0.00163}} \right) + 6 \times \frac{11}{2.35} = 81.8 + 28.1 = 110 \ [r.u.] \qquad (5)$$

The obtained threshold is larger than *100[r.u.]* shown in Fig.8, i.e. it has to give less noise rate than *100Hz.*

4. Conclusions

In order to find threshold in charge units from register units (direct solution), one has to specify where the zero-threshold is located on the register scale. The zero-threshold can be found using so called vertex frequency which is constant and related to the bandwidth of the front-end amplifier. The position of zero-threshold is different from channel to channel due to offset variations. It has been shown also a back solution, how to calculate thresholds in register units which correspond to a given charge unit.

Acknowledgments

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Appendix

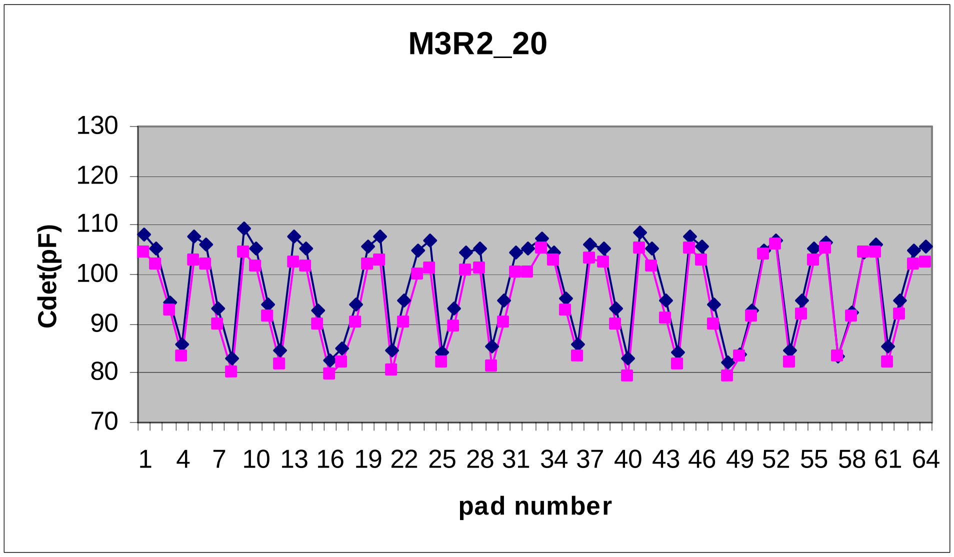

Fig.A1. Typical detector capacitances of cathode channels in M3R2C number 20.

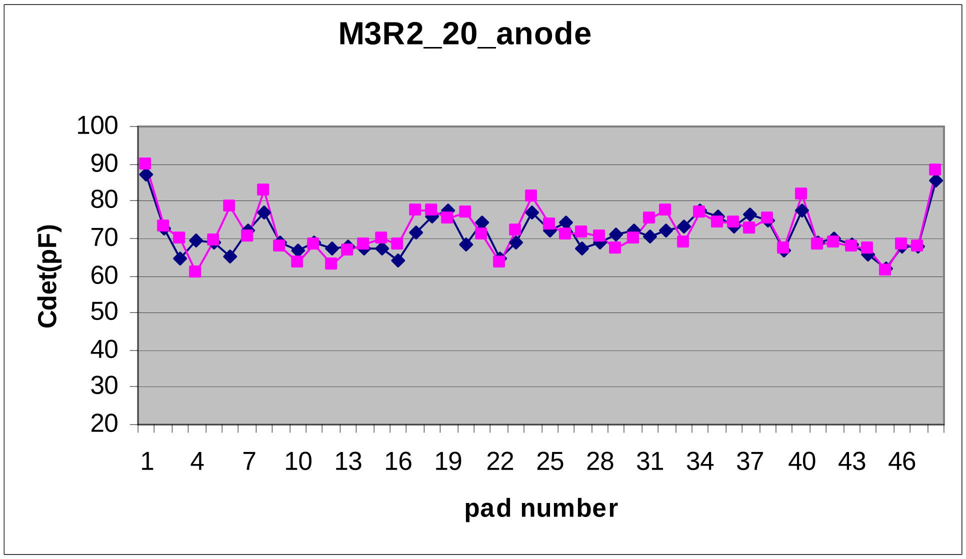

Fig.A2. Typical detector capacitances of anode channels in M3R2W number 20.

Table A1. Averaged C_{det} and sensitivity in the inner-most LHCb muon chambers.

MWPC type	$\langle C\,\mathrm{det}\rangle\ pF$ including SPB ~20pF	$\langle Sensitivity\rangle\ \frac{mV}{fC}$	Comment
M1R2 (CPC-DCRO)	**50**	**16**	C_{det} in range of 20-40 pF without SPB due to traces length
M2R1C (CWPC-DCRO)	**120**	**10**	C_{det} in range of 95-115 pF without SPB due to traces length
M2R1W (CWPC-SCRO)	**70**	**15**	C_{det} in range of 45-60 pF without SPB
M2R2C (CWPC-SCRO)	**100**	**11**	C_{det} in range of 75-95 pF without SPB due to traces length
M2R2W (CWPC-SCRO)	**80**	**14**	C_{det} in range of 55-75 pF without SPB
M3R1C (CWPC-DCRO)	**130**	**10**	C_{det} in range of 90-115 pF without SPB due to traces length
M3R1W (CWPC-SCRO)	**80**	**14**	C_{det} in range of 45-65 pF without SPB
M3R2C (CWPC-SCRO)	**110**	**11**	C_{det} in range of 75-100 pF without SPB due to traces length
M3R2W (CWPC-SCRO)	**90**	**14**	C_{det} in range of 50-80 pF without SPB
M4R1 (CPC-SCRO)	**70**	**15**	C_{det} in range of 45-65 pF without SPB due to traces length
M5R1 (CPC-SCRO)	**70**	**15**	C_{det} in range of 45-65 pF without SPB due to traces length