ATLAS Pixel Detector Timing Optimisation with the Back of Crate Card of the Optical Pixel Readout System

T. Flick[a], P. Gerlach[a], K. Reeves[a], P. Mättig[a]
for the ATLAS Collaboration

[a] Department of Physics, Bergische Universität Wuppertal, Germany
tobias.flick@physik.uni-wuppertal.de

Abstract

As with all detector systems at the Large Hadron Collider (LHC), the assignment of data to the correct bunch crossing, where bunch crossings will be separated in time by 25 ns, is one of the challenges for the ATLAS pixel detector. This document explains how the detector system will accomplish this by describing the general strategy, its implementation, the optimisation of the parameters, and the results obtained during a combined testbeam of all ATLAS subdetectors.

I. Context

The ATLAS experiment is one of the general purpose detectors that will start exploring unprecedented energies in 2007. One of the major challenges of operating in the LHC environment is the high bunch crossing rate, which is needed to observe rare physics events. After a short ramp-up phase in 2007, this bunch crossing rate will reach 40 MHz. This results in the need to assign the detector information to the correct 25 ns timing window.

The ATLAS pixel detector will act as the vertex detector within the ATLAS experiment. Although it is not included in the first level of the trigger system, it will be the device to tag B-jets by finding secondary vertices. This is one of the key techniques in much of the physics analysis that has been prepared for the next years. For this, the spatial resolution of the pixel detector is the most important feature, as can be seen in the fact that over 90% of the roughly 90 million channels of the whole ATLAS experiment are concentrated in the pixel subsystem, while occupying only 1/400000th of the volume.

To have any chance of exploiting sophisticated tracking algorithms, the hits seen by the sensor need to be assigned to their correct bunch crossing, meaning to the correct 25 ns timing window. As the pixel detector won't be read out every clock cycle, hits wrongly assigned are lost or, if the event to which they've been incorrectly assigned is read out, they will appear as ghost hits.

For the ATLAS pixel detector, as the innermost tracking device, there are several contributions to the timing to be taken into account. As a silicon detector, the collection of the charge released by the passing particles is below 10 ns [5]. This is degrading with irradiation, but can be treated as a constant offset of all pixel cells. The processing of the signal within the first electronic stages is limited by the permitted power-budget.

The timing of each individual ATLAS pixel detector module is important in the sense that the individual clock phases they are running with needs to be adjusted with a precision of less than 1 ns to not lose detection efficiency or produce ghost hits by assigning them to the wrong bunch crossing. To be able to separately adjust each of the 1744 modules within the pixel system, each is driven by its own clock. To cope with all different contributions to the timing difference, this can be delayed in steps of 300 ps with respect to clock delivered from the LHC, to which all internal pixel system clocks will refer. This report shows the results of a study made during the ATLAS combined test beam using a 25 ns timing period. A technique to determine the optimal setting for these clocks is described.

II. The Detector System

As a high energy physics general purpose experiment, the ATLAS experiment provides muon spectrometry, high performance calorimetry, and a very high resolution tracking system. The innermost part of the tracking system is the pixel detector. It is made of 1744 hybrid detector modules. Each module is comprised of: a $2 \times 6\,\mathrm{cm}^2$ sensor, implementing 46080 sensor cells, most of $50 \times 400\,\mu\mathrm{m}^2$ area; 16 readout chips per module, designed in a radiation tolerant deep sub-micron process; and a module controller chip (MCC) to steer the module, mounted on top of a flexible circuit providing the intra-module connectivity. The MCC collects and formats the outgoing data, as well.

III. Electronics

A. ATLAS Pixel Readout System

The readout electronics of the ATLAS pixel detector consists of four major parts:

- The Timing Interface Module (TIM, [1]) receiving the ATLAS-wide timing, trigger, and control signal, and distributing it to the BOCs as clock and command information.
- The Readout Driver (ROD)
  - preparing the control data sent to the modules
  - formatting (event fragment building) of the data sent by the modules
  - performing on-line histograming and calibration.

  To fulfil this, the ROD makes use of a chain of FPGAs for treating the data streams, and independent DSPs for the on-line monitoring and calibration calculations.

- The Back of Crate Card (BOC) acts as the off-detector opto-electrical interface. This is the main component of the timing. The modules are served with individual clock signals. These are derived from the TTC clock as received from the TIM.

- The Opto-Board, acting as the on-detector opto-electrical interface.

B. Back of Crate Card

This card was developed under the leadership of the Cavendish Laboratory, Cambridge (UK), for use in the ATLAS SCT and adapted to pixel detector usage by the authors. It's main function is the opto-electrical conversion of the signals sent to and received from the detector [3]. Conversion and alignment of received data for the first processing stages is done here. For the steering of the detector, clock and data are combined into a single optical signal.

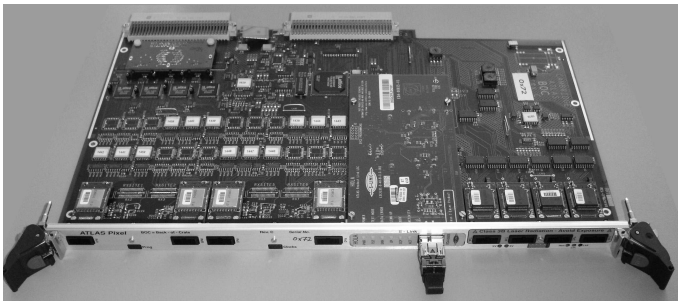

Figure 1: Back of Crate Card

On the detector, the opto-board [4] decodes this into clock and data, which are sent electrically to the modules. As the decoding is done synchronously, this enables the adjustment of the phase of the clock applied to each individual module. For this, the output stage of the Back of Crate Card is able to delay the output stream in steps of 300 ps, up to a maximum of 40 ns. This will allow one to compensate for the differences in cable lengths used, the variations in time of flight caused by the positions of the modules, and other module to module runtime variations.

C. Front End Electronics

The analogue part of each pixel electronics cell is made of a current feedback amplifier, a pulse shaper, and a discriminator applying a threshold to eliminate noise.

1) Time Over Threshold

The current feedback allows for measuring the charge collected within the connected sensor cell by counting the number of clock cycles the signal stays above threshold. Nominally, the feedback current is adjusted to result in a "Time Over Threshold" (ToT) value of 30 for a charge corresponding to the traversal of a minimum ionizing particle (20 ke^-). It is important to realize that for most hits, the charge will be shared by up to four detector cells. Thus, this charge measurement improves the spatial resolution [2] by means of a centroid algorithm, which will be applied off-line.

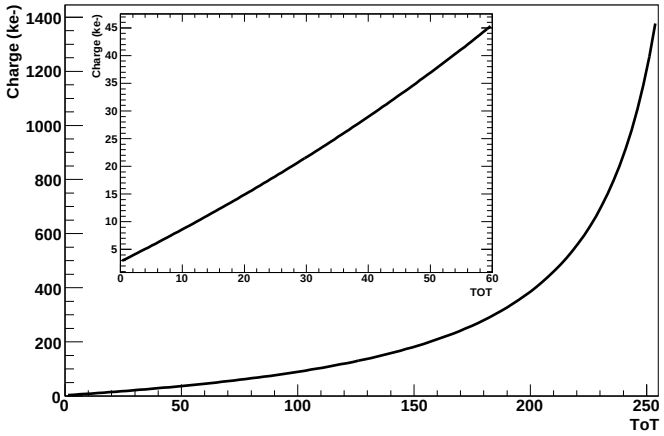

Figure 2: Mean translation of the time over threshold value into charge.

The averaged translation of the measured time over threshold values into the amount of charge collected is given in Figure 2. The time over threshold is measured in number of clock cycles; thus, in discrete numbers. The calibration of the translation into charge is sensitive to many parameters, such as supply voltages and temperature. Therefore, this translation is not applied in the following, but all analysis is done in ToT-values, only.

2) Timewalk

As an effect of the limited power budget and the pulse shaper of each amplifier, lesser charges are registered later than greater ones. This can be by up to three clock cycles.

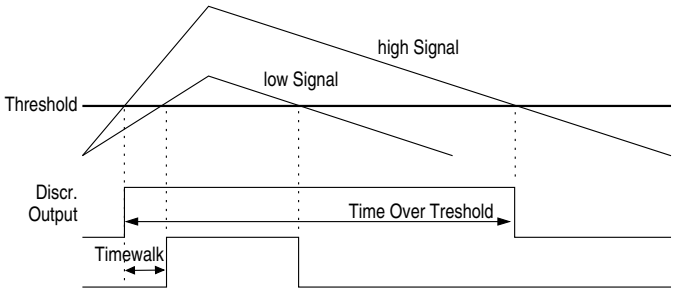

Figure 3: Sketch of time walk

In Figure 3, this is sketched by superimposing a high and a low output signal of the amplifier/shaper stage of a pixel. The slope of the falling part of the signal can be adjusted by the feedback current of the amplifier. This enables the tuning of the ToT. To first order, one can presume that the maximum output of the analogue stage is reached at the same time after particle

traversal, independent of the amount of charge collected.

The timewalk effect will cause a shift of hits with a ToT below a certain value into following events. This is unavoidable, but to be minimized.

IV. MEASUREMENT

In 2004, a slice of the barrel section of the ATLAS experiment was built up at CERN. This combined testbeam setup detected the results of collisions of highly energetic particles with a wire target in front of the slice, in addition to the particle beam itself. The pixel subsystem was comprised of six detector modules arranged in three layers. Each module had an incident angle consistent with what will exist in the barrel section of the final system. This results in a most likely cluster size of two to three pixels.

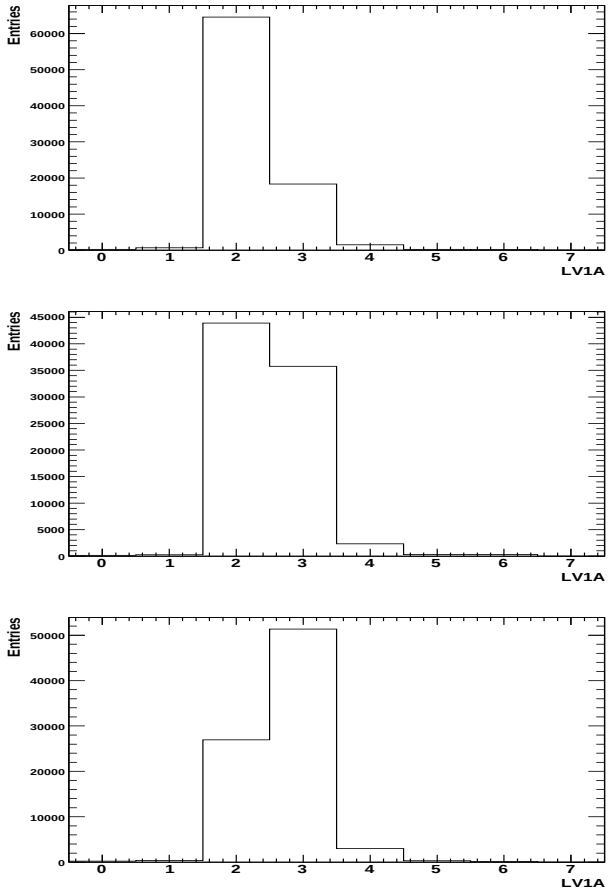

Figure 4: Number of hits per clock cycle for different clock phase settings.

A prototype of the trigger system enabled the recording of track data with the pixel system. For this measurement, an additional feature of the front-end readout electronics was used. For each trigger received, it is possible to cause up to 16 continuous clock cycles to be read out. (Because of bandwidths limits, it will not be possible to make use of this feature at an occupancy given by the ATLAS environment.) As the trigger signal has a fixed latency of 100 clock cycles, this can be used to read out not only the one clock cycle (bunch crossing) that caused the trigger, but also a selectable number before and after this trigger cycle.

Figure 4 depicts the number of hits recorded as a function of clock cycle for three different settings of the delay between event and readout time. One can see that the hits are assigned to different clock cycles by varying this setting.

As Figure 5 shows, the different bins are filled with hits of different charge collected. This is due to the timewalk explained before. For this arbitrary setting of the clock phase of the module, all hits are spread over three clock cycles.

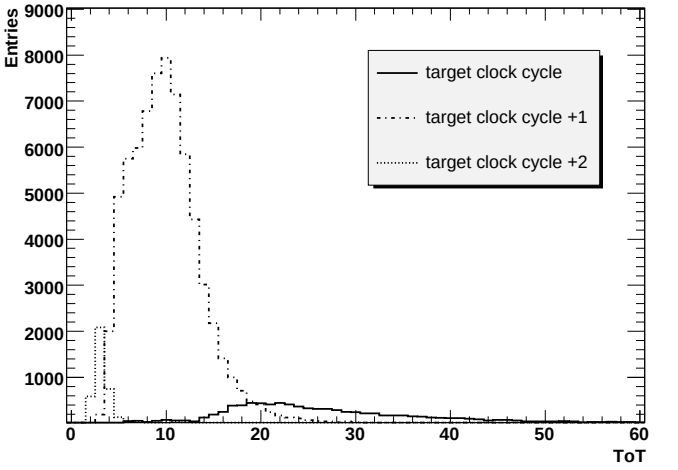

Figure 5: ToT distributions of hits registered to three consecutive clock cycles at arbitrary delay setting

A. *Efficiency*

One may define a registering efficiency as the fraction of hits with a given ToT value assigned to the expected bunch crossing, relative to all hits with this ToT. For one ToT value, the dependence of this efficiency on the delay is shown in Figure 6. Three values can be extracted from this. One is the height of the plateaux, which is the efficiency one can reach for the ToT value inspected. The other two are the delay settings, at which 50% effciency is reached. For the left edge, this is called the “in-time delay”, as for the right edge this is called the “out-of-time delay”. The difference of these values is the assignment time-window defined by the clock-cycle, which is 25 ns.

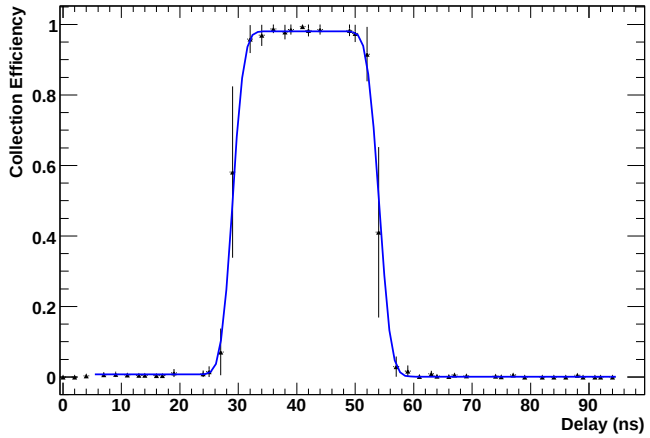

Figure 6: Efficiency vs. delay (fixed ToT=10)

If we now inspect the in-time delay for different ToTs, we can fit a function describing the time-walk behaviour of the front-end electronics. This function approximates the front-end behaviour by presuming that the time when the maximal output of the amplifier stage is reached is independent of the amplitude (see signals sketched in Figure 3). Geometrically, the in-time delay is then given by:

$$T(a) = \frac{t_0 \cdot s}{a} + c,$$

with t_0 the time of the maximum signal, a the amplitude of the signal, s the threshold applied, and c the minimal runtime.

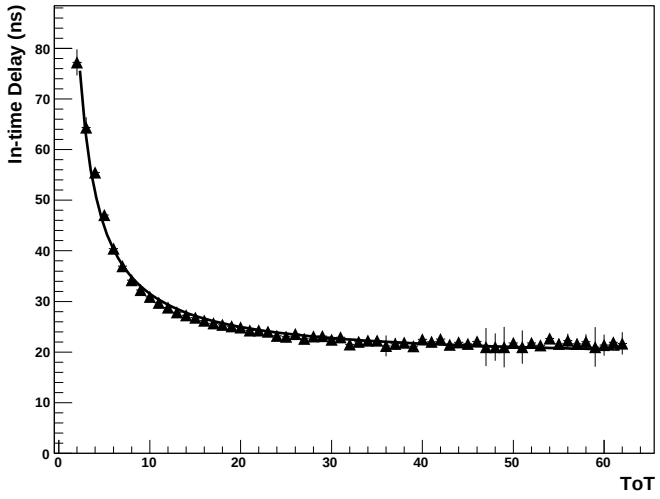

Figure 7: In-time delay as extracted from the rising edges of the efficiency vs. delay plots.

The minimal runtime is fitted as 18.4 ± 0.15 ns in the example shown. Adding the registering window width of 25 ns, one sees that low ToT hits will be registered too late. This is unavoidable. To optimise the delay setting, a map of all registering efficiencies for all ToT-Delay pairs is evaluated in Figure 8. One can think of Figure 6 as a horizontal slice of this.

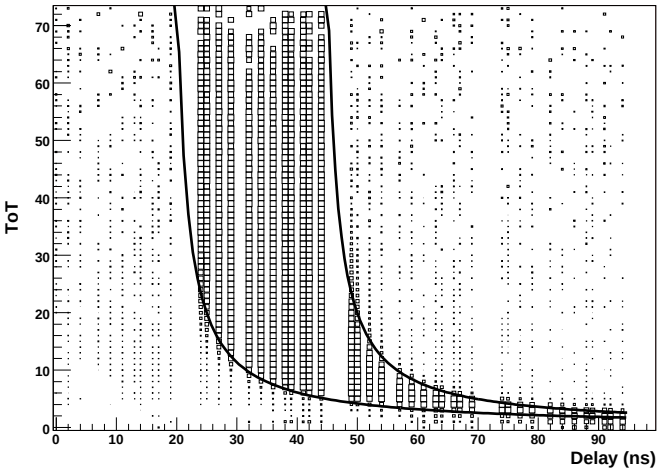

Figure 8: Efficiency of registering a hit correctly.

The curves shown in this map are derived from the fit to the in-time delay (Figure 7) and the registering window width. As one can see, they fit well with the borders of the high efficient region, except of for very low ToT values, which drop below the in-time (the lower) line. This is because the assumption that the time of maximum output of the amplifier is independent of the amplitude is not true.

The optimal delay setting may now be found in the maximum of Figure 9. Here, the sum over all ToTs of the efficiencies for a given delay is plotted. This is the integral of the vertical slices of Figure 8.

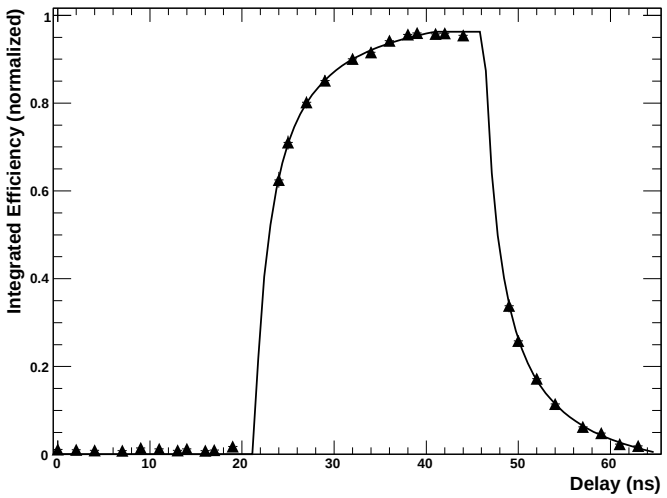

Figure 9: Total Efficiency.

The function fitted to this takes into account the values ob-

tained by the fit to Figure 7 and the fact that the ToT range is limited. In addition, there's a scaling factor applied to account for the fact that the curve does not reach 100%. This is caused by the structure of the beam used, as one can observe in the "out of band" entries in Figure 8. These are caused by out of bunch particles.

V. Results

As Figure 10 demonstrates, it is possible for nearly all hits to be registered correctly, except for those of very low charge. This does not effect the detection efficiency, as these hits with a very low amount of charge are primarily caused by unequal charge sharing of neighbouring sensor cells.

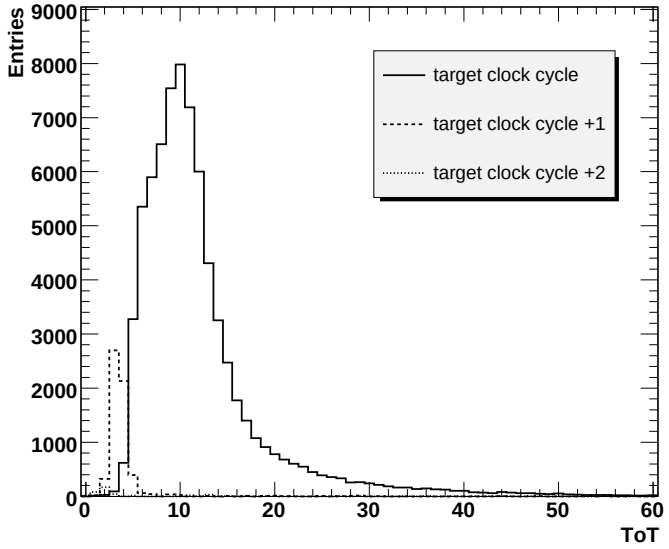

Figure 10: ToT distributions of hits registered to three consecutive clock cycles at tuned delay setting

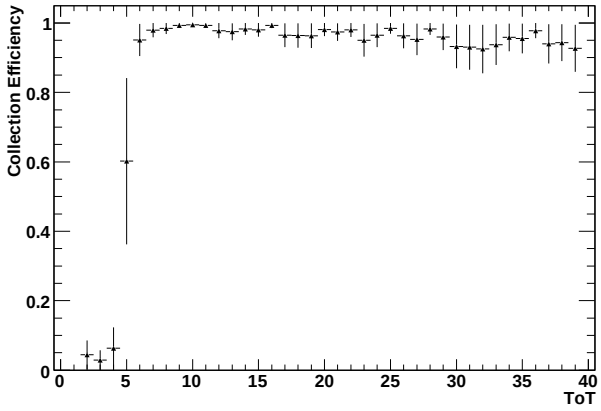

Figure 11: Efficiency vs. ToT (optimised Delay)

A simplified method is demonstrated in Figure 11. Here, only the in-time delay of hits with ToT=30 was measured, and the delay was set to this value minus 5 ns. This results in a competitive setting, where ToTs above 5 are assigned to their event correctly.

VI. Conclusion

A method was implemented and tested to optimise the clock phases of the ATLAS pixel detector modules with respect to the correct assignment of tracks to their bunch crossing. It measures the in-time and out-of-time delays and determines the maximum efficiency. This results in a very good performance of the detector system. Further modifications are needed to apply this method to the high occupancy environment of the LHC. For this, an "inverted" method minimising the hits registered to empty clock cycles is envisaged.

The authors would like to thank all who contributed to the ATLAS combined testbeam.

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