Radiation Tolerance Qualification Tests of the Final Source Interface Unit for the ALICE Experiment

For the ALICE collaboration

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Abstract

The ALICE Detector Data Link (DDL) is a high-speed optical link designed to interface the readout electronics of ALICE sub-detectors to the DAQ computers. The Source Interface Unit (SIU) of the DDL will operate in radiation environment. Previous tests showed that a configuration loss of SRAM-based FPGA devices may happen and the frequency of undetected data errors in the FPGA user memory area is also not acceptable. Therefore, we re-designed the SIU card using another FPGA based on flash technology. In order to detect bit errors in the user memory we added parity check logic to the design. The new SIU has been extensively tested using neutron and proton irradiation to verify its radiation tolerance. In this paper we summarize the design changes, introduce the final design, and the results of the radiation tolerance measurements on the final card.

I. The ALICE Detector Data Link (DDL) and Radiation

The ALICE Detector Data Link (DDL) is a high-speed, duplex, point-to-point optical link designed to interface the readout electronics of all the ALICE sub-detectors to the DAQ computers in a standard way [1]. The DDL consists of the Source Interface Unit (SIU), an optical cable of up to 300 meters, and the Destination Interface Unit (DIU). The DIUs are integrated onto the Read-out Receiver Cards of the DAQ (D-RORC). The DDL provides enough bandwidth to transfer data from the detectors to the DAQ at 200 MB/s per link [2]. The SIU will be attached to the Front-end Electronics; hence, it will be exposed to the radiation caused by the interacting particles. According to the latest simulations, the highest radiation level for the SIU card is expected at the inner radius of the TPC detector [3], where the total ionising dose is 1.6 krad, the neutron fluence is 3.9×10^{11} neutrons/cm^2, and the proton fluence is 8×10^9 for 10 years of operation [4]. The 1MeV neutron equivalent total hadron fluence is 1.5×10^{11} neutrons/cm^2. (The SIU card is not placed directly into the inner tracking system, where the radiation is even higher. From those sub-detectors data is transferred through custom radiation hard links before it is being multiplexed and sent over the DDL.)

The SIU hardware consists of three main components. The DDL protocol and additional logic functions are implemented in a programmable logic device (FPGA). The prototype SIU card has been built around an SRAM-based Altera APEX-E FPGA. The electrical transceiver performs serial-to-parallel and parallel-to-serial data conversion. The full-duplex optical transceiver makes the conversion between the high-speed differential electrical data and the optical signal. Auxiliary components are voltage regulators and a crystal oscillator.

The first radiation tolerant measurements of the prototype SIU components and the prototype SIU card are described in details in [5]. According to these measurements several electrical and optical transceivers, crystal oscillators, and voltage regulators have successfully passed the tests. We had not observed any functional errors at these components and the single-bit transmission errors of the optical transceivers also proved to be much below the permitted error rate.

According to these first measurements we found that from point of view of radiation tolerance, the most vulnerable component of the whole SIU card would be the FPGA device. We identified two issues that had to be investigated in details, namely the *device configuration loss* and the *data corruption* due to SEUs in the embedded user memory and the registers. In this paper, we shortly summarize these two problems and their solutions. We describe the final design, and show the new radiation tolerance test results.

II. Configuration Loss and its Solution

Tests have shown that though the FPGA tolerates the required level of total ionisation dose (TID), single event upsets (SEUs) caused by neutron or proton irradiation have a frequency higher than acceptable. These SEUs may produce data errors during operation, or if they happen in the device configuration SRAM cells, they may provoke corruption (or even loss) of the device configuration. The later is very critical, because it causes an immediate functional interrupt on the given device.

According to the tests, we have calculated the MTBF value and found that we would face 1 loss of configuration every hour in the DAQ system containing 400 DDL SIU cards. We also tested FPGAs of about the same size and complexity from Xilinx, but found very similar results as they are also based on SRAM configuration cell technology. See *Table 1* for the measurement results.

Table 1: Measurement results on configuration loss in Altera APEX-E and Xilinx VIRTEX II SRAM-based FPGAs

SEU cross sections /configuration cell	
$\sigma_{config\ cell}$ of 5-14 MeV neutrons	$(0.17 - 0.71) \cdot 10^{-13}$ cm^2 /logic cell
$\sigma_{config\ cell}$ of 48-50 MeV protons	$(5.5 - 10.7) \cdot 10^{-13}$ cm^2 /logic cell
$\sigma_{config\ cell}$ of 94-100 MeV protons	$(5.5 - 10.2) \cdot 10^{-13}$ cm^2 /logic cell
$\sigma_{config\ cell}$ of 171-180 MeV protons	$(4.5 – 9.0) \cdot 10^{-13}$ cm^2 /logic cell
^{60}Co γ irradiation (dose rate: 40 Gy/hour)	no damage up to 100 Gy
Calculated number of configuration errors	
# of config. loss in 10 years in 1 SIU card	20 – 50 (neutrons) 9 – 20 (protons)
# of config. loss per hour in 400 SIUs	~ 1 not acceptable

Since it was not acceptable for the DAQ system, a new, radiation tolerant DDL SIU had to be designed. We considered three possible ways to solve the problem.

The first option was to continue using Altera or Xilinx SRAM-based FPGAs and work out special mitigation techniques to recover from configuration losses. However, none of the discussed solutions seemed to be simple, all require additional logic circuits on the board (that are also target of radiation tolerance problems), and even with these costly (in terms of design and test work) additions we can not entirely eliminate the problem.

The second option was to use a custom, radiation hard ASIC. Although, this option is technically the most reliable, because the number of links in ALICE is small, we could not afford this solution (high NRE cost). Finally, the last option was the use of another kind of FPGAs that is based on a different silicon technology. In those FPGAs where the configuration is stored in flash memory cells, the configuration is intrinsically much more protected against irradiation. A detailed discussion of the options we considered can be found in the first part of [6].

Finally, we chose the flash-memory based ProASIC device family of Actel. These programmable logic devices combine the power of the FPGAs and the resistance against configuration loss seen in other type of FPGAs.

The block diagram of the re-designed SIU card is shown in *Figure 1*.

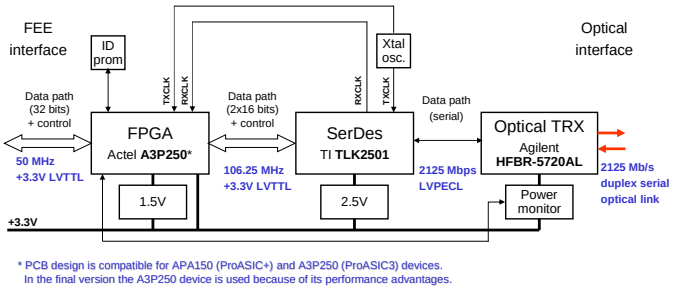

Figure 1: Block diagram of the final SIU card

The physical level of the data transmission is the same as before, the logic part has been re-built around an Actel ProsASIC+ or ProASIC3 device. See [6] for details.

After choosing the new FPGA device we had to verify its expected resistance with measurements. We found that neither a ProASIC+ evolution board nor a new SIU prototype board built with this device (see *Figure 1*) showed any configuration loss in proton and neutron irradiations. See *Table 2* for the measurement results.

Table 2: Measurement results on configuration loss in Actel ProASIC flash memory based FPGAs

SEU cross sections /configuration cell	
$\sigma_{config\ cell}$ of 5-14 MeV neutrons	no error
$\sigma_{config\ cell}$ of 171-180 MeV protons	no error
^{60}Co γ irradiation (dose rate: 40 Gy/hour)	no damage up to 100 Gy
Calculated number of configuration errors	
# of config. loss in 10 years in 1 SIU card	no error
# of config. loss per hour in 400 SIUs	0

III. Data Corruption Measurements

The other consequence of SEUs in the FPGAs is that upsets may change the status (content) of registers (logic cells) and/or the embedded user memory cells during operation. Although these events may not cause a functional interrupt of the device (it does not stop working), they result in bit errors in the data transmission. From the DAQ point of view a certain rate of data bit errors are acceptable if they are detected by the link protocol. From the beginning (i.e. the first prototype SIU) we measured not only the configuration loss of the FPGAs but the data corruption during operation as well. We developed several special test firmware to be able to measure data errors generated in the *register cells* (logic cells) and in the embedded *user memories* (e.g. FIFOs) separately. The method of these measurements is described in [5]. The results are summarized in *Table 3*.

It can be seen that the cross sections for errors generated by the irradiation are in the same magnitude for register cells and for memory cells. However, there are much more memory cells than register cells in the SIU design. It results that the vast majority of the single bit errors caused by the irradiation are generated in the memory cells, namely in the two FIFOs used in the design (one on the transmitter and on the receiver side). The goal was to achieve that these data errors are all detected. We had to re-design the SIU logic to fulfil this new requirement. This needed careful firmware development work but, fortunately, there was no need for change in the hardware.

Table 3: Data corruption measurements of SIUs with different FPGAs

	ALTERA APEX-E (0.18 mm CMOS) SRAM-based		**ACTEL APA150** (0.25 mm CMOS) Flash-based		**ACTEL A3P250** (0.13 mm CMOS) Flash-based	
	$\sigma_{register\ cell}$ [10^{-14} cm^2 /logic cell]	$\sigma_{memory\ cell}$ [10-14 cm2/bit]	$\sigma_{register\ cell}$ [10^{-14} cm^2 /logic cell]	$\sigma_{memory\ cell}$ [10-14 cm2/bit]	$\sigma_{register\ cell}$ [10^{-14} cm^2 /logic cell]	$\sigma_{memory\ cell}$ [10-14 cm2/bit]
5-14 MeV neutrons	0.166 - 0.706	0.29 – 0.51	No error	0.61	0.269	3.02
171-180 MeV protons	4.90 – 8.20	3.08 – 4.24	0.607	5.43	0.267	11.5
# of errors in 10 years in 1 SIU card	20 – 50 (n) 9 – 20 (p)	44 – 55 (n) 9 – 18 (p)	No error (n) 0.21 (p)	59 (n) 8 (p)	4.36 (n) 0.09 (p)	206 (n) 16.94 (p)
# of errors per hour in 400 SIU cards	0.91 (n) 0.22 (p) Config loss! Not acceptable	0.94 (n) 0.27 (p) Not acceptable if not detected	0 (n) 0.003 (p) Acceptable	0.84 (n) 0.115 (p) Not acceptable if not detected	0.063 (n) 0.00014 (p) Acceptable	2.94 (n) 0.24 (p) Not acceptable if not detected

IV. The Final SIU Design with Parity Check

There are several possible mitigation techniques, which can be used to avoid and/or detect the errors caused by SEUs.

One of the widely adopted methods is the so-called triple module redundancy (TRM). This solution, however, requires many extra logic resources, and therefore a larger FPGA device. The increased number of device resources (logic and memory cells) would also increase the chance of being affected by the high-energy particles.

In order to detect the bit errors that may occur in the FPGA's memory cells, one can use error detection schemes based on cyclic redundancy codes (CRC) or parity bits. The CRC checksum is a powerful protection mechanism used in serial transmission protocols. However, the behaviour of the error caused by SEUs in the embedded memory cells (isolated single bit errors) does not justify the complexity required by the CRC calculation. Therefore, a simple yet efficient error detection based on *parity check* logic has been implemented in the FPGA device.

The new and final functional block diagram of the SIU logic can be seen in *Figure 2*.

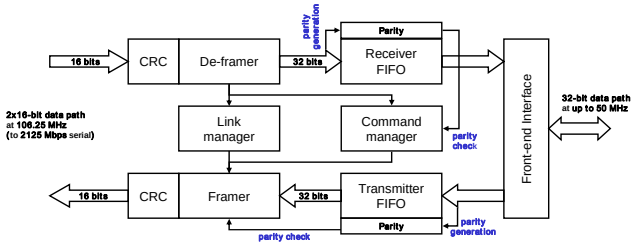

Figure 2: Block diagram of the FPGA design on the final SIU

V. Final Measurement Results

In order to test and verify this redesigned, radiation tolerant SIU we developed and carried out several series of radiation tolerance tests and measurements. With these tests we measured the bit error rates both in the registers and in the embedded memory cells, and tested their detection in radiation environment. Data corruption due to SEUs is detected by the parity check logic. If detected, the firmware attaches an error bit to the control information sent together with the data. During the measurements, the transmitted data was consisted of different known data patterns (alternating patterns, flying 0s or 1s, incremental data). We designed two different tests.

During the so called *loop-back tests* the SIU received data from the DDL link and the special firmware in its FPGA sent these data back trough the link. In this case the data went through the FPGA's memory cells twice. In the other measurement method the SIU, loaded with the final firmware, was plugged into a radiation tolerant *data generator*, which produced data according to the DDL protocol. In this case the data flow is only uni-directional. In both cases the measurement software compared the received data against the expected one and checked whether the error bit had been set in case of erroneous data. If it was set we considered the error to be *detected*. We carried out the measurements up to the neutron fluence of 10^{11} n/cm^2, which corresponds to the radiation level expected during 2.5 years of SIU operation.

During these measurements we found the SIU-imposed error bits attached to all erroneous events, that is, the data corruptions caused by the irradiation were fully detected by the parity check logic. The results of the measurements are summarized in *Table 4*.

Table 4: Measurement results on neutron, proton and γ irradiation of the final SIU card

	SIU card (v. 2.3) w/ ACTEL A3P250 FPGA
$\sigma_{\text{data error}}$ for 5-14 MeV neutrons	(0.4 - 1.0) * 10^{-14} cm^2/bit
$\sigma_{\text{data error}}$ for 171-180 MeV protons	(6 - 7.2) * 10^{-14} cm^2/bit
Co^{60} gamma irradiation	No effect up to 100 Gy (10 krad)
# of data errors in 10 years in 1 SIU	26 - 70 (n) 4 - 10 (p)
# of data errors per hour in 400 SIUs	0.4 - 1 (n) 0.06 - 0.15 (p)
Percentage of detected errors relative to all errors	**~ 100 %**

VI. Project Status

The ALICE Detector Data Link has been developed in collaboration of CERN and KFKI Research Institute for Particle and Nuclear Physics, Budapest. One component of the project was to test and evaluate a radiation tolerant version of the SIU card. With the measurements described in this paper we completed the evaluation of the radiation tolerant Source Interface Unit.

The detector data travelling through the DDL link is protected now in threefold way:

- 8 bit / 10 bit data coding is part of the DDL low level protocol,
- 16 bit CRC words accompany the data on its way between the Source and Destination Interface Units,
- and now, parity bits protect the data in both directions (to and from the detector) inside the SIU subject to irradiation.

The production of the DDL SIU cards has been started this year. More than the half of the 550 cards needed by the ALICE experiment has already been produced and their installation on the sub-detectors has been started. The production will be completed in the 4th quarter of 2006.

VII. Acknowledgment

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All proton irradiation were done at the cyclotron facility of TSL, (Uppsala, Sweden). All neutron irradiation were done at the cyclotron facility of ATOMKI (Debrecen, Hungary), as well as the total ionising dose measurements using their ^{60}Co gamma source.

The authors thank these institutions for their extensive help and support in carrying out of these measurements.

VIII. References

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