

Electronic Devices for Controlling the Very High Voltage in the ALICE TPC detector

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Abstract

The Time Projection Chamber (TPC) is the core of the ALICE experiment at CERN.

The TPC Very High Voltage project covers the development of the control system for the power supply that generates the 100kV necessary for the drift field in the TPC.

This paper reports on the project progress, introducing the control system architecture from the electronics up to the control level. All the electronic devices will be described, highlighting their communication issues, and the challenges in integrating these devices in a PLC-based control system.

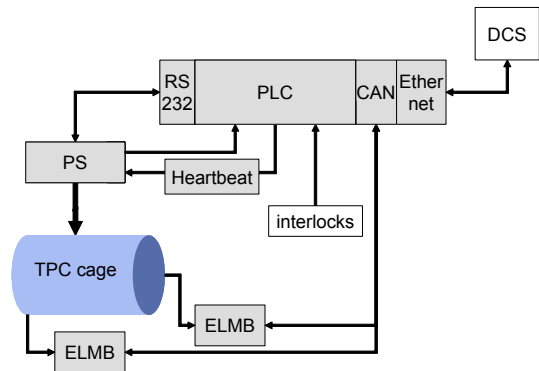


Figure 2: System overview

I. INTRODUCTION

The ALICE TPC is an 88m³ cylinder filled with gas and divided in two drift regions by the central electrode located at its axial centre (Figure 1). The drift field is generated by a 100kV power supply. A Control System was designed in order to supervise and control the power supply.

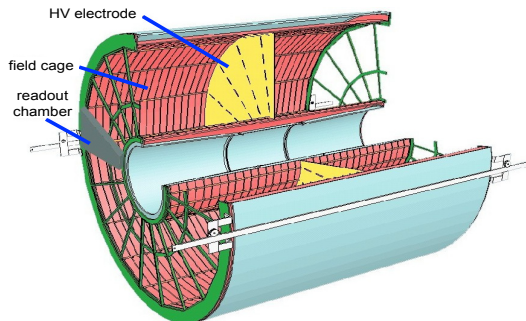


Figure 1: The TPC

II. SYSTEM OVERVIEW

The Power Supply (PS) is a Heinzinger PNC 150000 neg-2, customized for the experiment needs [1]. It can provide up to 150kV DC. The PS is controlled by a RS232 interface. A Programmable Logic Controller (PLC) controls the ramping and several safety features. Thanks to its simple architecture and its stand-alone characteristic, the PLC provides more reliability than a common PC. The chosen PLC is a Schneider Electric P575634M. As it directly controls the PS through the RS232, dedicated communication routines were implemented. Currents in the resistor rods of the field cage are monitored as voltage drops over a resistor. Monitoring is performed by two ELMBs [2] reading 16 analog inputs. Each ELMB is connected to the PLC through CAN bus.

The PLC checks that the voltages remain in range. Other relevant parameters for the operation of the PS are monitored through 13 interlocks (digital inputs) connected to the PLC.

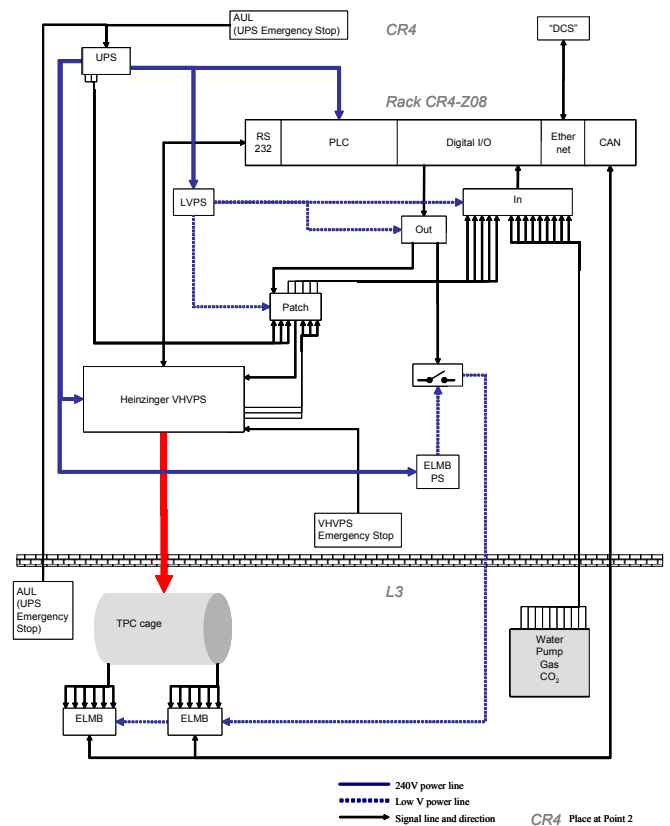


Figure 3: System detailed scheme

They provide status information about cooling water, UPS, gas condition and circulation. Figure 2 shows an overview of the system. The detailed scheme is presented in Figure 3.

III. CONTROL SYSTEM FEATURES

Under operating conditions the system must safely apply a DC voltage of 100kV to the central electrode placed half way between the two end plates of the detector. Four resistor rods supply the proper potential to the field cage [3].

The Control System (CS) was developed following the TPC subsystem requirements, covering the following features: control and monitoring of the PS, of the current in the resistor rods, of the cooling, and some additional equipment.

A. Normal operation

Voltage must be applied by a smooth ramp. Each ramp step of 10kV is followed by one minute pause during which the voltage is held while the system is checked (Figure 4). After 50kV, check pauses last 2 minutes. During the periodical check pauses voltage and current over the resistor rods are verified. At all times, the control system checks the state of all the services used by the TPC (cooling, gas, UPS...). In case any problem occurs, the control system performs a ramp down.

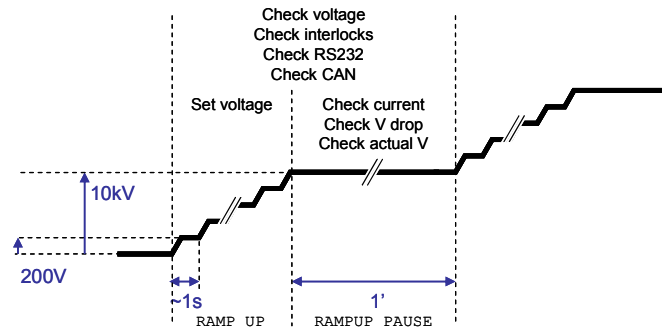


Figure 4: Ramping up scenario

Ramp down can be software-controlled (i.e. smoother and with intermediate pause) or direct (i.e. performed by the hardware slew rate limiter of the PS - faster). The former is executed in case of low priority faults, the latter in case of severe faults. All the parameters (final voltage, ramping speed, nominal values...) are downloaded by the supervisory system and accepted by the control system only in predefined, safe states. Final voltage reaches 100kV after about 20 minutes ramping.

B. Abnormal situation detection

Relevant external parameters need to be within a certain range to allow the operation of the PS. Such parameters are analog (voltage drops over the resistor chains and over the water) and digital (integral current, gas quality, water pump, UPS status) [4].

All relevant parameters are updated and compared to their nominal values at least once a second. In case one or more of these parameters are outside their nominal ranges, the voltage cannot be automatically ramped up. Should a similar situation occur during the standard operation (ramping up, fixed voltage at nominal value) an automatic ramping down of the output voltage is accomplished by the PLC. The reaction time of the PLC system which is controlling the PS is around 600ms after the deviation of one or more parameters is detected. However, before action is taken, several readings within about

3s are done to verify that the particular value is out of range over that time period.

Table 1: Error actions

Error	Action	Time [s]
Any interlock is open	SW ramp down	intlck dep
Voltage trip	SW ramp down	<4
ELMB not active	HW ramp down	<7
RS232 comm. failure	HW ramp down	<40
Current trip	HW ramp down	<1
HV Output is off	HW ramp down	<15
Enable Set Value is off	HW ramp down	<1
PLC not running	HW ramp down	<1

Table 1 summarizes the action to the possible abnormal situations that may occur. Errors associated with HW ramp down have higher action priority. The interlock error reaction time depends on the interlock. The long delay before detecting a RS232 communication failure was set in order to foresee the possibility of a temporary interruption of communication due to a strong magnetic field. If after 40s the communication has not yet recovered, then the ramp down is triggered.

IV. SYSTEM DETAILS

A. Power Supply

The PS was customized for matching the TPC requirements. Its main modification is the addition of an electronic controller that limits the slew rate in case of sudden power up or down. It is the first time that such a high voltage power supply integrates this feature. It makes use of an operational amplifier used as integrator and controlling a Pulse Width Modulator, as shown in Figure 5.

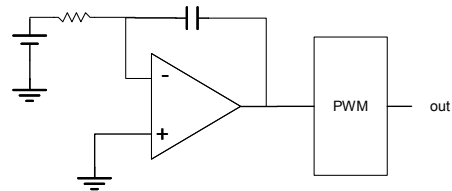


Figure 5: Ramp generator principle

The ramp generator can drive the output at a slew rate ranging from 333V/s to 1000V/s. This is performed in both ramping up and down.

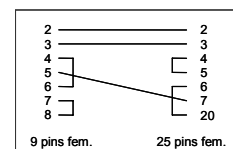


Figure 6: RS232 pin connection

The PS integrates a RS232 interface. This is used for communication PLC - PS. Data flow control is not provided by the PLC board. Therefore, commands and queries are sent through a low level layer implemented in the PLC routines. Those routines control that the data was correctly exchanged

between PLC and PS. The RS232 pins configuration is set to software handshake (Figure 6).

B. ELMB

Two Embedded Local Monitoring Boards (ELMB) are used for reading relevant analog parameters directly from the TPC. The ELMBs are placed on one side of the TPC and reads 8 channels. Analog input was set to the range 0-5V. The connector adapter used for voltage reading is the standard 1kΩ resistors network [5].

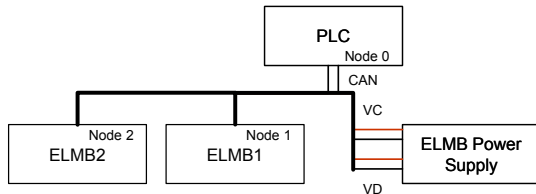


Figure 7: CAN bus connection

The loop interval between two SYNC messages was set to 50ms. This allows a total loop interval among all the channels of around 600ms. At every loop, the 8 channels are scanned and one PDO message is sent from each channel. Power lines are integrated in the CAN cable as shown in Figure 7.

C. Controller

The Schneider PLC controls the PS and monitors all the relevant parameters. It is a stand-alone system, able to react to abnormal situations independently from the supervision level status or actions. The PLC was configured and programmed through the Unity environment. Unity allows a mixed programming method that makes use of any PLC programming convention. Scripts and SFC programming were used in this project. The device was expanded in order to support RS232 and CAN bus connection. Relevant parameters are monitored through digital inputs, CAN connection to two ELMBs and RS232 interface.

Interlocks are directly connected to the PLC's digital inputs. For each interlock an action is triggered with different reaction time, after which the PLC starts a ramp down or does not allow to ramp up the system.

The ELMBs provide analog reading of voltage drops over the TPC resistor rods. CAN bus communication is implemented at the Application Layer. The information is retrieved at low level. For each scanned channel, the ELMB sends a Third Transmit Process Data Object (PDO3) message to the PLC CAN interface. The PDO3 frame is used for transferring analog values. A memory slot was allocated in the PLC for storing the message. The CAN interface stores in the memory the received CAN frame [6]. The data frame sent by the ELMB to the host (node 0 - the PLC) consists of the parts shown in Table 2.

Table 2: PDO3 frame

PDO3 COB-ID	Byte 0	Byte 1	Byte 2-5
380h+NodeID	Channel #	Ch status	ADC val.

Each ELMB (i.e. node) sends cyclically the value of each active channel. Byte 0 contains the channel number, while Bytes 2-5 contain the 32-bit ADC value in μV, LSB first. For each of the two ELMBs the PLC memory slot is periodically read (asynchronously). A routine was implemented for getting the PDO3 message, extracting information and storing it into an array. The same memory slot is then overwritten by the next incoming PDO3 message belonging to the next scanned channel. The time cycle is set to 600ms for each node. At each cycle 8 channels are refreshed for each node.

The PLC is interfacing to the PS through RS232. It allows control and monitoring of the PS: current (I) and voltage (U) setting, I and U reading. The communication was implemented at hand-shake level, since the PLC itself is not able to natively manage a message send and request. Basically, each send/receive command implies a routine similar to the example shown in Figure 8. The setting speed is around 200ms/message. The reading speed is lower (from 1s to 4s), due to the time needed by the PS to read the actual U or I.

Such an implementation is needed also to check if the communication is active. The PLC does not provide, functions for opening or closing the Com port.

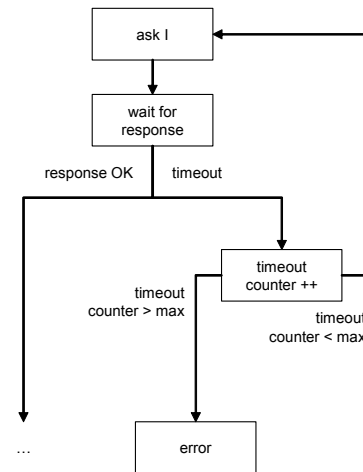


Figure 8: Example of the implemented RS232 messaging routine: asking for current

A RS232 communication failure may lead to a non controlled and potentially unsafe status of the system. For this reason the PS output is directly activated by an interlock controlled by the PLC. If the serial communication is lost, then the PLC sets the PS output to U=0V through the interlock. This triggers a fast ramp down. Such an interlock is implemented with a device working in the following way (see Figure 9 for a simplified schematic): it receives from the PLC a square signal of frequency 6.6Hz (heartbeat).

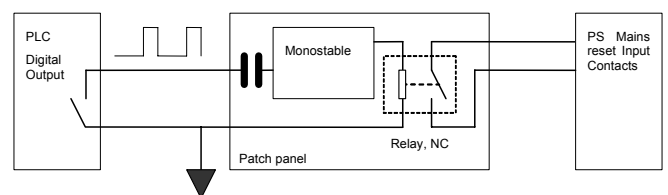


Figure 9: Heartbeat - interlock device

If the signal is on, the device keeps its output contact open. If the signal is flat, the output closes and the PS goes to 0V with internal slew rate limiter. Such an interlock is useful also for detecting a failure in the PLC. If the PLC is not able to produce the heartbeat during 220ms, then the interlock locks the PS to $U=0V$. A hardware ramp down is then triggered.

V. CONCLUSION

The system was successfully tested and used during the commissioning stage of the TPC.

The control system design had to match the main criteria of safety issues. Therefore, a PLC controlled and SCADA supervised architecture was chosen. PLC was preferred to PC for its reliability. Also, ELMB was found more adequate for taking measurements in the harsh environment of the experiment. Special effort was put on the communication within the electronic devices that, in conventional systems, are usually controlled in a transparent way by a common PC. Safety requirements were fulfilled.

The PLC is supervised by ETM PVSSII and ready to be integrated into the ALICE Detector Control hierarchy. A graphic interface allows full control by an operator. The safety procedures are anyway independent from the SCADA system. The output of the controlled PS is shown in Figure 10.

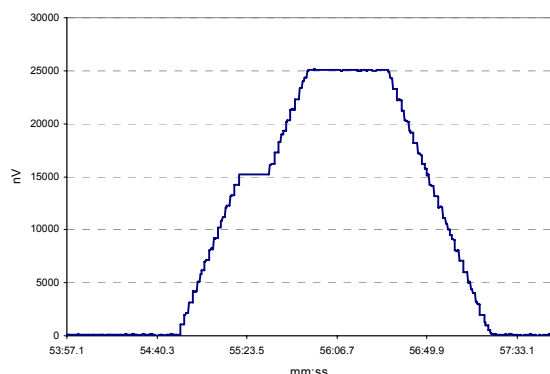


Figure 10: Ramp test of the PS. This plot shows the voltage drop over the last resistor. In this test intermediate voltage corresponds to $U=3kV$. Final voltage corresponds to $U=5kV$. Ramping speed was 100V/s. During normal operation the PS reaches 100kV.

VI. REFERENCES

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