The Hardware of the ATLAS Pixel Detector Control System

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Abstract

The innermost part of the ATLAS (A Toroidal LHC ApparatuS) experiment will be a pixel detector, built of 1744 individual detector modules. To operate the modules, readout electronics, and other detector components, a complex power supply and control system is necessary. The specific powering and control requirements are described, along with the custom made components of our power supply and control systems. These include remotely programmable Regulator Stations, the power supply system for the optical transceivers, several monitoring units and the Interlock System.

I. Introduction

Being the first sub-detector to be passed by particles coming from the interaction point, the main goal of the pixel detector is to reconstruct secondary vertices, such as present in B decays.

In order to do so, the pixel cells have a size of 50 µm x 400 µm, with 46080 pixels forming one detector module. In the central part the modules are loaded on 'staves', which are carried by three concentric shells, in the end caps the modules are mounted on three disks per side. Half staves and disk sectors with six or seven detector modules and individual detector modules are the relevant ensembles on which the power and control systems can act on.

A pixel module consists of the sensor itself and 16 read out chips, which are connected via bump bonds to the sensor cells and house the analog and digital part of the front end read out chain. The front end chips are supervised by the MCC (module controller chip) which is carried by a flex hybrid circuit attached on the top of each detector module. The data transfer is handled by optical links. While the opto board, the on detector part of the optical chain, sends the data, the BOC (Back of Crate) cards, located with a distance of ca. 100 m in the counting room, receive the data.

II. DCS-HW Requirements

Besides of the specific requirements for a special power supply or monitoring unit, there are some common aspects which must be considered for the design of all devices. The high power density inside the detector volume and the radiation tolerance, dependent on the location of the equipment, have impact on the construction of most of our components. Reliability, meaning any risks to the highly sensitive detector must be avoided, gains even further importance due to the fact that many components will be inaccessible over long terms.

Furthermore the design of our system is driven by the need to find a good compromise between the desire to control and tune small units of the detector individually and low costs on the other side.

Concerning the power supplies and all related monitoring units the ATLAS grounding scheme requires floating designs. Due to the radiation, which the front end chips and the detector sensors suffer during their lifetime, all power supplies must have adjustable outputs. For safety reasons over-current protections and interlock inputs are also required for all power supplies.

As all hardware must be integrated into the pixel and ATLAS wide DCS (Detector Control System) the interfaces of the various components should be compatible to it. Therefore the ELMB (Embedded Local Monitor Board) builds the core of all our applications [1]. The ELMB is a multi-purpose acquisition and control unit, which owns a CAN (Control Area Network) interface. Its communication is based on the CAN-open protocol, which was chosen by ATLAS DCS for its reliability.

III. Overview of the DCS HW System

The DCS hardware system consists of (see Figure 1):

- the power supplies needed to operate the sensors, the front end chips and the opto boards,
- the Regulator Stations,
- temperature, humidity and current sensors,
- monitoring devices for the readout of the sensors,
- the Interlock System and
- the DCS PCs communicating with the HW.

Figure 1 shows the schematic, and in terms of the Interlock System simplified, overview of the DCS hardware.

The pixel power supply system consists of four major components [2]. To operate the front end electronics, two low voltages, Vdd and Vdda, are required. Delivered by the commercial W.IE.NE.R (Burscheid, Germany) power

supplies (PL512), the LVs are regulated closely to the detector by the use of the Regulator Stations. The high voltage (700 V, 4 mA), which depletes the sensors, is provided by the EHQ-F007n-F modules, built by iseg (Rossendorf, Germany). As the high voltage does not require any further regulation, it is sent directly to the detector elements. The related LV-PP4 (patch panel 4) and HV-PP4 units distribute the power and monitor the current consumptions. The opto boards are supplied by the SC-OLink (Supply and Control for the Opto-Link).

Monitoring of various temperatures and some humidity sensors is performed by the BBM (Building block Monitoring) and BBIM (Building Block Interlock and Monitoring) crates. While the first just provide a reading of values, the second additionally create logical signals, which are fed into the Interlock System.

All main power supplies mentioned above (LV, HV, SC-OLink) plus the off-detector part of the opto link, the BOC card, are connected to the hardware based Interlock System. This consists of several units that guarantee safety for human operators as well as for sensible detector parts.

Besides the LV crates, which are connected via TCP/IP all primary power supplies, Regulator Stations, monitoring crates and the Interlock System are connected to the DCS PCs via the CAN-Open protocol.

IV. Power Supplies

All power supplies are located in the counting rooms, where all cables are routed to [3]. This gives an easy access and more flexibility during operation. Additionally this frees from problems due to radiation. On the other side the large distance of more than 100 m between source and load gives need for a LV regulation as close as possible to the detector. The remotely programmable Regulator Stations protect the sensitive read out chips, developed in deep sub-micron technology, against transients. In parallel they allow an individual tuning of each detector module to its optimal operation conditions.

While the LV and HV power supplies deliver the power for half staves, respectively disk sectors the related PP4 units split the primary output onto lines, which connect to each detector module individually. Additionally these PP4 crates provide a current monitoring for single detector modules. In this way a good compromise between the costs for hundreds of power supply channels and maximal available information is found.

The HV and LV power supplies are commercial systems, the Regulator Stations and the SC-OLink are custom made.

A. Supply and Control of the Opto Link

To operate one opto board three different voltages and one control signal are required, these four outputs build one complex SC-Olink channel [4]. While Vvdc (10 V, 800 mA) supplies the transceiver chips as well as the transmitter diode, the receiver diode requires an additional supply voltage Vpin (20 V, 20 mA). Viset (5 V, 20 mA) is used to adjust to operating point of the transmitter diode and the control signal, the fourth output, (2.5 V, 10 µs) allows to send a reset signal to the receiver control chip. In total 272 complex channels are required.

Usage of a single channel DAC (MAX5122, 12 bit), controlled by the ELMB, allows one to adjust the output voltages. Isolation of the floating outputs is given by transformers and opto couplers in all control and monitoring lines. As the DACs are powered separately, the output voltages remain unaffected if a power cycle of the CANbus for resetting the ELMBs is necessary. The precision for setting and monitoring is better than 0.5%. Additionally all channels own a hardware current limitation and there is one interlock input per complex channel.

B. Regulator Station

To protect the integrated circuits of the front end chips, that are manufactured in deep sub-micron CMOS technology, against voltages surges or spikes, a remotely programmable regulation station capable of providing individual floating power output with low ripple has been designed. The station is more 10 m away from the detector, and each FE line is continuously ‘sensed’ down at the module to promptly adjust the output voltages. One regulation station can power up to 84 modules (Vdda, Vdd, Vvdc) and communicate with the ATLAS Detector Control System via a CAN bus interface.

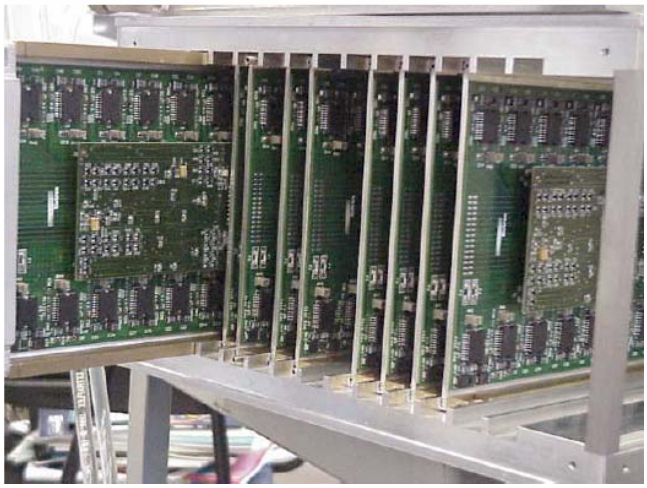

Figure 2: the Regulator Boards, each board is composed by a motherboard and a daughter board

The core of the Regulation Stations are printed circuit boards built on a highly dissipative substrate (approx. 10 W/board), see Figure 2. Each board houses 16 ST rad-hard voltage regulators (LHC4913+) and provide about 1 A at 2 V with 10 mV regulation step, around the typical range of operation of the front end electronics (~ 2 V, ~1 A). All channels are floating up to ± 10 V. Programmable digital trimmers are addressed by control signals that are opto coupled to preserve isolation. Channels can be inhibited individually or per board while kept floating. Further safety is given by a current compensation on each channel and a protection of the output voltages against accidental disconnection of the sense lines.

All adjustment and monitoring functions in a Regulator Station are supervised by one controller board, which is based on a FPGA (APA075 from ACTEL, Mountain View CA, USA). The FPGA can be reprogrammed via CAN bus to facilitate operation during the ten year operation of ATLAS. The need for programming the FPGA on demands derives from the fact that a degradation of the performances of the front end electronics is expected during the life of the experiment. The full system has been irradiated and is rad-tolerant up to a NIEL > 10^{12} 1 MeV n_{eq}/cm^2.

V. Monitoring

A. Low Voltage Monitoring

A distribution of the low voltages is required as six or seven detector modules are supplied by one LV W.IE.N.ER power supply channel each. This is performed by the patch panels no. 4, which are installed in direct vicinity to the LV crates. To have full information about the health of each detector module an additional current measurement per detector module is available. For debugging the system, especially to trace grounding problems, the current of the in- and output lines can be measured.

The core of the LV-PP4 are ELMBs. As done for the SC-Olink the use of opto isolators decouples the measuring circuits, which reach a precision of 2 – 10 mA for a measuring range between 0 and 2 A.

The construction of LV-PP4 is driven by the layout of the services, therefore each LV-PP4 block can handle up to 28 supply lines and 56 measuring channels. The measuring channels are grouped in the way, that a second card housing further op-amp and opto couplers can be added if the measurement of the return current becomes necessary. All together LV-PP4 will consist of 3500 up to 7000 monitoring channels (when all currents and their returns are measured).

B. High Voltage Monitoring

As the required depletion voltage will increase during the detector lifetime, the modularity of the HV system needs to be changed. This has not only effects on the total number of HV power supplies needed, but also on the mapping of the power supply channels to the detector modules, which is performed by the HV-PP4 crates.

A HV-PP4 is therefore not only capable of a current measurement of the HV-lines at a single module level (by the use of ELMBs), but it is also responsible for the correct mapping of the iseg HV channels to the detector modules. 16 HV-PP4 crates will be required for the experiment, each with up to 117 monitoring channels. The strongly varying depletion current requires a large dynamic range of 0.4 mA to 4 μA for these measuring circuits.

C. Building Block Monitoring

About 2000 temperature sensors are required inside the pixel DCS. We have chosen 10 kΩ NTC (negative temperature coefficient) thermistors, as they combine radiation hardness (up to 10^{15} n/cm²), a large relative change of their resistor of 4 %/K and small SMD casings (0603). Also the humidity sensor, Xeritron (from Hygrometrix, Alpine CA, USA) is chosen because of its radiation hardness.

While the signals of the temperature sensors mounted on the detector modules, opto boards and Regulator Stations are fed into the monitoring and Interlock System, see next section, all pure monitoring is handled by the BBM (building block monitoring) crates [5]. This includes the humidity sensors and all temperature sensors which are additionally installed inside the pixel volume.

The core of each BBM is again an ELMB which is used for the data readout. Its input circuitry is specially adapted to supply NTC and Xeritron sensors and to handle their signals.

VI. Interlock System

While the normal operation of the detector is steered by the DCS software, all safety relevant situations are handled by the Interlock System. In order to prevent damages to human beings or important parts of the detector, the hardware Interlock System is able to switch down all necessary power supplies and to operate completely independent from the rest of the control system.

Due to the dense circuitries of the front end chips the power consumption inside the detector volume is very high. As heat ups of the detector modules lead to a faster ageing or can cause severe damages to the detector, their temperatures are being monitored and in parallel the signals are lead into the Interlock System. As over temperature is a risk to opto boards and Regulator Stations as well, these units are also controlled by the Interlock System.

The risks of accidents involving humans refers to the damage potential to the eyes given by the infra-red lasers of the opto links. Therefore all lasers have to be switched off immediately once one of the fibre connectors at the detector or counting room side are opened.

In case of emergency the smallest necessary subset of power supplies is switched off in order to allow the rest of the detector to remain operational. In total the system handles 2150 incoming interlock signals and acts on 1100 interlock controlled devices. All circuits are built in negative logic; as soon as a cable is disconnected the related equipment is interlocked. An overview on the Interlock System is given in Figure 3, its components are described in more detail below [6].

A. Building Block Interlock and Monitoring

The BBIM (Building Block Interlock Monitoring) crates receive the module, opto board and Regulator Station temperatures as analogue voltages. These are digitized by comparator circuits, called Interlock Board, with exchangeable threshold plug-ins which allow to adapt to the needs of the different equipment.

The digital information is then sent as TTL signals to the Logic Unit. In parallel the BBIM crates house ELMBs that monitor the temperatures and deliver the information to the DCS software.

As the processing of the analogue signals should be close to the detector, the BBIM crates are mounted in the radiation

environment of the ATLAS cavern. Therefore all components of the Interlock Board have undergone intensive radiation tests and the required radiation tolerance criteria of 93 Gy and 5 x 10^{11} n/cm^2 (1 MeV) were reached.

B. Logic Units

The LUs (Logic Unit) combine all the incoming signals from the BBIM crates, the PP1 Boxes, the BOC-I-Box and the DSS (Detector Safety System) into logical interlocks with a granularity of half staves, respectively disk sectors. While the BBIM crates deliver the temperature alarms, the PP1 Boxes are sending signals when a part of the optical laser driven read out system is opened. Additionally DSS, an ATLAS wide system, provides an interlock signal in case of more general alarm conditions like smoke or failures in the cooling system.

Core of the LU is a FPGA (APA075) that is able to determine the current situation from the inputs and raises the corresponding interlock alerts.

Although the Interlock System is purely hardware based, it is required to communicate and explain the interlock actions to the rest of the DCS. This is realized by the use of ELMBs within the LU that read out the incoming signals and report them to DCS. In addition, the digital outputs of the ELMB are used to provide test signals to the Interlock System.

C. Interlock Distribution Boxes

The IDB (Interlock Distribution Box) receives the logical interlock signals on the granularity level of no more than seven modules and distributes the interlock signals to the connected power supply channels in order to switch off the smallest possible subset of power supply channels.

Therefore the IDB has to take the correct mapping of the power supplies into account which is especially difficult due to the fact that the modularity of power supply channels connected to detector modules changes during lifetime (HV). Further the number of power supply channels per crate is different for LV, HV and SC-OLink and cabling might change when e.g. single channels are broken. The needed flexibility is achieved by the use of another FPGA (APA075).

An ELMB is used for the monitoring of the interlock signals, outgoing to the power supplies. The combined information of the LU, IDB, PP1 and BOC-I-Box ELMBs ensures a consistent monitoring of all interlock activities.

VII. SUMMARY

The requirements of the pixel detector have made specific developments necessary for the hardware components of the power supply and detector control system.

An efficient operation requires a preferably individual adjustment of the different control parameters. Further design constraints are the high power density in the detector volume, the floating grounding scheme of the ATLAS detector and the sensitivity of the read out chips developed in deep sub micron technology. Especially the power supply system, consisting of nearly 5000 individually controllable supply lines, requires solutions which are adapted to the detector needs and which in parallel are economically priced.

The remotely programmable Regulator Stations, which are installed as close as possible to the detector modules, provide individual floating power outputs with low ripple to the front end electronics. At the same time they protect the sensitive chips against transients. The internal control of the Regulator Station is handled by a FPGA from ACTEL, while the link into the control system is handled by the ELMB, the ATLAS wide used front end IO unit.

The design of the supply system for the opto transceiver boards is based on components, which can directly be controlled by the ELMB. In this way a reasonable priced solution has been found which allows individual setting and adjustment for each of the more than thousand channels.

In the positions where common power supplies are used to provide voltages to several loads, additional monitoring units are integrated which allow to investigate the behaviour of individual modules. The design constraints, precision and compatibility to the ATLAS grounding scheme, are fulfilled by the presented LV monitoring system. In the final system more than 8000 monitoring channels complete the low and high voltage system.

As especially irradiated detector modules are very sensitive to temperature increases or can even be destroyed by heat ups, a thermal Interlock System is developed which acts directly on the related power supplies. In addition other equipment can suffer from extreme heat and human being must be protected against risks due to lasers. Therefore these devices are connected to the Interlock System as well. The presented interlock matrix, whose design is based on the use of FPGAs, allows a dedicated control of small equipment groups and helps in this way to keep the number of channels out of service as low as possible.

The presented hardware components passed intensive electrical studies and investigation in our system tests and are currently under production.

VIII. REFERENCES

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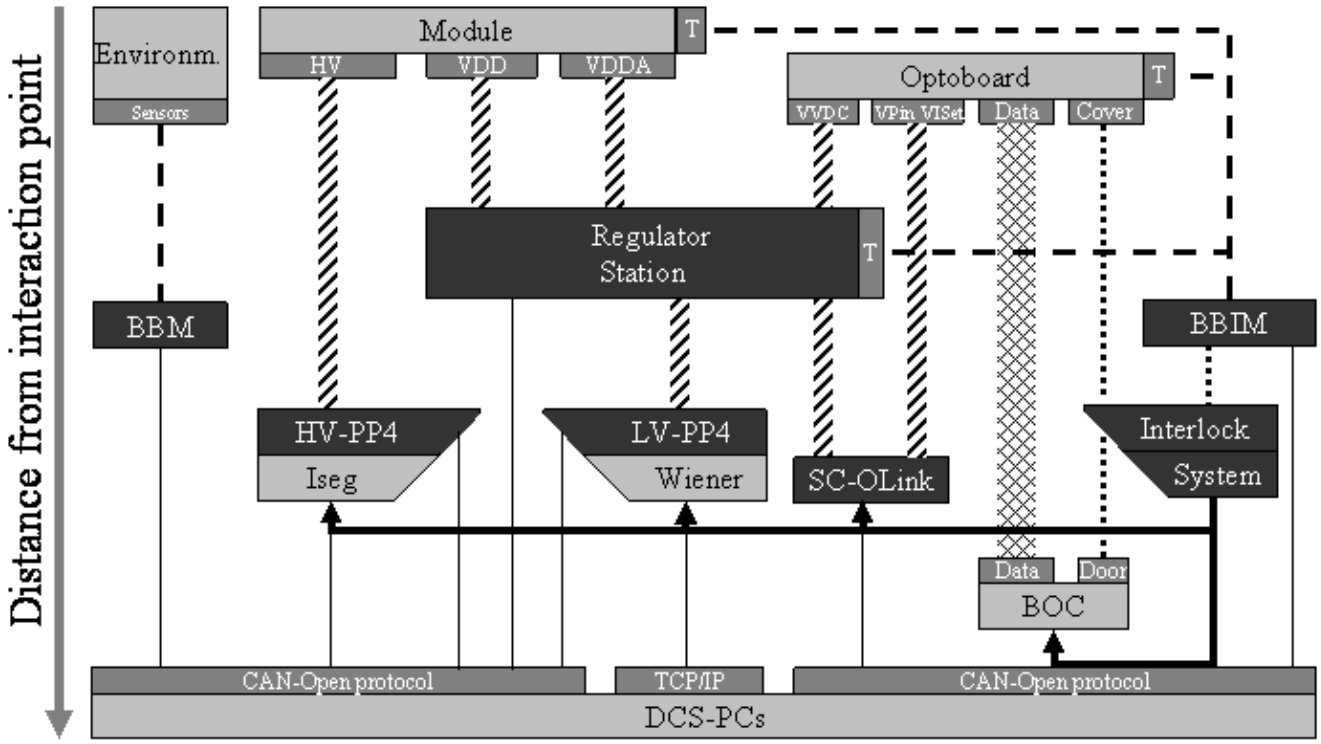
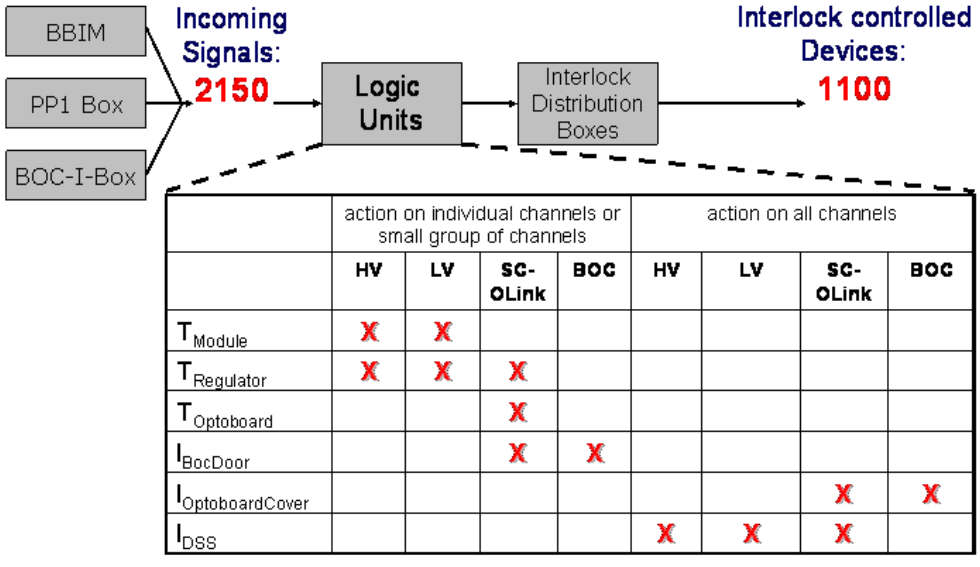


Figure 1: Overview of the DCS hardware (Interlock System simplified)



	action on individual channels or small group of channels				action on all channels			
	HV	**LV**	**SC-OLink**	**BOC**	**HV**	**LV**	**SC-OLink**	**BOC**
T_{Module}	X	X						
$T_{Regulator}$	X	X	X					
$T_{Optoboard}$			X					
$I_{BocDoor}$			X	X				
$I_{OptoboardCover}$							X	X
I_{DSS}					X	X	X	

Figure 3: Schematic overview of the Interlock System and the action matrix