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# The ALICE Silicon Pixel Detector control system and on-line calibration tools

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**On behalf of the Alice Silicon Pixel Detector project**

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Abstract: The ALICE Silicon Pixel Detector (SPD) contains nearly $10^7$ hybrid pixel cells. The operation of the SPD requires on-line control and monitoring of some 2000 parameters and $\sim$50000 DACs. Information for each channel is stored in a configuration database. Timing and data management ($\sim$ 6 GB of raw data for each calibration) are critical issues. An overview of the SPD electronics read out chain and of the detector control system is given with a detailed description of the front-end controls and the calibration strategy. The status of commissioning and a preliminary evaluation of the detector performance are presented.

Keywords: Solid state detectors; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Detector alignment and calibration methods (lasers, sources, particle-beams).

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## Contents





## 1. Introduction

The operation of the ALICE Silicon Pixel Detector (SPD) requires the on-line control and monitoring of a large number of parameters. This task is performed by the SPD Detector Control System (DCS). The DCS has also a key role in the calibration of the detector. These combined functions increase the complexity of the system, whose main features are presented and discussed in the following sections.

## 2. Main features of the electronics system

The SPD (see figure 1) constitutes the two innermost layers of the ALICE Inner Tracking System (ITS) at radii of 3.9 cm and 7.6 cm, respectively.

The detector consists of 120 half-staves (HS) mounted on 10 carbon fibre support sectors. Five pixel chip ASICs [1], 150 $\mu m$ thick, bump bonded to a 200 $\mu m$ thick silicon sensor containing nearly 41k active hybrid pixel cells with dimensions of $50\mu m(r\phi) \times 425\mu m$ (z) are forming a ladder. A HS is an assembly of two ladders glued and wire-bonded to a multi-layer interconnect cable (pixel bus) that distributes power and connect the pixel chips to a read-out Multi Chip Module (MCM) [2].

A MCM on each half-stave distributes the timing signals, provides the required analog references and performs data multiplexing and serialization. The communication between the MCM and

**Figure 1.** CAD design of the full SPD.

the counting room is via optical links on three single-mode fibres. The front-end electronics clock frequency is 10 MHz. The readout data stream uses a G-link compatible protocol with an 800Mb/s clock.

Zero suppression and data encoding are performed in the Link Receiver mezzanine cards (LRx) in the VME based Router readout modules. One Router with three LRx cards [3] serves a half sector (6 half-staves) and has optical links to the experiment DAQ and trigger system.

A unique feature of the SPD is that it can provide a prompt multiplicity trigger within the latency of the L0 trigger (850ns) [4].

The LV power supply requirements for the front-end electronics on each HS are 1.85V ($\sim 6A$) for the pixel bus and 2.6V ($\sim 0.5A$) for the MCM. The LV power supply (PS) system is based on 20 CAEN A3009 LV modules (12 LV channels each), housed in 4 CAEN Easy3000 crates located in the experimental area. Detector bias ($50 \div 100$ V, $< 7\mu A$) is provided by 10 CAEN A1519 HV modules (12 HV channels each) housed in a CAEN SY1527 mainframe located in the counting room. The SY1527 communicates with the software layer via ethernet (TCP/IP). The SY1527 communication with the LV modules is via a CAEN A1676 branch controller.

The FE electronics power dissipation is $\sim 1.3kW$. Cooling is based on an evaporative system with $C_4F_{10}$. The cooling plant provides one main cooling line for each SPD sector. Each line feeds 6 cooling capillaries, embedded in each sector, to which the staves are thermally coupled by means of thermal grease. The operating temperature of the detector is $\sim 25^oC$. The cooling plant is controlled by a PLC. Communication with the control PC is via ethernet (TCP/IP) using the OPC Server-client protocol. Efficient cooling is vital for this very low mass detector. Without cooling the detector temperature would increase at a rate of $1^oC/s$ . The detector temperature is therefore a critical parameter that must be monitored online and safety interlocks must be activated immediately upon problem. On each HS surface two series of 5 temperature sensors (Pt1000) are mounted. One group of Pt1000 resistors (120 in total) is read out via analog modules in a dedicated



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PLC that generates the corresponding temperature interlocks and sends online the detector temperatures readout, via ethernet, to the counting room. The second group of Pt1000 resistors (120 in total) is read out via the MCM that sends the resistances values to the off-detector electronics in the counting room (see section 6 for more details).

## 3. Detector operation issues

The operation of the SPD requires a tight control of many parameters such as timing, the pixel bus power supply voltage (Vdd), the reference voltages provided by an analog ASIC on the MCM (Analog Pilot [5]), and the settings of the various DACs in each front-end pixel ASIC. The objective of the SPD calibration is to adjust these parameters in order to obtain the highest efficiency and response uniformity of the pixels matrices. The pixels are practically based on a noise-free readout. Dead and noisy pixel identification is performed as part of the calibration phase.

Calibration is mainly performed using test pulses (TP) that can be generated in each FE chip. The pulses can be sent independently to each single pixel; the amplitude is programmable and is controlled by the Analog Pilot. The detector efficiency and the uniformity of response of the pixel matrices are studied by varying the pulse amplitude at various threshold settings (S-curves) [7].

The list of the noisy and dead channels is important for the offline particle tracks reconstruction.

The SPD has the capability to provide a prompt multiplicity trigger through its Fast-OR pulse. It is generated in each pixel chip when a particle hit is detected. The Fast-OR contributes to the L0 trigger input of the ALICE Central Trigger Processor (CTP). The Fast-Or efficiency is influenced by the settings of various pixel chip internal DACs. The Fast-OR characterization is an important step in the calibration phases.

Several calibration procedures are implemented using the TP and particles.

(a) DAC scan: a sequence of triggers is applied to the detector under test, using TPs or particles (radioactive sources during the integration phase and the particles produced by the interactions during the experiment data taking), while varying the references generated by the Analog Pilot and/or the DACs in the pixel chip. For each DAC value, the average efficiency of response and the average multiplicity are determined.

(b) Mean Threshold scan: the uniformity of the pixel matrix is studied by varying the TP amplitude. For each pixel, the efficiency of response is determined as a function of the threshold DAC setting. The TP amplitude that gives an efficiency of 50% represents the equivalent in voltage of the applied threshold.

(c) Uniformity scan: a sequence of TPs is applied to each pixel with an amplitude larger than twice the Mean Threshold of the chip. The uniformity of the response of the pixel matrix is determined from the response efficiency distribution (ratio of hits to pulses).

(d) Noisy and dead pixels identification.

(e) Fast-Or characterization: a sequence of TPs is applied to one pixel at a time. The efficiency map of the pixel matrix is determined from the corresponding number of generated Fast-ORs.



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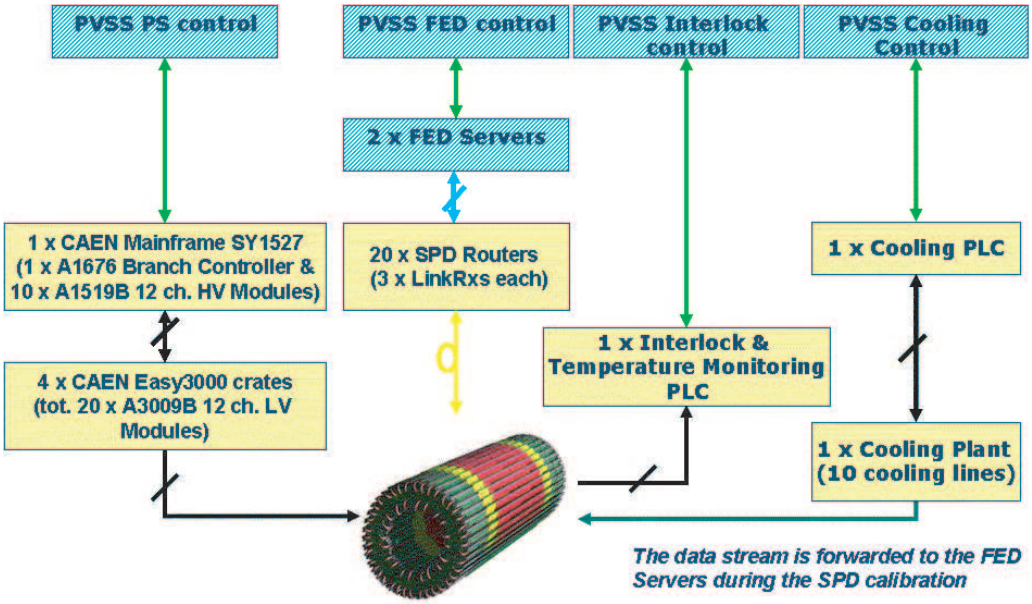


**Figure 2.** Block diagram that shows the SPD branches of the detector control system.

Automated configuration and calibration procedures are implemented in the Detector Control System that is also able to emulate the ALICE DAQ and trigger system.

The calibration raw data from the 1200 FE chips are analyzed online either by the DCS or by the DAQ system. The calibration sequence is iterated until the optimum parameter settings is determined. These settings, including FE chip DACs values, MCM chips configuration and power supplies voltages, are stored in an Oracle based configuration database. The configuration versions are tagged in function of the run (PHYSICS p-p, PHYSICS Pb-Pb, CALIBRATION, BEAM TUNING) for which they will be applied.

## 4. Control system

The system is based on a commercial Supervisory Control And Data Acquisition (SCADA) named PVSS. Five PVSS projects are running independently on different working nodes to control, respectively the cooling system, the Power Supply (PS) system, the interlock and monitor system and the FE electronics; the fifth project links together and monitors the 4 sub-system projects. In the future it is also planned to integrate the control of the Pixel Trigger electronics in the SPD DCS. A block diagram that represents the HW/SW interconnection is shown in figure 2.

Each main hardware branch is connected directly to an independent PVSS project that bridges the hardware with the logical control of the full system carried out through a Finite State Machine (FSM). The FSM is implemented using the State Management Interface (SMI++) [9].

The FSM receives the status (i.e. READY, NOT READY, ERROR) of the SPD sub-systems, and performs start-up, shut-down and standard operation procedures as well as emergency routines e.g. during cooling failures according to pre-defined sequences. The operation phases of the detector are controlled via a FSM.



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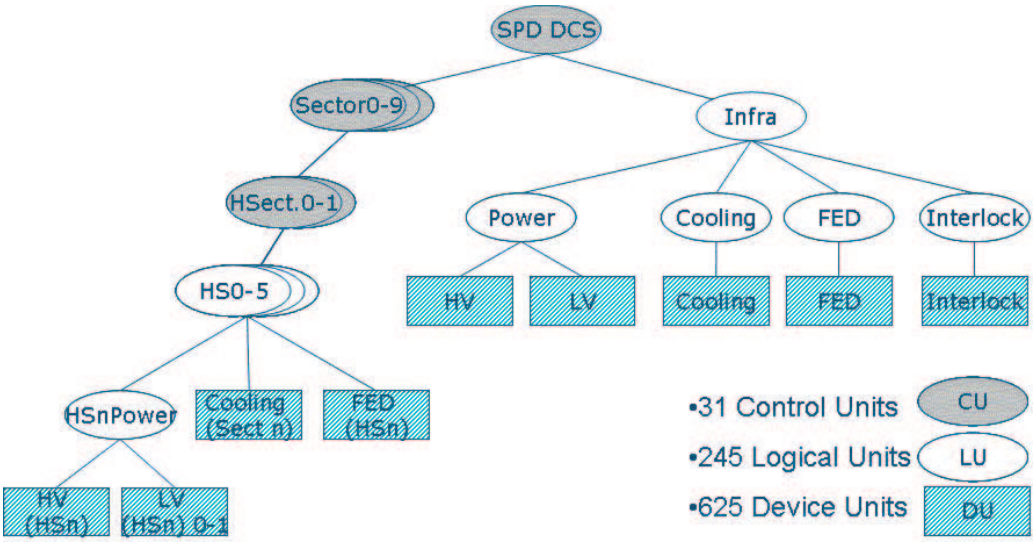


**Figure 3.** The SPD Finite State Machine hierarchy blocks diagram.

The lowest FSM software layer is formed by Device Units (DU) capable of sending instructions to the PVSS layer and provide to the upper layers a hardware state. The DUs can be connected together either via Logical Units (LU) or via Control Units (CU) that generate states as functions of their child processes states. The LU and CU are sending commands to the underlying level on the FSM hierarchy. The CU and its child processes form a logical domain and can run autonomously on a different computer but their use is limited by the CU high RAM consumption (5 MB/CU).

The FSM itself forwards the SPD status to the ALICE Experimental Control System ECS. Commands from the ECS are sent to the sub-systems from the top of the FSM to the bottom DUs.

The SPD FSM hierarchy is shown in figure 3. The SPD FSM top node *SPD DCS* has 11 branches: 10 to control the 10 SPD sectors and one dedicated to the SPD infrastructure. The SPD infrastructure such as power supply mainframe, crates and cooling are implemented in the *Infra* LU (right hand branch in figure 3). The state of the *Infra* LU is READY when all required infrastructure services are fully operative, otherwise the SPD DCS top node switches off the power supplies of all detector sub-systems. Once the Infra-LU reports the READY state configuration and data taking is initiated via the 10 sector CUs (left hand branch in figure 3).

Each sector CU (*Sector0-9*) is partitioned in 2 half-sector CUs (*HSector0-1*) including 5 half stave (*HS0-5*) LUs. The HS LUs retrieve information from the cooling system and switches off the power supplies in case of anomalies.

The HV and LV DUs are linked together via a LU (*HSnPower*) that provides the proper HS power-up and power-down sequence.

A set of macro-instructions is provided by the HS LU to the FE control DU that can execute monitoring, control and detector calibration. The SPD is ready for physics or for calibration when the on-detector and off-detector electronics is configured. Different sets of configuration parameters are making the switch between different SPD states e.g. calibration and physics.

The system comprises 31 CUs to provide the detector partitioning at the half-sector level. This structure allows to debug a detector subset without interfering with the normal data taking. The

SPD FSM contains 245 LUs and 625 DUs.

Each PVSS software layer contains translator scripts capable of converting macro-instructions into the sequence of operations required for the hardware. Background scripts continuously monitor the status of the hardware and take automatic actions to protect the system in case of abnormal states.

The PVSS layer controlling the PS system allows to upload the prescribed voltage settings in the SY1527 mainframe. The parameters are retrieved from a specific Oracle Configuration database (CDB). All voltages and currents are monitored online and archived during the detector operation phases. A HS power-up and power-down sequence is foreseen to activate or deactivate sequentially MCM, detector (HV) and FE chip supply. The sequence is controlled via the FSM. PVSS background scripts are used for monitoring the status and taking corrective actions if necessary.

The FED DUs control two Front End Device (FED) Servers (C++ based), one for the detector side A and one for side C. The FED Server is a stand alone application consisting of three software layers. The top one hosts a Distributed Information Management System (DIM - TCP/IP) server that allows the communication with the PVSS layer. The intermediate FED application layer hosts all the logical functions required. It retrieves the commands received by the DIM server, checks the hardware status, pulls or stores the data from/to the database and communicates with the driver layer to perform the required operations on the hardware. The FED server state machine is hosted in the application layer. The bottom software layer is the driver for the VME access to the off-detector electronics.

The system structure allows fast remote operator intervention and is highly modular. The communication between the different software applications is carried out via DIM. Most processes are fully automated in order to obtain the required reliability and safety of operation.

The power system (HV and LV) and the cooling system are controlled directly by PVSS.

The FSM represents also the operator interface to the detector and allows the interconnection to the general ALICE DCS.

## 5. Calibration procedures

The system is designed to allow fast and automated calibration procedures. The calibration of the full detector will be carried out during the LHC fill time ($\sim$ 70 mins); the updated configuration settings are calculated automatically.

Two calibration procedures can operate independently: DCS_ONLY and DAQ_ACTIVE. Using the DCS_ONLY procedure the ALICE DAQ and trigger system are emulated by the DCS system. This procedure is slower than the DAQ_ACTIVE during the data acquisition but allows calibration and debugging of a detector subset without interfering with the data acquisition of the other detector partitions. The block diagram of the DCS_ONLY procedure is displayed in figure 4. In this procedure the main detector data stream is forwarded to an internal Router dual port memory accessible via the VME bus. The PVSS and the FED servers perform the detector configuration and status monitor. The Routers then send triggers and data are read back via VME by the FED servers acting as software data buffer. The detector data are sent to a ROOT [8] based analysis tool. The tool defines the updated configuration and stores it in the CDB. The analysis results are stored in ROOT format files and forwarded to an Exchange File System (EFS) that allows the



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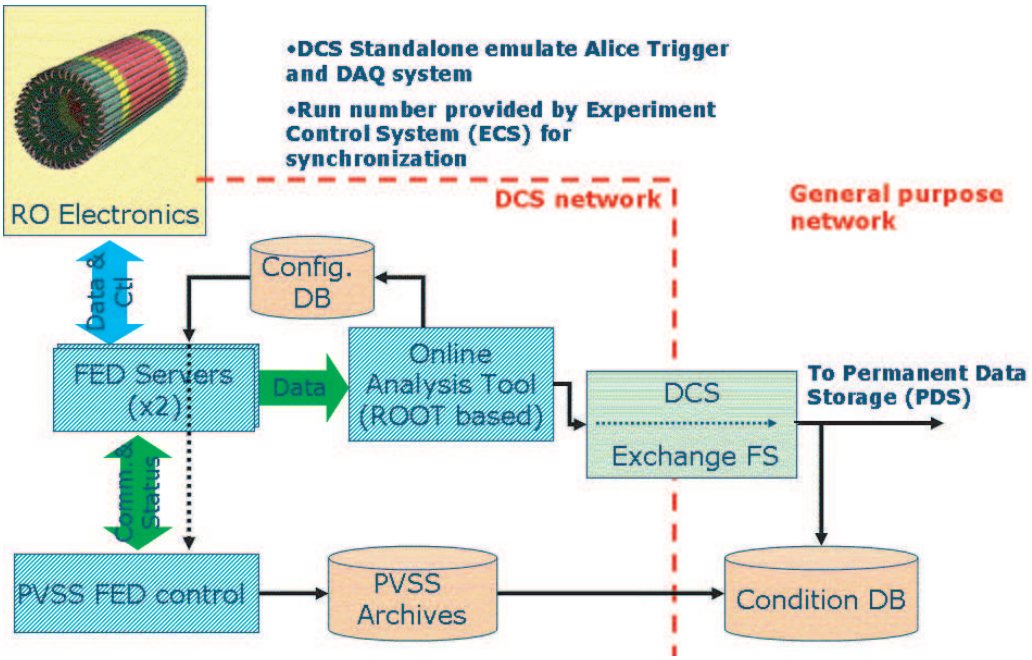


**Figure 4.** A block diagram of the DCS_ONLY calibration procedure.

communication with the offline network and the Permanent Data Storage (PDS). The analysis tool is controlled and retrieves the configuration parameters needed for the data analysis by PVSS. The communication between the 3 software tools such as PVSS, FED servers and Analysis Tool is performed via DIM. When the calibration is completed the DCS automatically moves the FSM from the calibration state to a standby state.

The Experiment Control System (ECS) is the user interface to the detector in operation. The ECS controls the ALICE sub-systems such as DAQ, DCS and Trigger. In the DCS_ONLY calibration procedure, the ECS sends the calibration start command to the DCS and disables the other two sub-systems. A new run can be started only when the DCS leaves its calibration state.

The DAQ_ACTIVE calibration procedure requires the DCS, DAQ and Trigger systems all to be active. A block diagram of this procedure is displayed in figure 5.

In this configuration the ECS issues the calibration start command to the different sub-systems and waits for confirmation of configuration executed by the DCS. Depending on the required calibration mode either the Trigger system or the Routers generate the readout sequences. The data are recorded in the DAQ Local Data Collectors (LDC). When the calibration procedure is completed, the ECS starts a set of LDC preprocessing scripts. These scripts analyze the raw data and generate ROOT files with the distributions of the detected hits on the pixel matrices (hit-maps). The files are forwarded automatically to a second level of processing that extracts the parameters needed for the reconfiguration of the detector. The processed and pre-processed data files are sent to the EFS that forwards them to the PDS, the CDB and the condition database used for track reconstruction. When this sequence of operations is completed the ECS closes the run and the system is placed in a standby condition.

The calibration procedure start request and the SPD sub-systems configuration request is per-



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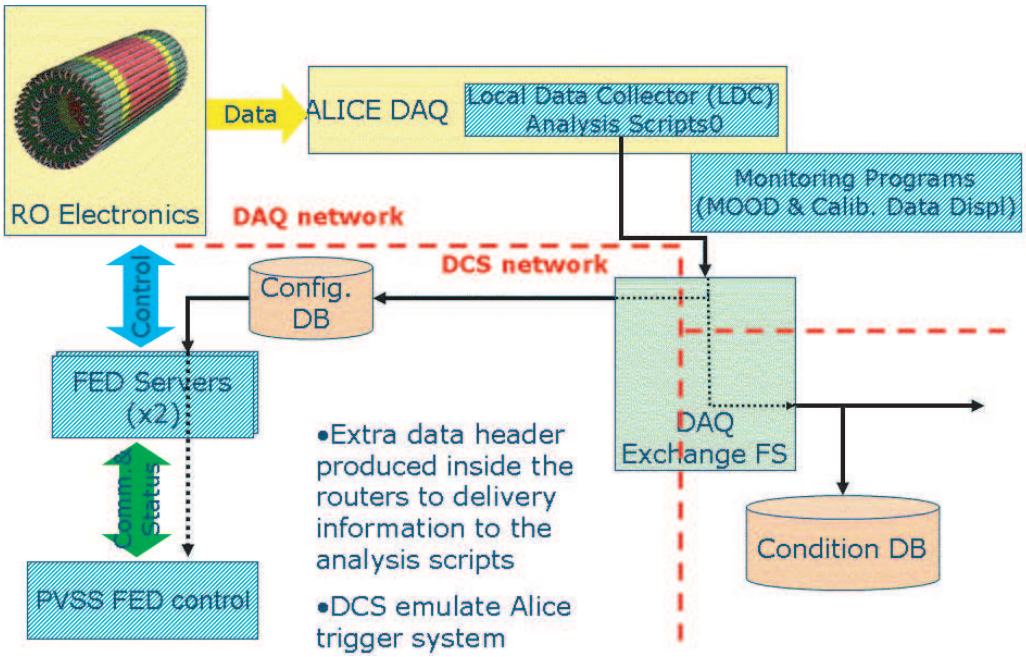


**Figure 5.** A block diagram of the DAQ_ACTIVE calibration procedure.

formed by the ECS. The two calibration procedures have been implemented in the system test facility at CERN and are used for the SPD sector characterization. Up to now 10 SPD sectors have been tested and the first five sectors have been tested again after the integration in the SPD half barrel.

The DAQ_ACTIVE procedure allows the fast calibration of the full detector using the parallel data readout functionality.

## 6. Safety interlocks

Efficient cooling is vital for this very low mass detector. In the case of a cooling failure, the detector temperature increases at a rate of $1^{o}C/s$ . The detector temperature is therefore a critical parameter to be monitored online and requires immediate activation of a safety interlock upon problems. The maximum temperature allowed for the detector is $40^{o}C$ and the interlock threshold is set at $35^{o}C$. Four levels of hardware interlocks and two levels of software interlocks are foreseen as displayed in figure 6. Each HS is equipped with 2 independent series of 5 temperature sensors (Pt1000) each. Any readout chip is associated which a Pt1000 sensor in order to monitor the status of the full HS. One of the series is readout by the Analog Pilot on the MCM and the data are encoded in the readout data stream. The Routers read the temperature values and assert the interlocks if needed. The other series are connected to analogue PLC modules. Two independent temperature monitoring systems have been foreseen for redundant measurements and improvement of the safety level.

The PLC scans the 120 chains in less than 1s. The hardware interlock lines are processed in a card with Single Event Upset (SEU) mitigation circuitry that provides direct safety interlock lines to the 20 LV power modules (one for each half-sector). The temperature readouts are also sent online to the counting room via an ethernet link.



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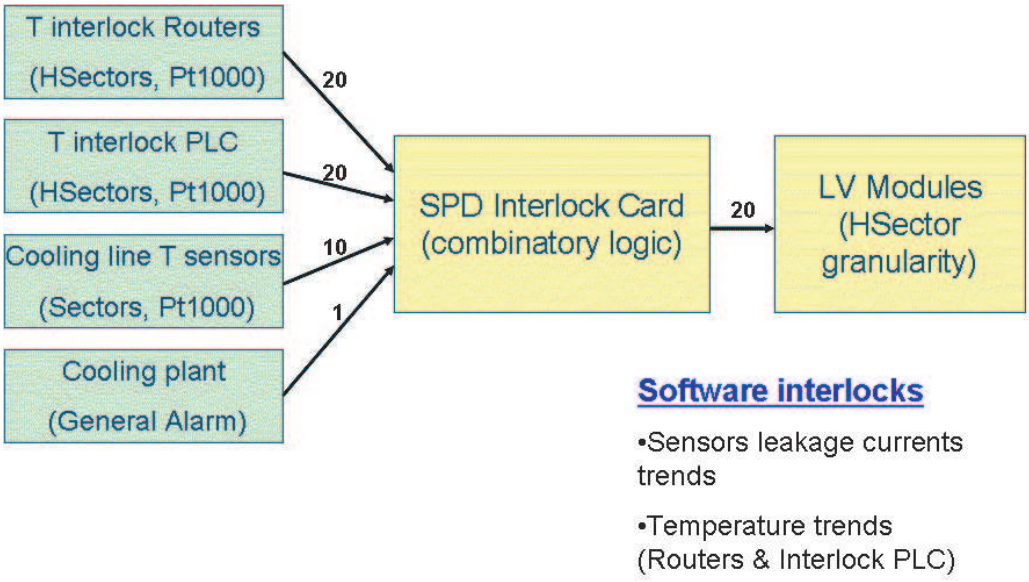


**Figure 6.** A block diagram of the SPD interlock interconnections.

On the cooling lines tempera-ture sensors have been placed. They are read back via the temperature monitor PLC. The PLC and the Routers continuously monitor temperature trends and assert preventive interlocks if malfunctions are observed. The detector bias current roughly doubles each increase of temperature of 8$^{o}$C. The PVSS controlling the power supply system monitors constantly the sensor bias currents and in case of dangerous trends it switches off the corresponding HS.

A set of PVSS scripts run in the background to provide the proper overall power-down sequence in case of a part of the system is switched off by a hardware interlock.

## 7. SPD integration and commissioning

The final test, integration and commissioning of the SPD is carried out in a dedicated area inside the Divisional Silicon Facility (DSF) at CERN. The area is equipped with the final cooling plant, power supply system, readout electronics and control system including temperature monitoring and safety interlocks. The DAQ system is a subset of the ALICE DAQ but with all the functionality. The trigger system is the final SPD partition.

The main objective is to test and commission the full detector with all the final systems and services before installation in the experimental area. Two FED servers are implemented and operational. Three working nodes are used to run the FSM, the DCS data analysis tools and the PLC for temperature monitoring and safety interlock.

The sectors are characterized in the DSF and the configuration parameters retrieved are stored in the CDB to generate a startup set for the ALICE operation.

At the time of writing 10 sectors and the first half barrel have been tested. The mechanical integration of the second half-barrel is almost finished.

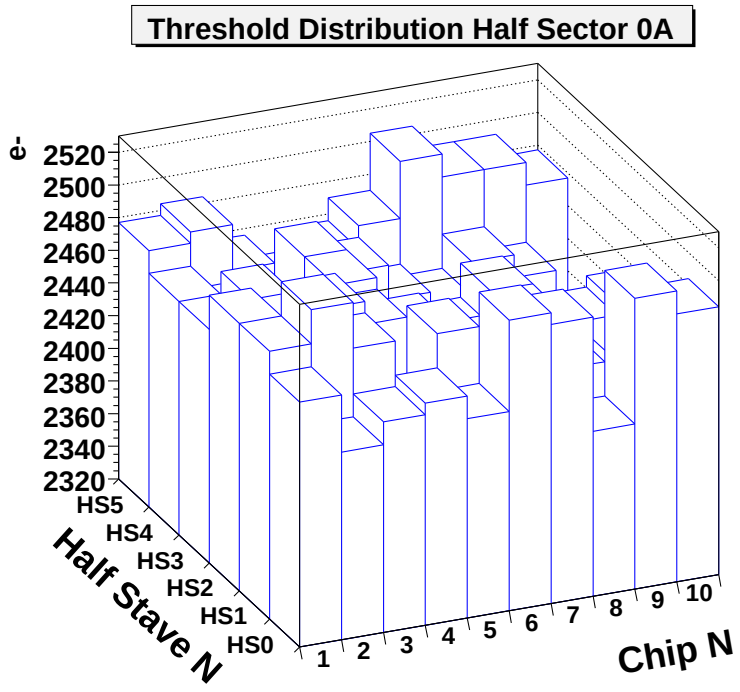


**Figure 7.** A histogram displaying the mean threshold distributions of the half sector 0, side A, FE chips.

## 8. SPD preliminary sector test results

During the commissioning phases the performances of the 10 sectors produced have been evaluated. The operation point of every HS has been verified in terms of minimum threshold, bias voltage and number of working pixels. The results obtained are in agreement with those found in the preceding HS production tests. Pixel matrix uniformity measurements have been performed using TPs. A good response uniformity of all the matrices was found while applying a TP equivalent of $\sim 5000e^-$ and applying a common threshold of $\sim 2500e^-$. Few pixels ($< 1\%$) did not respond correctly due to bump bonding problems and electrically malfunctioning pixels.

Combining the results of the electrical test pulse and the source measurements, a mean threshold of $\sim 2500e^-$ with an RMS noise of $\sim 200e^-$ has been found for all the HSs. In figure 7 the mean threshold distribution for one half sector is displayed. The test pulse has been calibrated and a conversion factor of $\sim 66e^-/mV$ has been determined [7].

The mean threshold has been evaluated individually reading single HSs and during the full sector readout. These measurements demonstrate that the system is not sensitive to common noise or cumulative effects. The values of mean threshold and RMS noise remained unchanged for both configurations of readout.

The measured mean threshold for all the HSs tested is in agreement with the operational requirements for ALICE.

The noisy and dead channels have been identified studying the uniformity of response of the pixel matrices and via dedicated noisy runs. The ratio of noisy and dead channels over the total

number of pixels is $10^{-5}$. All the noisy pixels identified can be masked in the FE chips and they will not influence the offline track reconstruction process.

The temperature distribution over the HSs has been analyzed and it is stable at $32 \pm 3^{o}$C on the HS surface, while the cooling system operates, without load, at $17^{o}$C. This measurement was carried out using a thermal camera and the two independent Pt1000 chains mounted on each HS.

The interlock system reacts in less than 2 s and the full detector configuration is performed in less than 60 s.

At the time of writing the first SPD half barrel is used to collect data with cosmic rays.

## 9. Summary

The SPD control system has been developed and it is used for the test, integration and commissioning of the sectors and the half-barrels, in conjunction with the final detector readout electronics and services in the dedicated area at the CERN DSF. The integration with the ALICE DCS and DAQ is nearing completion. The detector FSM prototype is operational and it has been integrated in the ECS.

The calibration procedures have been developed and implemented in the system test. Measured performance matches the challenging requirements as reported.

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