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# METROLOGICAL CHARACTERISATION OF A FAST DIGITAL INTEGRATOR FOR MAGNETIC MEASUREMENTS AT CERN

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# METROLOGICAL CHARATERIZATION OF A FAST DIGITAL INTEGRATOR FOR MAGNETIC MEASUREMENTS AT CERN

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**Abstract:** A Fast Digital Integrator (FDI) was designed to satisfy new more demanding requirements of dynamic accuracy and trigger frequency in magnetic measurements based on rotating coil systems for analyzing superconducting magnets in particle accelerators. In particular, in flux measurement, a bandwidth up to 50-100 kHz and a dynamic accuracy of 10 ppm are targeted. In this paper, results of static and dynamic metrological characterization of the FDI prototype and of the Portable Digital Integrator (PDI), heavely used at CERN and in many sub-nuclear laboratories, are compared. Preliminary results show how the initial prototype of FDI is already capable of both overcoming dynamic performance of PDI and covering operating regions inaccessible before.

**Keywords:** Converters, Magnetic Materials/Magnetics, Particle Accelerator Science & Technology/Nuclear and Plasma Sciences, Signal Analysis/Signal Processing.

## 1. INTRODUCTION

The Large Hadron Collider (LHC), currently in construction at CERN, is a particle accelerator designed to explore into the deepness of the matter more than ever done before. The 27 km long LHC is based on more than 8000 superconducting magnets. The trajectories of the particles beams are corrected by means of magnets; thus, an accurate measurement of the field quality is necessary to implement a suitable control of the trajectories as well as to focus the beam.

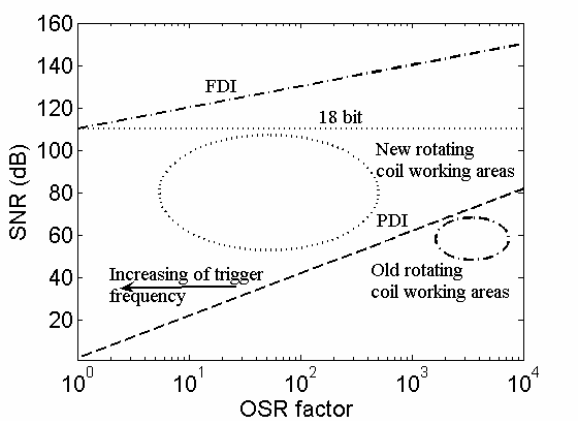



**Fig. 1.-PDI and FDI theoretical performance.**

Many magnetic measurement techniques are used at CERN, such as fixed coils for measuring the field variation, the flip coils for calibrating the coil, the Hall sensor for having a 3D description of the field [1]. The most accurate technique to figure out the magnetic field harmonics of a superconducting magnet is based on rotating coils, giving as output a voltage signal to be integrated by a suitable digital system [1]. The magnetic flux is measured between two angular positions measured by an encoder giving the trigger to the voltage integrator. The Portable Digital Integrator (PDI) is being used for about twenty years at CERN and in other international laboratories. Magnets are characterized by integrating along about 10 s the output voltage of a rotating coil, turning at maximum at 1 rps [2]-[5]. A new generation of rotating coils with a higher rotation speed up to 10 rps is developed at CERN for LHC and more advanced applications [6]. It will allow the dynamic effects of superconducting magnets to be figured out over a larger bandwidth up to 50-100 kHz and with higher target dynamic accuracy for the integrator system of 10 ppm (Fig. 1).

PDI is based on a voltage-to-frequency converter, therefore its performance get worse if the Over-Sampling Ratio (OSR) decreases, i.e. the coil trigger frequency increases (Fig. 1). Thus, measurement speed can not be increased now and PDI gets unsuitable for new requirements, especially for varying magnetic fields.

A new instrument has been conceived at CERN, the Fast Digital Integrator (FDI) [7]. FDI exploits a high-rate and high-resolution digital conversion, whose accuracy is not related to trigger frequency. In addition, it keeps the benefit of a larger OSR, owing to its maximum sampling rate of 800 kS/s (Fig.1).

In the following, in Section 2, the design proposal of the FDI measurement chain is recalled. In Section 3, preliminary experimental results of FDI metrological characterization are presented by comparing the PDI and FDI performances.

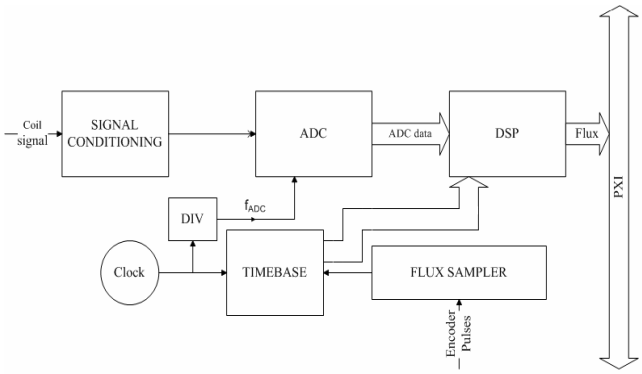



**Fig. 2. – FDI architecture.**

## 2. THE FDI MEASUREMENT CHAIN

The main design challenges are an accuracy requirement of 10 ppm, for 1 s of integration time with a bandwidth of 50-100 kHz, for an input full scale range of 10 V. FDI faces up these requirements by the digital conversion and the numerical integration of the coil signal (Fig. 2). The input signal is sampled at high sampling rate, up to 800 kS/s by means of a 18-bit SAR ADC. Then, the DSP carries out the numerical integration of the samples in the angular domain owing to the trigger pulses of an encoder mounted on the shaft of the rotating coil.

In order to reach the above-mentioned requirements, the design of the analog front-end is particularly critical. In Fig.3, the analog front-end of the FDI, including the ADC converter, the FPGA, and the DAC, is illustrated. The input configuration from the PGA to the ADC is differential. The PGA is an instrumentation amplifier Double Input Double Output (DIDO) providing 13 different values of gain, each one adjustable by a digital trimmer acting on the feedback resistors of the amplifier. The offset is also corrected automatically: a 16-bit DAC injects a compensating voltage at the amplifier input. In particular, the calibration procedure is carried out by three steps: (i) the input amplifier is short-circuited and, after measuring the ADC output code, the DAC output is changed until the null code is reached; (ii) for the selected gain, a suitable voltage reference coming out from the Voltage Reference Generator (VRG) of the board is applied to the PGA in order to reach a full scale signal at the ADC input; the gain is adjusted by means of a digital trimmer until this condition is not reached; the value of the digital word of the trimmer is stored in a non-volatile memory to trace the calibration; (iii) the coil is connected to the PGA input and the offset compensation procedure, as described at point (i) is launched to correct the offset generated by the coil resistances; the value of the DAC digital word is stored in a non-volatile memory. This procedure is carried out automatically by means of a dichotomyc algorithm to in order to minimize the time operation.

## 3. EXPERIMENTAL RESULTS

The FDI prototype and the PDI were characterized by carrying out dynamic and static tests, according to the standard IEEE 1057-1994 [8]. In the following, (i) the *measurement station* (ii) the *static tests* and (iii) the *dynamic tests* are reported.

### *3.1 Measurement station*

The DC performance was assessed by the Differential Non Linearity (DNL), and the AC performance by the Signal-to-Noise Ratio (SNR) through a FFT test. A metrological station was set up in order to carry out metrological tests on both PDI and FDI (Fig. 4). The station is based on DC DATRON 4000A and AC DATRON 4708 calibrators, remotely controlled via GPIB bus. Software applications were developed in MATLAB™ and LabVIEW™ (Fig. 4). The IEEE 1057-1994 standard provides common terminology and test methods for describing the performance of digitizing waveform recorders. Both the instruments considered in this work are digital integrators; however they can be seen as ADC. In fact, PDI is based on a VFC, then, according to

$$V_k = \frac{N_k * FS}{t_m * f_{clock}} \qquad (1)$$

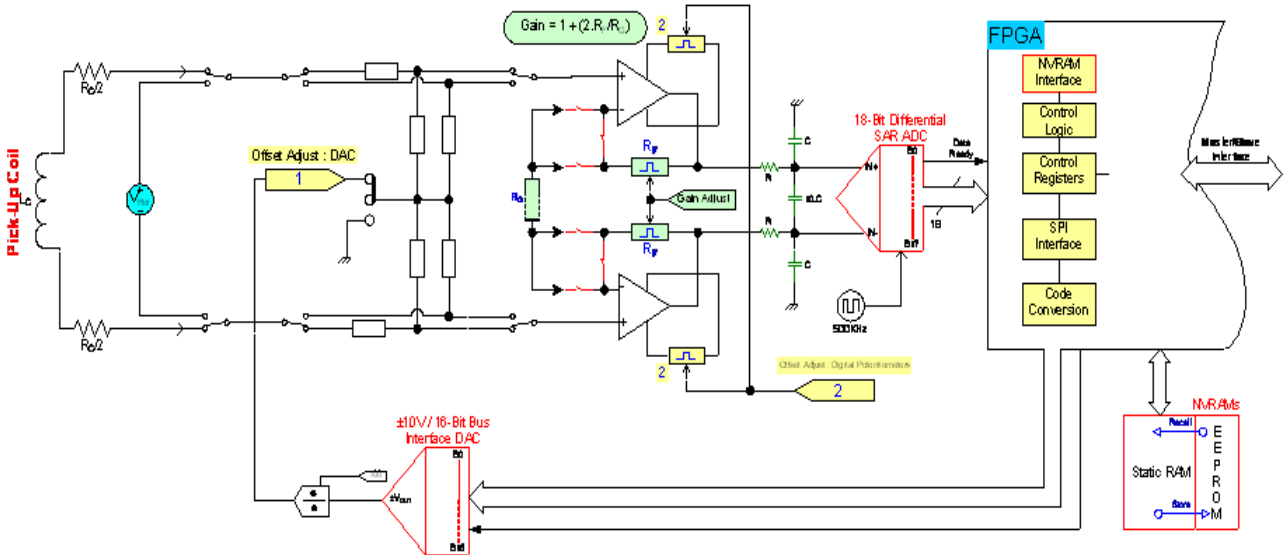



**Fig. 3. – FDI analog front-end scheme.**

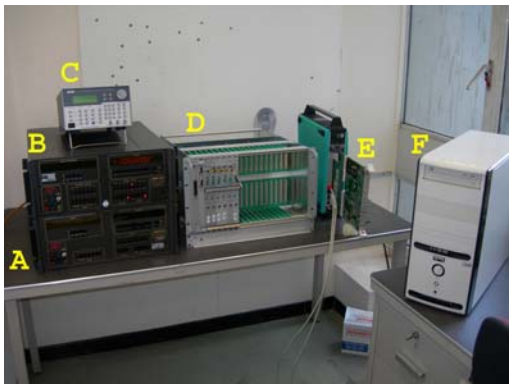



**Fig. 4. – The measurement station: A) DC calibrator DATRON 4000; B) AC calibrator DATRON 4708; C) Function generator TTi TG1010; D) PDI rack; E) FDI board; F) PC for data analysis.**

where $N_k$ is the number of counts at the output of the VFC with a frequency $f_{clock}$, in a measurement time $t_m$, and FS is the full scale range of the instrument in volt, the digital voltage output, $V_k$, can be evaluated by knowing the measurement time, that is the reciprocal of the trigger frequency. The function generator TTi TG1010 was used to generate the trigger (Fig. 4). It is noted that the trigger frequency, i.e. the PDI sampling rate, is inversely proportional to the PDI resolution.

The FDI measurement chain is a waveform digitizer; given that the ADC has a SAR structure, the FDI resolution is not dependent on the sampling rate that can be much higher than the trigger frequency. In order to compare PDI and FDI performance, the same throughput rate must be considered; owing to this, the FDI can benefit of a large over-sampling provided by the ratio between the ADC sampling rate and the considered trigger frequency.

### *3.2 Static tests*

The static test determines the DNL by measuring the transition levels of the ADC [8]. The PDI number of bits and the LSB are function of the trigger frequency. For the test a trigger frequency of 512 Hz was chosen, because this value represents a typical working condition. For a trigger frequency of 512 Hz, PDI has an LSB of 10.24 mV and the theoretical number of bit is 9.93 for a total number of transition levels of 975. The number of bit N is calculated as:

$$N = \log_2\left(\frac{FS}{LSB}\right) \qquad (2)$$

where LSB is the PDI resolution, evaluated by putting $N_k$ equal to 1 in (1), and FS is the full scale range of the PDI (10 V).

FDI resolution is 38 μV, with a full scale range of 10 V and a theoretical number of 18 bit; consequently, the transition levels are the 262143. This number is very huge, and the complete test would take a very long time, thus the DNL was computed on 13 groups of 7 thresholds for the PDI, and on 7 groups of 29 thresholds for the FDI (Tab. 1). In this way, it was possible to assess the DNL in local parts of the input range. Both PDI and FDI show a very good linearity

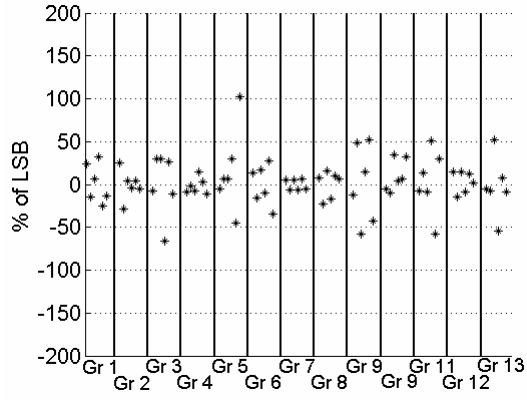
**Table 1. - Input range groups for DNL measurement: (a) PDI, (b) FDI.**

a)

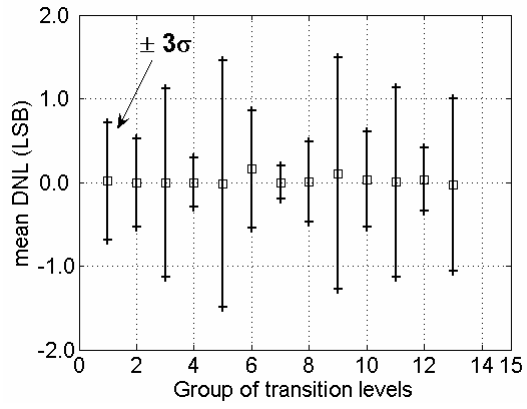
| Group | $V_{min}$ (V) | $V_{max}$ (V) |
|---|---|---|
| 1 | -3.999627 | -3.937339 |
| 2 | -3.037070 | -2.975974 |
| 3 | -2.032307 | -1.970925 |
| 4 | -1.530239 | -1.469885 |
| 5 | -1.039737 | -0.968706 |
| 6 | -5.385569 | -0.477423 |
| 7 | -0.035860 | 0.025450 |
| 8 | 0.466277 | 0.527722 |
| 9 | 0.968654 | 1.030345 |
| 10 | 1.469776 | 1.537562 |
| 11 | 1.971068 | 2.034552 |
| 12 | 2.963284 | 3.026860 |
| 13 | 3.927447 | 3.987292 |

b)

| Group | $V_{min}$ (V) | $V_{max}$ (V) |
|---|---|---|
| 1 | -4.540725 | -4.539844 |
| 2 | -2.024787 | -2.023720 |
| 3 | -1.021434 | -1.020492 |
| 4 | -0.015546 | -0.014508 |
| 5 | 0.991289 | 0.992416 |
| 6 | 1.995206 | 1.996313 |
| 7 | 4.509593 | 4.510699 |




a)




b)

**Fig. 5. – PDI DNL in different parts of the input ranges: (a) DNL for different thresholds groups; (b) mean and standard deviation for each group.**

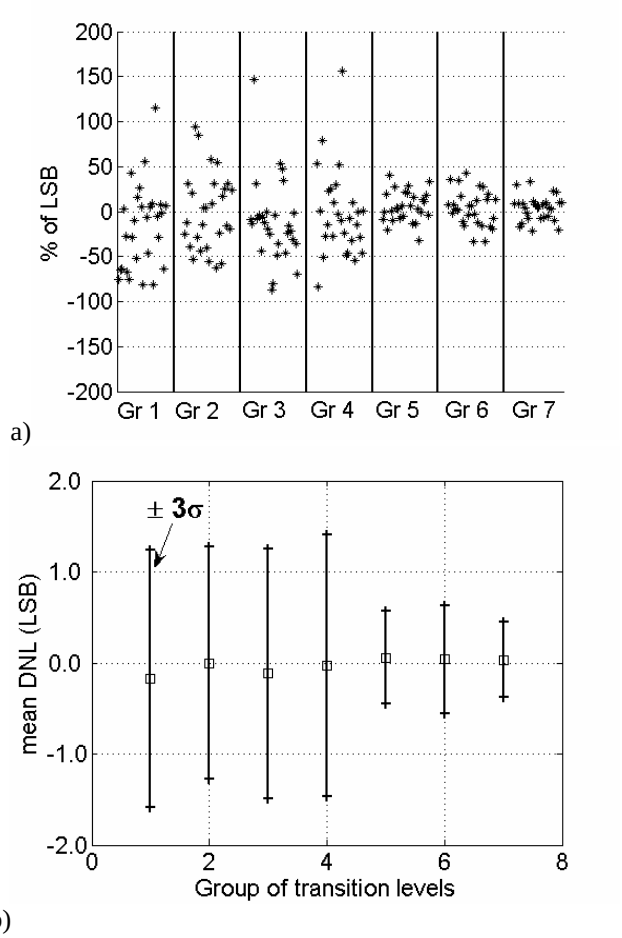



**Fig. 6. – FDI DNL in local parts of the input range: (a) DNL for different transition levels groups; (b) mean and standard deviation for each group.**

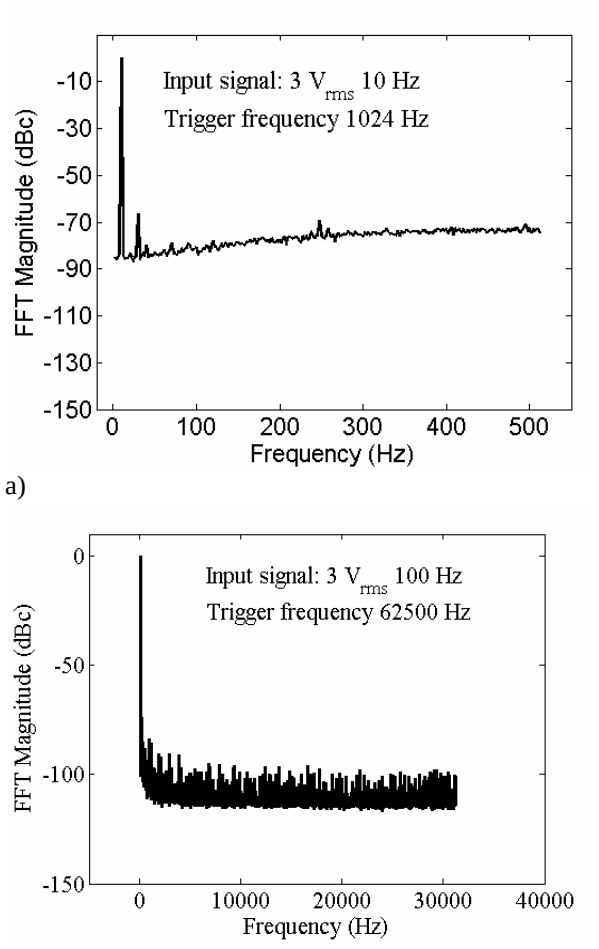



**Fig. 7. – Amplitude spectrum of a PDI (a) and a FDI (b) digitized waveform.**

with a static DNL that is within -1.5 LSB and 1.5 LSB (Fig. 5-6) However, PDI resolution at a typical trigger frequency of 512 Hz is much lower than the FDI LSB.

### *3.3 Dynamic Test*

The dynamic test aims to determine the SNR of the digitized waveform to evaluate the Effective Number Of Bits (ENOB) of the instrument, taking into account the noise and the distortion of all the measurement chain. The SNR was evaluated by the FFT analysis.

For the PDI, the SNR was evaluated at different trigger frequency values, with a sine wave input of 3 $V_{rms}$, at 10 Hz and 20 Hz. The amplitude spectrum of a typical digitized waveform is shown in Fig. 7a. The tests were performed at low frequency according to the typical measurement conditions of the PDI.

For the FDI, tests were carried out with a sine wave input, 3 $V_{rms}$, at a frequency varying from 10 Hz to 250 Hz; then, the SNR was evaluated on the signal decimated by a factor OSR given by the ratio between the sampling rate and the trigger frequency. The amplitude spectrum of a typical digitized waveform is depicted in Fig. 7b. The Spurious-Free Dynamic range (SFDR) for the FDI is around 110 dB against 70 dB of the PDI.

The evaluation of the SNR allows determining the ENOB of the two waveform digitizer: according to the standard IEEE 1057-1994, PDI ENOB results around 9 bit while FDI ENOB is about 12 bit.

In Fig. 8, a comparison between FDI and PDI performance is shown: the SNR is reported as function of the OSR (Fig. 9a) and of the trigger frequency (Fig. 9b). FDI allows to reach a higher accuracy even at high trigger frequency where the PDI cannot operate. However, the benefits of the over-sampling for the FDI does not correspond to the expected ones, because the non-linearity in bandwidth decreases the SNR. Since the static test showed a very good linearity of the ADC, the sources of this linearity must be investigated to get better performance. In particular, the ADC has a unipolar differential input, with a full scale range of 10 V, and a small external interface circuit was required to adapt the PGA outputs to the ADC inputs. Such an interface circuit must be improved.

## 5. CONCLUSIONS

A metrological characterization of the PDI and FDI was carried out. The static tests showed that both PDI and FDI digitizer present a satisfying linearity, although PDI resolution is much lower than the FDI one.

The digital conversion of the coil signal at high sampling rate allows the FDI to achieve better dynamic results than

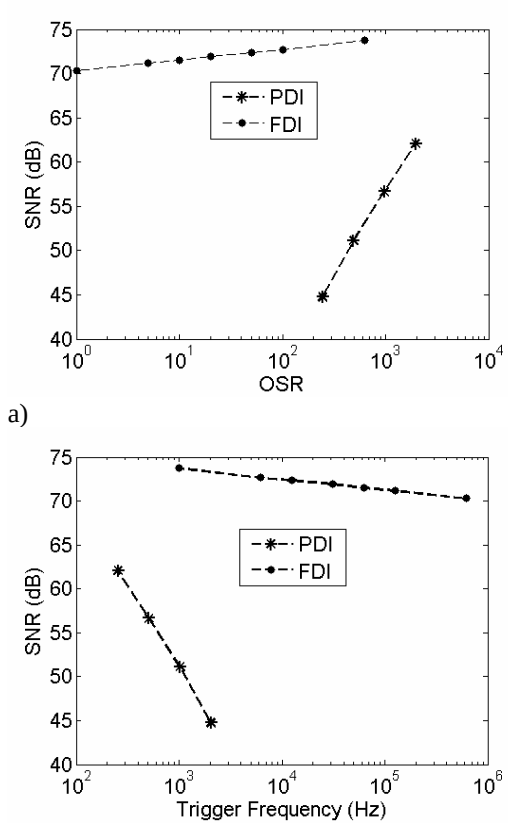



**Fig. 8. – FDI and PDI performance: SNR as function of OSR (a) and of trigger frequency (b)**

the PDI. While the PDI performance decreases to unacceptable targets by increasing trigger frequency, the performance of the second FDI prototype is never lower than 70 dB, even for a theoretical trigger frequency equal to the ADC sampling rate (OSR=1). FDI always benefits of a 18-bit digitization and moreover keeps the benefit of oversampling the input signal for OSR greater than 1.

In further work, the sources of FDI dynamic nonlinearity will be investigated in order to be corrected, by acting on the hardware design and by applying firmware correction by means of the DSP. A third prototype is under construction with the DSP on board and the final design of the analog front-end.

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