## The Octant Module of the ATLAS Level-1 Muon to Central Trigger Processor Interface

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#### Abstract

The Muon to Central Trigger Processor Interface (MUCTPI) of the ATLAS Level-1 trigger receives data from the sector logic modules of the muon trigger at every bunch crossing and calculates the total multiplicity of muon candidates, which is then sent to the Central Trigger Processor where the final Level-1 decision is taken. The MUCTPI system consists of a 9U VME crate with a special backplane and 18 custom designed modules. We focus on the design and implementation of the octant module (MIOCT). Each of the 16 MIOCT modules processes the muon candidates from 13 sectors of one half-octant of the detector and forms the local muon candidate multiplicities for the trigger decision. It also resolves the overlaps between chambers in order to avoid double-counting of muon candidates that are detected in more than one sector. The handling of overlapping sectors is based on Look-Up-Tables (LUT) for maximum flexibility. The MIOCT also sends the information on the muon candidates over the custom backplane via the Readout Driver module to the Level-2 trigger and the DAQ systems when a Level-1 Accept is received. The design is based on state-of-the-art FPGA devices and special attention was paid to low-latency in the data transmission and processing.

#### I. ATLAS FIRST LEVEL MUON TRIGGER

The ATLAS Level-1 trigger [1] uses multiplicities of  $e/\gamma$ ,  $\tau$ /hadron and jet candidates as well as the global energy information from the calorimeters and multiplicities from tracks found in the dedicated muon trigger detectors to generate the final trigger decision. An overview of the muon trigger system is shown in Figure 1 below.

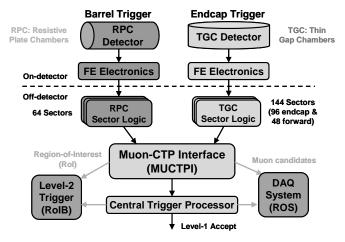


Figure 1: Overview of the ATLAS Level-1 muon trigger

The muon trigger detectors are resistive plate chambers (RPC) in the barrel region and thin-gap chambers (TGC) in the end-cap and forward regions of ATLAS. Coincidences of hits in different detector layers are used to identify muon candidates. The muon trigger electronics also determines the transverse-momentum  $(p_T)$  of the muon candidates and classifies them according to six programmable  $p_T$  thresholds.

The muon trigger detectors are segmented into sectors, 64 for the barrel, 96 for the end-cap and 48 for the forward region. Each sector can identify up to two muon candidates. At every bunch crossing the detector-specific sector logic sends information about the position and  $p_{\rm T}$  threshold of the muon candidates to the Muon to Central Trigger Processor Interface.

# II. MUON TO CENTRAL TRIGGER PROCESSOR INTERFACE (MUCTPI)

The MUCTPI combines the information from all of the muon trigger sectors and calculates total multiplicity for each of the six  $p_T$  thresholds, also resolving possible double counting of muon candidate tracks that traverse more than one detector region, and forwards these multiplicity values to the CTP which takes the final Level-1 decision.

In addition the MUCTPI provides data to the Level-2 trigger and to the DAQ system for events selected at Level-1. The DAQ system receives a formatted copy of the information on candidate muon tracks as well as computed candidate multiplicity. The Level-2 trigger system receives a subset of the candidates, ordered according to decreasing  $p_{\rm T}$ . This information is used to define regions of interest (RoIs) that drive the Level-2 muon-trigger processing.

The MUCTPI has to avoid double counting muons which traverse more than one set of trigger chambers [2], since this would lead to an unacceptably high rate of fake di-muon triggers. This effect is particularly marked for low- $p_T$  muons since their tracks are considerably deflected in the magnetic field of the toroid magnet.

Figure 2 below illustrates the overlap between the barrel and end-cap muon trigger chambers. Tracks for low and high- $p_{\rm T}$  muons are shown in the barrel and end-cap chambers. In addition an example of a muon track that would be detected in both barrel and end-cap systems is shown. The MUCTPI should detect this case and avoid double-counting this muon candidate in the multiplicity sum.

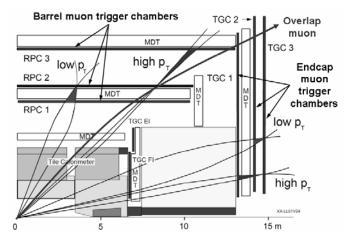


Figure 2: Barrel and end-cap muon trigger chambers

#### A. MUCTPI Architecture

The MUCTPI system consists of a 9U VME chassis with a special backplane and 18 custom designed modules. 16 MIOCT modules each receive the data from one octant in  $\phi$  and one half in  $\eta$  of the muon trigger detectors. The MIBAK backplane sums the multiplicities of all MIOCT modules, provides readout data transfer and distributes timing and trigger signals to all modules. The MICTP module receives the timing and trigger signals and forwards the multiplicities to the CTP. The MIROD module collects information from the MICTP and the MIOCT modules and sends the data after formatting to the Level-2 trigger and the DAQ system. Figure 3 shows the architecture of the MUCTPI.

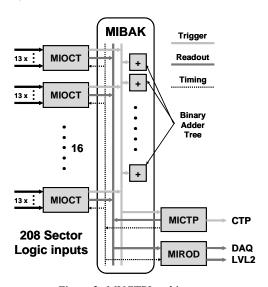


Figure 3: MUCTPI architecture

The different components of the MUCTPI system are introduced in the following sections.

## B. MIOCT Module

Each of the 16 MIOCT modules receives the muon candidates from 13 trigger sectors and forms the local muon candidate multiplicities. It also resolves overlaps between the sectors of an octant in order to avoid double-counting of muon candidates. A more detailed description of the design

and implementation of the MIOCT module is given in section III below.

## C. MIBAK Backplane

The MIBAK is a custom active backplane which receives the muon candidate multiplicities from the 16 MIOCT modules and forms the total multiplicity sums. The multiplicity summing is performed by a binary adder tree implemented using Altera MAX7000 CPLDs for low latency. In addition the backplane implements a bus for the transfer of readout data from the MIOCT modules and the MICTP to the MIROD. This shared readout bus uses a token passing protocol for arbitration and is based on Bus LVDS (BLVDS) [3] signaling. Finally the MIBAK distributes the trigger and timing signals with low-skew to all the modules in the crate. The MIBAK is mounted in the J3 position of the 9U VME crate.

#### D. MICTP Module

The MICTP module receives the total multiplicity sums for the 6  $p_{\rm T}$  thresholds from the MIBAK backplane and sends them to the CTP. It also writes the multiplicities into a pipeline for read-out by the MIROD module on reception of a Level-1 Accept from the CTP. In addition the MICTP receives the timing and triggers signals, such as the 40 MHz bunch clock, the Level-1 Accept, the LHC orbit signal and the event counter reset, from the CTP and distributes them through the backplane to the other modules in the MUCTPI crate. The MICTP also provides features for monitoring the multiplicity sums through the VME bus.

## E. MIROD Module

The MIROD module is the Read-Out Driver (ROD) of the MUCTPI. For every Level-1 Accept it collects the muon candidates from the 16 MIOCT modules and the multiplicity from the MICTP and sends them after formatting to the data acquisition and Level-2 trigger systems. The standard S-LINK [4] optical link mezzanine cards are used for this purpose. The MIROD also allows reading out the selected muon candidate data via the VME bus for monitoring purposes.

## F. MUCTPI Prototype

A working prototype of the MUCTPI exists [5] and a system with one MIOCT has been installed and is being used in the ATLAS underground counting room. Integration tests of the MUCTPI demonstrator with the central trigger processor, the RPC trigger sector logic as well as the DAQ and Level-2 systems have been successful and the system has recently been used in combined cosmic ray data taking runs [6]. Figure 4 below shows a picture of the prototype system with the MIOCT in the rightmost slot and the MICTP and MIROD with the S-LINK mezzanine cards in the center of the crate. The crate also contains a single-board computer (SBC) in the first slot for configuration, control and monitoring.

The existing demonstrator system provides almost all of the functionality and performance required. A redesign of the existing MIOCT prototype was however required, since greater flexibility and programmability is needed for the overlap handling. In addition only two modules of the original design, which dates back to 2000, were available.

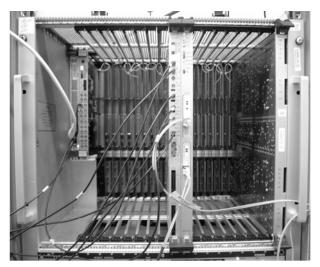


Figure 4: MUCTPI prototype system

## III. OCTANT MODULE (MIOCT)

The design and implementation of the revised MIOCT module is presented in the following sections.

#### A. MIOCT Architecture

The MIOCT is implemented as a 9U x 400 mm VME64x module. The 13 sector logic inputs use 32-bit parallel LVDS signalling at 40 MHz. Serial transmission was excluded because of the latency penalty of  $\sim$ 3 BC due to serialization and de-serialization. Using 2x68-pin high-density dual-stacked VHDCI connectors and low-skew SCSI-3 twisted-pair cable [7], it is possible to fit all 13 sector logic inputs on the front-panel of the module.

Figure 5 below shows the block diagram of the MIOCT module.

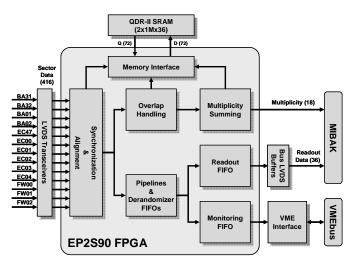


Figure 5: MIOCT block diagram

The main functionality of the MIOCT is implemented in one Altera Stratix II FPGA [8]. This chip features sufficient memory, logic and I/O resources to allow integration of the main MIOCT processing into a single device. There is an additional small FPGA for the VMEbus interface. The implementation is based on the VMEbus interface core [9] which was developed for the modules of the CTP.

Prototypes of the revised MIOCT are currently in production and will be available for testing very soon.

## B. Trigger Path

The signals received from the detector sector logic are resynchronized with the system clock received from the MICTP. The incoming sector words are aligned in time to compensate for the different latencies introduced by the RPC and TGC detector specific electronics and the different cable lengths. The MIOCT checks the alignments to be sure that the data word of each sector corresponds to the same bunch crossing.

The multiplicity summing logic counts the number of muon candidates for each of the 6  $p_{\rm T}$  thresholds, taking into account possible overlaps between sectors. The overlap handling logic suppresses one of the muon candidates if there is a candidate in the corresponding overlap zone of an adjacent sector as well. More details on the overlap handling are given in section D below. The total number of muon candidates is encoded into six 3-bit words and sent to the MIBAK backplane for overall summing.

The internal logic is operated at 4 times the bunch clock ( $\sim$ 160 MHz) in order to minimize the latency while maintaining a pipelined architecture. The latency of the trigger path is 3 BC, which is consistent with the existing demonstrator implementation.

## C. Readout Path

All the data received from the muon sectors are stored in pipeline memories for the duration of the latency of the Level-1 trigger. In case of a Level-1 Accept, data of all input channels are read out from the pipelines and written into derandomizer FIFOs. The readout window is programmable to  $\pm 2$  bunch crossings around the trigger. The data in the derandomizer FIFOs are zero-suppressed in order to reduce the data rate on the backplane, formatted and buffered until they are read out via the MIBAK backplane. The data sent by the MIOCT module can also be read out for monitoring purposes using the VME bus.

#### D. Muon Candidate Overlap Handling

Each MIOCT module receives data from four barrel, six end-cap and three forward sectors of the muon trigger. Figure 6 below illustrates the overlap regions between these sectors, the following types of overlaps between adjacent sectors can be handled by the MIOCT:

- Overlap between barrel sectors
- Overlap between barrel and endcap sectors
- Overlap between endcap sectors
- Overlap between forward sectors

Overlaps of chamber regions within sectors are handled by the detector sector logic. There is no overlap between adjacent octants.

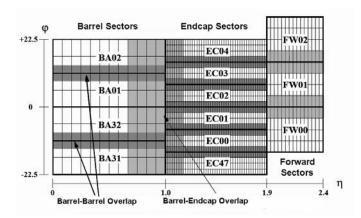


Figure 6: Overlap regions

Figure 7 below shows the block diagram of the implementation of the overlap handling scheme. In the first stage overlaps between muon candidates from different sectors are detected based on their location or sub-sector address and, in the case of the barrel/end-cap overlaps, their  $p_{\rm T}$  threshold and charge sign as well. There is one overlap detection unit for each of the overlap regions listed above. The second stage uses the overlap flags together with a comparison of the  $p_{\rm T}$  values to determine which of the two candidates in overlap should be suppressed. Finally the multiplicity is calculated from the  $p_{\rm T}$  values of the 26 candidates of the octant, ignoring the candidates that are flagged to be suppressed.

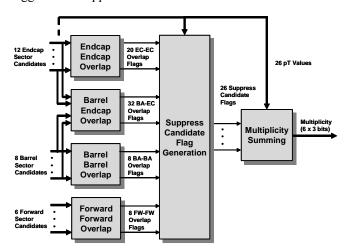


Figure 7: Overlap handling architecture

All the functional blocks of the overlap handling are implemented using programmable look-up tables (LUT). The overlap handling policy can therefore easily be changed by reloading these LUT through the VMEbus interface. The contents of the LUTs will be determined from offline simulations.

#### E. Snapshot/Test Memory

The MIOCT also features a snapshot and test data memory. The memory can be used to store the data from all 13 input sectors as well as the calculated candidate multiplicity and the candidate suppression flags. This is useful during the timing-in of the system as well as for diagnostics and monitoring purposes. The depth of the snapshot memory

is 128K bunch crossings per sector, which corresponds to  $\sim$ 36 LHC turns. For module test purposes, the memory can also be used to replay test data. Since the sector logic LVDS buffers are bi-directional this even allows performing a full functional test of another MIOCT module including the cable connections.

The snapshot/test memory is implemented using two 1M x 36 bit Quad-Data Rate (QDR) SRAM [10] devices. QDR SRAM features independent double data-rate (DDR) read and write ports. The memory devices on the MIOCT are clocked at 160 MHz, resulting in a bandwidth of ~23Gbit/sec for read and write access. The memory interface is implemented using an IP core from Altera. The routing between the FPGA and the QDR SRAM is critical and requires length matching and  $50\Omega$  controlled impedance. A signal integrity analysis tool (Cadence SpecctraQuest) was used to validate the termination scheme and the PCB layout.

#### IV. CONCLUSIONS

The MUCTPI interfaces the 208 muon trigger sectors to the CTP. It calculates the muon candidate multiplicities for 6  $p_{\rm T}$  thresholds and avoids double counting of muons detected in overlapping sectors of an octant. A working prototype system is installed in the ATLAS underground counting room and has been successfully used in combined cosmic data taking runs.

A new MIOCT module has been designed to replace the existing demonstrator. It features a flexible overlap handling architecture and the hardware implementation is highly configurable, being based on look-up tables in a large FPGA device. The new MIOCT will allow a seamless upgrade of the existing MUCTPI system since it is fully compatible with the MIBAK backplane.

#### V. REFERENCES

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