Installation and Test of the ATLAS Muon Endcap Trigger Chamber Electronics

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Abstract

For the detector commissioning planned in 2007, a sector assembly of the ATLAS muon endcap trigger chambers is being progressed in CERN. Final technical test of the electronics mounted on a sector must be made at this stage. For systematic test of the electronics (sector test), we have developed a DAQ system on top of the ATLAS online software framework. The system is not dedicated only for this test, but can be used also for the front-end detector part of the overall ATLAS DAQ system. In the presentation, the procedure, meaning and results of the sector test are discussed after brief introduction of the TGC electronics and the sector structure as a construction unit. We introduce plans of further detailed and elaborated tests for the whole system using cosmic ray and single halo muons when all the TGC sub-detector part is completed as concluding remark.

I. INTRODUCTION

Sector assembly and installation of the ATLAS muon-endcap chambers is being progressed in CERN for the detector commissioning in 2007. The thin gap chamber (TGC) is used for the muon-endcap trigger system [1]. The muon endcap system covers the both endcaps of the detector ($1.05 < |\eta| < 2.4$) to detect isolated muons and give the level-1 (LVL1) muon trigger signal with two ranges of the transverse momentum (pt) of low-p_T > 6 GeV and high-p_T> 20 GeV [2].

As at least three measurement points per track is necessary to identify a muon with even such coarse momentum estimation, there are three TGC stations per endcap (one (M1) has triplet chambers to measure three track points for a muon, and the other two stations (M2 and M3) have two measurement points for a muon each with doublet chambers). Every station has commonly twelve sectors to form a wheel. This 1/12 sector is an installation unit for the trigger muon endcap system for both the chambers and electronics. The sector is also the unit for the trigger and readout system.

A. Overview of TGC electronics system

Fig. 2 summarizes a structure of the TGC electronics system [3]. Electronics components are divided into two parts; on-detector and off-detector ones. The on-detector part is further separated into two parts, one is called Patch-panel and Slave board that is installed just behind the chamber (we call this unit as PS-board) and the other one is Hi-p_T and Star

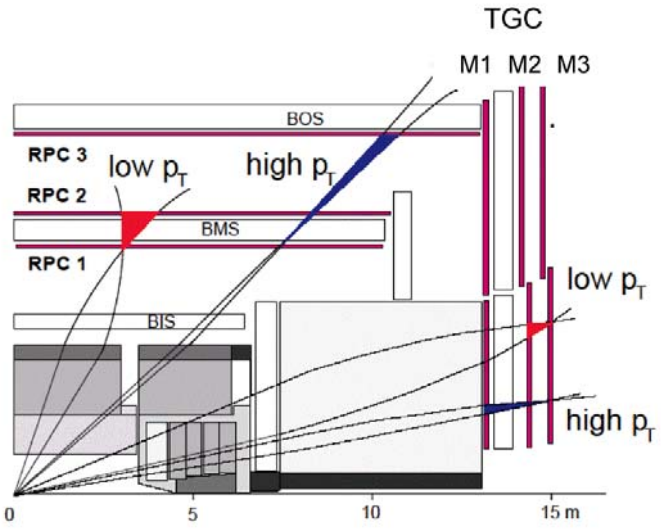

Figure 1: TGC Chamber layout in RZ plane of ATLAS endcap

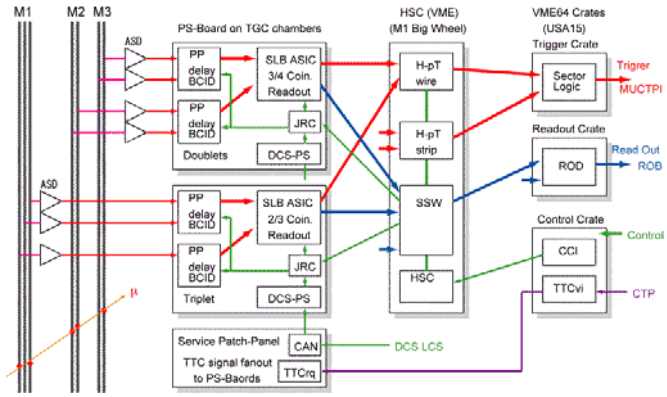

Figure 2: TGC Electronics Overview: The system is divided into three parts, two on-detector parts and one off-detector part.

Switch Control (HSC) crate that is installed at the outer rim of M1. A PS-board and an HSC crate are prepared for each 1/12 sector.

Digitized chamber-signals from Amplifier- Shaper-Discriminator (ASD) boards [4] attached directly to TGC are inputted to Slave Board ASICs (SLB IC) after synchronized and bunch crossing identified in Patch-panel (PP) ASICs (PP IC). SLB performs local coincidence to identify muon tracks

coming from the interaction point with $p_T \geq 6$ GeV, and output information of r, ϕ and Δr, $\Delta\phi$ for every muon candidate (low p_T coincidence with 2-out-of-3 logic using M1 or 3-out-of-4 logic using M2 and M3). The PP and SLB ICs are mounted together on a PS board. The PS board mounts also electronics for the detector control system (DCS) [5]. The output signals of SLB are fed into a Hi-p_T board, which is installed in an HSC crate and is approximately 15m away from the corresponding PS board. The Hi-p_T board contains Hi-p_T ASICs (HpT IC). An HpT IC combines information from two (for doublet) to three (for triplet) SLB ICs to make a global coincidence to find muon tracks with $p_T \geq 20$ GeV (hi p_T coincidence). HpT IC also makes data compression to send its output over a distance of about 90m with serial data transmission to the counting hut where the off-detector electronics are installed.

Signals for r (wire hit information of TGC) and ones for ϕ (strip) are separately processed in the independent streams up to hi-p_T coincidence operation, and the sector logic (SL) installed in the off-detector part combines these two streams and makes a coincidence in r-ϕ to identify muon signals in two dimensional space. At maximum two highest p_T muon candidates per trigger sector (72 trigger sectors/side) are selected after successful r-ϕ coincidence, and the information is sent to the MUCTPI (ATLAS level-1 MUon Central Trigger Processor Interface) [6]. Functionalities and design concept of the three main ASICs (PP, SLB and HpT) have been discussed in detail in [7].

So far we have discussed the on-detector parts of the electronics system. Since the electronics components used in the on-detector parts will suffer the total ionization dose for ten years of about 150 to 210Gy (15 to 21krad), and about 2 hadrons/10cm^2. The both values contain some safety factors. The ionizing dose will degrade gradually the functionality of the electronics and hadrons will damage them as single event upsets. We have, thus, checked the radiation tolerance of the components used in the system by irradiating them with γ-ray and proton beam for the same values as dose and number of hadrons estimated for ten years. We have used only the components, which clear conditions of the radiation tolerance tests. The details of this discussion will be found in [8].

Since hit information for both coordinates will be used not only for the trigger decision logic but also for the second coordinate information for the ATLAS muon reconstruction in offline analyses, a readout system must be implemented. Readout data are processed also in SLB ICs, each of which implements pipeline buffers during the LVL1 processing time and FIFO for selected events (de-randomizer). At every LVL1 accept (L1A) signal, data are serialized in SLB ICs and sent to a data distributor/concentrator, which is so called Star Switch (SSW). One SSW has 18 SLB IC inputs and one output. A sequential process of receiving data from SLB, storing in FIFO, format analysis and output to Readout Driver (ROD) will be done for all used channels in turn under the VME control. Basic concepts and functionalities of SSW will be found in [9].

ROD receives data from total several SSWs, the nuer depends on the configuration. Data received are stored in FIFO, which is prepared for every input channel. All the data stored in FIFOs are merged if these data have an identical L1A identification number. ROD sends data to the ATLAS central DAQ facility in the end.

The functionality, validity of the trigger logic and timing margin of the chain from the front-end ASD (actually using TGC) through both the trigger and readout lines up to central online data acquisition system has been confirmed in two test-beam experiments in 2003 and 2004 done at CERN SPS H8 muon beam dump facility [10].

B. 1/12 Sector as a unit of construction

In Fig.3 a photograph of one 1/12 sector is shown. From this photograph, one can find all the on-detector components of the TGC electronics system; the PS boards are mounted on the chamber surface while the HSC crate is put at the outer edge of the sector. This HSC crate handles signals of all the three corresponding sectors (of M1, M2 and M3), and mounted only on the M1 station.

Once the sector is installed in the whole ATLAS detector system in the cavern, one cannot access easily its electronics as well as cables. We have to test the electronics system after completion of the sector assembly and fix or repair quickly if we find incomplete connection of cables or damage of electronics components. Furthermore since the system involves the LVL1 trigger generation logic, confirmation of functionality of timing adjustment of the delay logic at this assembly stage is also the key issue from the signal synchronization point of view.

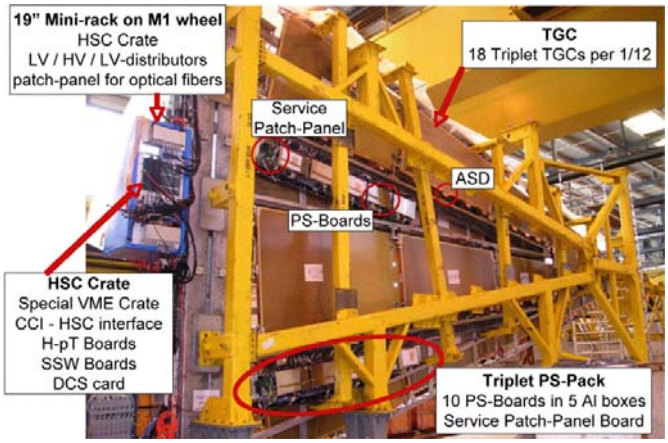

Figure 3: Setup of the on-detector components (M1)

In order to check all the functionalities and adjust timing of the electronics system, it is necessary to do almost full DAQ operation to the sector. We have made a lot of DAQ systems so far for the standalone electronics consistency check or the integrated beam tests with TGCs using the high energy muon beam. These DAQ systems constructed have been dedicated for specific purposes, but none of them can be used in the actual ATLAS online system, although various software codes in particular for individual module controls are re-

usable with minor modification. For the present electronics test of the sector assembly, we have reformed the DAQ system once more. We made it with being fully complied with the ATLAS online software framework [11].

In the following section we describe the installation and mass-test procedure of electronics using this DAQ system in detail and some experience to fix problems encountered actually in the sector assembly. We would like to discuss the timing adjustment procedure in detail. If the adjustment in the sector level is done well, then the timing signals in larger parts (whole M1, M2 or M3 station, each endcap-side or overall muon endcap) will be smoothly synchronized.

II. Construction and Test of Sectors

As discussed in the previous section, every station (M1, M2 and M3) of one endcap-side is divided commonly into twelve sectors. This sector is a unit of the TGC construction as well as the electronics segmentation. Although the chambers have been constructed in different countries of the collaboration, the sector assembly is being done in a building of CERN west area. Once one sector is assembled and passed an electronics connection test (we call this as sector test), the sector is carried to the ATLAS pit for the installation. After the installation of the M1 station is completed, then M2 and M3 stations will be followed for one side. Then the same procedure will be repeated for the other side.

Since it may be difficult and complicated to repair electronics as well as cables in the sector if it is installed in the detector in the ATLAS cavern, a careful and cautious check for hardware of the sector must be done at this stage, and the test should concern to check full facility and connectivity of electronics and cables for a sector. Functionality of all the readout chains is thus checked with this test using and signals readout by the off-detector test-ROD. The outputs of the test-ROD are checked in order to

- find and correct any wrong or loose cable connection,
- find and repair damaged hardware components, and
- confirm several basic functionalities of PP and SLB ICs (adjustability of delay timing and/or mask patterns) .

The delay timing adjustment is a key-issue for the test since all the channels in the sector must be synchronized at this stage.

The signal flow diagram of the electronics setup for the sector test is shown in Fig. 4. We inject a few hundreds of test pulses generated by TTC system [12] to all the channels concurrently in the test. The results are displayed in histogram style and we will see some mal-forms or malfunctions of the electronics from histograms. Each station has several layers (three layers for triplet and two for doublet). The test is done separately for each layer. From histograms shown in Fig. 5, for example, we can see a hole at the last channel in the top histogram but any other histograms. A channel hole means one missing channel that may come from insufficient connection of a cable, damaged cable, defective electronics, or dead channel in the chamber, though we cannot focus the exact point where the problem occurs actually from the histograms. After several inspections of various parts by hand, we can identify the problem.

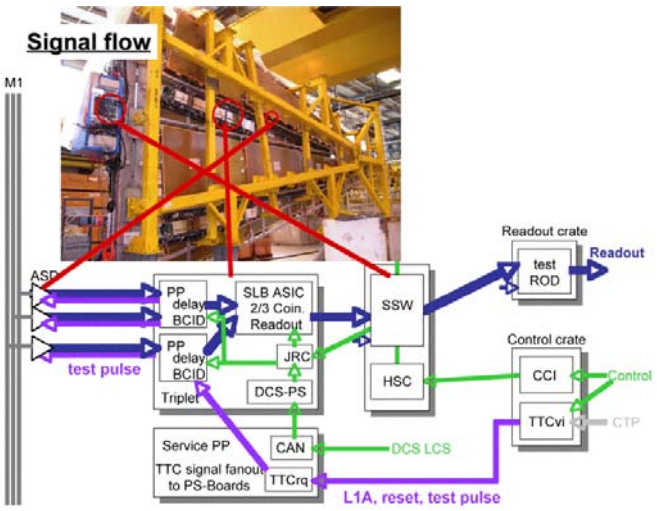

Figure 4: Diagram of the electrical signal flow for the sector test

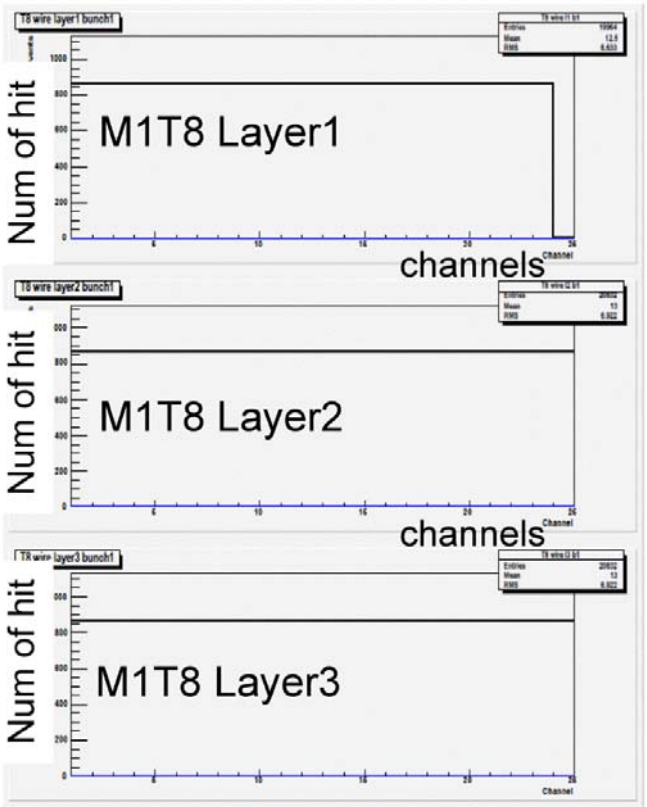

Figure 5: An example of signal detection problems found in the sector test The example are results of a sector test for M1 (triplet)

Changing the delay value to be set in the individual fine-delay adjuster facilitated in a PP IC, we can obtain delay curves. The fine delay for a channel can be set in precision of 25ns/32bit (~0.78ps step) where 25ns is a bunch-crossing interval of LHC. In each fine-delay value, we count how many test-pulses (events) are recognized in an interval of

each of previous, current or next bunch. At the sector test the delay curves for all the channels are accumulated. An example of the delay curves is shown in Fig. 6. From this figure, we can find that test pulses delayed between -50 and -25ns from the nominal delay are all detected in an interval of the previous bunch crossing signal, those between -25ns and 0ns are all detected in the current bunch. We can also find that if we advance the timing signal up to 25ns, then all the pulses are regarded as ones occurred in the next bunch, and no pulses detected rather than this bunch. With this result, we can conclude the timing adjustment unit in a PP IC works fine.

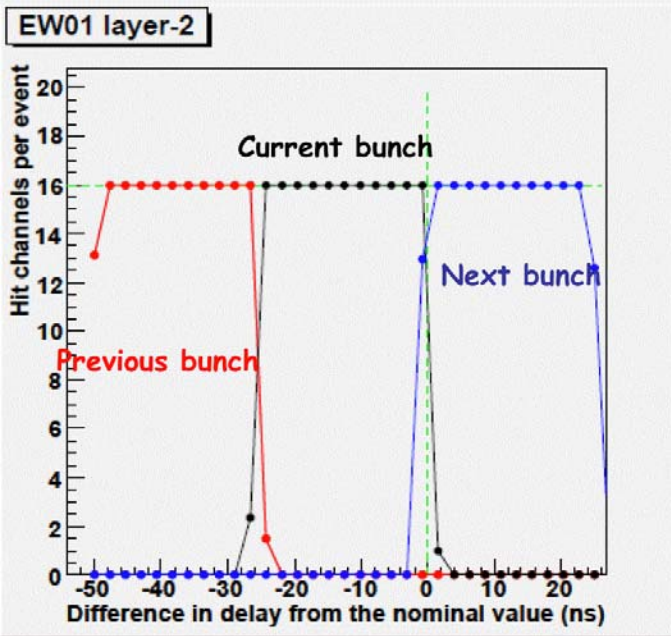

Figure 6: An example of Delay curve obned in a sector test

III. Summary and Outlook

A. *Summary of the Sector Assembly and Test*

In Fig. 7 we have shown the progress rate of the sector assembly. The abscissa is the days we have spent while the ordinate is accumulated number of sectors constructed so far. In the sector assembly site we have two assembly sections (called Jura and Salève in the figure). The assembly is made in parallel at two sections. From the slopes of the lines depicted in the figure, we can find that we need in average one week for one sector assembly including the test whose procedure we have described in the previous section. At the time of writing this document, we have finished the assembly of all the sectors (twelve) for one side of both M1 and M2. Figure 8 shows a picture of the whole M1 station completed in the ALTAS pit. Up to end of 2006, we will finish the whole sector assembly for one endcap unless we have serious problems in the sector assembly stage and/or installation in the pit.

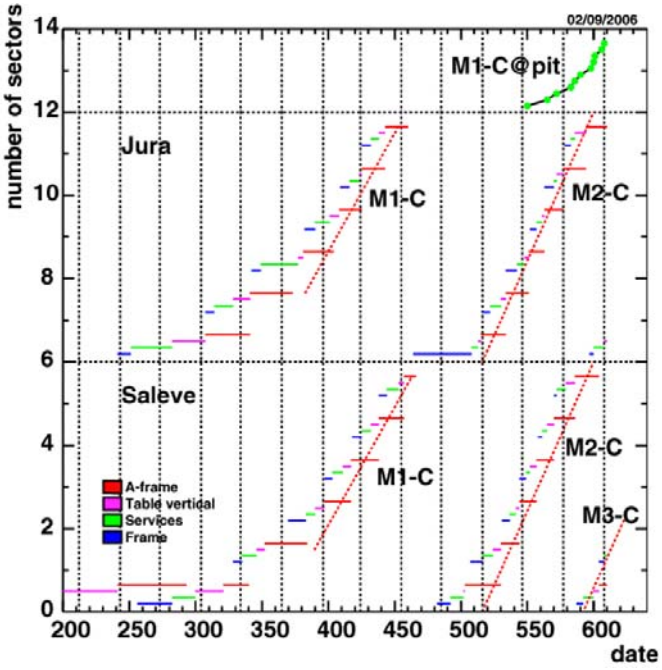

Figure 7: The integrated number of sectors constructed as a function of time (day) for assembly sections (called Jura and Salève). On top of these curves, the rate of the sector installation at the ATLAS pit is also shown in the figure.

B. *Cosmic Ray Test*

As we have discussed, we cannot test in detail the logic chain of the LVL1 endcap muon trigger while we can make debug and adjust the readout chain of our electronics with the sector test. The trigger generation logic must be also debugged and its full functionality must be confirmed in due course. The independent logic chain consists of the coincidence matrices of both low-p_T (implemented in SLB IC) and hi-p_T (implemented in HpT IC) and the r-ϕ coincidence logic implemented in the SL module. One interesting idea to confirm the functionality of this trigger path is to generate cosmic muon triggers using the TGC-trigger logic. We may have such a possibility although the original TGC (including electronics) setup for ATLAS endcap muon detection must be slightly modified.

Since the trigger logic assumes that a muon ordinarily comes from the interaction point to TGC with the dip angle between 40 and 90 degrees (the trigger towers (formed with M1, M2 and M3) always head toward the interaction point), the quite low acceptance will be anticipated if we use the coincidence logic with full three stations (a triplet one and two doublet stations). If, however, we relax the condition to recognize a cosmic muon only with one station (using only the inner most triplet M1 or the outer most doublet M3 with supplying faked signals to the other stations), cosmic triggers will be generated with a reasonable rate using the current setup of the coincidence matrices. If the service lines for TGC (gas, high voltage and optical fibre connection) are completed (at around December 2006), we will immediately begin this project.

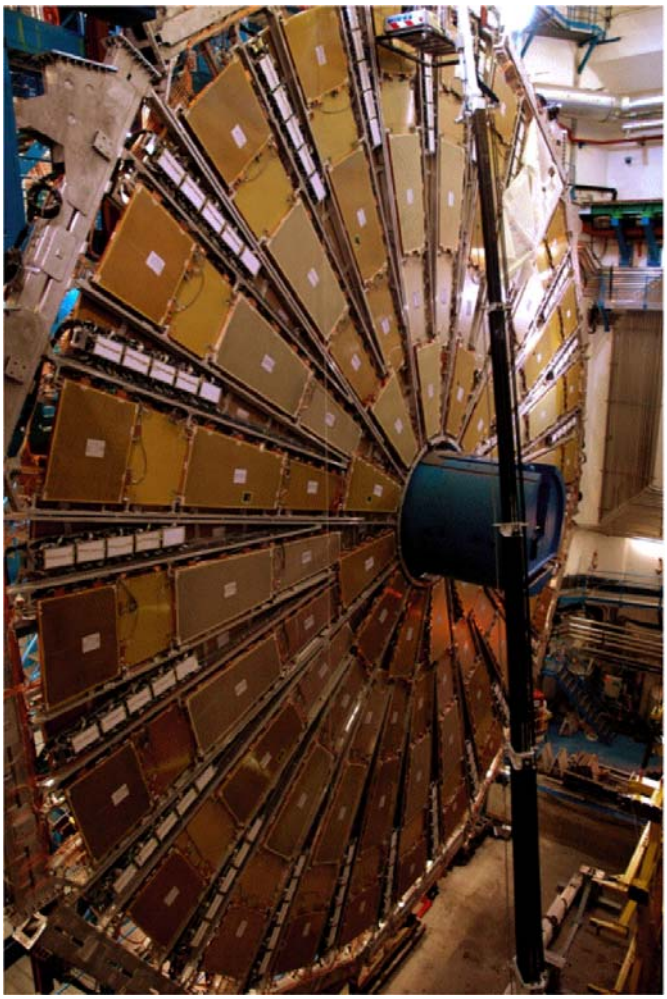

Figure 8: The completed M1 station of TGC in the ATLAS pit (Sept., 2006)

C. *Single Beam Halo Run*

When LHC is running in single beam mode before collision, we can check also our trigger logic using muons that produced in scattering of proton with residual gas in the beam pipe. In the trigger logic the chamber output signal must be synchronized roughly at the input of PP IC (the input of the trigger logic). Although this timing measured from the common bunch-crossing (BC) time is fluctuated among channel by channel due to different time of flight (TOF) of muon from the interaction point and different cable length, rough correction of timing fluctuation can be overcome if we know the distance between a chamber surface point and interaction point as well as the cable length (coarse delay setting). Since a low p_T coincidence matrix is installed in an SLB IC, the signals after PP IC are precisely made synchronized at the input of the SLB IC. This synchronization can be achieved using a fine delay adjuster with sub-nanosecond level implemented in a PP IC as discussed in the previous sections. In principle we can adjust timing up to the input of SLB for all the channels already in the sector test. But this adjustment is done sector by sector independently. We must confirm this synchronization over all the channels using the single beam halo run.

Since the BC timing will be available even in the single beam running mode, and the scattered muon will come into TGC in parallel with the beam, the low-pT, high-pT and r–ϕ coincidence logics will work fine without any modification of the logic configuration for halo muons. If we can have coincidence signals at the very end of the trigger logic, i.e., at the output of the SL (Sector Logic) as the consequence, it then means that the synchronization at the SLB input is well adjusted over sectors and even over stations. There is, however, an issue to do this test because the muon will hit the TGC before the BC timing if the beam and scattered muon come parallel into the detector at the same time, and the TGC is in front of the bunch crossing point. A simple idea to get over this issue is to re-adjust the coarse synchronization at the input of PP IC with TOF = -TOF (just reverse the sign).

Although we are not yet fixed when we do this test because it depends on the LHC running schedule, we foresee to have this test by the end of 2007.

IV. References

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