Status of the TTC upgrade

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Abstract

The TTC (Timing, Trigger and Control) system [1] broadcasts the timing signals (Bunch Clocks and Orbits) from the LHC machine to the experiments. Once at the detector level, it integrates the trigger information and local synchronous commands with these signals, for transmission to several thousands of destinations. The equipment for this second part of the system is fully produced, but the main network between the machine and the experiments required to be upgraded to ensure its easy maintenance. The design work began at the end of 2005 and the new modules will be tested during the summer 2006 and the structured test beam in September 2006. A status of this design work is given, including the description of the upgrade principle, the main modules, the results of the tests done on the prototypes and the plans for production and support of this system.

I. Upgrade Principle

As it was before 2005, the system was difficult to maintain for various reasons. The main ones were the following: obsolete components with really few spares (only 2 receiver crates per experiment), no documentation to reproduce the modules (no schematics, no manufacturing files), and no way to remotely monitor, in case of troubles, the status of the transmitter crate to be installed in the CCR (CERN Control Room).
Moreover, the quantity of required signals increased between the time the TTC system was specified and now. Three Bunch Clocks (BCring1, BCring2, BCreference) and two Orbits (Orb1 and Orb2, one per ring) are now required, instead of one pair of Bunch Clock and Orbit signals previously.
Finally, the last argument justifying a redesign of the TTC backbone was that no piquet service was foreseen for a 24 hours a day, 7/7 days on-call support of such a vital system. Such a piquet service is really rare and only the AB/RF team was willing to do it, provided that we use equipment they already support.

A. Criteria

A study was thus made [2] to allow a reasonable upgrade of the system, with the following criteria as a basis:

- Full compatibility with the experiment trigger systems, which use the outputs of the previous TTCmi receiver crate,
- Equal or better jitter performances than the previous system,
- Up-to-date components with a stock of spares and a fully documented design,
- Possibilities to remotely monitor the status of the transmitters and receivers, as well as to adjust phases, length and sources of the received signals (LHC Bunch Clocks and Orbits),
- Use the AB/RF standard transmitters and receivers, so as the AB/RF piquet service accepts to maintain and support the TTC backbone as it supports its own system.

B. System Overview

An agreement [3] between the experiments, the PH/ESS group in charge of the TTC support and maintenance, and the AB/RF group, was signed in November 2005. The specifications began at the same time and the system design in January. A design review happened in May [4], followed by the production of PCBs during the spring and summer 2006.

This agreement was based on a simple statement: the AB/RF group was already responsible for the transmission of the timing signals from SR4 (Echenevex Site, where the LHC RF is generated) to the CCR using their own equipment. The natural proposal was then to simply extend the transmission links provided by the AB/RF group up to the experiments, removing all the active components from the CCR.

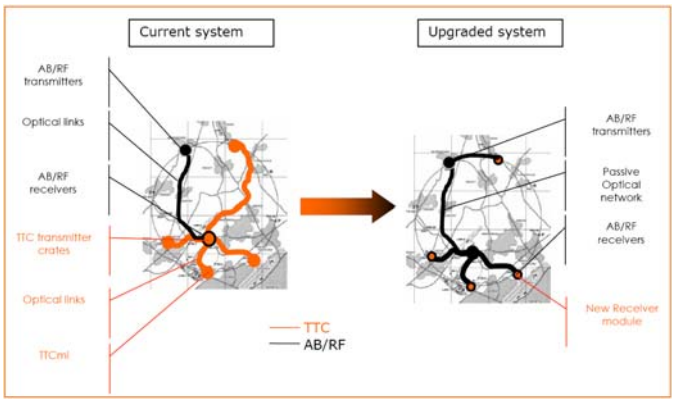

Figure 1: Principle of the TTC upgrade

The TTC transmitter crate will be removed from the CCR, and replaced by simple passive optical splitters. The transmission will be ensured from the SR4 by a 6U VME crate provided by the AB/RF group, equipped with their crate controller and their transmission modules (see figure2). Instead of being encoded following the TTC protocol at the CCR, Bunch Clocks and Orbits will thus be transmitted over parallel optical fibers from the SR4 down to the experiments.

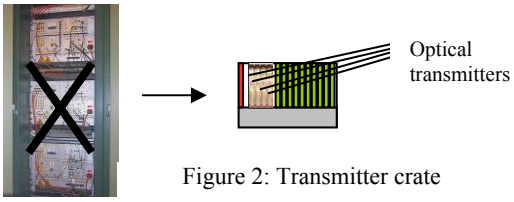

Figure 2: Transmitter crate

In the experiments, the TTCmi (old receiver crate) will be replaced by a 6U VME 64x standard crate, equipped with one crate controller, two or three AB/RF receiver modules, and with one RF2TTC interface module, allowing selection and adjustments of the signal sources before being transmitted to the experiments.

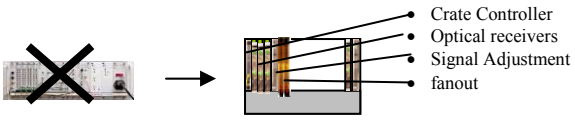

Figure 3: Receiver Crate

The AB/RF optical components to be used in the transmitter and receiver crates were already specified and selected at the end of 2005, but the modules housing them were not designed yet. As these lasers were initially supposed to transmit the 400 MHz Radio Frequency signal of the LHC (as a 0dBm continuous sinewave), they had to be as clean as possible in term of phase noise.
After a complete evaluation of the components made in collaboration between AB/RF and PH/ESS groups [5], the PH/ESS group designed the VME Analogue Optical transmitter and receiver boards according to the AB/RF specification. This set of Analogue modules will be detailed in the following section.

Nevertheless, as the TTC signals (40.078 MHz Bunch Clocks and 11 kHz orbit pulses) - as well as some other signals being used by the AB/RF group for their other applications - were digital, the use of such analogue modules to transmit them would have been an overkill.
PH/ESS, thus, proposed to AB/RF a second set of links, digital, based on SDH/SONET transmitters. After a first evaluation of these digital links made with AB/RF [6], PH/ESS designed one transmitter and one receiver boards, which could replace the analogue set where the signal to be transmitted is not analogue but digital. This set of Digital modules is currently being validated by the AB/RF before being fully standardized. It will be also detailed in the following section.

II. Module Description

The modules composing the receiver crates are here described. This includes the crate controller, the optical receiver modules (analogue and digital), the module in charge of the signal adjustments (RF2TTC) and a fanout module.

A. Crate Controllers

As each experiment standardised a different crate controller for its VME crates, different controller types will be used. The VP110 and the VP317 from Concurrent Technologies for ATLAS and ALICE respectively, the CAEN A2818 and V2718 for CMS, and finally the CAEN V1718 for LHCb.

B. Transmission Links

Two or three receiver boards will be installed in the receiver crate. The corresponding transmitters will be installed in the SR4 transmitter crate. As two types of transmission links (analogue and digital) were designed, both options are here presented.

1) Analogue Link

The lasers and receivers composing these modules were initially selected to transmit the 400MHz Radio Frequency signal, as a continuous sinewave.
It is composed of two modules [8] [9], one transmitter and one receiver, both of them equipped with 2 optical components. The selected link is the LBL 3GHz from MITEQ, designed to transmit analogue 0dBm signals with a very low phase noise (between 0.5 and 3 picoseconds according to the transmitted frequency). The components are uncooled, so a special heatsink has been designed to keep them at a temperature close to 35 degreC. The electrical interfaces of the lasers and receivers are direct SMA connectors fixed on the front panel, to isolate the analogue signals from the digital side of the modules dedicated to control and monitoring.

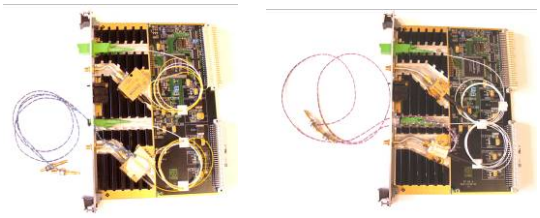

Figure 4: Analogue RF_Tx and RF_Rx modules

The VME interface was designed following the AB/RF standards (type of components, schematics, and firmware). The J2 connector of these modules is not used, as this part of the backplane used in AB/RF VME crates is custom.
These modules are monitored by the VME interface, by reading the VME registers storing the optical power level of the transmission link, both at the laser and at the receiver level.

These modules were fully satisfactory during evaluation [5]. The phase noise measured with 400 MHz sinewave 0dBm signal was less than 0.5ps (see also section III). However, their very high price (7 kCHF per transmitted signal), justified by their very good performances, required to find a cheaper solution for all the signals which did not need such a quality.

A study for a digital link was thus made.

2) Digital Link

These modules were developed by PH-ESS to substitute the analogue ones [10] [11]. Their mandate is to be used instead of the analogue links everywhere the signal does not need to be sinusoidal, but can be transmitted as digital clocks or pulses.

A study was made to identify the components able to transmit and receive various clock frequencies, as well as pulses of various width and periods.
The transmitters selected were the OCP-STX03 and OCP-STX-24, pin compatible, which have respectively 300MHz and 1.5GHz of bandwidth.
On the receiver side, the OCP-SRX-03 and OCP-SRX-24, AC coupled, were selected for clock reception, whereas the

Truelight TRR-1B43-00 was selected for pulses. Indeed, the cut-off frequency of the TRR's AGC (Amplitude Gain Controller) is low enough (below 3kHz) to transmit the 11kHz pulses used for the Orbit signals. Moreover, this component is used everywhere in the TTC system inside the experiments. It is really cheap (7$ piece) and still in production.
Each VME transmitter module can house three pigtailed lasers, which can be OCP-STX-03 or OCP-STX-24 without any hardware changes. To match with various kinds of amplitude and signal types, the electrical input signal is latched at the input of the board using a comparator, the threshold of which can be adjusted via VME registers.

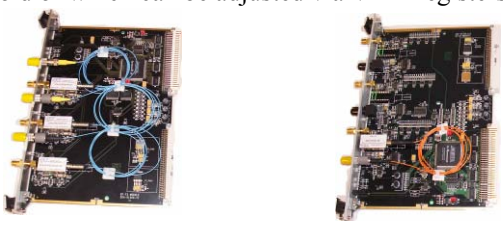

Figure 5: Digital RF_Tx and RF_Rx

Each receiver VME module can house three receiver modules. The design was done to allow various receivers to be used, requiring a minor hardware modification. For 400 MHz or 200MHz clocks, the OCP-SRX-24 can be plugged in. For 40 MHz, the OCP-SRX-03 or the TRR-1B43-00 are recommended. And for pulse (or not DC-balanced signals) reception, the TRR-1B43-00 will be plugged in. On Figure 5, the receiver module is equipped with two Truelight components and one OCP-SRX-03.
Once the conversion from optical to electrical is done (by an OCP or a Truelight component), the signal is converted to standard ECL using a comparator common to OCP and Truelight receivers. A threshold is applied to this comparator, which is adjustable via a VME register. The signal is then fanned out. One copy goes to the FPGA for frequency and signal detection (status accessible via a VME register) and one copy is transmitted to an ECL 50 Ohm coaxial cable driver to make the signal available on the front panel. This full signal path, from optical input to ECL output, is reproduced three times on the VME module.

The price of these modules is much more reasonable than the analogue ones (about 1.2 kCHF per transmitted signal, which is one sixth of the price of an analogue link).
These digital modules are being evaluated by the AB/RF group in charge of their maintenance and support, and by PH/ESS.

The signals delivered by the receiver modules are then transmitted to the RF2TTC module, in charge of their timing adjustment and multiplexing.

C. *RF2TTC Module*

The RF2TTC converts the three 40.078MHz Bunch Clocks (BC1, BC2 and BCref) and the two orbit signals (Orb1 and Orb2) from the optical receivers to ECL signals, and performs various adjustments on each signal before making them available for the in-detector TTC electronics.
The full functionalities are gathered in a specification document [4] [12].

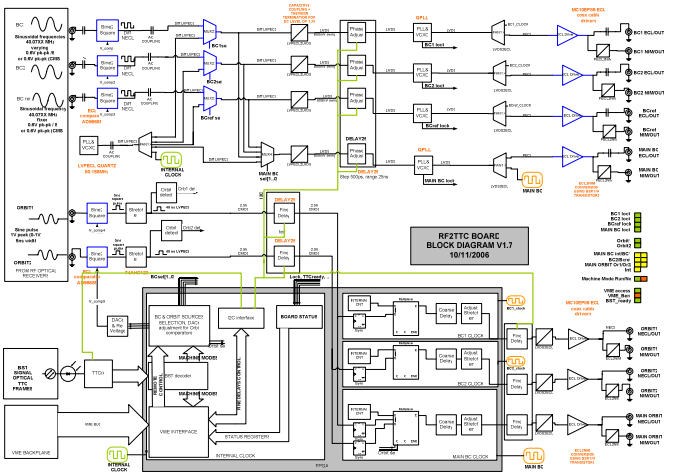

Figure 6: RF2TTC module diagram

The three Bunch Clocks (represented on the top part of the above diagram) are all treated in the following way:
A comparator with an adjustable threshold first converts the input signal into a PECL signal, before being multiplexed with an internal 40.078MHz clock in case of absence of the Bunch Clock on the front panel. The signal is then shifted by an adjustable delay with 0.5ns precision, before being cleaned by a QPLL and transmitted on the front panel via an ECL 50 Ohm coaxial cable driver with an AC-coupled output.
A global multiplexer allows selection between the three Bunch Clocks and the internal clock to generate a fourth Bunch Clock output, called Main BC, which can also be delayed.

Figure 7: RF2TTC module

The two orbit signals (middle and bottom right parts of the diagram) are first converted using the same adjustable comparator stage as for the Bunch Clocks. They are then lengthened to more than 25ns, finely delayed with 0.5ns steps, before going into an FPGA (grey block of the diagram), where they are synchronized to their corresponding clock, multiplexed with an internal orbit, and coarse delayed. Their length and polarity can be adjusted, and they are then again finely delayed before being transmitted by the ECL drivers.
A global multiplexer also allows selection between the two orbits and an internal one, synchronized to the Main Bunch Clock. This orbit signal is called Main Orbit and can as well be finely delayed before being transmitted.

The BST (Beam Synchronous Timing) optical signal (on the bottom left part of the diagram) is received, decoded and analyzed to recover the machine mode. This mode is useful to know when the timing signals are stable and can be used. In deed, neither the Bunch Clocks nor the Orbit signals are fully guaranteed out of the physics modes (flat top of the LHC energy curve). It is thus advised to use internal signals when the machine mode indicates that there is no beam.

All the adjustments are done using VME registers. Many status registers are available, as well as special configurations, for stand-alone or debugging work.

The prototype arrived at CERN at the beginning of October 2006 and is currently being tested.

D. *Fanout Module*

The TTC Fanout module is a 6U VME module designed by the PH/MIC group [13]. It is split in two identical parts. Each of them fans out one ECL input into 18 identical ECL outputs. The delay between the outputs is below 100ps. In addition to these eighteen ECL outputs, four NIM outputs are available for monitoring.
It is possible to daisy chain the two parts, giving a total of 35 ECL outputs and 8 NIM outputs for one ECL input.

Figure 8: TTC Fanout module

The second version of the prototype will be available in October 2006.

III. PERFORMANCES

A. *Optical Components*

The optical components were fully validated in term of phase noise and jitter, before the design of the boards themselves. The results of these measurements are gathered in two documents [5] and [6].
The test setup for the phase noise measurement is the following:

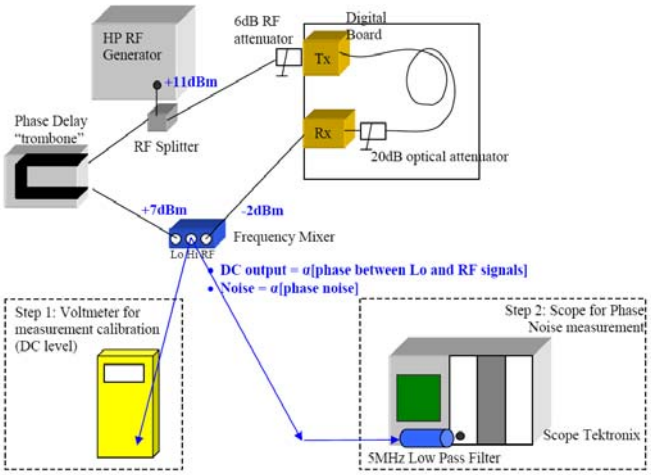

Figure 9: Setup for the Phase Noise measurement

This setup uses a frequency mixer, delivering a sinusoidal signal, function of the difference of the two input frequencies. As the two frequencies are the same (they come from a unique source), the output signal of the frequency mixer is a DC level, plus a function of the phase noise. Shifting the phase of one of the signals, to reduce this DC level as close as possible to 0, allows us to approximate this DC level (V) as a linear function of the phase noise (P): $V=\alpha.P$. Two measurements with slightly different phases give the α coefficient, and we can deduce the phase noise from the signal monitored on the oscilloscope (see fig. 10).

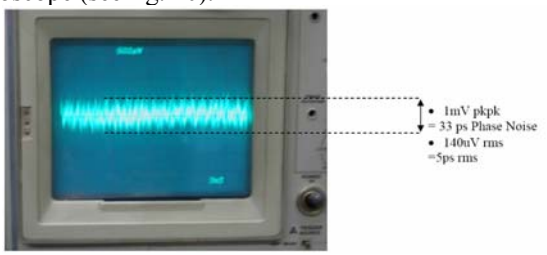

Figure 10: Phase noise measurement

The results measured for the Analog system are gathered on the table below:

Table 1: Phase Noise measurements

Freq (MHz)	Analog System Phase Noise (pkpk)	Digital System Phase Noise (pkpk)
10	20 ps	44 ps
40	5 ps	33 ps
400/160	0.4 ps (400 MHz)	6 ps (160 MHz)

B. *Preliminary System tests*

1) *Bunch Clock Transmission*

Some jitter tests of the complete modules were made in September 2006, using the 40.078 MHz and the 24 kHz signals of the SPS RF, generated close to the CERN Control Room in Prevessin. Digital clock and orbit were transmitted over the previous RD12 TTC, the analogue and the digital transmission systems. The recovered clocks were connected in the TTC laboratory in Meyrin site, to a 1GHz oscilloscope and their relative jitter was analysed.

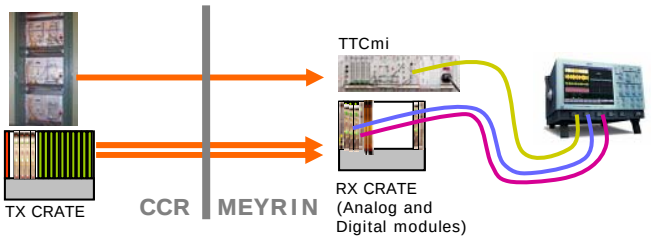

Figure 11: setup for jitter measurements of the three transmission schemes

The recovered signals are displayed on the figure 12, and the jitter results are presented on the table 2.

Figure 12: recovered clocks from the three transmission schemes

Two types of jitter were measured: the Cycle-to-cycle jitter (comparing two consecutive periods of the same signal), and the skew jitter (comparing the phase of one signal to the TTC RD12 recovered clock).

Table 2: jitter measurements

Jitter type	TTC RD12	Analog System	Digital System
Cy2Cy	29 ps rms	18 ps rms	27 ps rms
Skew	-	35 ps rms	36 ps rms

2) 25ns Structured Test beam

The three systems were also compared in the 25ns structured test beam occurring in September. The oscilloscope was triggered by a scintillator's output, and the delays between the trigger pulse and the three clock edges were analysed by the oscilloscope and gathered on one histogram.

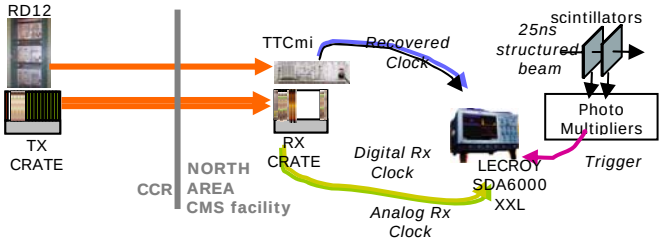

Figure 13: setup using the 25ns structured test beam

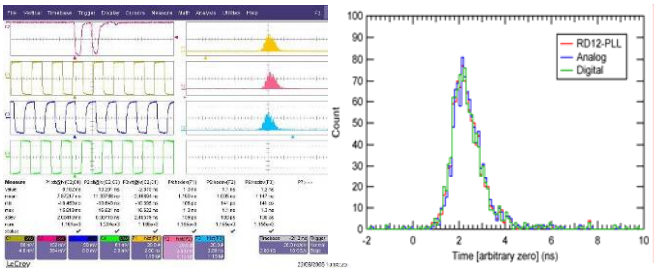

Figure 14: histograms of the jitter measurement between the particle triggers and the three recovered clocks

The three histograms were really identical, as the limiting factor in term of quality was more the jitter of the bunches (of the order of 2ns rms), than the jitter of the systems themselves.

IV. Status

The development of the new system is well advanced. The crates and crate controllers are available for the experiments. Five prototypes of each transmission and reception modules are available. They are currently being tested by the AB/RF and the PH/ESS groups. The RF2TTC prototype arrived at CERN at the beginning of October and is being tested now, together with its VME library. A second version of the TTC fanout is being produced and should be available end of October.

The fibres have been requested from the SR4 point (were the 40.078 MHz and the 11kHz orbit will be generated), down to the experiments control rooms. The installation campaign already began, and the path between SR4 and the CERN Control Room will be cabled by the end of November.

A library to control the full receiver crate, as well as an Application Program Interface (API), is being developed by PH/ESS for the experiments and will be delivered to them in November.

A Production Readiness Review (PRR) will occur at the end of 2006, once AB/RF has validated the transmission and reception modules, and once the experiments have had the opportunity to use the system and to give their feedback.

V. References

[1] TTC website: http://ttc.web.cern.ch/TTC/intro.html

[2] Web site of the TTC upgrade: http://ttc-upgrade.web.cern.ch/ttc-upgrade/

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[5] Baron, S., Baudrenghien, P., Monera, A.: MITEQ optical link evaluation report: http://ttc-upgrade.web.cern.ch/ttc-upgrade/New_system/MITEQ_link_evaluation2.pdf

[6] Baron, S., Baudrenghien, P., Monera, A.: Digital optical link evaluation report: https://ttc-upgrade.web.cern.ch/ttc-upgrade/New_system/Digital_link_evaluation.pdf

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[8] Schematics of the Analogue optical transmitter board: https://edms.cern.ch/file/715065/1/EDA-01331-V1_sch.pdf

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[10] Schematics of the Digital optical transmitter board: https://edms.cern.ch/file/750587/1/EDA-01380-V1_sch.pdf

[11] Schematics of the Digital optical receiver board: https://edms.cern.ch/file/750610/1/EDA-01382-V1_sch.pdf

[12] Schematics of the RF2TTC board: https://edms.cern.ch/file/724978/2/EDA-01357-V2_sch.pdf

[13] Schematics of the TTC Fanout board: https://edms.cern.ch/file/686063/2/EDA-01240-V2_sch.pdf

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