The Vertex detector of the LHCb Experiment: The VeLo

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Abstract

The LHCb experiment is the dedicated b physics experiment of the LHC that will study CP violation and rare b decays. Its vertex detector called *VeLo* (Vertex Locator) has been designed to achieve an impact parameter resolution of 14μm + 35μm/p$_T$ and a propertime resolution of 40fs^{-1}. The main components of the detector and module are introduced focusing on the radiation hard front end Beetle chip, the radiation tolerant silicon sensors and the readout system of the detector. In preliminary testbeam results a resolution of 8μm and 4μm for tracks of angle 0.16rad has been measured. Construction, assembly and commissioning are currently on going. The latest commissioning showing the successful performance of the VeLo alignment algorithm.

I. Introduction

The $LHCb$ experiment[1] (see figure 1) is the only dedicated b physics experiment located in the Large Hadron Collider(LHC) ring. It is a one arm forward spectrometer whose design has been optimised for the measurement of the $b\bar{b}$ pairs to study CP violation and rare b decays. These include excellent particle identification and vertexing. The vertexing and finding their location are the main tasks of the most forward tracking detector in LHCb called the Vertex Locator(VeLo) which is the main focus of this note.

II. The VeLo

The geometry of the vertex detector has been designed to measure the displaced vertices that are part of the topology of a $b\bar{b}$ event. It is called the Vertex Locator (VeLo) but it is not a vertex detector in the classical sense because it also has tracking capabilities which on average contributes around 13 hits to the global tracking. For LHCb to be sensitive to the expected oscillations in the B_s system the detector has been designed with the following goals in mind. A primary vertex resolution of 8μm for the x and y axis and 44μm in the z direction. The impact resolution of 14μm + 35μm/p$_T$ which results in a propertime resolution of 40fs^{-1}. This has been achieved by placing the detector in vacuum and as close as possible to the LHC beam with the edge of the sensors being only 8mm from the centre of the beam.

Another task the VeLo has been designed for is to contribute to the High Level Trigger(HLT) [3]. This is an offline trigger which first uses the Rz information of tracks to find B-decays and if promising the Phi coordinates. Once fitted the information is fed to the next stages of the HLT.

Physically the VeLo detector is approximately 1m long and is composed of two halves. Each half possess 21 modules whose instrumented face is perpendicular to the beam. The two halves are operated in vacuum and can be moved towards or away from the beam. The beam vacuum is separated from the detector vacuum by a 250μm thick aluminium $RFfoil$ on each side. The detector uses evaporative cooling with CO_2 gas and the electrical connection to the module is achieved by flat kapton cables through a 50 pin feedthrough. A detailed description of the VeLo can be found here [2].

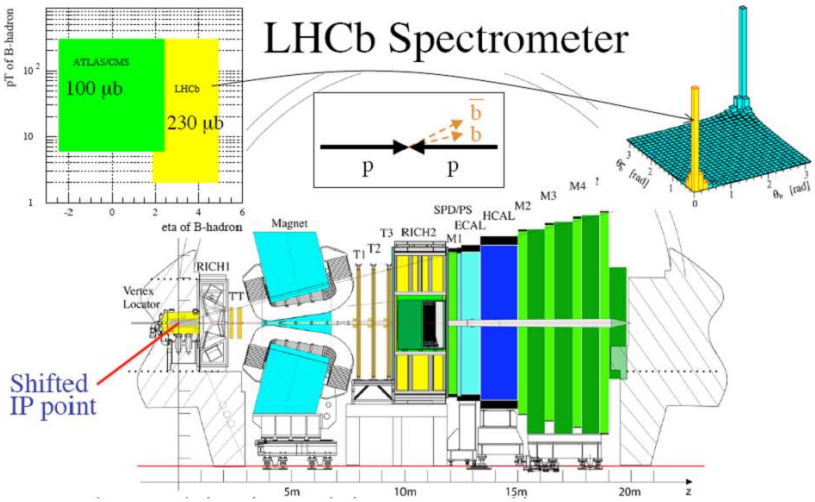

Figure 1: The LHCb spectrometer featuring the VeLo detector at the front.

The are a number of constraints that has influence the design of the VeLo module. The major constraints are:

1 The instrumented region to be placed as closed as possible to the beam to minimise the distance between the primary vertex and first point of measurement.
2 To be able to withstand the high radiation dosage expected at the LHC.
3 The position of the clusters to be measured in cylindrical coordinates.
4 Minimise the scattering from the supporting structures.

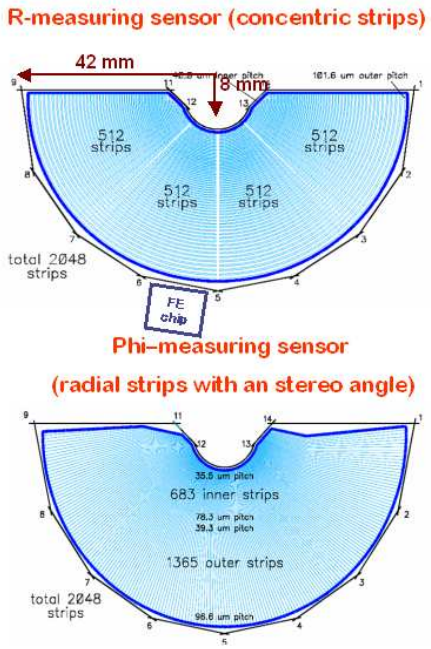

Figure 2: The Phi and the R measuring sensors that are part of each VeLo module.

The first constraint was addressed by having sensors with a semi circle shape as shown in figure 2 with the inner radius being 8mm and the outer radius 42mm. The cylindrical coordinates system is achieved by instrumenting each sensor with either concentric or radial strips. Each sensor has a total of 2048 strips whose pitch increases with respect to radius (40-100μm) keeping the occupancy of each channel uniform and allowing the complete surface to be instrumented.

The sensor is a single sided 300μm thick n-on-n oxygenated silicon fabricated by Micron. It has been designed to deplete from the back and after type inversion to deplete from the strips. This technology has been developed to allow sensors to withstand the high radiation environment that the VeLo will operate in, 1.3×10^{14} neq/cm^2/year at a radius of 8mm and 5×10^{12} neq/cm^2/year at the edge of the sensor (r = 42mm)[4].

The module (See figure 3) has two sensors of each type that are glued back to back on opposite surfaces of the hybrid. A double sided kapton circuit is also glued to its surface. The heat generated is efficiently removed due to the construction of the hybrid, a TPG plane in between a number of carbon fibre rectangles.

Another important features of the module is the paddle to which the hybrid is glued to. The purpose of the paddle was to move the supporting plate away from the beam in accordance to the last constraint previously listed. Physically the paddle is a carbon fibre shell with a height of 16cm whose surface has been treated to minimise outgassing during vacuum operation.

Figure 3: A VeLo module. The main components shown are the paddle, the hybrid, the front end chips and the sensor.

III. The Beetle chip and its selection

The front end readout chip that is employed by the VeLo module is the Beetle v1.5. The chip is radiation hard by virtue of the process technology (0.25μm standard CMOS with a thin gate oxide, $t_{ox} \approx \mathring{A}$) used for its fabrication and the consistent used of enclosed NMOS transistors. The latter reduces the shift in the transistor threshold voltage and eliminates leakage current paths. The design has incorporated triple redundant logic to minimise Single Event Upsets (SEU) and has been tested up to a radiation dose of 130MRads. A complete description can be found here [5].

The Beetle chip has 128 readout channels which can operate in analogue or binary mode. Each channel has an analogue front-end which consists of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. For VeLo operation the comparator that discriminates the acquired pulse is not enabled, only the shaper output is sampled and stored into the analogue pipeline.

A complete VeLo will require a total of 1344 chips. Ideally these chips will be identical in their characteristic and performance, making it easier to understand the capabilities and degradation of the VeLo during its operation at the LHC. In reality the performance tend to vary from chip to chip hence the need to test each single one and select a batch whose characteristics are within defined limits. The testing referred to as wafer probing[6] focused on the Beetle's power consumption, digital performance, characterisation of the analogue front ends and DACs used to bias the different circuits on the chip.

The power consumption focused on measuring the current drawn by an individual chip after power on and during normal operation. The digital performance mainly involved exercising the chip's communication on the I2C bus and the transfer of data. The characterisation of analogue front end was performed on each channel of the chip for a number of bias settings. From each pulse obtained parameters were extracted as shown for a typical pulse in figure 4. Finally all the DACs relevant to the operation of the chip were exercised allowing their gradient and correct operation of each bit to be measured and asserted.

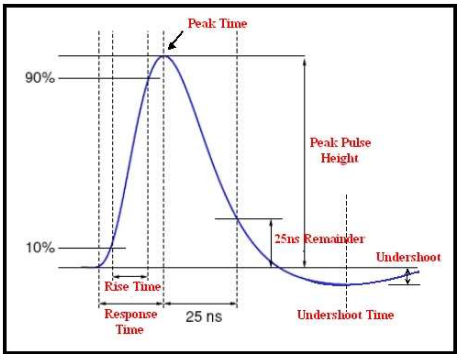

Figure 4: The typical pulse shape from a Beetle channel.

The analysis of all the measurements and tests, developed in Glasgow [7], resulted in 69 variables being defined that characterised the performance of a Beetle chip. For each variable distributions were created which included the values of the same type of chip from 18 wafers. A total of 4299 chips composed each distribution. The selection criteria was implemented as cuts about the mean of the distributions. The value of the cut was calculated by multiplying the RMS of the distribution by a factor. This factor has direct influence on the uniformity of the batch and thus the yield of the selection criteria.

A problem that was encountered during the analysis was related to the non correlation of the different distributions. For example chips with average currents would have a dac gradient which was outside the limits. The actual gradient would have little effect on the performance of the chip but a one factor policy would see chips like this being rejected even though important parameters such as the currents were within limits. To overcome this problem and maximise the yield, the variables were classify into two groups. The first group contained all the variables whose value was deemed important towards the performance and operation of the chip. A very stringent cut would be placed on their distributions. The second group would contained the rest of the variables and cuts were placed mainly to guarantee functionality.

The first group was composed of 18 variables such as currents, all the digital performance and some pulse shape parameters such as $PulseRiseTime$ and the ratio of $Remainder/PulseHeight$. The second group was composed of the remaining 51 variables. The value of the two factors were obtained from a yield map (factor$_1$ vs factor$_2$). It was reasoned that a batch of 2000 chips (a yield of ≈50%) would provide a generous margin over the required number and the corresponding factors (2.2 and 3.5) result in chips whose uniformity is adequate for VeLo operations. The resulting current distribution of the selected chips is shown in figure 5 and typical analogue parameters for a Beetle 1.5 in table 1.

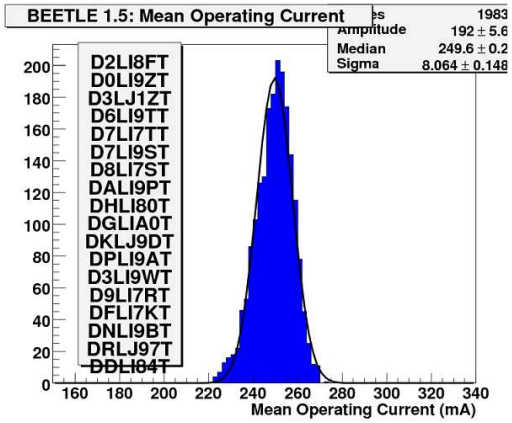

Figure 5: The operating current distribution of the selected Beetle chips.

Variable	Mean	RMS
Pulse Response Time (t90)ns	40.78	0.80
Pulse Rise Time t(90-10)ns	15.41	0.67
Undershoot - Peak Time ns	62.79	1.70
Peak Pulse Height (ADC)	71.64	2.92
Undershoot/Peak Height	-0.113	0.00646
25ns Remainder/Peak Height	0.135	0.032

Table 1: The mean obtained from the distribution featuring ≈ 2000 chips and its RMS for the analogue parameters obtained during the wafer probing. The chips were exercised using the VeLo settings (ITP=24,VFS=56 and VFP=20).

IV. The VeLo DAQ

The VeLo DAQ is composed by a number of systems that performs all the necessary operations to control the front ends, provide clock and triggers and read the digitised data. The implementation of the DAQ has physical components distributed in the counting room (60m from the beam), the balcony (20m from the beam) and outside the VeLo tank. The last two positions require boards to be tolerant to radiation levels of 500Rads and 100kRads respectively.

The control board is located in the balcony and receives the Timing and Fast Control (TFC) signals such as the trigger and the clock and together with the I2C signals to operate the front ends. These are routed to five outputs with each output connected to an individual hybrid through the Repeater board attached to the outside of the VeLo tank.

The repeater board performs a number of functions which are implemented in the mezzanine cards that it carries. The two main ones are: the $Low\ Voltage$ card and the $Driver$ card. The $Low\ Voltage$ card powers the front ends and mezzanines through 8 radhard voltage regulators. The $Driver$ card amplifies the analogue signals from the front ends before they are transmitted at 40MHz through a 60m cable to the receiver card

located in the counting room. The output of the module consists of four analogue links with each link connected to a driver card.

The receiver card is part of the TELL1[8] board which digitises the incoming analogue signal. The TELL1 is an FPGA based signal processing board on which a number of algorithms have been implemented such as zero suppression, clustering and Finite Impulse Response filters with which to process the incoming signal. If a trigger is received the data is sent to the readout network which is implemented as gigabit ethernet and internet protocol (IPV4) with the final destination being the computing farm.

V. Performance of a VeLo module

There has been a number of testbeam conducted by the VeLo group to understand and measure the performance of the VeLo module design. The results presented in this note are from the 2004 testbeam that was carried out at the North Area Facility at CERN. The main results obtained from a module with a 300μm thick Phi sensor are shown in figures 6, 7 and 8. The first graph shows the resolution as a function of strip pitch measured during the testbeam at 250V(middle line). For comparison the corresponding binary resolution and the resolution obtained from a previous Hammatsu prototype at 180V are also shown. The binary resolution is the upper line while the results from the prototype provide the lower limit. The higher resolution of the prototype sensor is attributed to diffusion of the charge which at lower voltages plays a significant role thus allowing the charge to be shared more effectively.

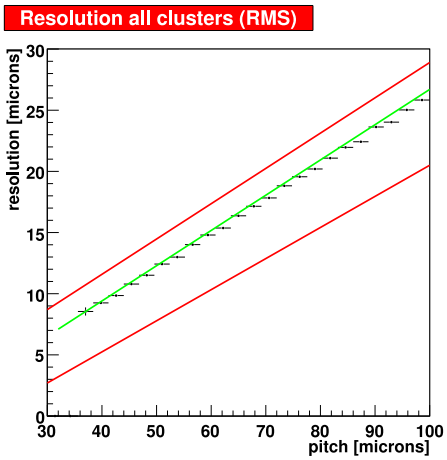

Figure 6: The measured resolution of the Phi module at 250V versus the pitch. The measurement is the middle line while the simulation are represented by dots. This is compared to the resolution obtained with a binary readout scheme(top red line) and the results of an earlier prototype at 180V(bottom red line).

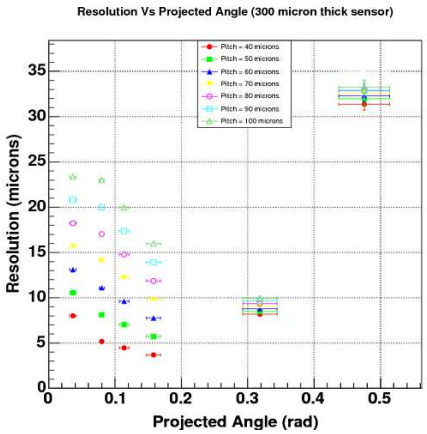

Figure 7: The resolution of clusters for different strip pitch as a function of track angle measured for the 300μm thick Phi module. The average track expected by the VeLo is 0.12rad almost coinciding with the best resolution measured.

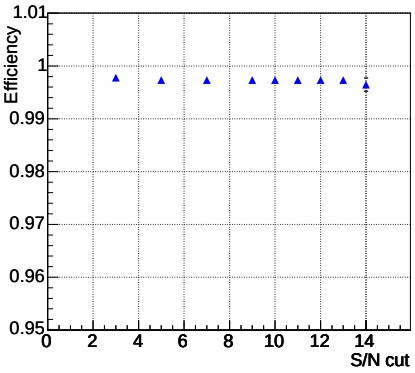

Figure 8: The efficiency of the PHI 300μm thick sensor module as a function of the cut placed on the signal to noise ratio.

The second graph shows the resolution of different strip pitch with respect to angle track. The change is mainly due to the change in geometry that the incident particle experiences. As the angle increases the charge deposited by the track is distributed over a greater number of channels increasing the sensitivity when determining the centre of the cluster. The same effect occurs throughout the sensor as tracks incident on the different strip pitches follow the same trend. The encouraging news is that the average angle of the tracks expected to traverse the VeLo is 0.12rad[4] roughly coincides with the optimal resolution.

The third graph features the efficiency of the module with respect to signal to noise cut. The efficiency is constant throughout much of the range of the cut with a value ≈99.8%. It is only when the cut is greater than 13 that efficiency slightly deteriorates. This together with the two previous graphs shows that the current module design is expected to deliver the design goals for the VeLo.

VI. COMMISSIONING

The current focus of the VeLo group is on the construction, assembly and commissioning of the complete detector. The modules are being constructed at Liverpool and the burn-in performed at CERN before they are assembled into the final mechanics. Once assembled, the detector will be taken to into the pit (IP8) where the complete detector will be commissioned. To ensure the performance is satisfactory, a number of smaller commissions are conducted prior to this one. As production versions of the components become available the complexity and thoroughness of the commission increases. The exercise incorporates everything that is related to the VeLo, software and hardware and they are fondly referred to as ACDCs (Alignment Challenge and Detector Commissioning).

The first ACDC, conducted in July 2006, was an online DAQ exercise. The second, performed in August 2006, included three production grade modules that were powered using production Repeater boards and their data read using the production chain together with cables. On the software side employing the alignment algorithm developed for the VeLo[9] was a great achievement. For the third ACDC, scheduled for November 2006, the final right half mechanics will be installed in the testbeam area containing 10 production modules. This will be the dress rehearsal for the final commissioning since at least 6 modules will be read and controlled simultaneously.

Preliminary results from ACDC2 results are shown in figure 9. Four graphs are shown featuring residuals of only straight tracks from a tested module. The distributions are separated into x and y axis (left and right) together with before and after alignment (top and bottom). The success of the alignment algorithm is evident in the decrease of the sigma of the fitted gaussians to the distributions (50μm to 16μm and 22μm to 19μm for the x and y axis respectively) and their centring around zero. The favourable results of the alignment resulted in the testing of other software components such as the tracking and simulation.

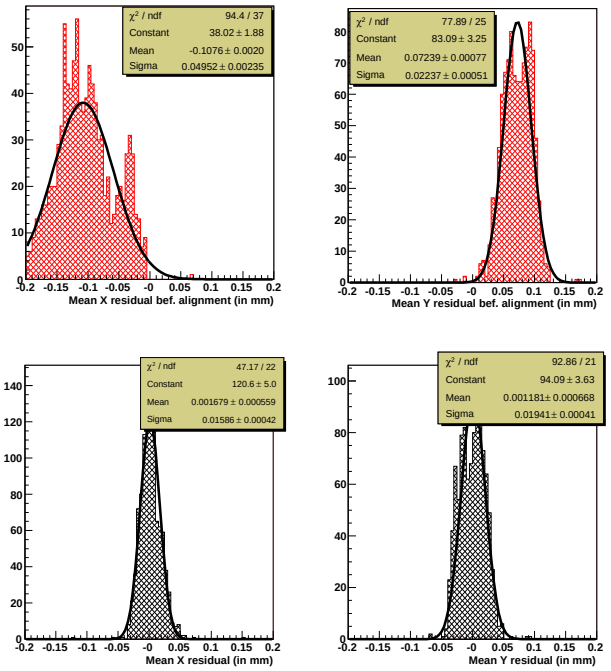

Figure 9: The preliminary residual distributions obtained for straight tracks. A decrease in the sigma of the fitted gaussian and a mean zero are evidence of the alignment performed favourable.

VII. CONCLUSION

The VeLo is a key detector required by the LHCb experiment to achieve its physics program. Its unusual shape is due to the need to maximise its performance with respect to impact parameter resolution, propertime resolution and incorporate acquired data into the second level trigger. The module has been designed to operate in vacuum and in the harsh LHC radiation environment. Radiation tolerant oxygenated n-on-n silicon sensors and the Beetle readout chip, tested upto 130MRads are the key elements of the module.

The selection criteria of the Beetle presented was developed to maximise the performance uniformity of the modules. The yield was $\approx 50\%$ but the resulting number provided a generous margin to complete the VeLo detector. The performance of the module during 2004 testbeam is summarised as having a resolution of 8μm and 4μm for tracks of angle 0.16rad for the smallest strip pitch. This is within the necessary values to achieve the design goals. Currently the group is focussing its efforts on the construction, assembly and final commissioning of the complete detector. Preliminary work with the data taken with ACDC2 allowed modules to be aligned using straight tracks by applying the VeLo alignment algorithm.

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