FEC-CCS: A common Front-End Controller card for the CMS detector electronics.

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Abstract

The FEC-CCS is a custom made 9U VME64x card for the CMS Off-Detector electronics. The FEC-CCS card is responsible for distributing the fast timing signals and the slow control data, through optical links, to the Front-End system. Special effort has been invested in the design of the card in order to make it compatible with the operational requirements of multiple CMS detectors namely the Tracker, ECAL, Preshower, PIXELs, RPCs and TOTEM. This paper describes the design architecture of the FEC-CCS card focusing on the special design features that enable the common utilization by most of the CMS detectors. Results from the integration tests with the detector electronics sub-systems and performance measurements will be reported. The design of a custom made testbench for the production testing of the 150 cards produced will be presented and the attained yield will be reported.

I. INTRODUCTION

The CMS Tracker control system [1] which was initially developed for the needs of the CMS Tracker detector is now adopted by the majority of the CMS detectors as a front-end electronics control system. The flexibility of the design architecture, the availability of the Front-End (FE) ASIC chipset in a radiation tolerant technology as well as the availability of the optical link components were the main reasons that established this system as a "*common*" FE control system for the CMS detectors. The CMS detectors that are using this "*common*" control system are ECAL, Preshower, PIXELs, RPCs and TOTEM.

The design architecture of the control system is illustrated in Fig. 1. The system uses a ring topology configured in a local area network, allowing for a variable number of network nodes to be added in the ring depending on the FE electronics system topology of each CMS detector sub-system. This flexibility of the design architecture is further augmented by the availability of a radiation tolerant ASIC chipset (CCU, PLL, QPLL, DCU) that permits the customization of the FE control functionality depending on the requirements of each CMS detector sub-system.

The connectivity of the control system for the on-detector part is realized with copper links while for the long distance connection with the off-detector electronics controller is realized with a 4 way optical fiber link. The physical layer of the link (electrical or optical) is capable to simultaneously transport to the front-end ASICs the 40MHz LHC clock along with a set of four Trigger Commands and to establish a 40Mbps bi-directional Data Link for control information transactions. The Trigger Commands are clock synchronous and are used for signaling to the front end system the LV1A Trigger, the Resynchronization cycles, the Bunch Crossing tick marks, and the Calibration cycles.
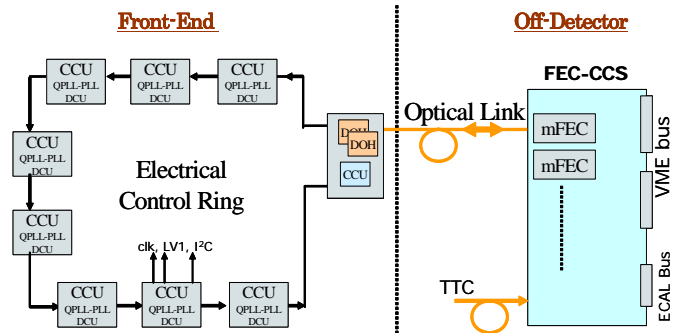

Fig. 1: Front-End electronics Control System

The Front-End Controller card (abbreviated as FEC in the Tracker subsystem) is located in the counting room and serves as the master node of the control rings. In the ECAL detector electronics subsystem this card serves a more central role acting as a local controller for the synchronization of the readout links and the triggers links and is denoted as Clock and Control System card (abbreviated as CCS). Special design considerations were taken in the design of the card in order to address the functionality requirements of both subsystems, thus leading to a "*common*" hardware design, a card named FEC-CCS.

II. FEC-CCS ARCHITECTURE

The FEC-CCS card is a 9U VME64x compliant card following the design rules for custom VME hardware in CMS. The FEC-CCS card functions as a VME carrier for the mezzanine Front End Controller modules (mFECs) that host the functionality of the master controller node for the control rings. Up to 8 mFEC modules can be populated on a FEC-CCS card allowing flexibility in the configuration of the card to tailor for the different needs of the detector subsystems.

As shown in the block diagram in Fig. 2, the FEC-CCS card features a Local Bus that interconnects all the mFEC modules with an FPGA circuit (VME FPGA) that creates a bridge connection with the VME bus. This establishes a "slow

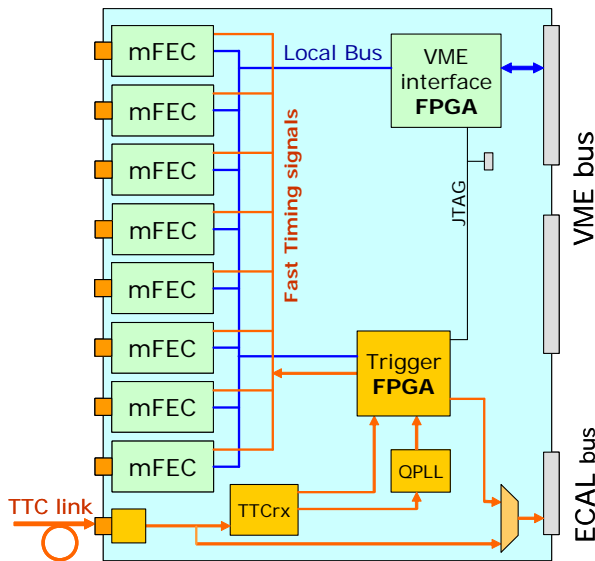control path" that relays slow control transactions from the VME to the mFEC modules.

Fig. 2: Block Diagram of the FEC-CCS card.

The FEC-CCS card features also a "fast timing path" that relays fast timing information from the experiment TTC network to the mFEC modules. The fast timing signals arrive from the TTC link and are decoded by an on board TTCrx ASIC. The TTCrx provides the 40.08MHz system clock and decodes the two channels of the TTC signal: Channel A providing the LV1 accept and channel B providing fast control commands. The fast timing signals are distributed to the mFEC modules though the Trigger FPGA circuit that implements the sub-detector specific Trigger Command handling. A QPLL ASIC is inserted in the timing path between the TTCrx and the Trigger FPGA to reduce the jitter of the system clock and to operate as local clock generator in the absence of the TTC signal.

Fig. 3: Photo of the FEC-CCS card

For the ECAL, Preshower and TOTEM subsystems the FEC-CCS card delivers some extended functionalities like the fanout of the TTC signal and the merging of the TTS (Trigger

Throttling Signals) signals via a special backplane connector that connects to a relatively short length "ECAL bus".

The photo in Fig. 3 shows the final production version of the FEC-CCS card. The performance of the card has been tested successfully in a VME64x crate and all the functionalities have been verified. The measured trigger latency of the FEC-CCS cards was found to be 5 BX (bunch crossings). The power dissipation of a fully configured card (8 mFECs) is ~30W drawing 7A @ 3.3V and 1A @ 5.0V.

A. The mezzanine FEC(mFEC)module

The mFEC is the Front-End Control module for the control link. It is implemented as a mezzanine module that can be plugged into different types of carrier boards. For most test applications a PCI carrier board is most suitable, for installation in the experiments the 9U VME FEC-CCS card will be used. The mFEC consists of a transmit FIFO for data to be sent out of them FEC onto the token ring and a receive FIFO for data coming back from the ring. The two FIFOs are accessible through a Local Bus interface. The mFEC is handling the insertion and circulation of the token on the ring. It generates the data packets that are encoded using the 4b5b encoding scheme. The mFEC also generates the CRC for the transmitted data and checks the CRC for the received data packets. More information about the operation of the mFEC can be found in [2].

B. The VME FPGA

The VME FPGA implements a VME64x compliant slave interface offering D32, A32, VME bus transfers. The block diagram of the VME FPGA is depicted in Fig. 4. The design makes use of the Plug & Play feature available in VME64x implementing a Configuration ROM (CR) and a Command and Status Register (CSR) containing the necessary information for automatic enumeration of the card during the VME system initialization.
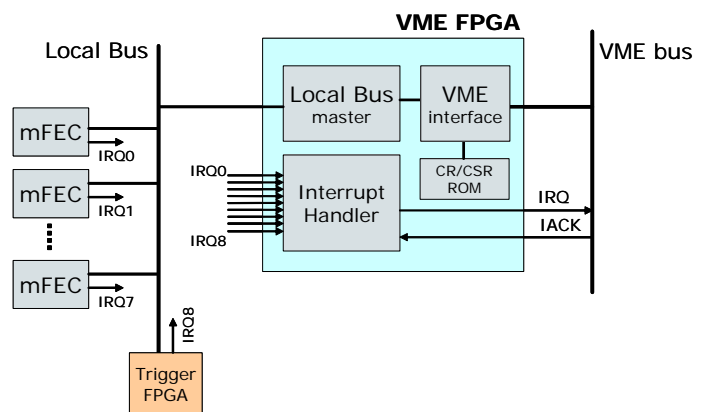

Fig. 4: Block Diagram of the VME interface FPGA.

To communicate with the 8 mFEC modules the VME FPGA implements a Local Bus master node logic. The operation standard for this bus was chosen to be compliant with the Local Bus protocol used by the PCI 9054 PCI Bus Master I/O accelerator chip from PLX technologies [3]. The VME to Local Bus bridge supports VME Block Transfers.

The VME FPGA implements a VME Interrupter logic that can be connected to anyone of the seven VME bus interrupt lines. The Interrupter logic prioritizes the interrupt signals received by the 8mFEC and the Trigger FPGA and modifies their priority order every time an interrupt request is acknowledged sending at the bottom of the priority list the most recently serviced interrupt signal. The mFEC modules generate interrupts every time a packet containing control information from the front-ends return to the mFEC receive FIFO. The user software can exploit this functionality to implement interrupt driven data transfers to/from the front-end electronics.

C.   The Trigger FPGA

The Trigger FPGA is the central component in the fast timing path implementing all the Trigger Command encoding functions as well as all the subsystem depended custom logic. As depicted in the block diagram of Fig. 5, the Trigger FPGA implements a Control Ring Clock Encoder that encodes four "*Control Ring Trigger Commands*" on the 40MHz clock signal with a simple encoding scheme, just by selectively removing a number of pulses over three consecutive clock cycles from the clock stream. Possible transmission patterns are: 100, 101, 110 and 111.
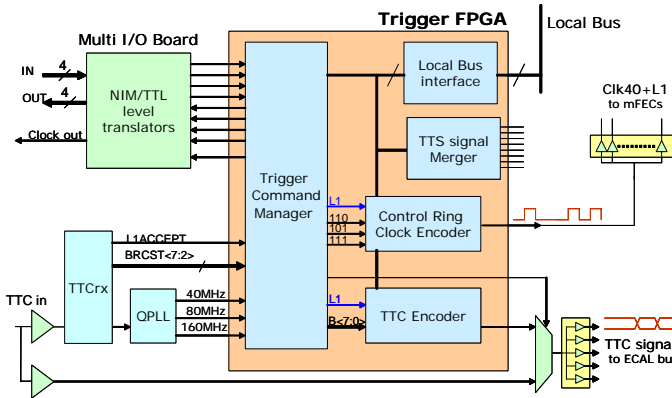

Fig. 5: Block Diagram of the Trigger FPGA.

The Trigger FPGA receives the LV1 accept signal and the B channel broadcast commands from the TTCrx ASIC and assigns them to the four Control Ring Trigger Commands. The LV1 accept signal is always assigned to the '100' Control Ring Trigger Command. The B channel TTC commands are mapped on the remaining three Control Ring Trigger Commands ('101', '110', '111'). Unfortunately these Control Ring Trigger Command assignments are not common among the CMS detector FE electronics. To accommodate for these differences a LUT with five pages, one for each subsystem, is implemented. The pages are user selectable through the Sub-System Identification (SSID) configuration register.

The Trigger FPGA has two distict modes of operation: the "*Remote*" mode which is activated when the TTC signal is detected at the optical input of the card and the "*Local*" mode which is activated on its absence. In the "Remore" mode, the received TTC signal is propagated to the ECAL bus. In the Local mode a TTC encoder circuit in the Trigger FPGA generates the required TTC signal carrying the locally generate Trigger commands as described in the following section of this paper.

To support the ECAL bus functions a Trigger Throttling System (TTS) signal merging logic, combines five TTS signal sources from adjacent VME cards using the priority encoding scheme which is defined by the CMS DAQ group. The combined TTS signal is propagated to the DAQ Fast Merging Modules (FMMs).
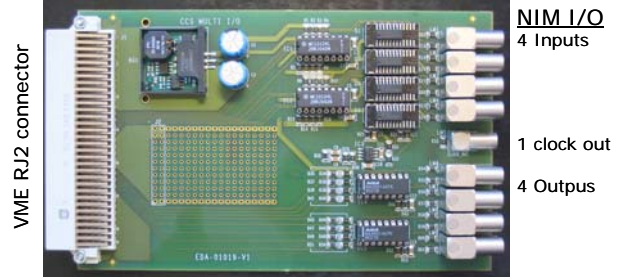

Fig. 6: Photo of the Multi I/O Card.

The Trigger FPGA has a set of four input and four output signals to interface with external equipment. This functionality proved to be extremely useful for system operation in standalone test setups where external trigger sources could connect directly to the FEC-CCS card, without the necessity of a TTC crate, and where the firing of laser pulses for calibration purposes could be command by the FEC-CCS card. Since most of the equipment use NIM signalling levels a level translator card (Multi I/O) has been built and is shown in Fig. 6. The card is 3U rear VME transition card that connects the RJ2 rear VME backplane connector.

D.   Local Trigger Command Generation

The Local Trigger Command generation logic is based on a flexible user programmable logic that can be configured according to the functionality required by the target system setup. A set of eight identical "*Command Channels*" bearing elementary logic circuitry are the sources of the locally generated commands. As depicted in the block diagram in Fig. 7 there are four "Trigger Command Channels" that correspond to the four available Control Ring Trigger Commands ('100', '101', '110', '111') and four "Auxiliary Trigger Command Channels" that can be used to signal commands to external equipment.
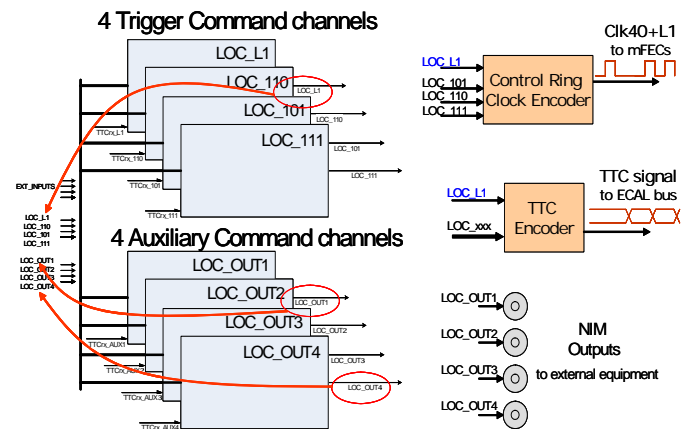

Fig. 7: The Command Channels

The trigger output signals of the command channels are retrofitted to their inputs thus allowing to trigger one another enabling the user to create sequences of multiple trigger commands. With the use of a programmable frequency generator in the Trigger FPGA circuitry, periodic sequences of commands are also possible to produce.
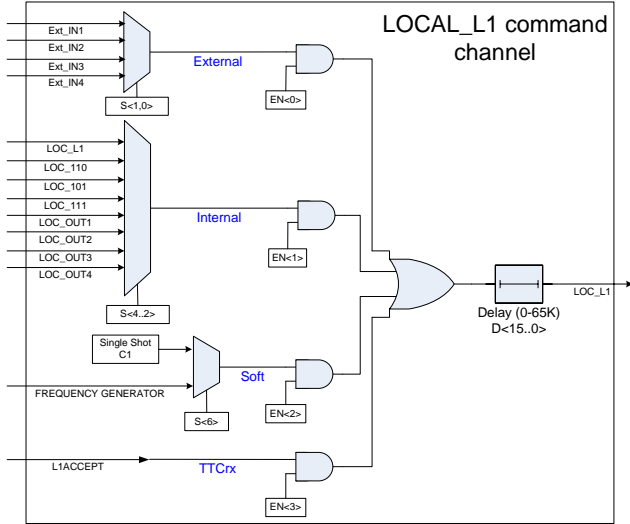

Fig. 8: Block Diagram of a Command Channel.

Each command channel has four different trigger sources that that can be individually selected or mixed. The block diagram of a command channel is depicted in Fig. 8. The trigger sources are four input signals from external equipment, internal signals from the other command channels, software controlled, single shot or periodic trigger signals or signals that can be assigned to TTCrx B channels commands. All external input signal are routed though a special circuitry that allows "debouncing" and synchronisation of the signal with the 40MHz system clock as well as the possibility for programmable prescaling of the received trigger events. A programmable delay in the command channel logic facilitates the proper timing of the locally generated trigger commands with respect to external signals or other trigger commands to match the timing requirements of the target test setup.

III. INTEGRATION WITH DETECTOR SUB-SYSTEMS

A. The CMS Tracker Case

A schematic diagram of the CMS Tracker readout and control system [4, 5] is shown in Fig. 9. In this system there is a clear distinction and separation of the readout system and the control system. There are separate VME crates hosting the Front End Driver (FED) cards and the FEC cards. There is no direct communication between the two crates. The FED and the FEC crates receive the trigger commands via identical TTC signals from a Tracker TTC crate equipped with a set of cards that generate and fanout the TTC signal and also establish the two Trigger Throttling feedback loops. The first Trigger Throttling feedback loop is relized by the APVE (APV emulator) card while the second by the TTS signals from the FEDs and the FMM and LTC cards.

The successful operation of the FEC-CCS card in the Tracker readout and control system has been demonstrated in

multiple setups, namely the Tracker electronics integration centre, the Tracker Integration Facility (TIF) and the CMS Magnet Test and Cosmic Challenge (MTCC) test setup that took place during the summer of 2006.
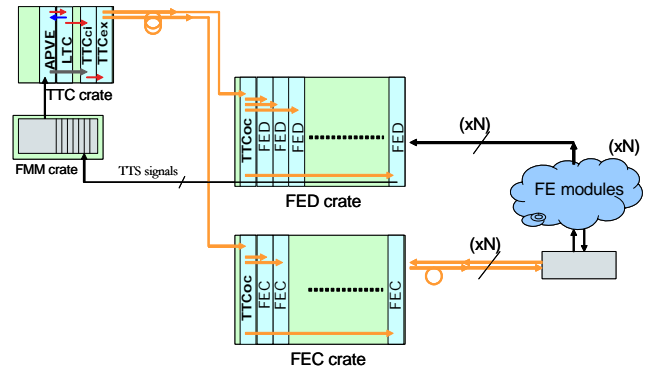

Fig. 9: The CMS Tracker Readout & Control System.

A number of FEC-CCS cards have also been distributed to external institutes to equip the facilities of the tracker integration test setups.

B. The CMS ECAL Case

A schematic diagram of the CMS ECAL readout and control system [6] is shown in Fig. 10. In this system the readout, the trigger and the control systems coexist in the same crate. The FEC-CCS card plays a more central role here distributing the clock and the trigger commands to the DCC (Data Concentrator Card) and the TCCs (Trigger Concentrator Cards) through the special ECAL backplane bus and merging the TTS signals generated by these modules. This set of DCC, FEC-CCS and TCC modules forms an "entity" of off-detecor electronic modules capable to readout and control one ECAL supermodule structure.
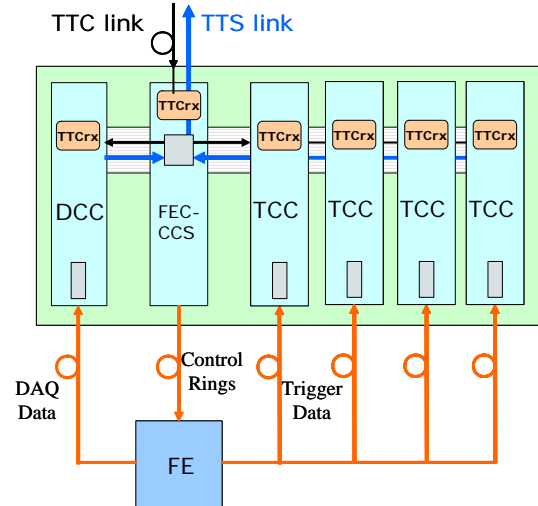

Fig. 10: The CMS ECAL Readout & Control System.

The successful operation of the FEC-CCS card in the ECAL readout and control system has been demonstrated in five different test setups. The Local Trigger generation logic proved to be very flexible and versatile, permitting to adapt to the requirements of each test setup namely the supermodule integration hall in building 867, the H4 cosmics calibration

stand, the H4 test beam stand and the H2 ECAL+HCAL test beam stand. The successful operation of the ECAL readout and control system using an external TTC signal source was demonstrated during the summer 2006 CMS MTCC run.

The Preshower [7] and the TOTEM [9] detectors will be using a variant of the ECAL backplane bus while the Pixels [8] detector will follow the Tracker detector system approach.

IV. PRODUCTION & TESTING

For the production testing of the 900 mFEC modules and the 150 VME FEC-CCS cards a common custom made test bench has been prepared and operated at CERN. The production testing was performed in two stages. In the first stage all the 900 mFECs were tested using one selected FEC-CCS card as carrier. In the second stage the 150 FEC-CCS cards were tested while being populated with the previously tested mFEC modules.
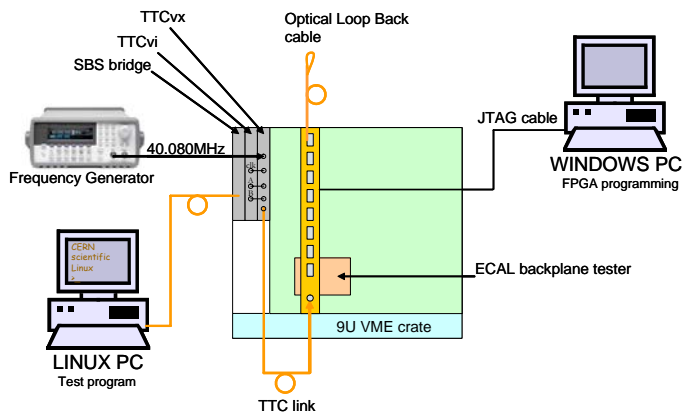

Fig. 11: The FEC-CCS Production Testing Setup.

As can be seen in Fig. 11, the production test bench is assembled around a 9U VME crate hosting a FEC-CCS card. The crate is equipped with a TTCvi and a TTCvx card to generate a TTC signal with properly encoded trigger and B channel commands. A frequency generator tuned at 40.080MHz serves as the LHC clock reference generator. A set of optical loop back cables have been specially prepared to connect at the mFEC optical ports creating virtual control rings allowing the transmission of control packets. A PC running WINDOWS OS and a firmware programming tool is used for the card firmware uploading via the JTAG bus. A second PC running LINUX OS, acts as a VME crate controller and executes the specially developed test software. The production testing procedures involve the transmission of control packets of variable length on the rings, the decoding of trigger commands, the locking of the QPLL on the LHC clock frequency and the functionalities of the ECAL backplane.

From the 900 mFECs that were tested 35 modules were found to be defected. A post production of 50 more modules was executed to compensate for the rejected modules. The production testing of the 150 FEC-CCS card is currently in progress. The cards show very high production yield. Nearly 60 prototype FEC-CCS cards have been already delivered to

the CMS sub-systems to participate in various detector test benches and test beam data taking systems.

V. CONCLUSIONS

The FEC-CCS card has been developed as a common Front End Controller card for the CMS detectors. Adopting a modular hardware design, using the mFEC modules, and a flexible, user programmable timing logic we have succeeded in developing a card that merges the requirements of different CMS detectors.

The operation of the card has been successfully demonstrated in numerous system setups. The production testing is near to its completion and cards are currently being delivered to equip the CMS electronics subsystems.

Having a common hardware module minimized the development effort and the associated cost and will certainly facilitate the maintenance during the operation period of the CMS experiment. To enable the seamless utilization of the FEC-CCS modules across the different CMS subsystems a high level of programmability has been introduced in the firmware design so that not only a common hardware module but also a unique firmware version could be deployed to all the cards for all the sub-systems thus minimizing the effort for system maintenance and support for the years to come.

VI. REFERENCES

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