RF Issues and Developments at the LHC Machine

A. Butterworth, L. Arnaudon, P. Baudrenghien, J. Molendijk

CERN, 1211 Geneva 23, Switzerland

andrew.butterworth@cern.ch

Abstract

The main RF system of the LHC, which uses 400MHz superconducting cavities, will be used to capture, accelerate and store the injected beam. A separate transverse damper system using electrostatic deflectors will be used to damp transverse oscillations. The associated low-level RF (LLRF) equipment is responsible for fast control of the accelerating voltage and phase in the cavities, the phase and radial position of the beam, and the synchronization of beam transfers between SPS and LHC. The LLRF system combines high-frequency analogue components with digital signal processing using FPGAs and DSPs. The extensive use of digital technology allows not only to achieve the required performance and stability but also to provide full remote control and diagnostics facilities needed in a machine where most of the RF system is inaccessible during operation.

I. INTRODUCTION: THE LHC RF SYSTEMS

The LHC will have one RF acceleration system and one transverse damping system. An additional RF system is foreseen for future high intensity operation:

1. *The 400 MHz main acceleration system* [1], which is used to capture, accelerate and store the beams. There are 2 independent RF systems, one per ring, each using 8 Cu/Nb superconducting cavities cooled by liquid helium at 4.5º K. Each tunable cavity is driven by a 300 kW klystron amplifier, and has a variable main power coupler allowing it to produce 1 MV at injection and 2 MV at top energy.
2. *The 200 MHz capture RF system* [2], which facilitates capture of the injected beam coming from SPS. The large 200 MHz bucket allows capture of beams with a longitudinal emittance of 1.0 eVs.. However, up to nominal intensity, the SPS is capable of producing beams with an emittance of 0.6 eVs which can be injected directly into the 400 MHz bucket [3] and so this system will only be installed, if necessary, at a later stage. The 200 MHz system uses room temperature copper cavities developing 0.75 MV per cavity, each powered by a 300 kW tetrode amplifier.
3. *The transverse damper system* [4], which uses electrostatic kickers to damp transverse beam oscillations. The beam position and angle are inferred from two beam position pickups and the trajectory is corrected on the following turn by the kickers. The feedback has a power bandwidth of around 3 MHz to damp injection errors and a low power bandwidth of 20MHz to damp all possible coupled bunch modes, the bunch frequency being 40 MHz. The damper can also be used to excite the beam for measurements and to clean particles out of the abort gap.

II. SLOW CONTROLS

Slow controls for the high-power RF equipment, which includes high voltage power supplies, klystrons, RF waveguide power distribution, cryostats and ancillary equipment, is based on industrial controls using Schneider PLCs [5]. PLC supervision is implemented using the tools provided by the CERN/AB controls group [6]. The system uses industrial components, with the exception of a small number of in-house hardware developments:

- RF power meters with a bandwidth of 50 MHz to 2.7 GHz.
- Optical arc detectors for protection of the waveguide distribution system from damage due to discharges.
- A universal temperature conditioner capable of driving the wide variety of temperature sensors used in the cavity cryo-modules.
- A fast interlock system, opto-isolated with readout via Ethernet or a variety of fieldbuses.

Sequencing and scheduling of equipment for accelerator operation is accomplished via the accelerator control system using the FESA (Front End Software Architecture) framework [7] and its interface with the General Machine Timing system [8].

III. LOW-LEVEL RF SYSTEMS

The RF systems require many feedback loops for fast control of the RF and beam parameters, as well as fast timing for synchronization between accelerators. These fast RF controls are referred to as *Low-Level* RF (LLRF) systems.

A. Challenges of the LHC beam

High beam current: At high beam intensity (0.56 A DC at nominal intensity), beam-induced fields due to the cavity impedance result in beam instability, and fast RF feedback loops around the cavities are required to reduce the impedance seen by the beam [9].

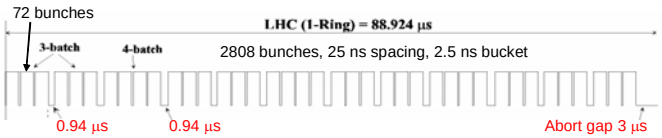

Figure 1: Longitudinal LHC beam structure. 3 or 4 PS batches of 72 bunches are transferred at each injection from the SPS.

Transient beam loading: The uneven distribution of the beam around the LHC circumference (Figure 1), with gaps between the injected batches, means that the cavity is subject to frequent large step changes in the beam current, which must be compensated by fast feedback, with consequent large power transients in the RF equipment [10].

Negligible natural damping: The longitudinal damping time in LHC due to synchrotron radiation for protons at 7 TeV is about 13 hours. In order to retain control of the longitudinal emittance blow-up due to RF noise, the phase noise (jitter) in the total RF system as seen by the beam must be limited to below 0.17° rms, or about 1 ps at 400 MHz [11].

B. *The RF Low-Level system layout*

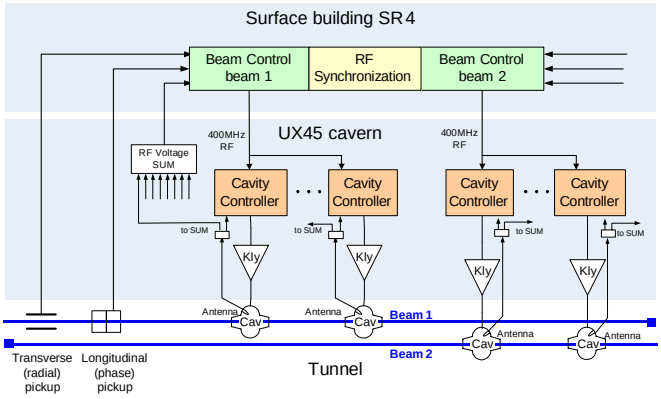

Figure 2: 400 MHz Low-Level system layout (simplified)

A schematic layout of the 400 MHz LLRF system is shown in Figure 2.

The cavity controller implements feedback loops to control the phase and amplitude of the accelerating field in the cavity, using a field measurement from an antenna in the cavity and generating the corrected RF signal which is fed to the klystron. A fast analog feedback path, designed to reduce the effective cavity impedance, with a total delay of around 600 ns, operates in parallel with a slower digital path, designed to give precise control of the 400 MHz fundamental. This direct feedback gives an impedance reduction of a factor 10. A third path, with a one-turn delay, serves to reduce the impedance by a further factor of 10 at the revolution frequency harmonics. The cavity controller also contains slower loops for cavity tuning, which maintains the cavity resonant frequency at the correct value, and for linearization of the klystron amplifier response.

The beam control system implements feedback loops to control the phase and radial position of the beam, measuring by means of longitudinal and transverse beam pickups, and acting on the RF frequency which is sent to the cavity controllers. In addition, the beam control system implements the frequency program which tracks the accelerator's magnetic field during acceleration.

The RF synchronization system provides synchronization between the two LHC rings and fast timing for bunch-into-bucket transfers from the SPS. The synchronization system also provides revolution frequency and bunch clocks to the experimental detectors [12].

IV. Technology Choices for Low-Level RF Implementation

As described above, the LLRF is implemented as a hybrid analog and digital system. FPGAs (mostly Xilinx Virtex-2 and 4) are used to perform fixed-point calculations at 40 or 80 Msamples per second, synchronous with the RF frequency. Examples of the algorithms concerned are digital filters: FIR, IIR, CIC, Half-band, Hilbert etc. and the CORDIC (COordinate Rotation DIgital Computer) algorithm which is used for trigonometric operations and phase comparison. Board control logic, including the VME interface, is implemented in the same FPGAs, usually at an independent clock frequency of 50 MHz.

DSPs (TigerSHARC from Analog Devices) are used for floating-point calculations at the revolution frequency (11kHz) or slower. Examples include the cavity tuning loop, where the frequency response is limited by the mechanical stepper motor actuator to a few Hz, and the beam control loops which must be fast only with respect to the synchrotron frequency, which in LHC varies between 21 and 62 Hz.

High Frequency analog electronics is used where the highest bandwidth and lowest group delay are required.

A. *Integration: crate and form factor*

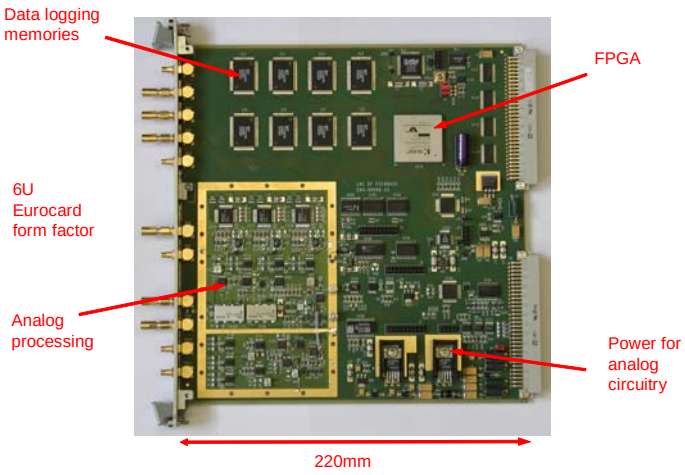

Figure 3: Typical RF Low-Level module: RF feedback

The use of digital technology promises to reduce drastically the amount of space required, as the equivalent of many analogue modules can now be implemented in a single FPGA. However, when considering the physical layout for the LLRF electronics, a number of requirements were identified:

- RF front-end electronics with shielding boxes take up a lot of board space, and the standard VME 160mm Eurocard format was judged by the RF designers to be rather restrictive.
- Large numbers of inter-board connections are required, with multiple clocks, triggers and digital signals.

- High quality linear power supplies are required for the analog RF circuitry.

After considering a number of options, it was decided to define a custom 6U Eurocard format with a depth of 220 mm (Figure 3). A P1-only VME backplane provides an A24/D16 interface, with a custom P2 backplane providing the LLRF-specific interconnects [13].

The custom crate is shown in Figure 4. The four leftmost slots have a card depth of 160 mm and are used to house the PowerPC CPU board and other standard VME modules such as General Machine Timing receivers. A short VME P2 bus is present in these slots to provide an A32/D32 interface. The 15 remaining slots are 220 mm deep with the custom P2 backplane and are used for the LLRF-specific boards.

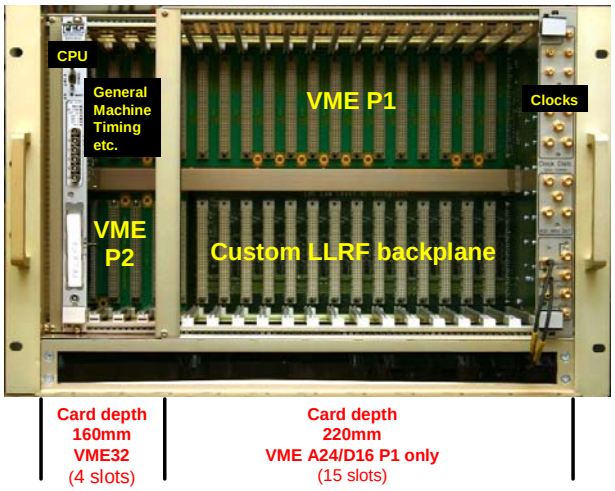

Figure 4: Custom LLRF VME crate

The custom LLRF backplane has a number of features:

- Timing and triggers
- Boot status and cold reset for FPGAs
- Interlocks and alarms
- Beam synchronous 20 and 40 MHz clocks and revolution frequency
- Absolute 10 MHz reference clock for frequency generation
- Digital data exchange between neighbouring boards at 1 Gbit/s
- Serial encoded distribution of function data at 1kHz, 16 channels
- JTAG daisy-chain for reconfiguring FPGAs
- Linear power supplies +/-12V, +/-6V
- 3.3V switched-mode supply for digital electronics

A module serial number bus is also provided, based on Dallas ID chips installed on each board. This allows the serial numbers of all the boards installed in the crate to be read remotely, and gives the possibility of implementing a database-driven management system for calibration data.

V. EMBEDDED DIAGNOSTICS

Since a large part of the RF equipment is inaccessible during beam operation, the provision of adequate remote control and diagnostics is essential. All LLRF VME boards are equipped with on-board data logging memory used to implement "virtual oscilloscopes" to acquire data from "virtual test points" inside the digital signal processing logic. Two parallel sets of memory buffers are provided. One is dedicated to Post-Mortem capture, and runs continuously at full rate until frozen by a Post-Mortem trigger from the backplane. The other, the "observation" buffer, is available for user diagnostics, has configurable sampling rate, and is triggered by a separate backplane trigger line which can be used to synchronize acquisitions between boards in a crate. An example is shown in Figure 5.

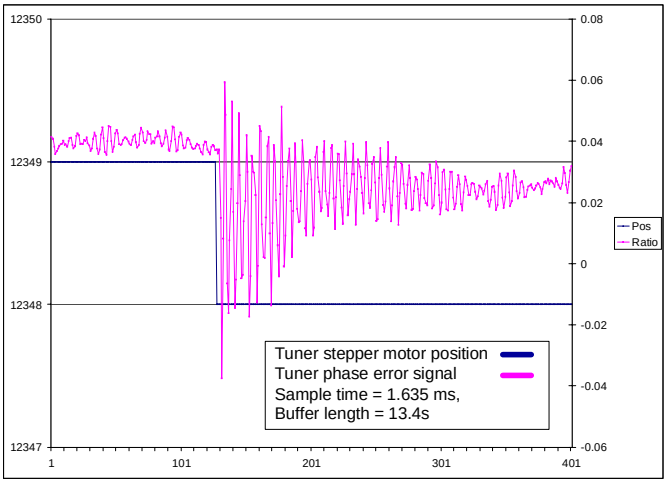

Figure 5: Mechanical resonance of cavity at 144 Hz observed on tuner error signal after motor step

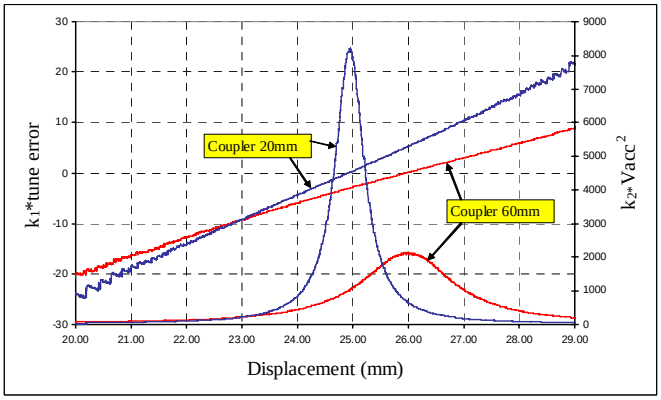

Figure 6: Automated cavity tuner resonance calibration scan

This embedded signal acquisition also enables automation of measurement and calibration procedures (Figure 6).

The logging memory is implemented using PC industry standard cache memory chips, with sufficient depth for acquiring 64 LHC turns at 40Msamples/s. The data is tagged with a revolution frequency marker for time-axis correlation purposes.

VI. HARDWARE DEVELOPMENT STRATEGY

A. Tools

For FPGA programming, the project team has standardized on Visual Elite [14], a graphical environment on top of VHDL which provides a structured design flow, graphical functional simulation and facilitates code reuse. Design portability is important, as although the target devices are mostly Xilinx, some Altera Stratix are also used.

Cadence [15] is used for board design, and its automated FPGA symbol creation facility allows efficient integration of the FPGA designs. The hierarchical features of Cadence allow concurrent design effort, for example development of the RF and digital parts of a board in parallel.

B. Design re-use

In addition to re-use of design components, the flexibility of FPGA-based systems has allowed many entire board designs to be re-used for diverse applications with only firmware modifications. For example, the tuner control DSP board is re-used as the beam control loops processor, the Direct Digital Synthesizer board used for cavity conditioning is re-used for the frequency program, and the 1-turn RF feedback board is re-used in the transverse damper.

VII. RADIATION ISSUES

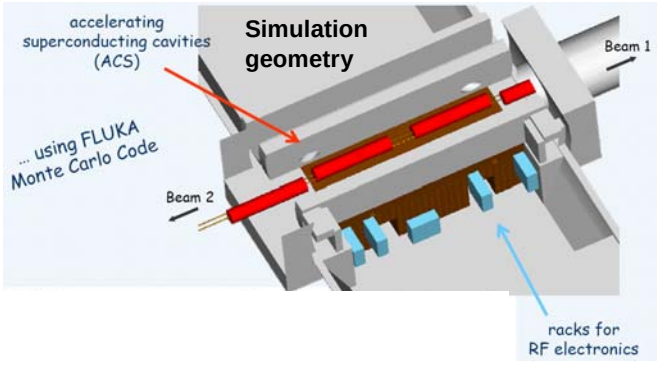

Figure 7: Geometry for FLUKA simulations [16]

Although the RF systems were designed from the outset without active semiconductor electronics in the beam tunnel, the racks containing the LLRF electronics were foreseen, to minimise cable delays, to be placed on a platform close to the cavity modules and shielded only by a 1.2 m thick concrete wall. The shielding was designed for personnel protection from X-rays generated by the cavities during high-power conditioning, but was not foreseen to shield against high-energy hadrons produced during beam operation. With a total of around 250 large SRAM-based FPGAs (typically 1 or 2 million gate Virtex devices) in the racks, it was important to estimate the risk of single-event errors, since a spurious re-configuration of one of these devices could result in the loss of a feedback loop and subsequent beam instability and dump.

A programme of simulations was undertaken using the Monte Carlo code FLUKA [17], to estimate the hadron flux produced by proton interactions with the residual gas in the beam pipe. The geometry used is shown in Figure 7. The results of the simulations showed, as expected, that the risks of radiation damage due to total integrated dose and displacement damage were negligible [16]. However, the expected number of single-event errors due to high-energy neutrons in the FPGA configuration latches was estimated at between 20 and 200 per year under nominal beam and vacuum conditions. This was judged incompatible with reliable beam operation. Since the physical layout precluded the installation of additional shielding around the racks, a decision was taken to relocate them to a position further away from the beam axis and behind an additional shielding wall. In the new location the neutron flux is calculated to be lower by a factor of 4 and there is sufficient space to install additional shielding, should it prove necessary.

Single-event mitigation techniques such as triple modular redundancy were also considered. However, it was decided to avoid the additional complexity of this approach initially, but to ensure that the unused capacity of the devices is sufficient to add redundancy for critical blocks if required at a later date. A hard reboot of all devices will be performed at the end of each LHC fill.

VIII. CONCLUSION

The principal components of the two systems required for LHC startup, the 400MHz RF and transverse damper, are currently being installed in the LHC tunnel. A new, mainly digital, Low-Level system is under construction, implemented using FPGA and DSP technology in a custom VME format with a LLRF-specific crate. The basic functionality of the cavity controller has been successfully tested; the beam control and RF synchronization systems are not yet fully implemented, but must be available for the LHC engineering run at the end of 2007. Extensive embedded signal diagnostics have been designed into the system for remote operation. Possible radiation problems have been considered and precautions taken to avoid them.

IX. ACKNOWLEDGEMENTS

Hardware developments for the LHC Low-level RF, damper and controls: D. Glenat, G. Hagmann, W. Hofle, D. Landre, R. Louwerse, A. Rohlev, V. Rossi, D. Stellfeld, D. Valuch, U. Wehrle. FLUKA simulations: K. Tsoulou, V. Vlachoudis, A. Ferrari.

X. REFERENCES

[1] D. Boussard, T. Linnecar, “The LHC superconducting RF system”, LHC Project Report 316, CERN, 1999

[2] LHC design report, vol. 1, “The LHC main ring”, pp 138-140

[3] J. Tuckmantel, “Simulation of LHC with a realistic RF system”, Chamonix XI, CERN-SL-2001-DI, CERN, 2001

[4] E. Gorbatchev et al., “Transverse damping systems for the future CERN LHC”, Particle Accelerator Conference, Chicago, 2001

[5] L. Arnaudon et al., “Control of the LHC 400 MHz RF System (ACS)”, EPAC2004, Lucerne, Switzeralnd, 2004

[6] F. Locci, “AB/CO supported solution for interfacing PLCs with the machine control system”, 42nd meeting of AB/CO Technical Committee, CERN, 2003

[7] A. Guerrero et al, “CERN Front-End Software Architecture for accelerator controls” ICALEPCS 2003, Gyeongju, Korea, October 2003

[8] J. Lewis et al. “The Evolution of the CERN SPS Timing System for the LHC Era,” ICALEPCS 2003, Gyeongju, Korea, October 2003.

[9] P. Baudrenghien et al., “The LHC Low Level RF”, EPAC2006, Edinburgh, 2006

[10] J. Tuckmantel, P. Baudrenghien, “Adaptive RF Transient Reduction for High Intensity Beams with Gaps”, EPAC2006, Edinburgh, 2006

[11] J. Tuckmantel, “Synchrotron Radiation Damping in LHC and Longitudinal Bunch Shape”, LHC Project Report 819, CERN, 2005

[12] S. Baron, “TTC system upgrade project definition”, EDMS 628545, CERN, 2005

[13] A. Butterworth et al., “Control of the Low Level RF System of the Large Hadron Collider”, ICALEPCS2005, Geneva, Switzerland, 2005

[14] Summit Design, Inc.,

http://www.summit-design.com/products/visual_elite.html

[15] Cadence Design Systems, http://www.cadence.com

[16] A. Butterworth et al., “Estimate of radiation damage to low-level electronics of the RF system in the LHC”, Radiat Prot Dosimetry.2005; 116: 521-524

[17] http://www.fluka.org/