DC to DC Power Conversion

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Abstract

We present results from a capacitor charge pump DC-DC converter prototype using 0.35um HV-CMOS technology fabricated in April 2006. The purpose of this prototype is to test the switch technology both for achievable efficiency and for radiation tolerance. The IC of this test device contains only switches, with all clocks being externally supplied and driven and the capacitors also external. The configuration used is a 4 capacitor stack producing a nominal x4 input current multiplication factor. The goal for this type of device is to be of low enough mass and high enough radiation tolerance to be placed on individual modules in the innermost layers of the Atlas collider detector. Irradiation results will be presented if available. A prototype test card for use with a silicon strip stave prototype is under development.

I. Introduction

This paper describes the progress in our program to develop a switched capacitor DC to DC power conversion module to decrease the amount of current which must be supplied to the ATLAS inner tracker. Over the last two decades the density of silicon tracker modules has increased in each new detector and the proposed upgrades for the LHC detector continue this trend. At the same time the reduction in feature size of the ASICs used in the front end electronics has resulted in lower power supply voltages. The ABCD chip used in the ATLAS SLT tracker uses a 3.3 volt power supply and the proposed upgrade for the pixel detector will use a 1.3 volt power supply [1]. These factors have conspired to increase the current in the power supply busses to the point that the mass of the cables required to transport the power is a determent to the detector. Fig. 1 shows the pixel detector radiation length as a function of pseudorapidity. The green and yellow areas are dominated by power cables. Fig. 2 shows the estimated voltage drop in the cables supplying 2 volts to the pixel detector. Clearly, only 25% of the power is delivered to the detector. Also shown is the corresponding line for a module with a 4:1 power converter that would deliver 62% of the power to the detector and reduce the mass of the supply lines by a factor of 4.

There are two other programs to attack this problem underway. (1) Groups at Bonn and Rutherford Appleton Laboratory have connected up to six modules in series with appropriate shunt regulators to 'reuse' the current [2]. Their work has been reported at the 2006 Hiroshima conference at Santa Cruz. (2) Satish Dhawan at Yale has a contribution to this conference describing a 'buck' regulator to accomplish DC to DC conversion.
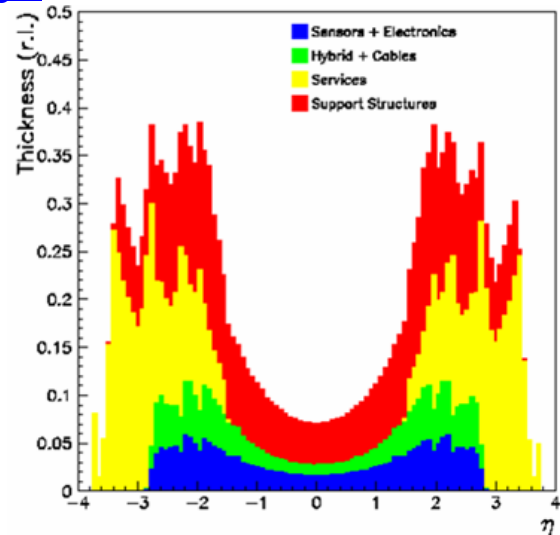

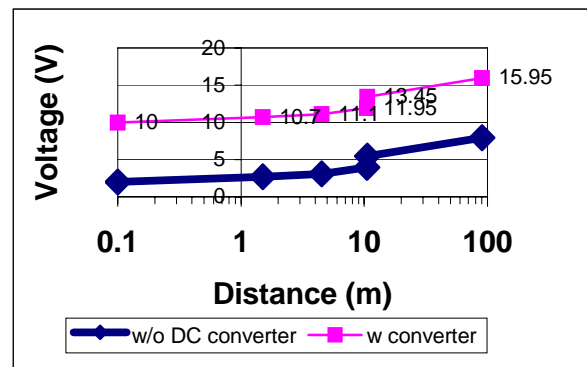Figure 1: Radiation thickness of ATLAS pixel detector vs. pseudorapidity.

Figure 2: Voltage vs distance from pixel detector on proposed pixel power line.

II. Switched Capacitor Options

Switched capacitor circuits are used frequently in industry to step up voltage for displays, a low current application, however devices which step down are rare, mostly divide by two and are not radiation hard at the level required by LHC inner detectors.

There are many circuit topologies that accomplish the same task. They vary by the number of transistors, the number of capacitors and the maximum voltage swings incurred during the operation. M. Makowski and D. Maksimovic [3] have analyzed the general problem. We have selected the circuit shown in Fig. 3 for prototyping because it is efficient in the sense that the charge accumulated in the charging half-cycle is transferred to the output node in the

following half-cycle and because the capacitors, in normal operation, have the lowest potential.

Divide by 4 Stack

4 capacitors – 10 switches
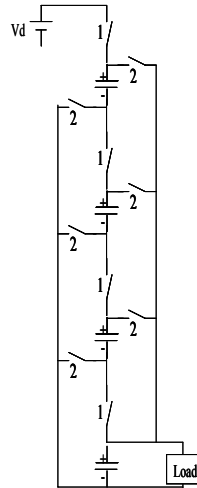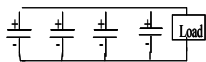
- Phase 1 - Charge
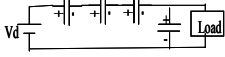
- Phase 2 - Discharge

Figure 3: A divide by four switched capacitor circuit.

In order to achieve the desired level of radiation hardness, the cmos switches have to be fabricated in a submicron technology with a thin (<10nm) gate oxide but the maximum drain-source voltage in normal processes is less than five volts. We have designed our first prototype using a commercial high voltage process (H35) that uses an extended drain structure that will hold off up to 50 volts, has a 0.35 micron minimum feature size and has a 9nm gate oxide. Table 1 is a partial list of the transistors available in this including the transistors used in our prototype.

Table 1: H35 process transistors

Device Name	Min. L(μ)	Max. Vgs(v)	Max Vds(v)	On Res. L = min W= 50mm	Cg (pf)
NMOSI	0.5	3.6	3.6	0.06	125
NMOS50T	0.5	3.6	50	0.54	364
PMOS50T	1.0	3.6	50	0.73	369

The NMOSI transistor is not a high voltage transistor but it is isolated in a triple well whose potential can be moved from ground to the input potential (Vdd). It has a significantly smaller 'on' resistance.

III. CIRCUIT SIMULATION

The circuit in Fig. 3 has been simulated with Iout = 1 amp using the design kit provided by the foundry. To keep the total mass small, the switched capacitors have a value of 0.2 uf. The output capacitor is chosen to be 4.7 uf to reduce the ripple.

The figures of merit that we use to judge the circuit are:
- Voltage efficiency – ε_V = 4*Vout/Vin
  - Vout is a function of the load, Vout = Vin/n for no load
- Current efficiency – ε_I = Iout/4*Iin
  - Charge is lost charging the gate capacitance of the switches
- Power efficiency - $\varepsilon_P = \varepsilon_V * \varepsilon_I$

Fig. 4 shows the power efficiency vs transistor width (with minimum length) for three frequencies and Fig. 5 shows the voltage and current efficiency as a function of period for transistors with the optimum width.
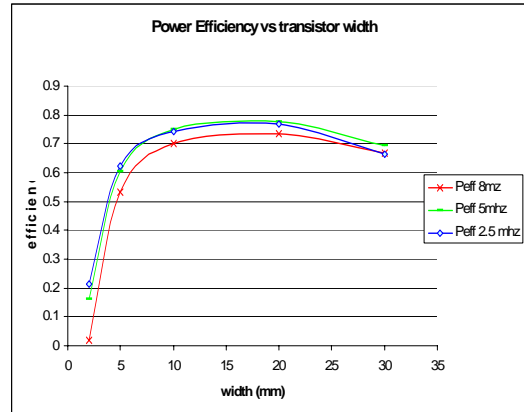
Figure 4: Power efficiency vs transistor width for clock frequencies of 8 Mhz, 5 Mhz and 2.5 Mhz.

At a operating frequency of 5 Mhz the maximum voltage effiency is 82% and the maximum current efficiency is 92%. The ripple was 1.2% and the output impedance is 0.25 ohms. A final circuit must include a clock generator and probably a post regulator which will reduce the efficiency by at least 10%.
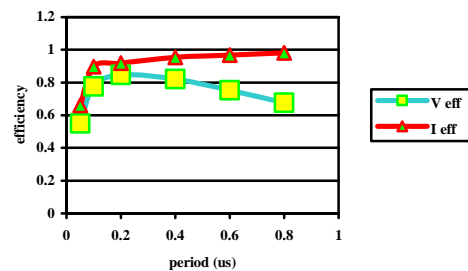
Figure 5: Voltage efficiency and current efficiency vs period.

IV. DC2DC_0 PROTOTYPE

We are preparing a fully functional design for submission next year. In the meantime we were able to submit a test chip, DC2DC_0, for a divide by four stack sized to supply 0.25 amps. The purpose was to test the concept, characterize the transistors and test the radiation hardness of the transistors. The circuit is shown in fig. 6.

Fig. 7 shows Vout vs Vdd for output loads of 10 ohms and 100 ohms. Unfortunately the ratio of the input current to the

output current is approximately one due ta parasitic transistor in the MODNI transistors during the discharge cycle. This feature is known to the present design kit but was announced after our submission. This problem can be fixed in the next submission by adding bulk bias control to the triple well transistors.
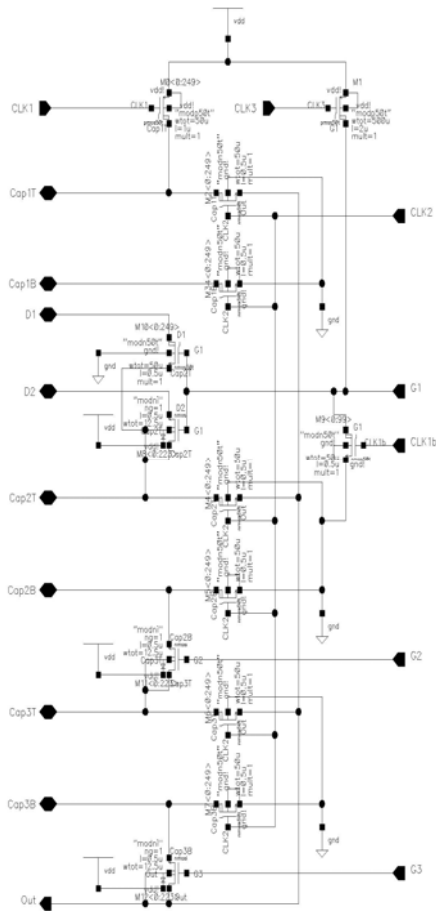

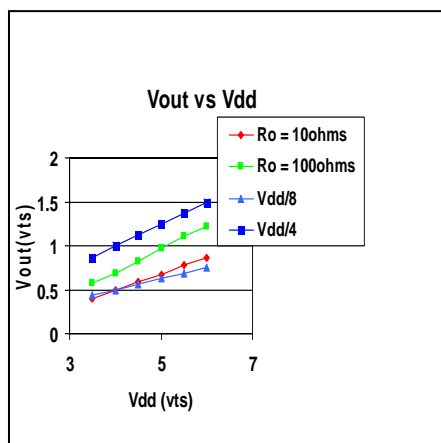Figure 6: DC2DC_0 circuit diagram

Figure 7: Vout vs Vdd for DC2DC_0 configured as a divide by four stack.

Each of the transistor types have been characterized using an Agilent 4156C and the results were compared with the models supplied by AMS for both hspice and eldo. Fig. 8 shows two curves for the NMOS50T. In general the models

for the n channel devices compare poorly. In particular the 'on' resistance of the switches, the rds at low vds, is nearly 40% greater than the models predict. This will lead to larger transistors in the final design.
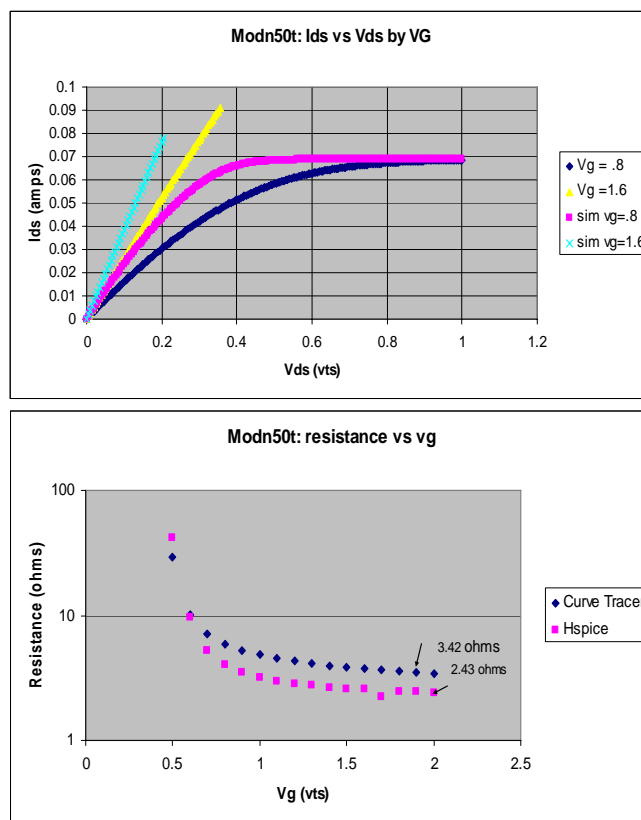

Figure 8: Comparison of (a) the measured and simulated I-V curves for a nmos50t (Modn50t) and (b) the resistance (rds at low vds) vs Vg.

V. RADIATION TESTS

After the conference we exposed one chip to the 55 Mev proton beam at the 88" cyclotron at LBNL. A beam current of 30 na was focused to approximately 1 cm in diameter and, over a period of about 4 hours, the delivered dose was about 70 Mrad. Three transistors, a nmosi, a nmos50t and a pmos50t, were powered with a Vdd of 4 vts in a diode configuration and the gates (and drains) were clocked at 1 Khz to about 0.8 vts. The results are still being analyzed but in general all transistors seem to have survived with threshold shifts of less than 0.2 volts. The transistors were characterized after the radiation and figures 9a and 9b show the before and after IV curves for the nmos50t. The most important result affecting the circuit is that the rds has increased by about 10%. . The tests were conducted at room temperature and the chip was not refrigerated after the test.

The leakage current during the off state of the switches was monitored during the run and for five days after the run. The currents started in the nanoamp range and quickly increased to a maximum of 4 microamps. Two days after the run all of the leakage currents had decreased to less than 0.6 microamps and they remained steady for the next three days.
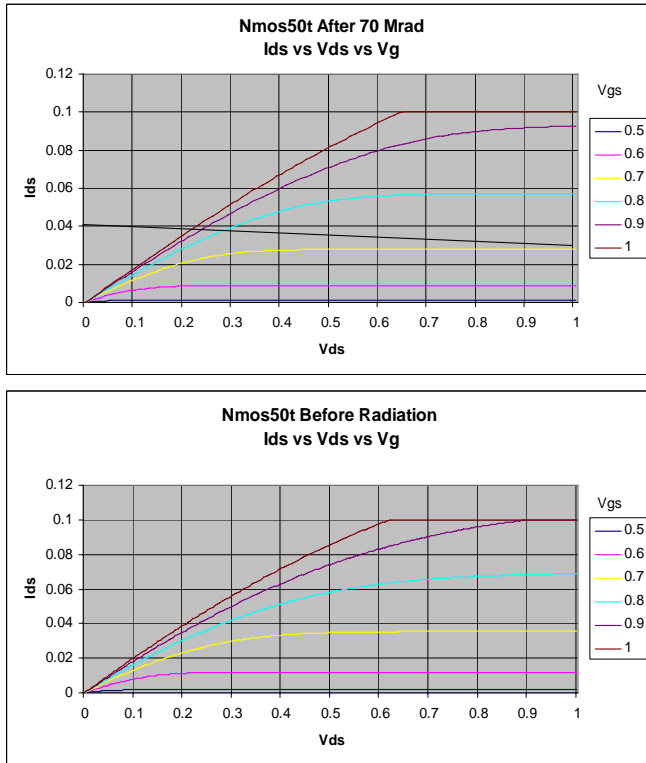
Figure 9: Characteristic curves for a nmos50t transistor before and after radiation with 55 Mev protons to a dose of 70 megarads.

VI. CONCLUSIONS

We have tested a prototype switched capacitor DC to DC converter fabricated with a commercial CMOS 0.35 micron high voltage process (H35). The resistance of the switches falls within the parameter variations of the process but is 40% greater than the models predict. The chip was exposed to a 55 Mev proton beam to a dose of 70 Mrad and the transistors survived with threshold shifts of less than 0.1 vt.

The next generation of this chip is being designed to supply one ampere. It will have internal clock generation, bulk bias control and post regulation. We plan to submit it for fabrication in February 2007.

VII.   REFERENCES

[1] F. Campabadal et al., "Design and performance of the ABCD3TA ASIC for readout of silicon strip detectors in the ATLAS semiconductor tracker," Nucl. Instrum. Meth. A552: 292-328, 2005

[2] "Sixth International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors," Carmel Mission Inn, California September 11-15, 2006

[3] M. Makowski, D. Maksimovic, "Performance limits of switchedcapacitor DC-DC converters," IEEE PESC, 1995 Record, pp. 12151221