April 21, 2008

Performance of the TileCal super-drawers from a global analysis of the MobiDICK tests

ATL-TILECAL-PUB-2008-007
22 April 2008

David Calvet [a], Vincent Giangiobbe [b]

[a] *LPC Clermont-Ferrand*
CNRS/IN2P3 - Université Blaise Pascal
24 avenue des Landais, - F-63177 Aubière cedex
[b] *Univerità di Pisa e Istituto Nazionale di Fisica Nucleare, Sezione di Pisa*
Polo Fibonacci Largo B. Pontecorvo, 3 - 56127 Pisa

Abstract

This note describes a global analysis of the tests of the TileCal front-end electronics, which has been performed in order to determine the spread of the characteristics. These results could be used to define the acceptance limits for further tests of the front-end electronics.

All the TileCal super-drawers have been tested during their production in the LPC Clermont-Ferrand, during their installation in the TileCal modules at the surface at CERN, and later inside the modules either in the Atlas cavern or still at the surface. The tests at CERN have been performed using a dedicated mobile test bench (MobiDICK) and the results of the tests performed at the end of the certification phase have been archived (see figure 1).

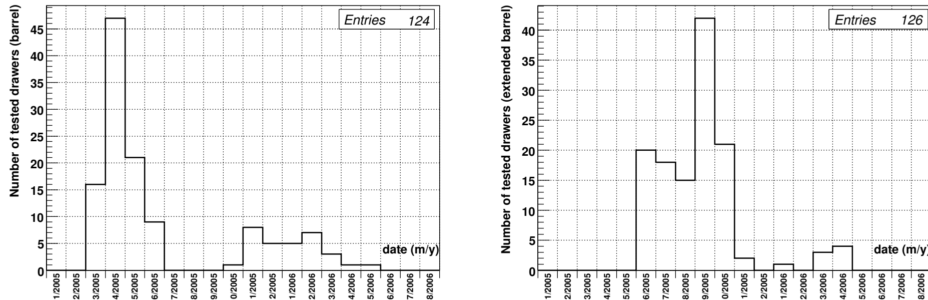

Figure 1: *Time schedules of the tests that have been used in this note. Left : long-barrel modules (tested in the ATLAS pit). Right : extended-barrel modules (tested on surface).*

In this note, a short description of the TileCal front-end electronics is given in section 1. The mobile test bench (MobiDICK) is then described in section 2. Section 3 presents the list of tests performed by the MobiDICK system. For the tests where the information is relevant, a global analysis of the results is also presented. By global analysis we mean an analysis of the results obtained for all the tested and certified super-drawers. Such a global analysis gives an idea about the spread of the TileCal electronics characteristics. It constitutes the best knowledge we have on the dispersion of super-drawer performances. This information should be useful to define the acceptance limits for the super-drawers further tests. It gives also a cross-check about conformity with respect to the original requirements.

1 The TileCal super-drawers

All components of the TileCal front-end electronics are located in the so-called super-drawers [1]. A precise description of the super-drawers electronics can be found in [2]. Each super-drawer is made of two physical drawers which are electronically connected together and can be easily inserted into the module girders. A barrel module (LB) needs two super-drawers to be read out, an extended barrel (EB) module needs only one super-drawer. Therefore, 256 super-drawers are requested to read out the entire TileCal. Each super-drawer is an independent and complex electronic system containing:

- 45 PMT blocks for an LB super-drawer, 32 for an EB super-drawer. Each PMT block contains a light mixer, a photomultiplier, a voltage divider card and a 3in1 card. Each 3in1 card contains a shaper, a charge injection system (CIS) to simulate pulses, a charge integrator circuit for calibration, an amplifier with gains 1/2 and 32, and some control logic;
- the photo-multiplier high voltage distribution system (48 channels): two HVbus cards, two HVopto cards able to deliver individually tuned high voltage to 24 photomultipliers, and one HVmicro to control the overall system;
- up to 96 digitizing channels, to digitize the photomultiplier pulses (low gain and high gain) at 40 MHz, distributed on 8 digitizer cards for an LB super-drawer and 6 for an EB super-drawer. The two outputs of each 3in1 card (low and high gain) are connected to the two inputs (low and high gain) of a given digitizer channel;
- an optical link interface to the Atlas DAQ and TTC systems;
- 9 analog signal summing cards, called adders, for an LB super-drawer and 7 for an EB super-drawer to build the level 1 trigger signals. Each 3in1 card is connected to one adder card and up to six 3in1 cards can be connected to the same adder card, in order to build a single analog signal for each trigger tower ("hadron" output of the adder card). For each adder, the signal of one 3in1 card (corresponding to the cell which is the farthest away from the detector center in this tower) is also connected to the "muon" output of this adder card;
- an ADC called ADC-I to digitize the calibration currents from the 3in1 cards (outputs of the charge integrator circuits).

The super-drawers are cooled with water at a pressure below the atmospheric pressure in order to avoid leaks. Dry air is also flowing inside the girder to flush humidity away.

2 The MobiDICK system

The MobiDICK system (for *Mobile Drawer Integrity Checking system* [3, 4]) has been designed to check the integrity of the TileCal super-drawers after their insertion in the TileCal modules at CERN. The first version of this system was ready in May 2003 for the delivery of the first production super-drawers. All super-drawers have been tested with MobiDICK during their insertion.

An upgraded version of the MobiDICK system has been delivered in March 2005, including a new system to provide a high voltage input to the super-drawer and a LED driver to be able to study the response of the super-drawer to light pulses. Therefore, the present version of the MobiDICK system is able to test all functionalities of a super-drawer. All super-drawers have been tested at least once with this new version of MobiDICK.

The MobiDICK system is fully contained in a custom aluminum box which has a width of 50 cm, a depth of 33 cm and a height of 41 cm. It contains three

fans, a custom VME crate and a laptop (see figure 2). The total weight of the box including the crate and the electronics cards is about 20 kg. The box is connected to the super-drawer via a single custom multi-connector cable and an optical fiber. The system is controlled by a software running on the embedded laptop which acts as the user interface.

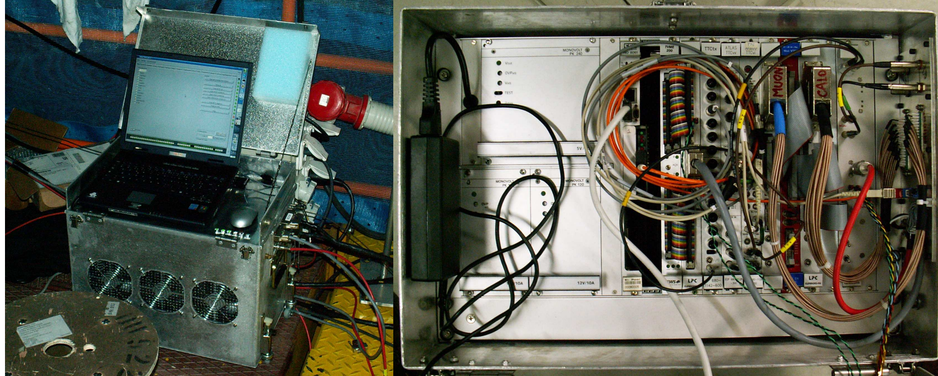

Figure 2: *Left: the MobiDICK system, with the embedded laptop visible and the cable going to the super-drawer. Right: view of the VME crate inside the aluminum box.*

2.1 The MobiDICK software

The MobiDICK software is divided in two parts: one is running in a VME processor in the VME crate, the other one on the laptop. These two parts communicate using the Internet Protocol and a Client/Server architecture.

The Server software is a C program running under LynxOS [5]. This program performs all the electronics tests under the requests of the Client and sends back the results of the tests to the Client. The electronics tests are performed with the help of electronic boards controlled via a VME bus.

The Client software is a C++ program running under Linux, using the ROOT [6] libraries. This program is the interface between the operator and the system. It sends requests to the Server to perform the electronics tests and gets results from it. The Client can also control a cooling circuit test box, through the parallel port of the laptop [3]. The results of the tests are then analyzed by the Client program to help the operator understand the problems.

In order to communicate with a given super-drawer, some parameters must be known, such as the TTCrx addresses or the ADC-I serial number. All the relevant super-drawer parameters are held in a local data base on the laptop. Moreover, using the wireless connection of the laptop to the Internet, the Client software is able to send SQL requests to the central super-drawer data base (in the IN2P3 computing center in Lyon), in order to get the most up to date parameters.

2.2 The MobiDICK hardware

The VME crate contains five sets of VME cards:

- the **Server processor**,
- the **CANbus interface**,
- the **TTC system**,
- the **Trigger ADC**,
- and the **HV power supply and LED driver**.

2.2.1 The Server processor

The Server is hosted on a RIO2 [7] VME processor. This card is the master of the VME bus and controls all the other VME cards. Since the Server program is running on it, it is the central part of the system.

On the PCI bus of the RIO2 processor is plugged a *Simple S-LINK to PMC interface* (or SSP [8]). Then, on this SSP card is plugged an *Optical Dual G-LINK S-LINK Interface* (or ODIN [9]). Then, the ODIN card is connected to the super-drawer using an optical fiber. The purpose of the ODIN card is to receive the data sent out by the super-drawer readout electronics. The data words are then stored in a FIFO on the SSP card until the Server program reads them out.

It is planned to replace the RIO2 processor by the VME processor which has been chosen as the Atlas ROD Crate Controller (VP110), in order to have full support of the card during the Atlas lifetime.

2.2.2 The CANbus interface

The CANbus interface is made of two modules. The first module is a TVME200 VME card holding two TIP816 [10] modules. Each of these modules is an independent CANbus interface. These two modules are then connected to an LPC-made card called PP, which is mainly used to provide the +12 V power supply of the VME backplane to the super-drawer CANbus interfaces and to dispatch the signals from the two TIP816 modules to a single non standard cable going to the super-drawer.

2.2.3 The TTC system

The TTC system is made of two modules. The first module is a TTCvi [11] VME card, which generates the commands to the super-drawer readout electronics — configuration as well as trigger —, on request of the Server. This TTCvi card is then connected to the TTCex [12] card, which converts these command electrical signals into optical signals, which are sent to the super-drawer readout electronics using an optical fiber.

2.2.4 The Trigger ADC

The Trigger ADC is made of three modules. The first module is a CAEN V792 [13] VME ADC, which digitizes the signals coming out of the super-drawer adders. Because these signals are differential, they are first processed by two LPC-made cards called DIFF2ADC, one for the muon trigger cable, one for the hadron trigger cable.

2.2.5 The HV power supply and LED driver

The HV power supply and LED driver is made of two modules. The first module is an LPC-made card called HVLED which provides a -830 V high voltage input to the super-drawer, converted from the +12 V power supply of the VME backplane by a DC/DC converter. On the same LPC-made card is implemented a LED driver which delivers a voltage (20 V) able to light two LED's in continuous or pulsed mode (with a width of 20 ns).

This card is controlled by the DIFF2ADC card, which has basic I/O capabilities, accessible through the VME bus.

3 Tests performed by MobiDICK

The tests performed by the MobiDICK system on the super-drawers are divided into eleven sets, in the following order: *CommMB, Adder, DigShape, DigNoise, Integ, CommHV, DigNoiseHV, Opto, NominalHV, IntegHV, DigShapeLED*.

For each super-drawer, the results of all tests have been saved to disk and, therefore, can be re-analyzed offline. In the following sections, these eleven sets of tests are described and, for some of them, a global analysis using all tested super-drawers is performed. The aim of such a global analysis is to study the spread of some characteristics over all super-drawers, in order to refine the bounds on these characteristics. For most of the tests, a simple distribution of one measurement over all super-drawers is enough, but for some tests a more complex analysis is needed.

3.1 Test *CommMB*

This is the first and most basic test of the super-drawer readout side performed by MobiDICK. The purpose of this test is to check the communication with the ADC-I card, the 3in1 cards and the motherboard TTCrx ("mezzanine card"):

1. the communication with the ADC-I card is established, through CANbus, using the IDALLOC DEFID command. In case of success, the serial number of this card is read back;
2. the parameters of this super-drawer are extracted from the super-drawer data base using its ADC-I serial number, which is unique among all super-drawers;
3. the firmware version of the ADC-I is verified;

4. the communication with every single 3in1 card through the ADC-I card is verified. All control bits of these cards are flipped and the status register is read back to check the commands were successful. All operations are done with the CANbus;
5. the communication with every single 3in1 card through the motherboard TTCrx is verified. All control bits of these cards are flipped, sending commands through the TTC system. The status register is read back by CANbus to check the commands were successful. In this test, a null value is used instead of the motherboard TTCrx address (broadcast mode);
6. the motherboard TTCrx address is verified: the first working 3in1 card is selected and checked three times with the previous sub-test, using the expected motherboard TTCrx address, the expected address minus one and the expected address plus one. In the last two tests, the communication with the 3in1 card should fail.

3.2 Test *Adder*

The purpose of this test is to check the analog summing cards (adders) functionalities, using the charge injection circuit of the 3in1 cards (CIS).

3.2.1 Description of the test

In order to check that the adders are really performing an analog sum of the outputs of up to six 3in1 cards, a known charge is injected on these cards one by one, verifying at each step that the increase in the adder output is consistent with what is expected. Therefore, this test is a loop on all channels:

1. all the 3in1 cards are configured to disable the charge injection input. Then, the signals coming out of the trigger cables are digitized using the "Trigger ADC" set of cards in MobiDICK: these values are the "pedestals" (one pedestal value for each adder card);
2. the charge injection input is then enabled on one 3in1 card (with a charge of 7 pC);
3. the trigger signals are digitized and the differences between these signals and the pedestals are computed and compared to what is expected: there should be no increase for the adders which are not connected to this 3in1 card and there should be an increase of a known value for the adder to which this 3in1 card is connected;

   These new digitized signals become the new pedestals.
4. the charge injection input is then enabled on one more 3in1 card and the test goes back to the previous step. This loop is performed until charge injection is enabled on all 3in1 cards.

All commands are sent through the TTC system with a null value instead of the motherboard TTCrx address (broadcast mode).

3.2.2 Global analysis

As mentioned above, the adder signal is an analog sum of up to six 3in1 cards (corresponding to six PMTs). The adder signal will give a fast information about the energy deposited in a η-tower in TileCal. Two outputs are available :

1. trigger for hadrons : sum of cells in all TileCal layers,
2. trigger for muons : cell of the last TileCal layer only.

For every channel of every drawer an adder signal has been measured by MobiDICK both for the muon and the hadron triggers. The main idea of the following test is to estimate the total spread of the adder signal. This will request to identify and separate the spread introduced by MobiDICK from the spread due to the drawers themselves. As a first approach the global distribution of the adders response is shown on figure 3. Long-barrels and extended-barrels have been treated separately. In principle the same distribution is expected for long-barrels and extended-barrels while a difference in the RMS can be seen on figure 3 both for hadron and muon trigger signals. On figure 4 the adders

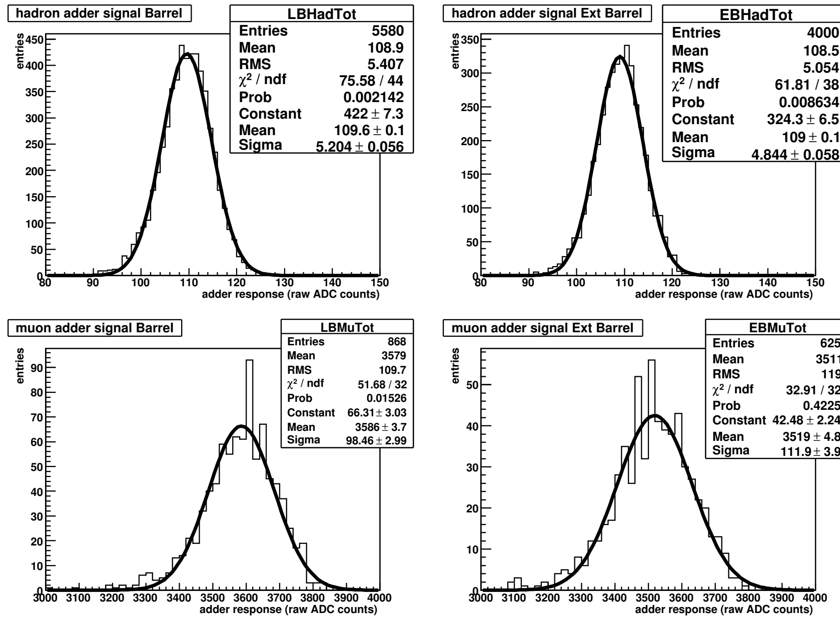

Figure 3: *Adder response distribution for all drawers and all channels.*
Top left : LB, hadron trigger;
top right : EB, hadron trigger;
bottom left : LB muon trigger;
bottom right : EB, muon trigger.

response is shown for the hadron trigger as a function of the channel number. The channels have been grouped by adder (separated by dashed lines). For

each channel the mean value and the RMS of the adder response have been computed merging the results obtained for all drawers. An example of adder signal distribution for one channel is given on figure 5 (left). The mean value and the RMS are obtained fitting the distribution with a gaussian function. The mean adders response computed over all drawers is expected to be independent of the channel number. Indeed only statistical fluctuations due to incoherent noise (both in drawers and in MobiDICK) should be seen when going from a channel to the other. This is the case for adders number 1, 2, 3, 4, 9 in LB and 1, 2, 3, 4, 5 in EB. On the other hand a systematic dependence can be seen between the mean adder response and the channel number for adders 5, 6, 7, 8 in LB and 6, 8 for EB (see figure 4). This systematic effect could be induced by the MobiDICK system itself. Each adder is indeed connected to a given electronic chain in MobiDICK (differential amplifier + ADC). Any difference in the behavior of a given channel of this chain with respect to the other inside MobiDICK, would produce a dependence of the response with respect to the channel number.

This hypothesis has been checked on figure 4 where the adders have been ordered with respect to the channel number in MobiDICK. Clearly there is a systematic non-linear effect on MobiDICK channel 5, which can be seen both in LB and EB test results (MobiDICK ADC number 5 is connected to adder 5 for LB and adder 6 for EB). The same effect can be observed for MobiDICK channels 5, 6 and 8[1]. One can conclude about this effect that there are hints indicating that the non-linearity comes from MobiDICK electronics and not from drawers. More investigations would be needed before drawing stronger conclusions. In this note, the choice has been made to correct for this effect assuming that it comes from MobiDICK itself.

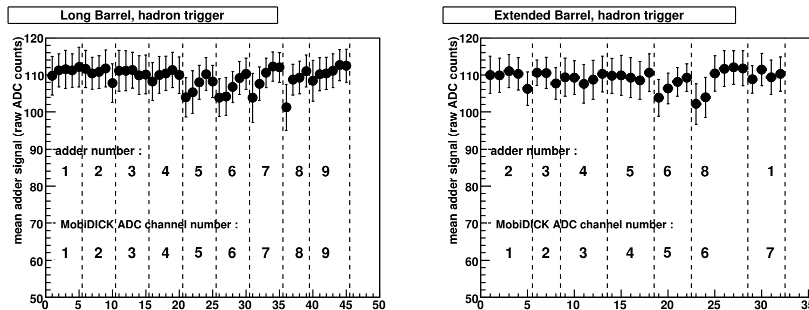

Figure 4: *Adders response (raw ADC counts) for hadron trigger in Long Barrel (left) and Extended Barrel (right) as a function of the channel number (ordered by adder).*

[1]for MobiDICK ADC number 7 (connected to adder 7 in LB and adder 1 in EB) the systematic effect is only visible for LB.

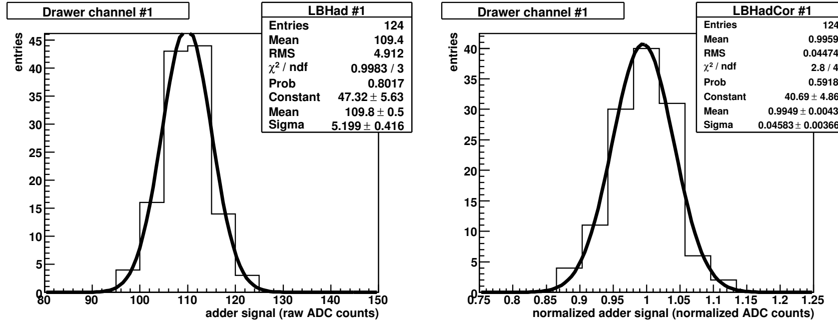

Figure 5: *Left : example of adder response distribution over all drawers for 1 channel. Right : the same distribution after normalization.*

The channel-to-channel variation in the mean adder signal introduces a spread on the global adder response. This spread is non-gaussian and is different for LB and EB. This can explain why the RMS differs between LB and EB on figure 3. Since we are interested only in the spread due to the noise in drawers the channel-to-channel variation of the adder signal has to be removed. A simple way is to normalize the adder response $R_{channel\ i}$ for each channel :

$$R_{channel\ i}/\langle R_{channel\ i}\rangle \qquad (1)$$

where $\langle R_{channel\ i}\rangle$ is the mean response (obtained after a Gaussian fit) in channel i computed over all the drawers. Figure 5 shows a typical adder response distribution in one channel before (left), and after normalization (right). The normalization is applied individually in each channel. Figure 6 shows the variation of the normalized adder response as a function of the channel number. As expected the normalized response is centered around 1 for all channels. All dependences between the adder response and the channel number have been removed. It is now possible to determine the global spread of the adders response (for all drawers and all channels). The global distributions of the adders response after the normalization are shown in figure 7. It has to be noticed that the spread is smaller after normalization since the systematic dispersion which is suspected to come from a non-linearity in MobiDICK acquisition chain has been corrected (see table 1). In addition RMS for LB and EB are now compatible. From now on LB and EB results will be merged together (see figure 8).

The noise introduced by the "Trigger ADC" set of cards in MobiDICK is also contributing to the measured spread on the adders response. This additional spread can be estimated by performing a signal acquisition with MobiDICK when no drawer is connected. MobiDICK response consists then only in pedestals and the spread is due to incoherent noise introduced by MobiDICK electronics. Figure 9 shows MobiDICK response when no drawer is connected. It has been done respectively for the LB and the EB configurations. As expected

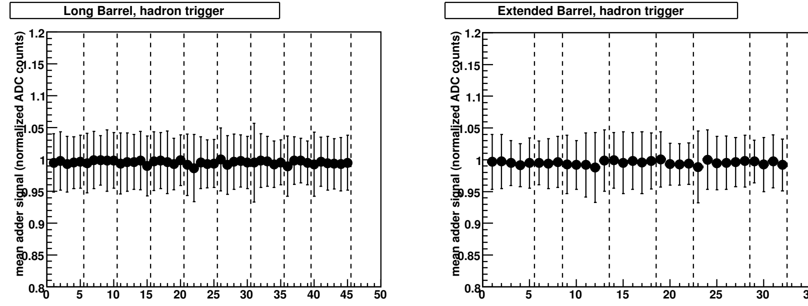

Figure 6: *Normalized adders response (normalized ADC counts) for hadron trigger in Long Barrel (left) and Extended Barrel (right) as a function of the channel number (ordered by adder).*

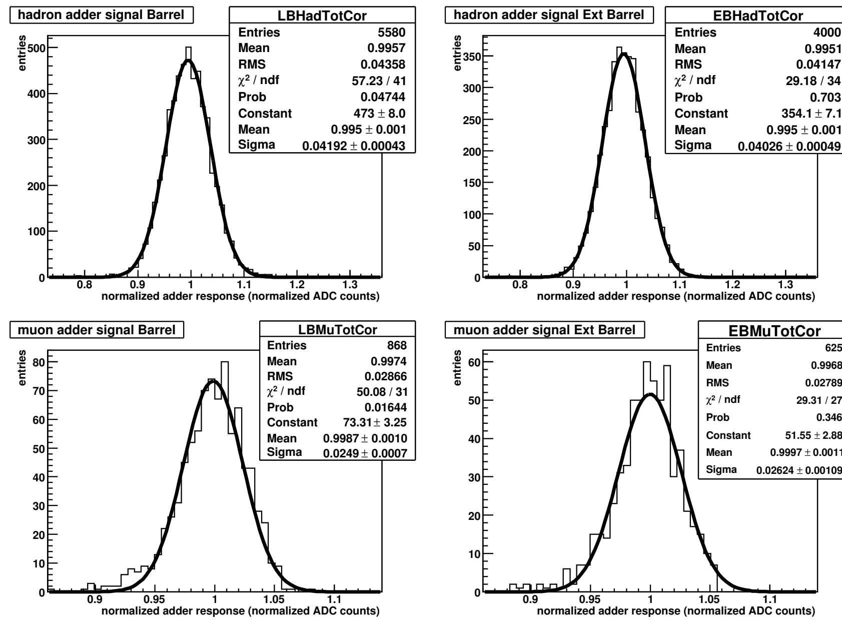

Figure 7: *Normalized adder response distribution for all drawers and all channels.*
Top left : LB, hadron trigger;
top right : EB, hadron trigger;
bottom left : LB muon trigger;
bottom right : EB, muon trigger.

	$(\sigma/mean)$	$(\sigma/mean)$ after normalization
LB, hadron trigger	(4.77±0.05)%	(4.17±0.04)%
EB, hadron trigger	(4.53±0.05)%	(4.06±0.05)%
LB, muon trigger	(2.74±0.08)%	(2.56±0.07)%
EB, muon trigger	(3.18±0.08)%	(2.46±0.08)%

Table 1: *Spread of the adders response.*

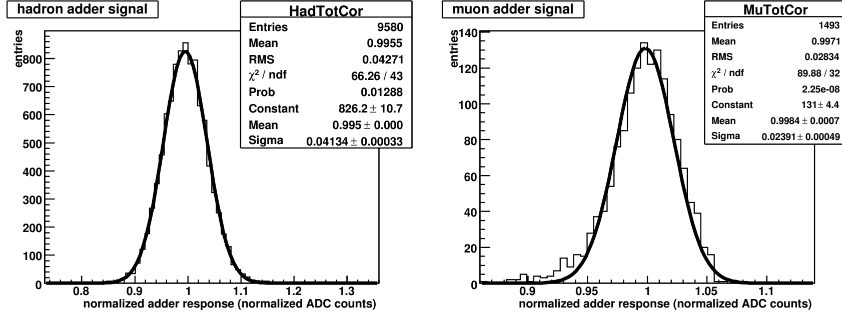

Figure 8: *Left : normalized response of the adder cards for the hadron trigger. Right : normalized response of the adder cards for the muon trigger.*

there are no differences in the MobiDICK noise between LB and EB configurations since within MobiDICK the same kind of electronic chains (differential amplifier + ADC) are used for both configurations. In order to evaluate the influence of MobiDICK noise on the spread of the adder signal, the measured pedestal $Ped_{channel\ i}$ in each channel i has to be normalized the same way as equation 1 :

$$Ped_{channel\ i}/\langle R_{channel\ i}\rangle$$

where $\langle R_{channel\ i}\rangle$ is the mean adder response in channel i. The second column in table 2 gives the normalized noise $\sigma_{noise}/mean$ introduced by MobiDICK electronics (see figure 10). The contribution of this noise is negligible compared with the adder signal spread for the muon trigger signal since this signal is amplified with respect to the hadron trigger signal (amplification is done inside the drawers).

Table 2 gives respectively the measured spread of the adder signal, the influence of MobiDICK noise and the corrected adder signal spread after MobiDICK contribution has been subtracted. Results are presented both for hadron and muon triggers. LB and EB results have been merged since no systematic differences have been seen between them.

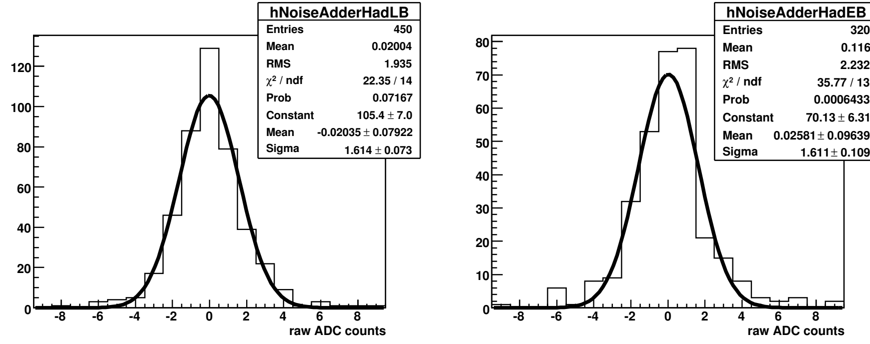

Figure 9: *Noise introduced by MobiDICK system. Left : LB configuration; Right : EB configuration.*

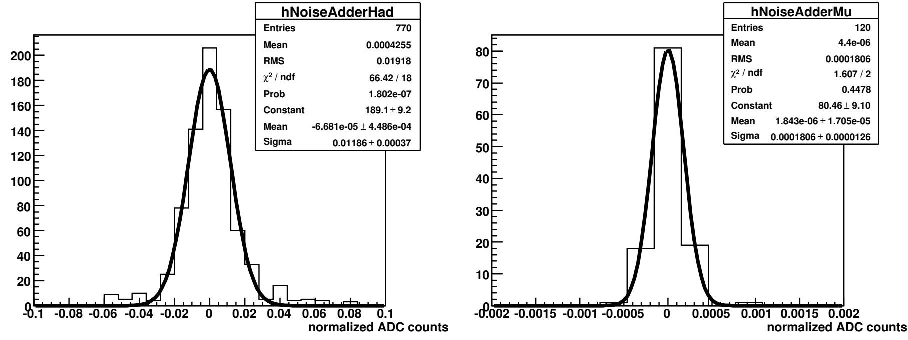

Figure 10: *Normalized noise introduced by MobiDICK system. Left : hadron trigger; right : muon trigger.*

	$(\sigma/mean)$ after normalization	MobiDICK noise after normalization	$(\sigma/mean)$ adder only
Hadron trigger	$(4.10\pm0.03)\%$	$(1.18\pm0.04)\%$	$(3.93\pm0.05)\%$
Muon trigger	$(2.50\pm0.05)\%$	$(0.018\pm0.001)\%$	$(2.50\pm0.05)\%$

Table 2: *Spread of the adders response.*

3.3 Test *DigShape*

The purpose of this test is to check the digitizers functionalities and the data readout, using the charge injection circuit (CIS).

3.3.1 Description of the test

The motherboard and all digitizers are first configured using their TTCrx addresses. The 3in1 cards are then configured to enable the charge injection input. Finally, the data are read out and analyzed, including a fit of the digitized pulse shape (see figure 11). Two steps are performed:

1. the injected charge is a small one (10 pC using a 5.2 pF capacitor), in order to test the high gain circuits. This charge is injected on all 3in1 cards at the same time, allowing to detect faulty digitizers very quickly. Then, this test is done a second time with a big charge (800 pC using a 100 pF capacitor) in order to test the low gain circuits;
2. the injected charge is a big one (800 pC), in order to test the low gain circuits. This charge is injected on a single 3in1 card, and no charge is injected on the others, to check the connectivity with the digitizers, in order to find 3in1 cards which would have been connected to a wrong digitizer channel.

All commands are sent through the TTC system.

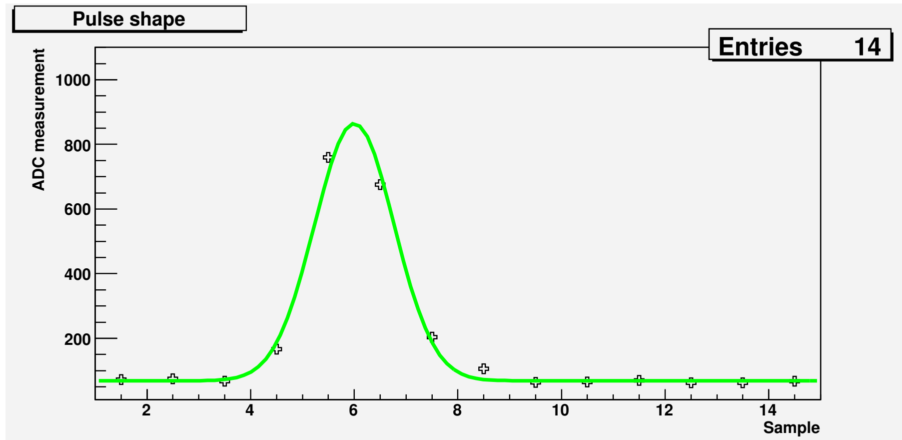

Figure 11: *Example of a digitized pulse shape generated by the CIS.*

3.3.2 Global analysis

We would like now to check the stability of the fit parameters of the pulse digitized shape, over all the available channels. During the test and validation procedure the digitized pulse shape $s(t)$ has been fitted by a gaussian function

$\mathcal{G}$ with a constant offset p called pedestal, and a scale factor h corresponding to the pulse height :

$$s(t) = p + h \times \mathcal{G}(\mu, \sigma) \tag{2}$$

The free parameters are p, h, the time when the maximum is reach μ and the width of the gaussian σ. An example of such a gaussian fit is represented on figure 11. This fit is easy to implement and gives sufficiently good results for the test and certification phase.

For the analysis of the global *DigShape* test results, a better fit procedure has been used. Instead of fitting the pulse shape with equation 2, it has been fitted by the expression :

$$s(t) = p + h \times f(\alpha t - \tau) \tag{3}$$

In equation 3, p is still a constant offset, $f(t)$ is a normalized pulse shape which corresponds to the measured response of the 3in1 card for a given injected charge[2]. This function is represented on figure 12. In equation 3, α is a fixed convertion factor between ns and sample number (one sample corresponds to 25 ns). The other free parameters of the fitting function 3 are the pulse height h and the phase τ corresponding to the time where the pulse is the highest. Figure 13 shows the digitized signal corresponding to a given channel. On the left, a gaussian fit has been applied. On the right, the fit has been performed using equation 3. A better agreement can be seen in the case of the fit by equation 3.

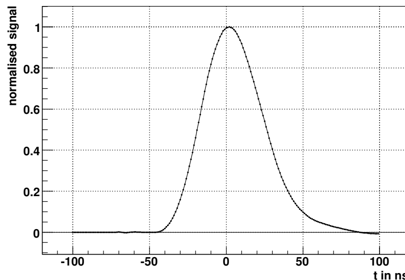

Figure 12: *Normalized pulse shape $f(t)$ measured after the 3in1 card for a given injected charge.*

The new fit function (equation 3) has been now implemented in MobiDICK, instead of the gaussian fit.

Figure 14 shows the distribution of the parameters p (pedestal) and h (pulse height) obtained from the fit with function 3. These distributions combine the results for all the channels of all the tested super-drawers.

[2]Here, the injected charge corresponds to the 5.2 pF capacitor. Files containing the normalized pulse shapes can be found in *TileConditions* athena package.

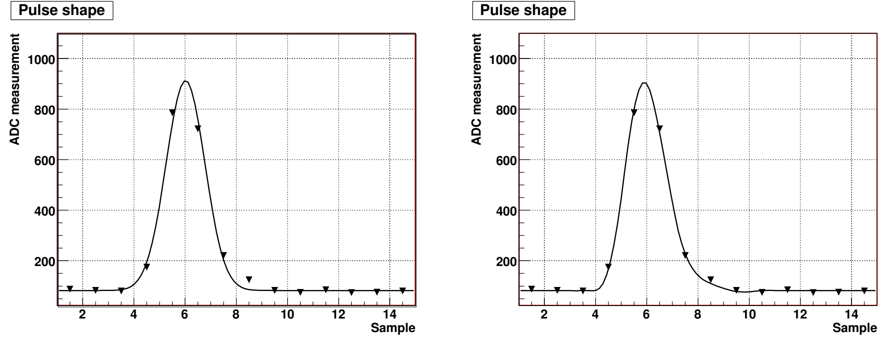

Figure 13: *Digitized signal from a given channel (high gain signal) on the left : fit with a gaussian function, on the right : fit using the normalized pulse shape.*

The distributions of the pulse shape parameters can be well described by a gaussian function with a mean μ and a RMS σ. μ and σ give a quantification of the homogeneity for the results of *DigShape*. These parameters have been reported in table 3.

	high gain		low gain	
	pedestal	pulse height	pedestal	pulse height
μ (ADC)	76.2 ± 0.1	831.1 ± 0.2	74.4 ± 0.1	1092.0 ± 0.2
σ (ADC)	8.54 ± 0.06	14.4 ± 0.1	8.57 ± 0.06	22.3 ± 0.2
σ/μ (%)	11.2 ± 0.1	1.73 ± 0.01	11.5 ± 0.1	2.04 ± 0.02

Table 3: *Mean value μ and RMS σ of the pedestal and pulse height distributions.*

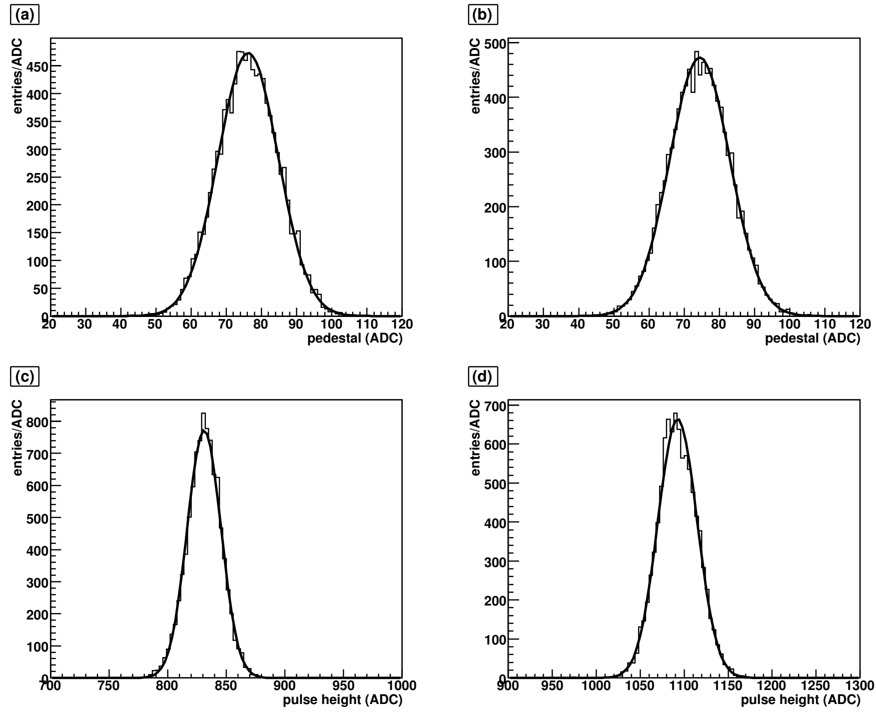

Figure 14: *Distributions of the fit parameters p and h (from fit function 3), for each channel of all the tested super-drawers :*
(a) : distribution of the pedestal value, high gain
(b) : distribution of the pedestal value, low gain
(c) : distribution of the pulse height value, high gain
(d) : distribution of the pulse height value, low gain

3.4 Tests *DigNoise* and *DigNoiseHV*

The purpose of these tests is to measure the digitizers noise and to check the data integrity.

3.4.1 Description of the test

In order to have a reasonable statistics, one thousand events are readout at maximum trigger rate, without charge injection, therefore containing only pedestal information. The digitizers are put in calibration mode in order to read both high gain and low gain data:

1. the BCID's of all TileDMU's are checked;
2. all CRC's are checked;
3. the pedestal average and RMS (digitizer noise) for each channel are computed and checked.

This test is performed twice (see figure 15):

1. with the high voltage distribution electronics off, and a digitizer configuration of 0xAB[3] for the event and bunch counter (*DigNoise*);
2. with the high voltage distribution electronics on (but without high voltage input), and a digitizer configuration of 0xA8[4] for the event and bunch counter (*DigNoiseHV*).

3.4.2 Global analysis

For each channel in each super-drawer, the noise level has been measured during the *DigNoise* test. It has been determined both for high gain and low gain configurations. As an example, figure 16 shows the distribution of the digitizer noise (high gain mode) in channel #2, for all the super-drawers composing the long barrel. From this distribution (which is gaussian) it is possible to extract the mean noise in channel #2, computed over all the available super-drawers. Repeating the same exercise for all the 48 channels, one can estimate the mean digitizer noise profile as a function of the channel position.

Figure 17 shows the profile of the digitizer noise (average over all super-drawers) as a function of the channel number. The top plots give respectively the long barrel and extended barrel results for high gain, and the bottom plots show the same for low gain[5]. The white symbols on figure 17 show the digitizer noise when only the read-out electronics is switched on. First it can be noticed that the noise level is twice as small in low gain mode than in high gain mode. This is due to the analog amplification that is performed by the 3in1 card between the high gain and the low gain response (factor 64 between low and

[3] In this configuration the TTCrx of the digitizers have both bunch counter and event counter enabled.

[4] Both bunch counter and event counter of the TTCrx are disabled.

[5] The error bars which have been represented correspond to the RMS of the noise distribution by channel.

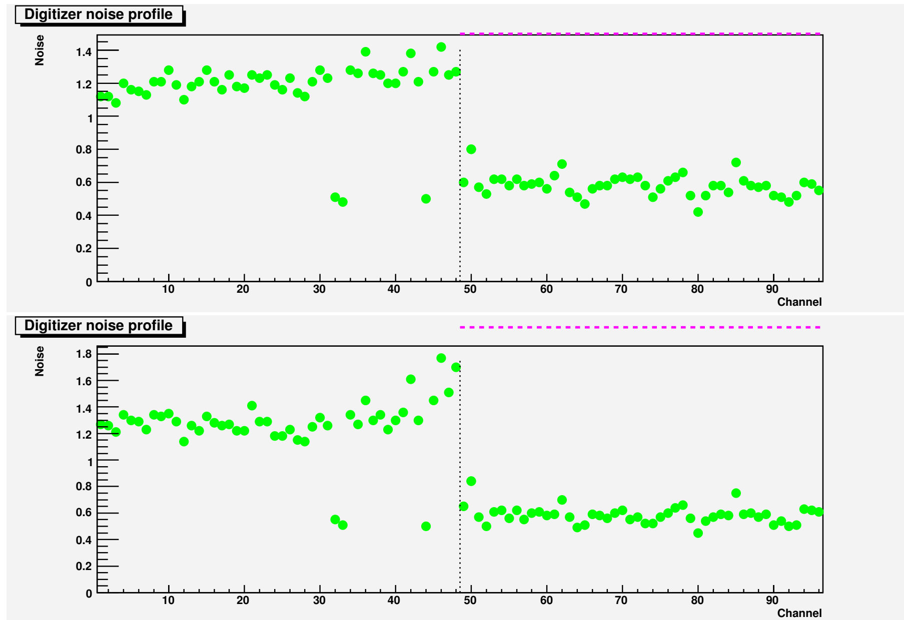

Figure 15: *Example of noise profile of a super-drawer. Left: high gain, right: low gain. Top: DigNoise, bottom: DigNoiseHV.*

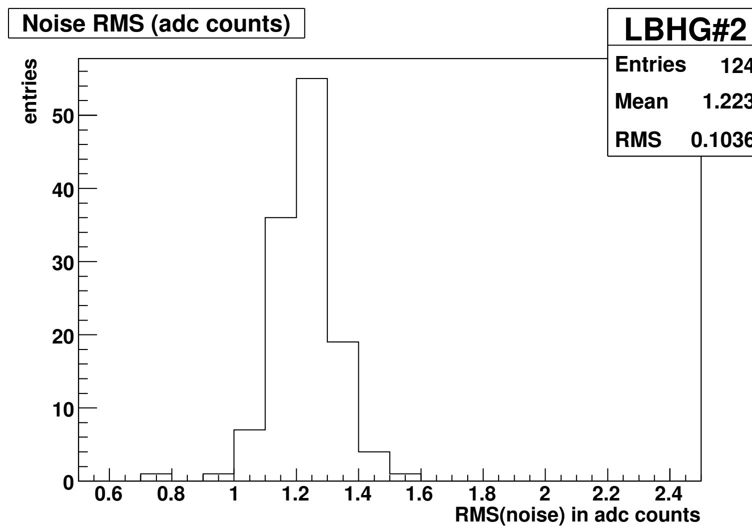

Figure 16: *Distribution of the digitizer noise in a given channel, for all the super-drawers which have been tested (Long barrel).*

high gain response). One can see also that the noise is almost independent of the channel number except at the edges of the super-drawers where the noise increases systematically (this is clearly visible in the long barrel, for the high gain results).

The *DigNoise* test has been performed a second time, with the high voltage distribution electronics on (but without high voltage on the PMT's). The same profiles showing the noise evolution with respect to the channel number can be repeated, in order to check the contribution of the HV distribution electronics to the digitizer noise. Black markers on figure 17 show the digitizer noise profile as a function of the channel number, for long barrel and extended barrel, in high gain and low gain modes (HV distribution electronics on). Comparing black and white symbols, the noise is globally 10% higher in high gain mode, if the HV electronics is switched on. Moreover, there is a large increase of the noise level for channels 40 to 48. This corresponds to the patch-panel side. A smaller increase of the noise can be seen also between channels 10 to 1. This effect is clearly visible for long barrel and extended barrel modules, in high gain mode.

For low gain results, the fact that the HV distribution electronics is switched on has a negligible influence on the digitizer noise. On can see on figure 17 (lower plots) that the noise level does not increase when the HV electronics is switched on.

When the HV distribution electronics is supplied, the total digitizer noise $\sigma_{HV+Readout}$ is a combination of the readout and the HV electronics noise. Knowing the noise contribution $\sigma_{Readout}$ which is due only to the readout electronics (see figure 17), it is possible to extract the noise increase induced by the HV electronics. Assuming that the noise contributions are independent, one gets :

$$\sigma_{HV} = \sqrt{\sigma^2_{HV+Readout} - \sigma^2_{Readout}} \tag{4}$$

Figure 18 shows the noise contribution of the HV electronics to the digitizer noise. For high gain mode (top), equation 4 has been used. For the low gain mode, since no systematic noise increase has been observed due to the HV electronics, only the direct difference ($\sigma_{HV+Readout} - \sigma_{Readout}$) has been plotted. Figure 18 (top) shows that in high gain mode, the noise increase for the channels that are close to the edge of the super-drawer, is mainly due to the HV electronics. In the internal drawer (channels 1 to 24) the noise level looks systematically higher than in the external drawer (except after channel 40). This can be due to noise killer cards (RC filters) that have been inserted between the HVbus cards and the HVdivider cards, for the external drawers. The noise killer cards have been designed in order to reduce the digitizer noise for the channel numbers above 40. The noise was much bigger than presently before these cards were added. For low gain (bottom plots in figure 18), one confirms that the fact the HV distribution electronics is switched on has no significant influence on the digitizer noise.

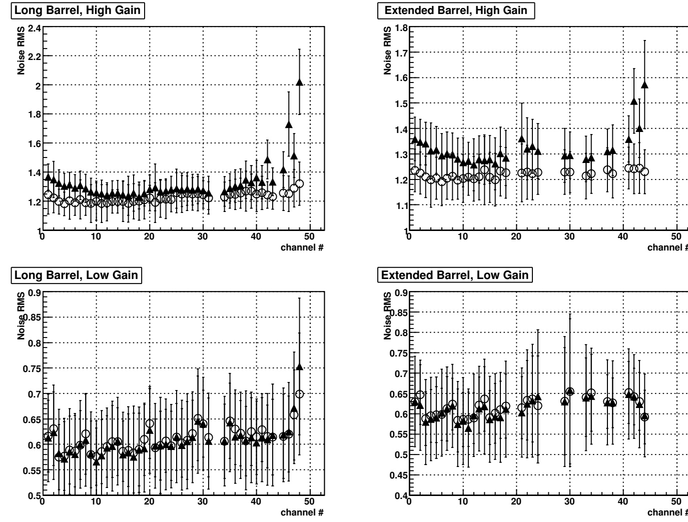

Figure 17: *Distribution of the mean digitizer noise as a function of the channel number.*
Open symbols : only the readout electronics is supplied;
black symbols : the HV distribution electronics is switched on.
The error bars correspond to the RMS of the noise distribution by channel.

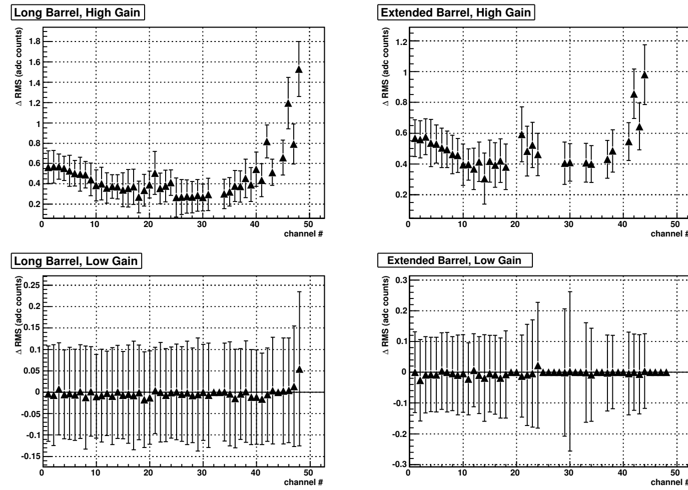

Figure 18: *Difference between the digitizer noise after and before the HV electronics is turned on. Top : high gain mode (quadratic difference); bottom : low gain mode (direct difference).*

3.5 Tests *Integ* and *IntegHV*

The purpose of these tests is to check the linearity and noise level of the ADC-I and of the charge integrator circuit of the 3in1 cards.

3.5.1 Description of the test

For each single 3in1 card and for each charge integrator circuit gain (therefore a total of 288 single tests):

1. the pedestal RMS is computed over one hundred measurements and verified;
2. the charge integrator circuit input is connected to the DAC, with an increasing setting. The charge integrator circuit output is digitized by the ADC-I. The resulting curve is fitted with a line and checked to be linear (see figure 19). The slope is verified.

This test is done twice:

1. with the high voltage distribution electronics off (*Integ*);
2. with the high voltage distribution electronics and the high voltage input on. At this stage, only the pedestal RMS is checked (*IntegHV*). The result of this test is unfortunately modified by any light leak which might occur in the module or the finger.

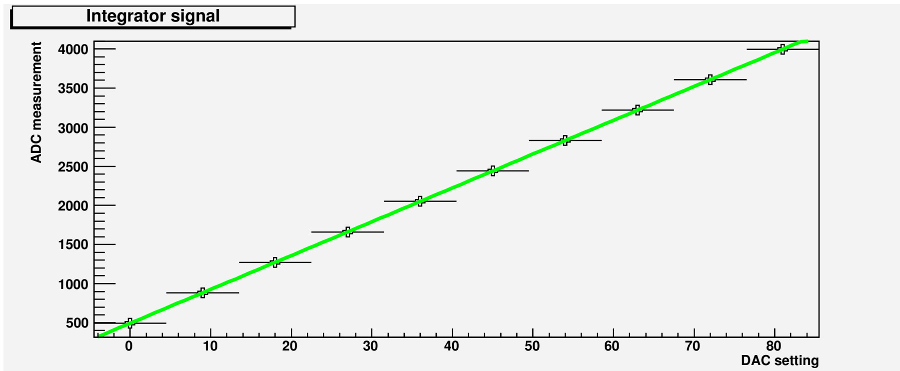

Figure 19: *Example of a charge integrator circuit response.*

3.5.2 Global analysis (*Integ* only)

It has been mentioned above that the test *Integ* checks the linearity between the digitized injected charge (DAC) and the digitized response (ADC) that is obtained after the ADC-Integrator (ADC-I) card. The following relation is expected between DAC and ADC :

$$ADC = slope \times DAC + pedestal \quad (5)$$

The purpose of the global test is to plot the distribution of the pedestal and the slope values, for all the readout channels and all the super-drawers. Each of the 6 different gains of the charge integrator circuits have been treated separately. As an example, figure 21 shows the distribution of the slope value for the 6 different gains. As expected, the slope increases with the gain. It can be seen also that the distributions are not gaussian. A tail can be systematically seen on the low signal side. This behavior is due to a slight drift in the ADC-I cards features. This can be shown for instance by plotting the evolution of the slope mean value (computed over each super-drawer) as a function of the ADC-I cards serial number[6] : see figure 20. On this plot, two different samples of *ADC-I* cards can be identified : for serial number smaller than 20 000 (region *I* on figure 20) the slope is systematically higher than for serial numbers higher than 20 000. In order to have a clear vision of the global spread on the pedestal and the slope values, the two samples of ADC-I cards have been considered separately[7]. Figures 22 and 23 show respectively the distributions of the slope values (for the 6 available gains) for *ADC-I* cards serial numbers lower and higher than 20 000.

For the two different samples of ADC-I cards, the expected gaussian spread of the slope value is now observed. The slope distributions have been fitted with a Gaussian function and the parameters (mean and RMS called σ) have been reported in table 4. About 1.8% difference can be seen between the two samples of ADC-I cards.

Figures 24 and 25 represent the distributions of the pedestal value (see equation 5) for the 6 gains, respectively for ADC-I cards serial numbers smaller and higher than 20 000. Again, the mean pedestal values are about 1-2% higher for the first sample of ADC-I cards (see table 5).

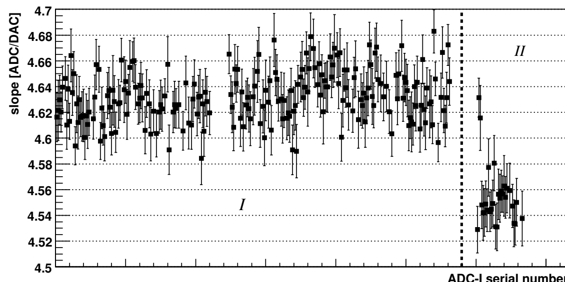

Figure 20: *Example of evolution of the slope value (for a given gain of the charge integrator circuits) as a function of the ADC-I cards serial number :*
Sample I *: serial number* $<$ *20 000; Sample* II *: serial number* $>$ *20 000*

[6]Each ADC-I card has a unique serial number.

[7]Two ADC-I with serial numbers $>$ 20 000 are considered in the sample of ADC-I with serial number $<$ 20 000, since they have the same characteristics.

gain	ADC-I serial number $< 20\ 000$ mean [ADC]	σ [ADC]	σ/mean [%]
1	4.631 ± 0.001	0.0270 ± 0.0002	0.583 ± 0.004
2	42.842 ± 0.002	0.276 ± 0.002	0.644 ± 0.005
3	47.450 ± 0.002	0.295 ± 0.002	0.622 ± 0.004
4	90.14 ± 0.01	0.595 ± 0.005	0.660 ± 0.006
5	124.96 ± 0.01	0.855 ± 0.007	0.684 ± 0.006
6	167.65 ± 0.01	1.158 ± 0.009	0.691 ± 0.005
gain	ADC-I serial number $> 20\ 000$ mean [ADC]	σ [ADC]	σ/mean [%]
1	4.549 ± 0.001	0.0229 ± 0.0007	0.50 ± 0.01
2	42.09 ± 0.01	0.246 ± 0.007	0.58 ± 0.01
3	46.62 ± 0.01	0.252 ± 0.007	0.54 ± 0.01
4	88.58 ± 0.02	0.53 ± 0.02	0.60 ± 0.02
5	122.75 ± 0.03	0.76 ± 0.02	0.62 ± 0.02
6	164.70 ± 0.03	1.03 ± 0.03	0.62 ± 0.02

Table 4: *Spread of the slope value.*

gain	ADC-I serial number $< 20\ 000$ mean [ADC]	σ [ADC]	σ/mean [%]
1	513.2 ± 0.2	19.0 ± 0.2	3.70 ± 0.04
2	502.5 ± 0.3	22.9 ± 0.2	4.56 ± 0.04
3	501.3 ± 0.3	23.7 ± 0.2	4.72 ± 0.04
4	489.4 ± 0.4	32.8 ± 0.3	6.70 ± 0.06
5	478.8 ± 0.5	41.4 ± 0.3	8.65 ± 0.06
6	466.8 ± 0.6	52.5 ± 0.4	11.25 ± 0.09
gain	ADC-I serial number $> 20\ 000$ mean [ADC]	σ [ADC]	σ/mean [%]
1	506.3 ± 0.8	19.8 ± 0.9	3.9 ± 0.2
2	499.4 ± 0.9	25.5 ± 0.6	5.1 ± 0.1
3	498 ± 1	26.8 ± 0.7	5.4 ± 0.1
4	486 ± 1	37.0 ± 0.9	7.6 ± 0.2
5	475 ± 2	46 ± 2	9.7 ± 0.4
6	462 ± 2	59 ± 2	12.8 ± 0.4

Table 5: *Spread of the pedestal value.*

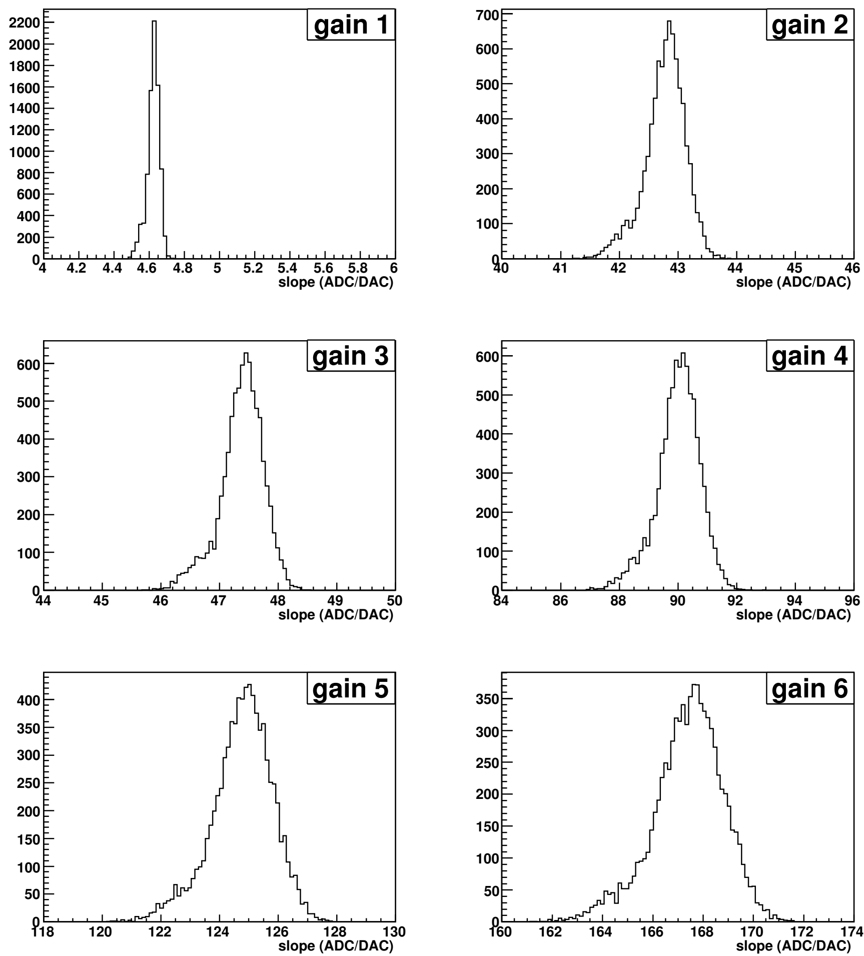

Figure 21: *Distribution of the slope value (see equation 5) for the 6 gains of the charge integrator circuits.*

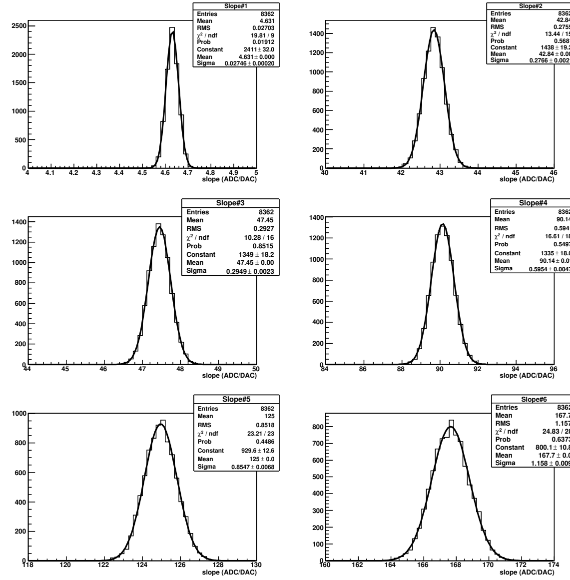

Figure 22: *Distribution of the slope value for the 6 gains of the charge integrator circuits, and for ADC-I serial numbers < 20 000.*

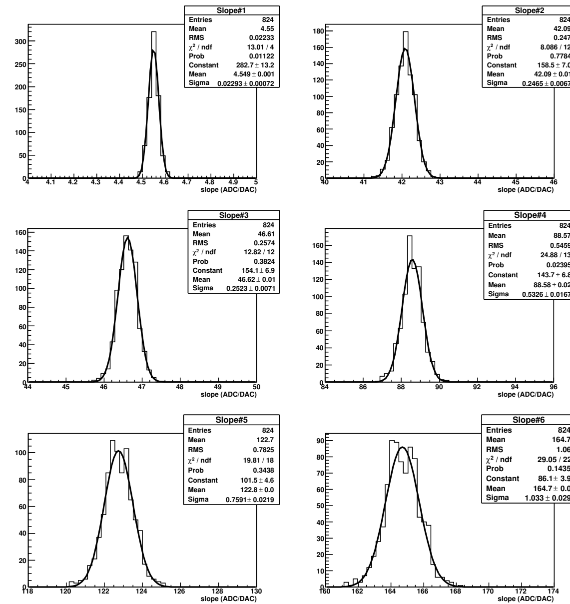

Figure 23: *Distribution of the slope value for the 6 gains of the charge integrator circuits, and for ADC-I serial numbers > 20 000.*

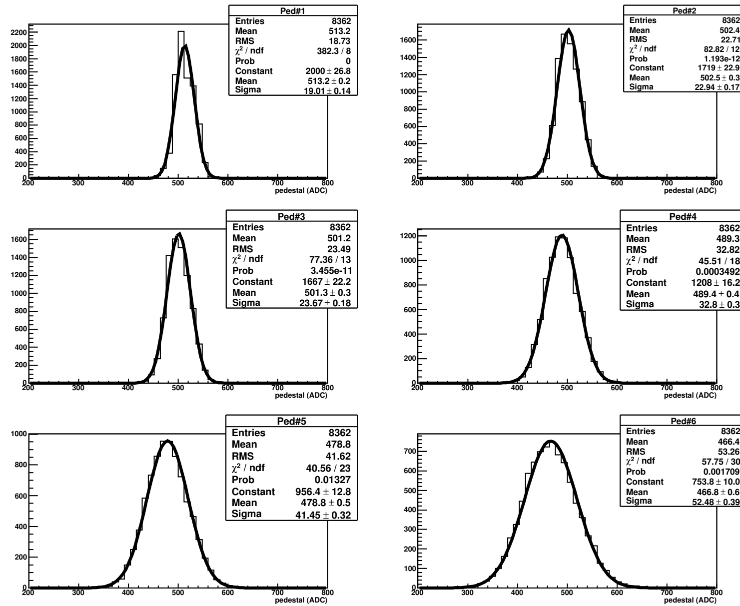

Figure 24: *Distribution of the pedestal value for the 6 gains of the charge integrator circuits, and for ADC-I serial numbers < 20 000.*

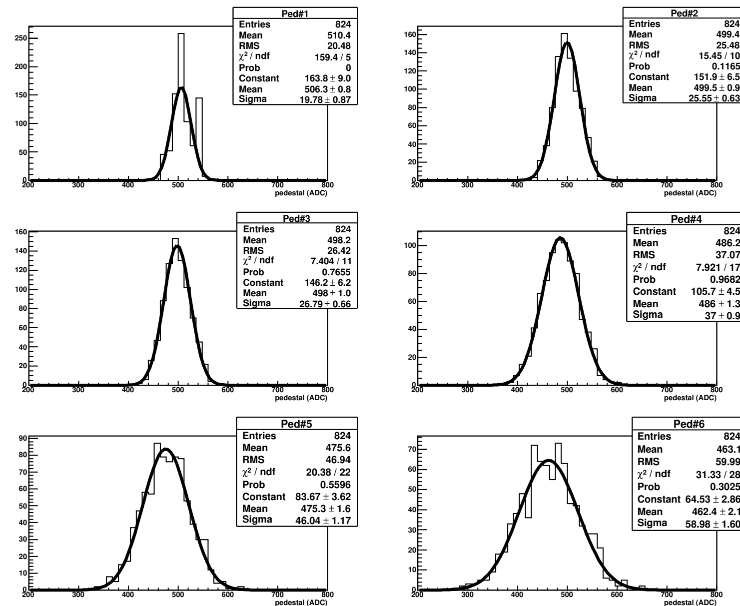

Figure 25: *Distribution of the pedestal value for the 6 gains of the charge integrator circuits, and for ADC-I serial numbers > 20 000.*

3.6 Test *CommHV*

The purpose of this test is to check the communication with the high voltage distribution electronics:

1. the communication with the HVmicro card is established, through CAN-bus. In case of success, the global status register of this card is read back and verified. Otherwise a loop over all possible node numbers is performed until communication is established;
2. the software version of the HVmicro card is verified;
3. the values of the low voltages and temperatures monitored by the HVmicro card are verified;
4. the serial numbers of the two HVopto cards and of the HVmicro card are compared to what is expected from the super-drawer data base.

3.7 Tests *Opto* and *NominalHV*

The purpose of these tests is to check the functionalities of the high voltage distribution electronics.

3.7.1 Description of the tests

For the test *Opto*:

1. the four HV switches (odd/even internal/external) are all switched off. Then, they are switched on one by one and verified;
2. the HV is set to 700 V on all the channels. Then, for each channel, the measured voltage is read out and compared to the expected one;
3. the HV is set to 600 V on all the channels. Again, for each channel, the measured voltage is compared to the expected one.

For the test *NominalHV*:

1. the nominal HV's are restored on all channels from the HVmicro EEPROM;
2. for each channel, the measured voltage is compared to the expected one, and the voltage setting (which comes from the EEPROM) is compared to the nominal HV expected on this channel, from the super-drawer data base.

3.7.2 Global analysis

The *Opto* test consists in requesting a given HV value and then measuring the voltage that is available on each PM. This test is performed in 2 steps : first a 700 V voltage is set, and then a 600 V voltage. Figure 26 shows the distributions of the measured HV on each channel and for all drawers (LB+EB). The distribution of the HV measured is fitted with a Gaussian function (between $\mathrm{HV}_{requested} \pm 1\ V$). The mean $HV_{measured}$ value and the width σ are obtained from this fit.

For the *NominalHV* test the reference HV values are taken from the HVmicro EEPROM and the difference between the reference and the measured HV value is measured for all channels and for all drawers. Figure 27 shows the difference between the requested HV and the measured one for all channels and for all drawers. As before, the distribution is fitted with a Gaussian function.

Table 6 gives the difference ΔHV between the requested HV and the measured one, together with the width σ of the distribution. There is a very good agreement between the requested voltage and the measured one in all cases. Nevertheless the measured HV distributions always show a tail in the low values side. It means that the measured HV is systematically a bit too low. This is a known effect introduced by the HV regulation loop (in HVopto cards), which needs at least one hour or more to be completely stable [14]. This condition is not achieved during the MobiDICK test procedure which lasts only a few minutes for safety reason (no water cooling of the super-drawer is available).

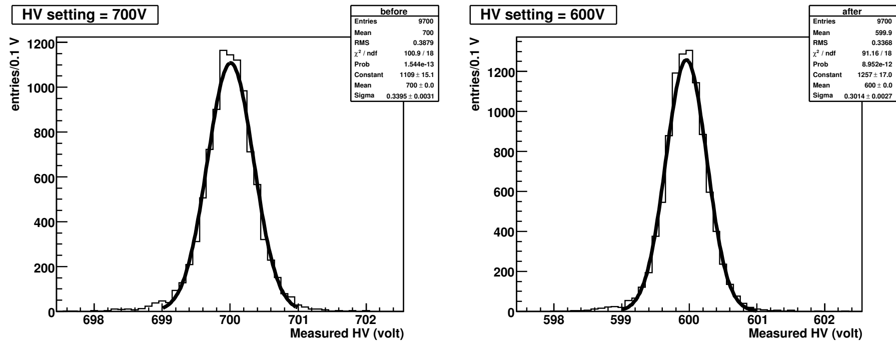

Figure 26: *Distribution of the HV value for all channels and for all drawers in the* Opto *test.*

$HV_{setting}$ (V)	ΔHV (V)	σ (V)	σ/HV (%)
700	0.007 ± 0.003	0.340 ± 0.003	0.0486 ± 0.0004
600	-0.042 ± 0.003	0.301 ± 0.003	0.0502 ± 0.0005
Nominal HV	-0.058 ± 0.003	0.323 ± 0.003	

Table 6: *Difference* $\Delta HV = HV_{setting} - HV_{measured}$*, and width* σ *of the distribution for the 3* HV *settings.*

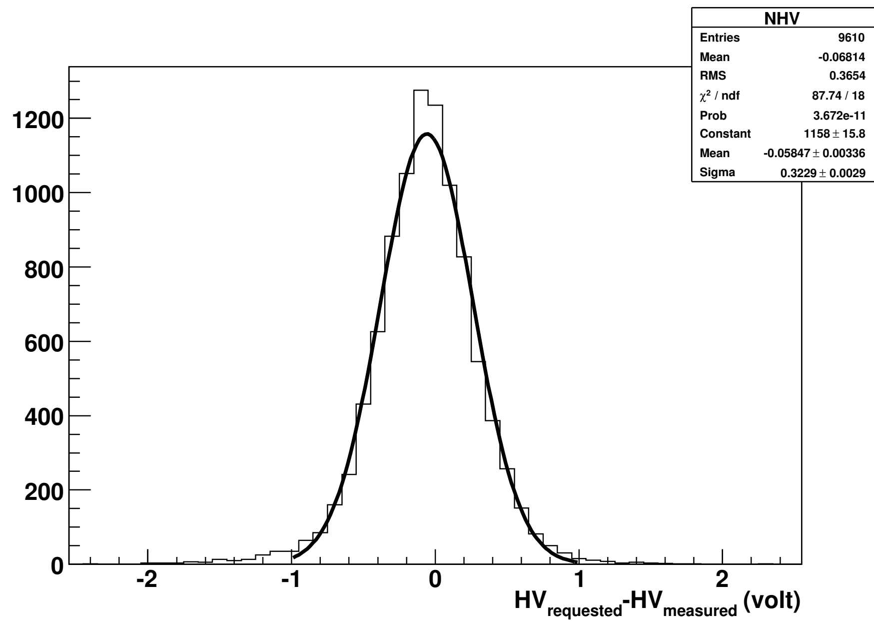

Figure 27: *Distribution of the difference between measured and requested HV value for all channels and for all drawers in* NominalHV *test.*

3.8 Test *DigShapeLED*

The purpose of this test is to check the response of the super-drawer to a light pulse similar to the one produced by particles in the tiles. The outputs of the MobiDICK LED driver are connected to two small boxes containing a blue LED in front of an optical fiber connected to the “laser” fiber of the TileCal module. The LED pulse is synchronized with the trigger signal sent to the super-drawer. The digitizers data are read out and analyzed, including a fit of the digitized pulse shape (see figure 28). No global analysis has been made for this test because of the large expected fluctuations on the pulse amplitude due to the fact that HV’s are not tuned to the nominal ones.

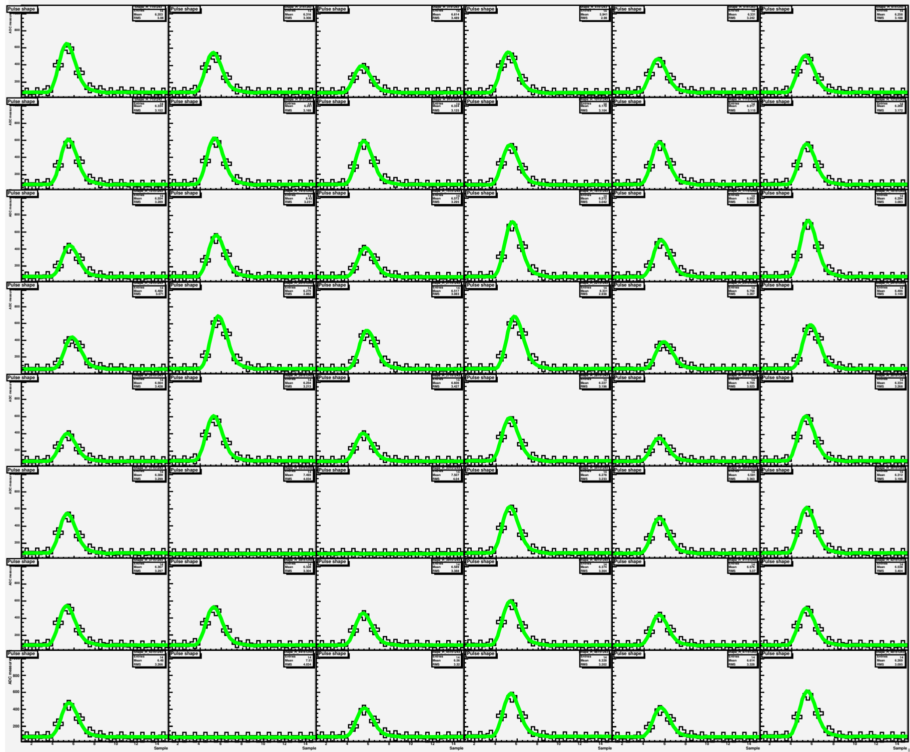

Figure 28: *Example of response of a super-drawer to a light pulse produced by a blue LED. Three channels are flat because no photomultipliers are connected to them. The variations in amplitude are likely due to untuned nominal HV’s, and time stabilization of PMTs (several hours in some cases).*

4 Conclusions

This document gave a description of the MobiDICK system and the way it performs the test of the front-end electronics of TileCal. During the insertion procedure and the test of all super-drawers in ATLAS pit, the test was divided in a sequence of eleven sets.

All the super-drawers composing TileCal have been tested. A large amount of results are then available. From these data, an analysis of the electronics response obtained during the tests has been done. This study gives a good estimate of the real dispersion of the TileCal front-end electronics characteristics. For all the tests allowing such an analysis, a significant information is the ratio between the spread (root mean squared) and the mean value of a given parameter, the mean and the spread being computed over all the super-drawers. This information has been quoted in table 7.

A few comments can be done on these results. First we can confirm that the global dispersion is low enough and acceptable with respect to the original requirements. It has been also clearly identified that two different samples of ADC-I cards have been used. The two samples give slightly different performances for the charge integrator circuit of the 3in1 cards.

Test		Tested parameter	
Adder		**Digitized adder cards response**	
	Hadron trigger :	(3.93 ± 0.05)%	
	Muon trigger :	(2.50 ± 0.05)%	
DigShape		**Pedestal**	**Pulse height**
	High gain :	(11.2 ± 0.1)%	(1.73 ± 0.01)%
	Low gain :	(11.5 ± 0.1)%	(2.04 ± 0.02)%
Integ		**Slope**	**Pedestal**
		ADC-I serial number < 20 000	
	gain 1 :	(0.583 ± 0.004)%	(3.70 ± 0.04)%
	gain 2 :	(0.644 ± 0.005)%	(4.56 ± 0.04)%
	gain 3 :	(0.622 ± 0.004)%	(4.72 ± 0.04)%
	gain 4 :	(0.660 ± 0.006)%	(6.70 ± 0.06)%
	gain 5 :	(0.684 ± 0.006)%	(8.65 ± 0.06)%
	gain 6 :	(0.691 ± 0.005)%	(11.25 ± 0.09)%
		ADC-I serial number > 20 000	
	gain 1 :	(0.50 ± 0.01)%	(3.9 ± 0.2)%
	gain 2 :	(0.58 ± 0.02)%	(5.1 ± 0.1)%
	gain 3 :	(0.54 ± 0.01)%	(5.4 ± 0.1)%
	gain 4 :	(0.60 ± 0.02)%	(7.6 ± 0.2)%
	gain 5 :	(0.62 ± 0.02)%	(9.7 ± 0.4)%
	gain 6 :	(0.63 ± 0.02)%	(12.8 ± 0.4)%
		Relative difference between the two ADC-I samples [a]	
	gain 1 :	(1.77 ± 0.03)%	(1.3 ± 0.2)%
	gain 2 :	(1.76 ± 0.02)%	(0.6 ± 0.2)%
	gain 3 :	(1.75 ± 0.02)%	(0.7 ± 0.2)%
	gain 4 :	(1.73 ± 0.02)%	(0.7 ± 0.2)%
	gain 5 :	(1.77 ± 0.03)%	(0.8 ± 0.4)%
	gain 6 :	(1.76 ± 0.02)%	(1.0 ± 0.4)%
Opto		$\boldsymbol{HV}_{Setting}$-$\boldsymbol{HV}_{Measured}$	
	700 V requested :	(0.0486 ± 0.0004)%	
	600 V requested :	(0.0502 ± 0.0005)%	

Table 7: *Relative dispersion (RMS over mean value) of the most relevant characteristics of the TileCal front-end electronics.*

[a] This is the relative difference between the mean values obtained with ADC-I serial number<20 000 and ADC-I serial number>20 000 respectively (see tables 4 and 5).

Acknowledgments

We would like to warmly thank all the people who contributed in the tests of the super-drawers with MobiDICK, in particular Georges Glonti, Franck Martin, Fabrice Podlyski, Claudio Santoni and François Vazeille.

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