Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors

Federico Faccio, *Member, IEEE,* and Giovanni Cervelli

***Abstract*—The study of the TID response of transistors and isolation test structures in a 130 nm commercial CMOS technology has demonstrated its increased radiation tolerance with respect to older technology nodes. While the thin gate oxide of the transistors is extremely tolerant to dose, charge trapping at the edge of the transistor still leads to leakage currents and, for the narrow channel transistors, to significant threshold voltage shift—an effect that we call Radiation Induced Narrow Channel Effect (RINCE).**

***Index Terms*—Deep submicron CMOS transistors, narrow channel effect, radiation effects, RINCE.**

I. Introduction

THE sharp decrease of Total Ionizing Dose (TID) effects in thin gate oxides (below about 10–12 nm) of MOS structures was initially shown by N. Saks and co-workers in publications dating back to 1984 and 1986 [1], [2]. The results presented were obtained on laboratory-grade oxides, but were verified on commercial-grade oxides around a decade later, when available commercial CMOS processes with lithographic dimensions as small as 250 nm were using gate oxides 5.2 nm thick [3].

Although the gate oxide becomes thinner, hence less sensitive to TID, the Shallow Trench Isolation (STI) oxide of modern CMOS technologies does not scale down correspondently. As a consequence, radiation-induced charge trapping in the STI oxide still leads to macroscopic effects such as source-drain or inter-diffusion leakage currents, ultimately limiting the radiation tolerance of conventional CMOS circuits. Nevertheless, it is possible with Hardness-By-Design (HBD) layout techniques to eliminate this limitation, and eventually push the tolerance of circuits up to the high level allowed by the gate oxide itself (well above 1 Mrd). In these techniques, the NMOS transistor is annular (Enclosed Layout Transistors, or ELT) to prevent radiation-induced leakage at the edge of the transistor, and the p+ guardrings effectively cut leakage paths between adjacent n+ junctions at different potential [4].

This explains why the use of commercial CMOS technologies for the design of radiation-tolerant Application Specific Integrated Circuits (ASICs) has grown considerably in the last decade. The largest scale application of this approach is found in the High Energy Physics (HEP) community, where tens of different mixed-signal ASICs equip the detector systems of the Large Hadron Collider (LHC) experiments under construction at CERN [5]. These ASICs, manufactured in a commercial 250 nm CMOS technology, represent a production volume of more than 2000 silicon wafers (200 mm). Other successful examples of HBD in both the 250 nm and 180 nm nodes can be found [6], [7] and HBD itself has become a recognized subject for dedicated sessions and courses at international conferences such as NSREC [8].

With the semiconductor industry racing toward ever smaller feature sizes in CMOS technologies, the 90 nm node is in use today for top-end digital products such as microprocessors and memories, and the 130 nm is widely available for ASIC design. These advanced processes require very complex sequences of manufacturing steps to achieve the integration of transistors with excellent electrical performance in close proximity to each other. Of particular interest for the TID tolerance of a technology, STI-related steps (trench etching, thermal and High Density Plasma oxidation) are tuned for optimal source-drain isolation and to reduce narrow channel effects. Because of the different challenges in different technology nodes, these processing details also vary—sometimes significantly—and this might ultimately result in noticeably different radiation-induced edge effects in transistors. It is therefore interesting to study the state-of-the-art technologies in this respect, to understand the radiation effects and their relevance, anticipate the radiation performance of commercial integrated circuits, and evaluate whether HBD techniques are necessary for applications in different radiation environments.

This paper concentrates on a commercial 130 nm CMOS technology in view of its use for ASIC design in applications requiring TID hardness up to the 100 Mrd level (HEP experiments).

II. Experimental Details

A. Test Structures

Measurements were performed on a set of custom-developed test structures in a commercially available 130 nm CMOS technology. Similar measurements were performed beforehand on samples provided by the same foundry, and also from a second source (in both cases they were Process Monitoring Devices, PMD). Although the PMD test structures did not allow for a thorough investigation, the results were qualitatively similar to those presented hereafter.

The custom-developed test structure, named "TID1", was designed as four columns of 16 pads each, giving access to all terminals of NMOS and PMOS transistors of different types: "core transistors" with 2.2 nm thick gate oxide, or "I/O transistors" with thicker oxide (about 5 nm), available for I/O or analog applications using a V_{dd} of 2.5 V. Different transistor

Manuscript received July 8, 2005; revised August 26, 2005.

The authors are with the Physics Department, Microelectronics Group, CERN, 1211 Geneva 23, Switzerland (e-mail: federico.faccio@cern.ch).

Digital Object Identifier 10.1109/TNS.2005.860698

sizes were chosen: a W array with $L = 0.12\ \mu m$ (W from minimum size, $0.16\ \mu m$, to $2\ \mu m$), two transistors with $W = 10\ \mu m$ ($L = 1$ and $10\ \mu m$). All these transistors were designed with the conventional open layout. Additionally, an annular ELT transistor with minimum size ($W = 1.6\ \mu m$, $L = 0.12\ \mu m$) was also included, together with a series of Field Oxide Transistors (FOXFETs) whose source and drain were either n+ diffusions or n-wells. The distance between the diffusions/wells was chosen as the minimum allowed by the design rules, and twice it; the gate material was the first metal layer (M1) and the transistor W was $200\ \mu m$.

B. Test Setup

TID1 was customized for measurements at a wafer probe station using the following equipment:

- X-ray irradiation system (SEIFERT RP149), in which a 3 kW X-ray tube uses a tungsten target typical of radiation-effects studies on semiconductors [9];
- Karl-Suss PA200 semi-automatic 8-inch wafer probe station is installed inside the X-ray irradiation cabinet, where the X-ray tube and a CCD camera can move via a computer-controlled motorized stepper. This allows the operator to either obtain a view of the chip under test to correctly position the probe tips of the probe card on the pads, or to position the X-ray tube over the chip to perform the irradiation. The wafer chuck is from Digit Concept and it is thermally controlled over a range of -20 to $+200°C$, although in this work we have used it to keep the temperature steady at $25°C$ during irradiation and measurements, and to raise it to $100°C$ for the annealing steps;
- custom-developed probe card with 32 probe tips (two columns of 16, to match the size and pitch of the pads in TID1). As for any high-precision low-noise measurement, the signal line is "protected" by a guard surrounding it all the way from the measurement instrument until almost the probe tips;
- semiconductor parameter analyzer (HP4145B) performs the static transistor measurements, applying and measuring currents and/or voltages (typically, I_d is measured as a function of V_{gs} and V_{ds});
- voltage source to keep the transistors under correct bias during the irradiation and annealing steps;
- Keithley 707 switching matrix connects the measuring channels of the HP4145B, or the output of the voltage source, to the appropriate pads in the TID structure;
- all the instrumentation is controlled by a PC running Labview, in particular the full measurement of the transistors connected to 32 pads in TID1 (up to 25 transistors) could be done sequentially and fully automatically.

This unique test setup enabled us to perform all the characterization, irradiation and annealing operations on an individual chip without the need for any manipulation, hence ensuring that the extremely thin and fragile gate oxide of the transistors under test was not damaged due to mounting on a package or other handling.

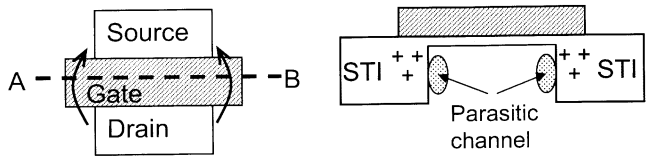

Fig. 1. Top view of an open-layout NMOS transistor (left). On the right, the same transistor is viewed along the A-B line (from the source or drain). The radiation-induced positive charge trapping in the STI is represented by the multiple crosses. This charge modifies the electric field at the edge of the transistor, possibly opening a conductive channel even when the main transistor is turned off. Leakage current can hence flow between source and drain—as indicated by the arrows in the top view.

C. Irradiation Conditions

In this paper all doses are expressed in SiO_2.

Irradiation was performed at room temperature typically at a dose rate of about 458 rd/s; however, for one chip containing NMOS transistors the dose rate was lowered to 20 rd/s. All transistors were irradiated in steps up to a maximum TID of 136 Mrd, and were kept under "worst case" bias during irradiation and annealing: all terminals grounded for PMOS transistors, and all terminals grounded except the gate, which was kept at 1.5 V for core NMOS (this value was increased to 2.5 V in the case of I/O transistors with thicker gate oxide). FOXFETs were also biased as NMOS, with 2.5 V on the gate.

III. Results and Discussion

A. Core Transistors

The results obtained on the ELT NMOS transistors demonstrate the extremely high TID tolerance of the gate oxide of the studied technology, since the radiation effect on their characteristics—leakage current, threshold voltage, subthreshold slope, transconductance—is practically unnoticeable.

On the other hand, the open-layout NMOS transistors were affected by TID, as typically observed in any commercial technology [10]. As shown in Fig. 1, positive charge trapped in the lateral STI oxide opens a conductive channel through which leakage current can flow between source and drain—the parasitic lateral transistors turn on. Since this leakage current is small compared to the current that can flow in the main transistor, it influences the subthreshold region of the transistor I-V curve but not the region above threshold, as shown in Fig. 2. The operational consequence is that the NMOS transistor would have trouble working as a switch (it could never be turned completely off) or, in an analog circuit, in weak inversion. In an analog circuit where its bias would keep it well above threshold, this transistor would not suffer any significant radiation-induced degradation, in a way very similar to the ELT transistor.

1) Radiation-Induced Narrow Channel Effect (RINCE)

It is interesting to observe that the maximum value of the leakage current, defined as the drain-source current for $V_{gs} = 0\ V$, has little dependence on transistor width, nor on transistor length. In Fig. 3, the leakage current is plotted versus the TID for different transistor sizes. Although the pre-irradiation value changes with size, depending on the V_{th} of the transistor, which in turns depends on its size, all curves peak approximately at a

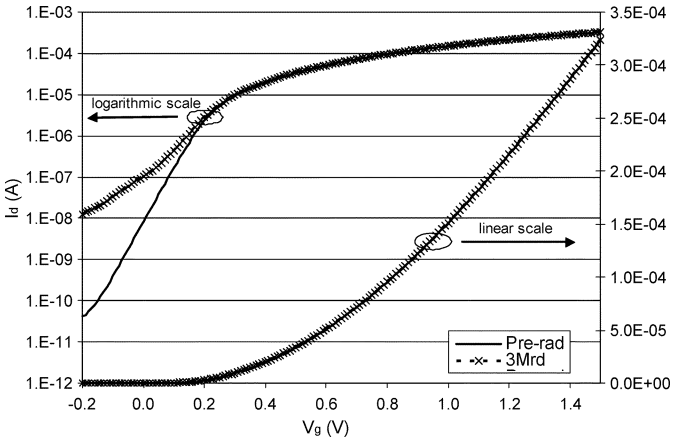

Fig. 2. I_d curve in logarithmic (left) and linear (right) scale for a 10/10 μm NMOS transistor before and after 3 Mrd ($Vds = 1.5$ V), showing the radiation-induced leakage current between source and drain.

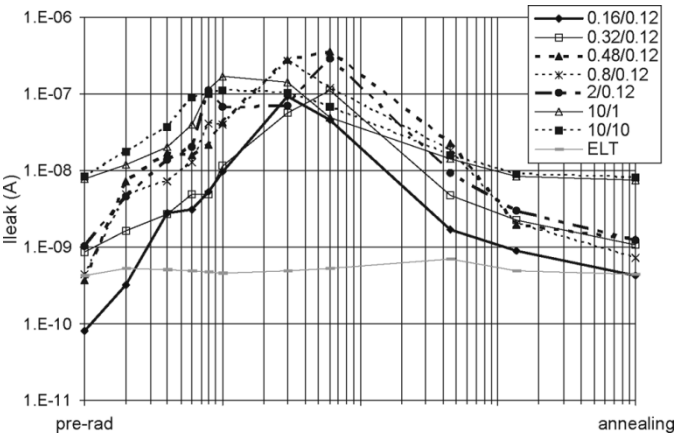

Fig. 3. Evolution of the leakage current with TID for different NMOS transistor size, up to 136 Mrd. The last point refers to full annealing at 100°C. The first point to the left is the pre-rad value.

few 10^{-7} A. Even more interestingly, all curves reach a peak for a TID of about 1-6 Mrd, and then decrease when the irradiation continues at the same dose rate up to 136 Mrd. A similar peak is shown in Fig. 4 for the threshold voltage shift of transistors of different size: V_{th} has been extracted by linearly fitting the square root of the I_d vs V_{gs} curve in saturation ($V_{ds} = 1.5$ V) and finding the intersection of the line with $I_d = 0$. In this case, the voltage shift is strongly dependent on the transistor width, the transistors with W larger than about 1 μm showing only a marginal effect.

The observations in Figs. 2–4 can be explained as follows. Radiation-induced positive charges are quickly trapped in the STI oxide at the transistor edge, and their accumulation eventually builds up an electric field sufficient to open an inversion channel through which source-drain leakage current flows [11]. This can only be observed when the current in the parasitic lateral transistor is larger than the current in the main transistor at the same V_{gs}, which happens after some 200 krd (Fig. 3). While the build-up of positive trapped charge is fast, the formation of interface states is known to be a slower process [12]. In NMOS transistors, the negative charge trapped in interface states only starts to compete with the oxide-trapped charge with some delay, giving origin to a well-known rebound effect.

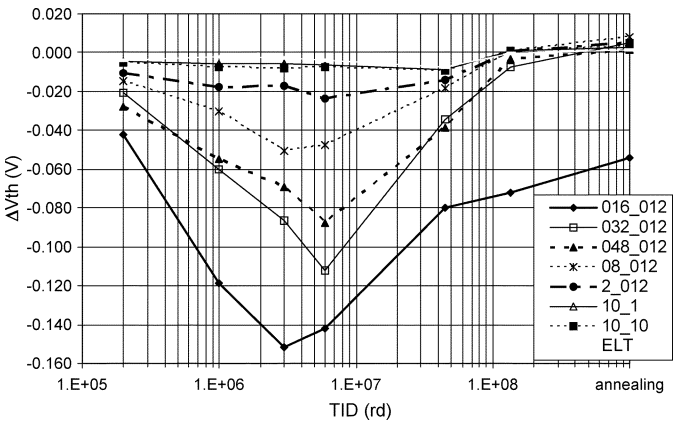

Fig. 4. V_{th} shift with TID for different NMOS transistor size, up to 136 Mrd. The last point refers to full annealing at 100°C.

In the case of the STI oxide in the studied technology, and at the dose rate used for our test, this happens when the TID reaches a value between 1 and 6 Mrd. From this point on, the interface states contribute significantly to the charge balance at the transistor edge, increasing the V_{th} of the parasitic lateral transistor and hence decreasing the leakage. We point out that in this paper we call these trapping centers interface states because of their properties of being amphoteric (we will see later that they trap positive charge in PMOS transistors) and with slow buildup. Nevertheless, we have not addressed their detailed nature in our study.

For narrow channel transistors, the charge balance at the transistor edges not only determines the accumulation, depletion or inversion condition of the parasitic lateral transistor, but also influences the electric field of the main transistor. This effect is known in CMOS technologies as "narrow channel effect", and it is observable in any deep submicron process as a decrease of V_{th} with transistor width [13]. In the presence of positive charges trapped in the lateral STI oxide, narrow channel effect should decrease the threshold of sufficiently narrow NMOS transistors, whilst it should increase it (in absolute value) for PMOS transistors. This is indeed what we observe in Fig. 4 for NMOS and Fig. 5 for PMOS transistors: in both cases the effect is as expected more pronounced for narrower transistors. In the case of the PMOS the charges trapped in the interface states are also positive and add to the effect of the oxide-trapped charge,; thus rather than the "peaking" observed for NMOS V_{th} in Fig. 4, in Fig. 5 we observe an increase of the slope of the V_{th} shift with TID.

The different sensitivity to TID of transistors with different gate width illustrated in Figs. 4 and 5 has not been reported before, and we refer to it as "Radiation-Induced Narrow Channel Effect" (RINCE).

The increasing importance of interface states with accumulated TID is further confirmed by the following test. We have cyclically performed irradiation and annealing steps to NMOS transistors, where annealing steps were at 100°C for a few hours (4–60 hours, but typically about 15). Initial irradiation steps of 1 Mrad were used, then increased to eventually reach a TID of 102 Mrd. Measurements were performed after each irradiation and annealing step, and we defined Δleakage the increase in the leakage

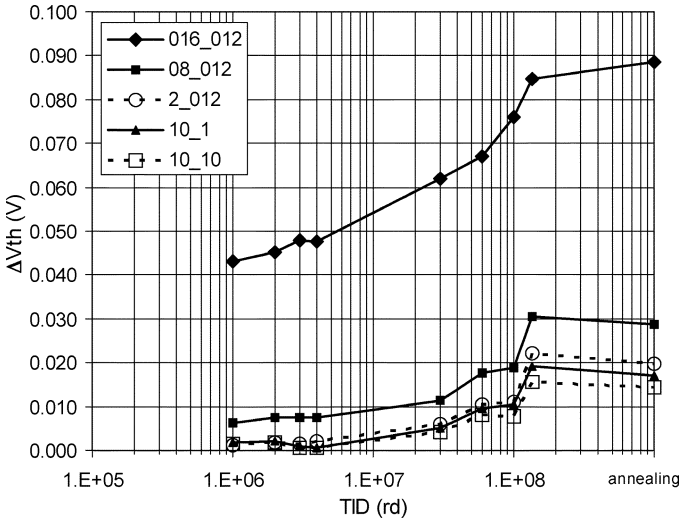

Fig. 5. V_{th} shift (absolute value) as a function of TID for PMOS transistors of different size, up to 136 Mrd. The last point refers to full annealing at 100°C. For PMOS transistors, due to the absence of radiation-induced leakage currents, V_{th} was more easily extracted as the V_{gs} corresponding to a specific Ids indicated by the foundry.

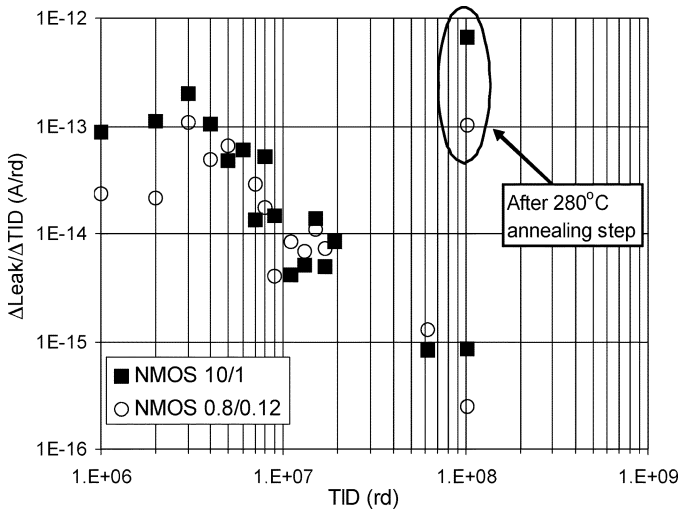

Fig. 6. Increase of the leakage current per rd $(\Delta\text{leak}/\Delta\text{TID})$ as a function of TID for 2 sample NMOS transistors of different size.

current due to each irradiation step. Fig. 6 depicts the derivative of the leakage current with respect to the incremental TID $(\Delta\text{leakage}/\Delta\text{TID})$ versus TID for every irradiation cycle (or the increase of the radiation-induced leakage normalized to 1 rd of TID). The idea was to anneal a good fraction of the oxide-trapped charge at the end of each cycle, then irradiate again and observe the effect of the freshly trapped charge on the leakage. From isochronal annealing measurements [14] that will be detailed in Section III-A-2 we know that about 60% of the oxide-trapped charge gets released in 15 hours at 100°C, whilst 80% of it should be de-trapped by a 60 hour annealing step at high temperature. We would therefore expect each TID step to induce the trapping of a comparable (within a factor of 2) amount of "fresh" charge, hence the quantity depicted in Fig. 6 should not change considerably with the accumulated TID. Instead, the dramatic decrease observed—more than 2 orders of magnitude—points out that the relative influence of freshly trapped charge on the leakage current becomes negligible with TID. This is only possible if the negative charge in the interface states largely dominate the charge balance at the transistor edge. After the last cycle at 102 Mrd, we performed an annealing for 2 hours at 280°C (this is the maximum temperature of our oven), with the chip unbiased. We then irradiated it with the usual procedure up to 1 Mrd (additional), and measured it again. This time, as shown in the last two points in Fig. 6, the relative degradation was large again, indicating that this high temperature step healed the interface states, and the freshly trapped oxide charge dominated the charge balance again.

2) Isochronal Annealing Results

Among the techniques used to study the characteristics of radiation-induced charge trapping in MOS oxides, isochronal annealing is one of the simplest to setup. The technique consists of measuring the effect of sequentially emptying a fraction of the traps through a succession of short annealing periods at increasing temperatures [14]. The sample is cyclically heated to reach a dwell temperature, kept in that condition for a dwell time, then cooled down to room temperature to be measured. The dwell temperature is increased at each subsequent step, typically by 20°C. The difficulty of the experiment is often to ensure that the heating and cooling times are short compared to the dwell time, so that the effects during heating and cooling are minimal.

The thermal inertia of the temperature controlled chuck used for our work is such that the heating and cooling times are far too long for an isochronal annealing study. Therefore, we were obliged to remove the silicon die containing the TID1 test structure from the wafer probe station for each thermal cycle, during which is was consequently un-biased, and to bring it back for the measurement at the end of the cycle. In agreement with previous work reported in the literature [15], we chose dwell times of 360 s, and temperature steps of 20°C. The sample was positioned on a pre-heated bulky metal plate inside an oven for each annealing step. Given the thermal conductivity of silicon, the tiny mass of the silicon die, and the large mass of the metal plate, the sample was heated almost instantaneously to the dwell temperature. At the end of the dwell time, the sample was extracted from the oven and positioned for 120 s on top of a bulky metal plate pre-cooled to −20°C, ensuring a quick cooling. It was then measured at our probe station, where the thermally controlled chuck imposed a temperature of 25°C.

The sample was irradiated at 458 rd/s up to 1 Mrd, a TID level chosen to maximize the radiation effects induced by the charge trapped in the oxide. The dwell temperature was increased in steps from 40 to 240°C, and the parameter chosen for the estimate of the un-annealed fraction of the trapped charge was the leakage current. From the un-annealed fraction, we could extract the energy levels of the traps. With this information, and with simple mathematics based on Arrhenius' law, it is possible to estimate the evolution of the trapped charge in any dose rate environment, and at any annealing temperature.

To verify the capability of this method to lead to reliable forecasts, we compared the measured evolution of a sample irradiated to 1 Mrd with the forecast obtained using the results of the isochronal study. The annealing for the comparison was at 100°C for 15 hours. As shown in Fig. 7 for the leakage current,

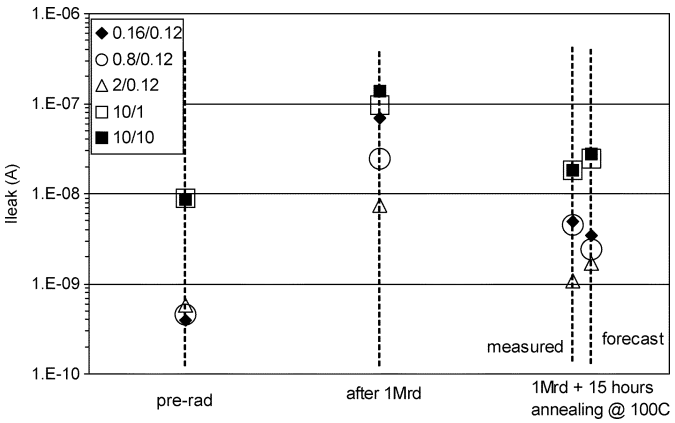

Fig. 7. Leakage current evolution of NMOS transistors with different aspect ratio quickly exposed to 1 Mrd (in 36′) and annealed at 100°C for 15 hours. The forecast is a prediction that uses the energy levels extracted from the isochronal annealing study.

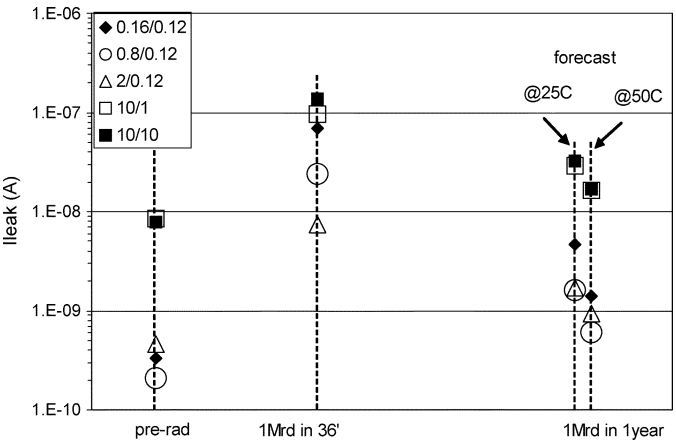

Fig. 8. Forecasts of the leakage current evolution of transistors at a dose rate more typical of real applications, and at two temperatures. The damage is considerably smaller than for the measured fast irradiation also shown.

the forecast is close to the effective evolution of the transistor (within a factor of 2). From this experiment, we estimated that 60% of the charge is released in 15 hours at 100°C.

The results of the isochronal annealing study were used to tailor the details of the last test in Section III-A-1, but most of all they are generally useful to predict the evolution of the transistors' electrical characteristics in low-dose-rate environments typical of real applications in space or HEP experiments. One such example is shown in Fig. 8, where we predict the leakage current of the transistors when the TID of 1 Mrd is accumulated over a 1 year period. Whilst a quick irradiation increases the leakage by more than 2 orders of magnitude for the smallest W transistor, the prediction for a real application is an increase by a factor of only 10 at 25°C, and drops to a factor of 4 if the transistor operates at 50°C, a more realistic junction temperature for an operating circuit.

It is important to note that the isochronal annealing technique just described allows prediction of the time-temperature evolution of the charge trapped in the oxide only, and not of the interface states. Given that the contribution of these latter tends

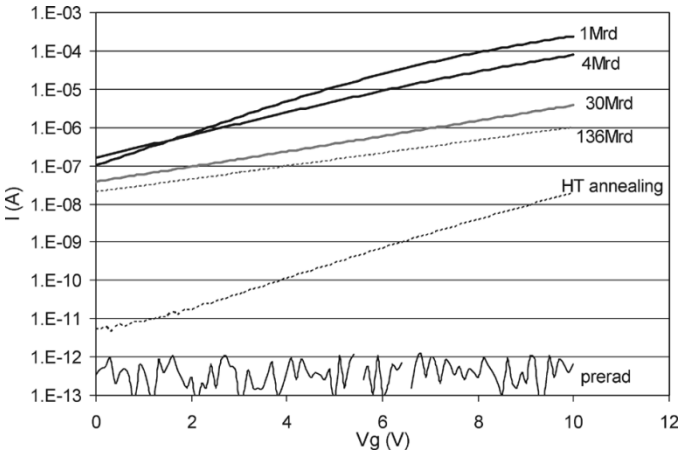

Fig. 9. I_d vs V_{gs} curve of a 200/0.92 μm FOXFET with n-well source and drain, for different TID and finally after full annealing at 100°C.

to decrease the radiation-induced effects on the transistor characteristics, it is expected that our forecast for low-dose-rate environments is generally a worst case evolution of the transistor behavior. Taking into account this likely over-estimate and the general decrease of the damage at higher TID levels shown in Figs. 3 and 4, new perspectives open on the use of open-layout transistors also for multi-Mrd radiation environments.

B. FOXFETs

Other than source-drain leakage, TID can induce failure in integrated circuits by opening conductive channels under the STI oxide. The leakage current in this case can flow between adjacent n+ diffusions at different potential, such as electrodes of neighbor NMOS transistors (source or drain), diodes or resistors, or between n-wells at different potential. When studying the performance of a technology in a radiation environment, FOXFETs are useful to understand if such leakage currents are likely to appear.

Fig. 9 summarizes the radiation response of the device with n-well source and drain at minimum distance (0.92 μm) and $W = 200$ μm. Due to the presence of protection diodes, the FOXFET's gate voltage could only be swept between 0 and 10 V, and before irradiation no current is measured in this range in the I_d vs V_{gs} curve. After 1 Mrd, this voltage swing is almost entirely in the subthreshold working region of the transistor due to the V_{th} shift induced by charges trapped in the oxide. Further exposure to TID increases the V_{th} and degrades the subthreshold slope, indicating the formation of interface states. This behavior agrees well with our model for the evolution of leakage current and V_{th} shift of transistors presented in Section III-A-1. The transistor current increases with TID until about 1–4 Mrd, then decreases with further integrated dose in a way very similar to that shown in Fig. 3 for the leakage of NMOS transistors. Full annealing (1 week) at 100°C seems nevertheless to also heal a part of the interface states, since the subthreshold slope recovers; this behavior has been observed before for interface states [16], although it is not typical.

FOXFETs integrated with n+ diffusions as source and drain show a qualitatively very similar behavior, but in this case the maximum leakage current observed is in the nA range.

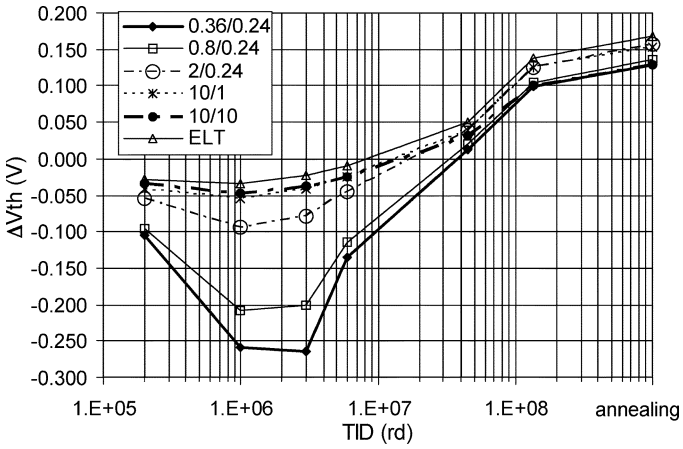

Fig. 10. Threshold voltage shift for I/O NMOS transistors with TID, up to 136 Mrd. The thicker gate oxide of these transistors is itself subject to noticeable radiation effects, as witnessed by the "rebound" observable for the ELT transistor.

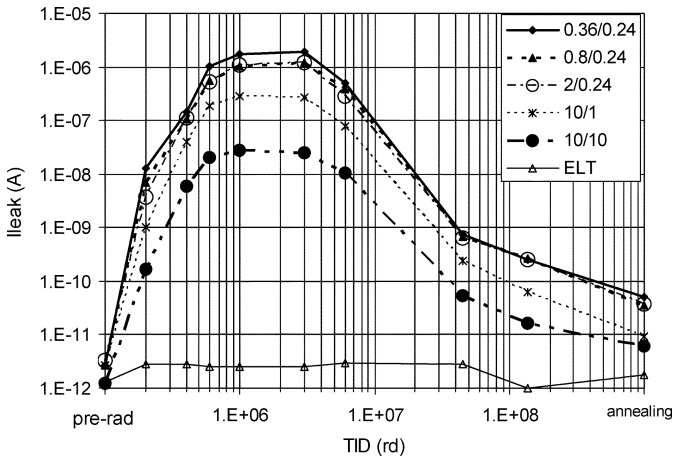

Fig. 11. Leakage current for I/O NMOS transistors up to a TID of 136 Mrd. The leak is due to charge trapping in the STI that opens a conductive path (the lateral parasitic transistor turns "on") and, for narrow transistors, influences the $\mathrm{V_{th}}$ of the main transistor (RINCE).

C. I/O Transistors

I/O transistors are available to allow the integration of ASICs in the 130 nm technology within systems requiring 2.5 V logic levels. They are also recommended for on-chip analog circuitry, wherever the 1.5 V supply voltage of the core transistors does not provide enough room for stacked transistors, as frequently used in analog circuit architectures.

Exposure of I/O transistors to TID up to 136 Mrd has given results conceptually similar to those presented already for the core transistors, but with the addition of a noticeable sensitivity of the thicker gate oxide itself. This is evident in the evolution of the $\mathrm{V_{th}}$ with dose for the enclosed (ELT) NMOS transistor, shown in Fig. 10. The rebound observed is due to early trapping of charges in the oxide, and later formation of interface states. This latter continues during the high-temperature annealing, to give a considerable final shift (about 150 mV). In analogy with the core devices, the narrower the transistor the larger the RINCE observed, and in Fig. 10 the narrower transistors show a pronounced negative "peak" in the $\mathrm{V_{th}}$ shift at doses around 1–3 Mrd due to trapping of positive charges in the lateral STI oxide. At doses larger than about 10 Mrd, the $\mathrm{V_{th}}$ rebound is due to radiation effects in the gate oxide (as demonstrated by the ELT result) and not in the lateral STI. This was not observed for the core transistors in Fig. 4. In Fig. 11, the "off" current of NMOS I/O transistors exceeds the $\mu\mathrm{A}$ for the narrower transistors at doses between 1 and 3 Mrd where, as it was for the core transistors, it peaks before decreasing at larger TID.

The radiation-induced threshold voltage shift for PMOS transistors is shown in Fig. 12. In this case, the larger contribution to the shift comes from charges trapped in the gate oxide rather than from RINCEs: the wider transistor with $\mathrm{W} = 10\ \mu\mathrm{m}$ has a shift of about 300 mV after 136 Mrd, whilst the narrower one does not reach 450 mV. Annealing only improves the situation slightly, since the major contribution to the damage comes from interface states.

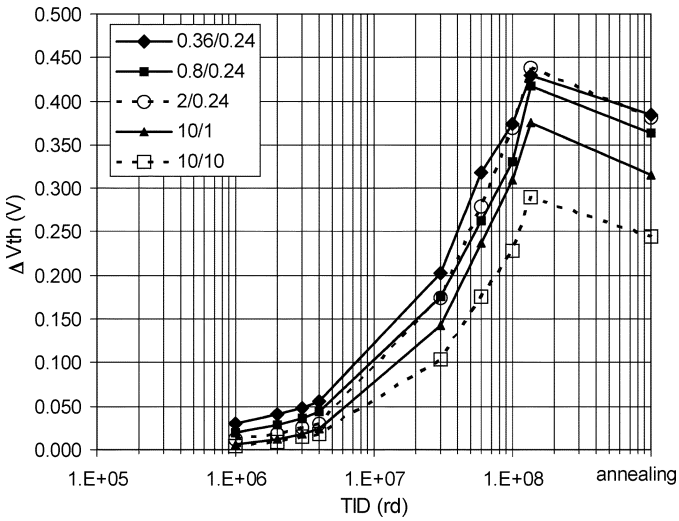

Fig. 12. Threshold voltage shift for I/O PMOS transistors with TID, up to 136 Mrd.

D. SRAM

It is interesting to observe how the radiation response of transistors described above influences the functionality of circuits in a radiation environment. For this purpose, we have irradiated a 16 kbit SRAM circuit designed in the same 130 nm CMOS technology, and manufactured in the same production run as the TID1 test structure. The circuit has been designed using the SRAM generator of a commercial library and IP provider, in which the memory cell uses narrow transistors (down to 0.15 $\mu\mathrm{m}$).

Although the nominal operating voltage for the memory is 1.2 V, before irradiation it is capable of correctly functioning down to a $\mathrm{V_{dd}}$ of 0.875 V (at a clock rate of 10 MHz). In Fig. 13, we report the minimum voltage for correct operation of the SRAM as a function of TID: the minimum supply voltage increases with TID until eventually, above 3 Mrd, it starts to decrease. As a result, the curve peaks in a way and at a dose comparable to what was observed for the core transistor's leakage (Fig. 3) and threshold voltage (Fig. 4). Thus the radiation tolerance of the circuit correlates well with the response to TID measured on core transistors.

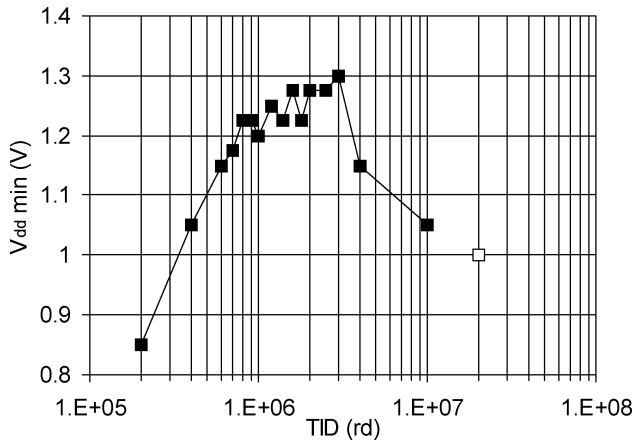

Fig. 13. Minimum Vdd for correct operation of the SRAM as a function of TID. Before irradiation, this value was 0.875 V. The white point refers to full annealing at 100°C.

IV. Considerations on ASICs Design and Radiation Tolerance of Commercial Components

The results of III can be used to anticipate the consequence of certain design choices on the radiation tolerance of ASICs, and more generally to predict the radiation tolerance of commercial components manufactured in 130 nm CMOS technologies.

If the radiation tolerance of the 2.2 nm gate oxide of the core transistors in these technologies is absolutely excellent, the lateral isolation of the transistors is still a source of problems for applications in radiation environments, in particular for transistors with small width. Nevertheless, we observe that the leakage current per transistor—in a fast irradiation—is limited to a fraction of 1 μA, whilst for older technologies it was common to reach values 2–3 orders of magnitude larger [17]. Also the time-temperature evolution of the charge at the transistor's edge (oxide-trapped charge and interface states) is such that considerably less damage is expected for the low-dose-rate environments typical of real applications. The same applies for inter-transistor isolation, which even at laboratory dose rates shows a modest leakage current. For these reasons, we believe that the TID tolerance of commercial circuits designed using 130 nm technologies is very likely to be generally superior to the tolerance of their counterparts in older CMOS technologies. In some cases, components could even stand multi-Mrd radiation levels, and this should not come as a surprise in light of the results presented in this paper.

For ASIC design, the key question concerns the need to use systematically HBD techniques such as ELT transistors and guardrings. Although this allows to design very reliable radiation tolerant circuits, it comes at the cost of lower density, lower performance, and larger power consumption. Additionally, it requires the development of a dedicated digital library where all cells are carefully designed with HBD an investment in manpower and time that only relatively large design groups can afford. Can this be avoided?

A careful look at the results in Figs. 3–5, and at the results of the isochronal annealing studies in Section III-A-2, reveals that the damage on transistor characteristics in a low-dose-rate environment is limited—especially for transistors with W larger than about 0.5 μm. Also the isolation between n-wells and transistors should be maintained in the absence of guardrings, since the level of inter-transistor leakage is very modest even at laboratory dose rates, and will be considerably lower in the field. This suggests that digital circuits designed using commercial libraries could survive even in high TID environments. The result on the SRAM in Section III-D is a good indicator in this respect: the memory uses by definition quite aggressive layout techniques to minimize the area, including minimum size transistors. Although in Fig. 13 it appears that the memory fails at a TID of about 800 krd, since it does not work anymore at the V_{dd} of 1.2 V that is its design specification, we can nevertheless predict that failure would not occur in the field at a much lower dose rate.

For analog circuits, where most often design is anyway full custom, it is wiser to layout almost all transistors as ELTs. Although this is mandatory for any transistor working in weak inversion, since this region is the most affected by TID, it can be avoided for transistors that are biased deeply in strong inversion. This is the case for current mirrors that typically also require a very small W/L ratio that is impossible to achieve with only one ELT transistor.

To summarize, HBD techniques to mitigate TID effects can in principle be avoided, or at least only used for some portions of the circuits (the analog parts and very sensitive digital circuits in terms of timing) only if the decision of doing so is taken as the result of a risk management approach, which relies on the full analysis of the constraints (TID, dose rate, temperature, speed, power consumption, ...). Also, since this means basically to rely on the natural radiation tolerance of the technology, it is necessary to monitor it constantly during the full manufacturing life of the circuit—for instance with dedicated test structures for TID sensitivity evaluation for each lot, such as the TID1 used for this study.

All the above is valid for the core of the design, where core transistors are used. For the periphery of the circuit, where the input/output functions are implemented, the situation could be very different. In the situation where the circuit should have 2.5 V interface capability, and where I/O transistors with thicker gate oxide are used, the radiation tolerance of the full circuit could well be limited by the input/output circuitry. We have seen in Section III-C that I/O transistors are considerably more damaged by TID effects, and that even enclosed transistor can have, in a multi-Mrd environment, considerable radiation-induced threshold voltage shifts. Therefore, the designer has to carefully evaluate the impact of these effects on the I/O circuitry, especially wherever signals are transferred at high speed and where timing shifts could induce communication failure.

Two last considerations are worth mentioning. First, all the results presented were collected on samples coming from only one production lot. Although older and considerably less complete test structures were measured in the past giving qualitatively similar results for the same and also for a different foundry, we are not able to predict the variation of the effects over the lifetime of the technology—especially in the presence of small modifications of the process, which are at this stage of maturity unlikely. Second, the discussion has been centered on the design of circuits for multi-Mrd environments, such as for HEP

experiments at high luminosity colliders, the relevant applications for the authors. For more "moderate" radiation environments, where the TID accumulated over a period of a few years does not exceed 100–200 krd, we believe that the natural radiation tolerance of the technology is sufficient for most applications without the need for HBD techniques. Of course, Single Event Effects still require to be addressed.

V. Conclusion

The study of the TID response of transistors and isolation test structures in a 130 nm commercial CMOS technology has shown the adverse contribution from oxide-trapped charge and interface states to the radiation-induced edge effects of deep submicron transistors. In particular, it has shown how this can influence, in modern technologies, the characteristics of the main transistor, an effect we called Radiation-Induced Narrow Channel Effect (RINCE). This effect is expected to increase its importance in more modern technologies with smaller feature sizes.

The results of this work indicate that the 130 nm technology core transistors have the potential of standing high levels of TID. This has been confirmed on an SRAM test circuit, suggesting that the natural radiation tolerance of the technology could enable commercial-grade circuits to meet radiation requirements for harsh environments. Precaution has nevertheless to be used, since process variations could compromise the radiation tolerance with no warning. It should therefore be envisaged to verify the results on hardware produced, in the same technology, at different times to "average" the radiation performance over a significant sample of products, covering at least the natural processing variability. At the same time, it would be very interesting to repeat the measurements on samples from different manufacturers of 130 nm CMOS technologies, which has only be done for one other vendor and with un-complete test structures. This would allow a more confident conclusion on the trend of the radiation-tolerance of the 130 nm node.

Acknowledgment

The authors are grateful to G. Anelli and M. Letheren of the CERN Microelectronics Group for their patient review of the manuscript, and their valuable contribution to improve it.

References

[1] N. S. Saks, M. G. Ancona, and J. A. Modolo, "Radiation effects in MOS capacitors with very thin oxides at 80° K," *IEEE Trans. Nucl. Sci.*, vol. NS-31, no. 6, pp. 1249–1255, Dec. 1984.

[2] N. S. Saks, M. G. Ancona, and J. A. Modolo, "Generation of interface states by ionizing radiation in very thin MOS oxides," *IEEE Trans. Nucl. Sci.*, vol. NS-33, no. 6, pp. 1185–1190, Dec. 1986.

[3] W. Snoeys *et al.*, "Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip," *Nucl. Instrum. Methods Phys. Res. A*, vol. 439, pp. 349–360, 2000.

[4] D. R. Alexander, "Design issues for radiation tolerant microcircuits for space," presented at the Short Course Nuclear and Space Radiation Effects Conf., Indian Wells, CA, Jul. 1996.

[5] F. Faccio, "Radiation issues in the new generation of high energy physics experiments," *Int. J. High Speed Electron. Syst.*, vol. 14, pp. 379–399, 2004.

[6] D. Mavis, "Microcircuits design approaches for radiation environments," presented at the 1st European Workshop Radiation Hardened Electronics, Villard de Lans, France, 2004.

[7] S. Redant *et al.*, "The design against radiation effects (DARE) library," presented at the RADECS2004 Workshop, Madrid, Spain, Sep. 22–24, 2004.

[8] R. Lacoe, "CMOS scaling, design principles and Hardening-By-Design methodologies," presented at the Short Course Nuclear and Space Radiation Effects Conf., Monterey, CA, Jul. 2003.

[9] L. J. Palkuti and J. J. LePage, "X-ray wafer probe for total dose testing," *IEEE Trans. Nucl. Sci.*, vol. NS-29, no. 6, pp. 1832–1837, Dec. 1982.

[10] J. V. Osborn, R. C. Lacoe, D. C. Mayer, and G. Yabiku, "Total dose hardness of three commercial CMOS microelectronics foundries," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3, pp. 1458–1463, Jun 1998.

[11] O. Flament, C. Chabrerie, V. Ferlet-Cavrois, and J. L. Leray, "A methodology to study lateral parasitic transistors in CMOS technologies," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 3, pp. 1385–1389, Jun. 1998.

[12] M. R. Shaneyfelt *et al.*, "Interface-trap building rates in wet and dry oxides," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 6, pp. 2244–2251, Dec. 1998.

[13] S. Wolf, *Silicon Processing for the VLSI Era*. Sunset Beach, CA: Lattice Press, 1995, vol. 3, The submicron MOSFET, pp. 222–226.

[14] L. Dusseault *et al.*, "Prediction of low dose-rate effects in power MOSFET's based on isochronal annealing measurements," *J. Appl. Phys.*, vol. 81, pp. 2437–2441, Mar. 1997.

[15] F. Saigné *et al.*, "Experimental validation of an accelerated method of oxide-trap-level characterization for predicting long term thermal effects in metal oxide semiconductor devices," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 2001–2006, Dec. 1997.

[16] J. Schwank, "Total dose effects in MOS devices," presented at the Short Course Nuclear and Space Radiation Effects Conf., Phoenix, AZ, Jul. 2002, p. III-47.

[17] G. Anelli *et al.*, "Total dose behavior of submicron and deep submicron CMOS technologies," in *Proc. 3rd Workshop Electronics LHC Experiments*, London, U.K., Sep. 22–29, 1997, pp. 139–143.