Asynchronous Data-dependent Jitter Compensation

by

Michael Price

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Abstract

Data-dependent jitter (DDJ) caused by lossy channels is a limiting factor in the bit rates that can be achieved reliably over serial links. This thesis explains the causes of DDJ and existing equalization techniques, then develops an asynchronous (clock-agnostic) architecture for DDJ compensation. The compensation circuit alters the transition times of a digital signal to cancel the expected channel-induced delays. It is designed for a 0.35 μm BiCMOS process with a 240 $\times$ 140 μm footprint and typically consumes 3.4 mA, a small fraction of the current used in a typical transmitter. Extensive simulations demonstrate that the circuit has the potential to reduce channel-induced DDJ by at least 50% at bit rates of 6.25 Gb/s and 10 Gb/s.

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My parents let me build and tweak audio electronics when I was in high school, and put up with loud noises, smells, stains and burns so I could teach myself the important things about engineering before arriving at MIT.

Finally, I would like to single out two of my role models, even if they didn't know they were role models. Their inspiration is hidden in this thesis.

- Prof. Jeff Shapiro, my academic advisor, is incredibly well-organized and rigorous but still manages to be devoted and inventive. He's a living example that success in a demanding academic environment doesn't have to be draining.
- Mike Axiak, a fellow student, is completely unafraid of learning new things and more productive than anyone else I know. I'll never match his brilliance, but I'll be content to be a fraction as easygoing, open-minded, or helpful as he is.

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Chapter 1

Introduction

Everything in nature is a lowpass filter. Thanks to parasitic capacitances, dispersion of electromagnetic fields, and even Newton's second law, we are unable to generate signals that change instantly. Were it not for this simple inconvenience, electronic devices could transmit data at arbitrarily high speeds. The bandwidth of the medium between two devices limits the data rates that they can use to communicate.

Modern computers and networking equipment need to process data at several Gb/s, yet the industry relies on particularly low-bandwidth (but inexpensive) copper wires and printed circuit board (PCB) traces. The intersymbol interference (ISI) caused by these low-bandwidth channels results in jitter, which is an uncertainty in the transition times between symbols. A slew of equalization techniques has cropped up to fight bandwidth limitations. Most equalizers alter the shape of transmitted pulses (emphasizing high-frequency components) in order to reduce ISI and jitter in the received signal.

Adjusting the timing of pulses directly can reduce jitter in a more energy-efficient manner. It will be demonstrated below that jitter compensation can be performed by small analog circuits without attempting to recover a clock. The phenomenon of jitter in serial links, along with existing equalization techniques, will be examined first.

1.1 Serial links

Consider a serial link, or high-speed link, to be a digital communications system consisting of a transmitter, channel, and receiver. We will focus on the lowest-level transmission of 1s and 0s, while keeping in mind that the encoding scheme is another important tool for maximizing system performance [2]. Several "channel impairments" establish constraints on the speed and reliability of a link [24]. First and foremost is high-frequency loss: the Nyquist frequency for the desired bit rate is typically well above the -3 dB bandwidth

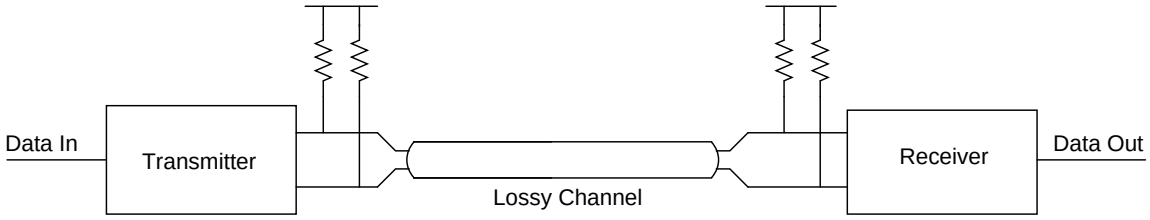

Figure 1-1: A serial link.

of the channel. As a result, the received signal looks very different from the transmitted one; it may be difficult to recover the exact bit sequence that was transmitted. The remaining sections of this introduction examine the implications of high-frequency loss as well as noise and crosstalk.

1.1.1 Typical link scenario

A typical application of high-speed link technology is found in network routers and switches. These devices selectively transmit information between a set of ports connected to computer network adapters and other networking equipment by Category 5 and fiber-optic cables. Inside the router, microprocessors and crosspoint switches on several line card PCBs communicate through traces on the cards, or across a larger backplane PCB. The channel for each link consists of a differential trace across the PCB[s], along with card connectors and vias.[1] This link is shown in schematic form in figure 1-1.

In the context of a modular system, the line cards (and the associated ICs) are replaced more frequently than the backplanes. As IC device sizes shrink and on-chip bandwidth increases, the channel does not necessarily improve. Many serial link design techniques (including jitter compensation) are intended to squeeze the highest possible speeds from this existing hardware.

1.1.2 Channel loss mechanisms

Circuit board traces suffer from skin effect and dielectric loss [6]. An appropriate model for the frequency response of a trace from one end to the other is

$$H(j\omega) = \exp\left[-l\left(\underbrace{\frac{j}{F_v c}}_{\text{prop delay}} + \underbrace{(1+j)\sqrt{2\pi^2\mu\sigma\omega}}_{\text{skin effect}} + \underbrace{2\pi\frac{\sqrt{\epsilon_r}\tan\delta}{c}\omega}_{\text{dielectric loss}}\right)\right]$$

[1] Most PCBs are manufactured with FR4 fiberglass dielectric, which is lossy but inexpensive.

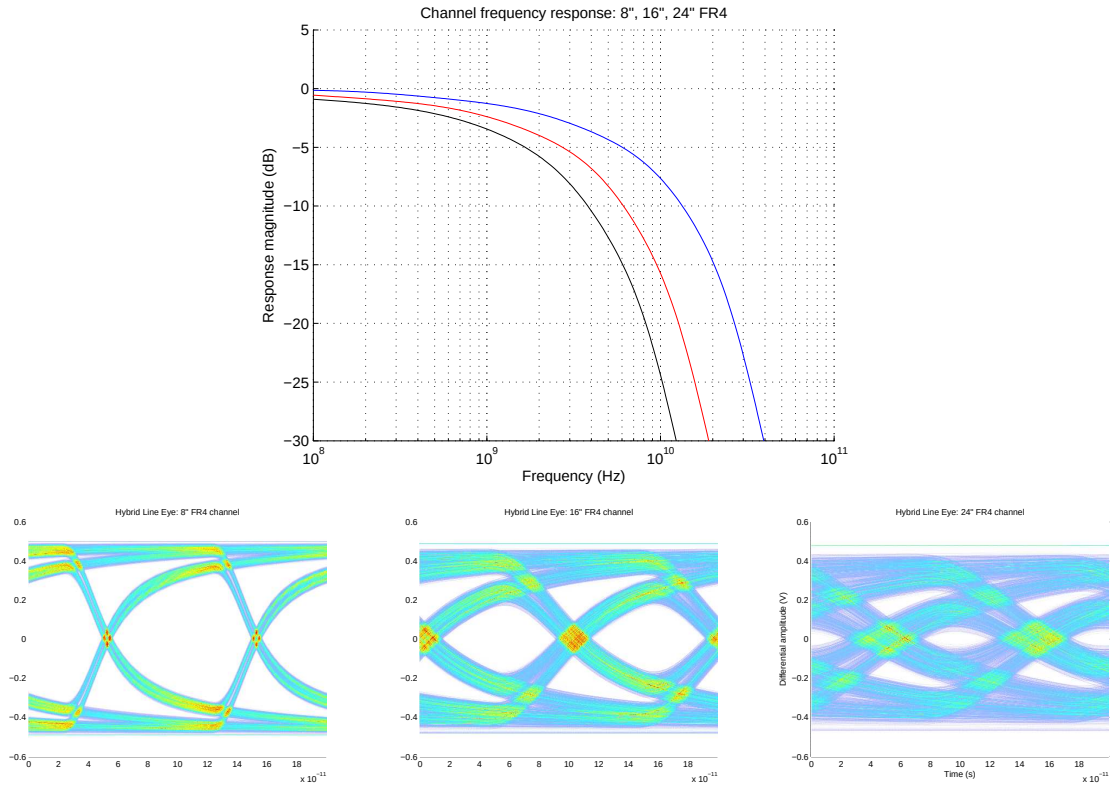

Figure 1-2: Frequency responses and eye diagrams for 8”, 16” and 24” long FR4 channels.

where l and F_v are the length and velocity factor of the trace, μ and ϵ_r are the permeability and dielectric constant of the dielectric, σ is the conductivity of the trace, and c is the speed of light.

The narrowing of the trace’s effective cross-sectional area (skin effect) contributes an $e^{-\frac{1}{\sqrt{\omega}}}$ factor to the channel’s frequency response. A dielectric loss proportional to $e^{-\omega}$ takes over at high frequencies.

Approximate responses of some short FR4 channels and the corresponding eye diagrams are shown in figure 1-2. Response aberrations due to trace discontinuities, connectors, and reflections are not included in the model. These aberrations do contribute jitter, but it is important to concentrate on the bulk loss first. The eye diagrams show that high-frequency loss causes the sampling window to shrink as the channel gets longer.

The propagation delay (e^{-jt_d} component) will be ignored from now on, as it has no effect on link performance in feed-forward equalization scenarios.

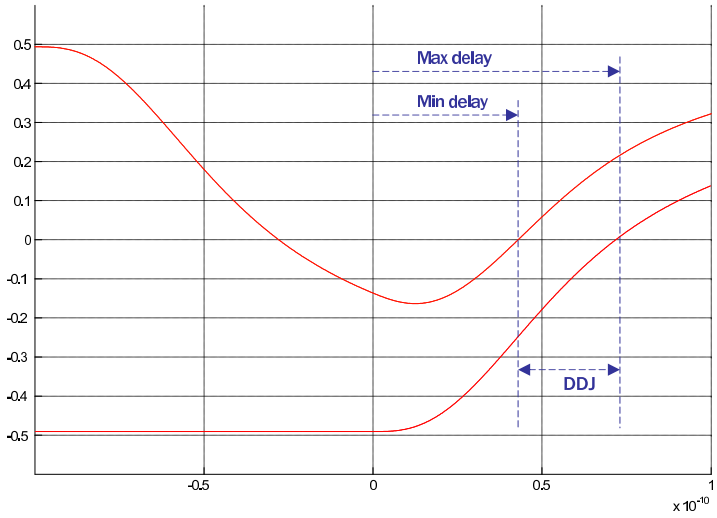

Figure 1-3: Data-dependent transition delays: A rising edge following a stream of mostly zeros exhibits higher transition delay than a rising edge following a stream of mostly ones.

1.1.3 Jitter

Jitter is a timing error in a digital signal—the difference between the expected and actual transition times. When a digital signal (bitstream) is passed through a linear filter and then thresholded, the amplitude distortion introduced by the filter is eliminated but the phase distortion remains. This operation introduces deterministic jitter in any high-speed link [5].

Consider the case in figure 1-3 of 2-level pulse amplitude modulation (PAM2) where the transmitted signal has a perfectly uniform clock, so the transitions are evenly spaced. When transitioning from 0 (low) to 1 (high) after a long sequence of 0s, the step response of the channel takes about 70 ps to reach the the threshold voltage. This time is the maximum transition delay. When transitioning from 0 to 1 after a sequence of 1s followed by a single 0, the transition delay is smaller (about 40 ps) since the channel has not fully settled to 0 before the transmitted transition. These two transition delays mark the boundaries of the channel-induced data-dependent jitter (DDJ) distribution.

As the deterministic component of the jitter increases, the sampling time required for a desired bit error rate (BER) must be confined to a narrowing window. When many intervals of the signal are overlaid to create an eye diagram (figure 1-4), this sampling window is visible as the “open” part of the eye. The distribution of transition time errors, equivalent to a horizontal cross section of the eye diagram, is shown at right.

Once the peak-to-peak jitter magnitude reaches one bit period, it is no longer possible to recover the original bitstream with a uniform sampling clock. Hence it is important to minimize the jitter introduced by

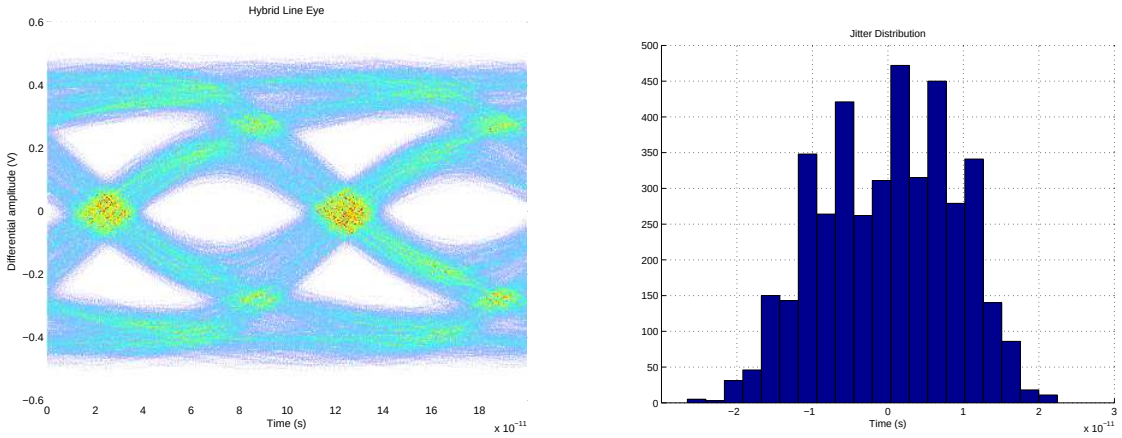

Figure 1-4: Eye diagram (left) and the corresponding jitter distribution (right).

each component of a high-speed link.

The extents of a DDJ distribution caused by channel loss depend only on the channel's frequency response. (This will be explained more fully in section 2.2.1.) In order to characterize this jitter distribution and develop a compensation scheme, the channel must be modeled as a linear system. This work assumes that the channel is fully described by a frequency response fitting the model of section 1.1.2. The loss estimates computed by this model are smaller than losses encountered in practice because the model ignores the parasitic elements in connectors, IC packages, and measuring equipment.

Jitter caused by outside interference, including EMI and crosstalk from nearby signals, is classified as bounded uncorrelated jitter (BUJ); jitter caused by random noise is classified as random jitter (RJ). The jitter compensation circuit described below focuses solely on eliminating DDJ.

1.1.4 Noise

The signal-to-noise ratio of a channel limits its information-carrying capacity, but random noise is not the main limiting factor in modern serial links. Stojanovic et al. computed statistics for the voltage disturbances reaching the receiver by representing transmitter jitter and carrier phase noise as random processes and adding them to thermal noise [23]. In a multi-tone communication scheme, these disturbances imposed a capacity limit between 60–70 Gb/s for a 26" long FR4 channel. The bit rates that have been achieved in practice (rarely over 10 Gb/s) are frustratingly low in comparison.

In a PAM2 serial link, the receiver makes bit decisions by sampling its input voltage waveform and comparing the sample to a fixed threshold. Even if ISI is subtracted out by an equalizer, the receiver needs to have an open sampling window: a range of time and voltage for which its bit decision is likely to be

correct. The effect of noises generated on each side of the link can be lumped as follows:

- Assuming that the transmitter includes a high-gain limiting amplifier with limited slew rate, voltage noise on the transmit side is converted to random jitter in the transmitted signal.
- Thermal noise in the receiver's termination resistors reduces the vertical eye opening.

Due to the high currents and low impedances involved, RJ is usually small; RJ measured at the transmitter typically has an RMS magnitude around 1 ps [9]. A BER of 10^{-15} requires a margin of 8 standard deviations (e.g. 8 ps) on either side of the sampling time. This will close the sampling window at a bit rate of 60 Gb/s.

Random noise at the receiver is a larger concern. The thermal noise (V_n) due to the termination resistors is white, bandlimited by the receiver circuitry:

$$\sigma_{V_n}^2 = 4kTR\,f_c$$

where k is Boltzmann's constant, T is temperature, R is the resistance (typically 50 Ω), and f_c is the upper bandwidth limit in Hz. Assuming that the transmitter's voltage swing is limited to V_s and the resolution of the comparator is V_c, an approximate condition for having a vertically open sampling window is:

$$V_s|H(j\tfrac{\pi}{T})| - V_n > V_c$$

where $H(j\omega)$ is the channel's frequency response and T is the bit period. (This is a worst-case scenario in which a stream of alternating zeros and ones appears similar to a sinusoid at the Nyquist frequency $\omega_n = \frac{\pi}{T}$ at the receiver.) The maximum data rate according to this constraint is shown in figure 1-5; transmitter output swing is limited to a typical value of 400 mV.

The theoretical maximum bit rates computed by this simple model for PAM2 are lower than the bounds found in [23], but still higher than the data rates we are concerned with (10 Gb/s and below). Henceforth the effects of random noise will be ignored.

1.1.5 Crosstalk

Crosstalk is an undesired mixing between multiple channels, as shown in figure 1-6. Crosstalk causes BUJ because the disturbances often occur during transitions. It should be possible to cancel crosstalk by using parameterized analog filters to emulate and subtract out the undesired voltages [17]. However, the crosstalk

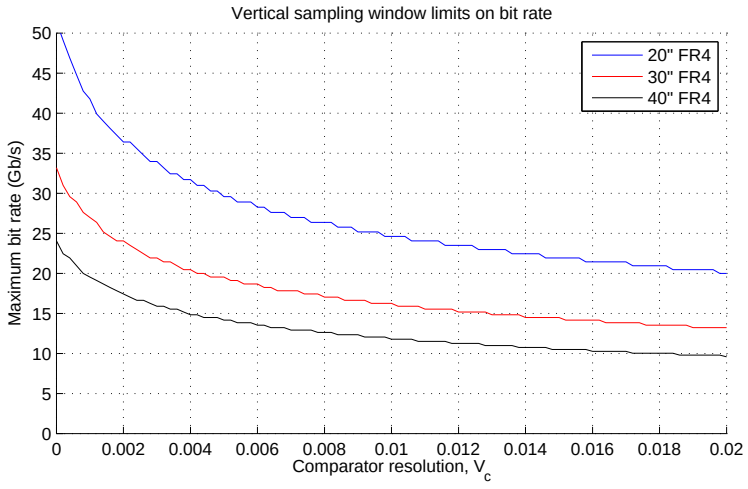

Figure 1-5: Noise-limited bit rates for a PAM2 link as a function of the comparator resolution V_c.

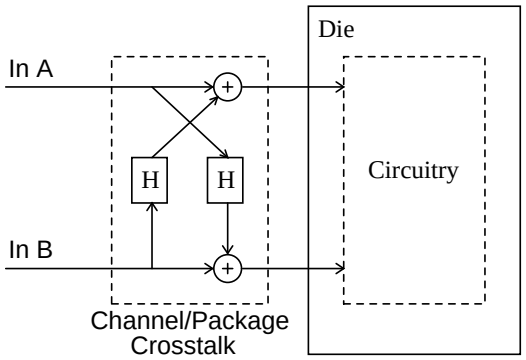

Figure 1-6: Block diagram of crosstalk between two channels.

cancellation systems reported so far have been highly application-specific (i.e. [22]). Inventing a general system for BUJ compensation is important but beyond the scope of this work.

1.2 Project summary

Finite channel bandwidth causes DDJ, which is a pervasive problem limiting serial link performance. Jitter compensation circuits reduce DDJ by introducing variable-width pulses into a bitstream before it is transmitted. A low-power integrated cell described below can be inserted into existing serial links, as shown in figure 1-7. The compensation scheme is based on the observation that channel transition delays can be estimated using the previously transmitted data.

The jitter distribution in the received signal can be condensed significantly by the compensator, which

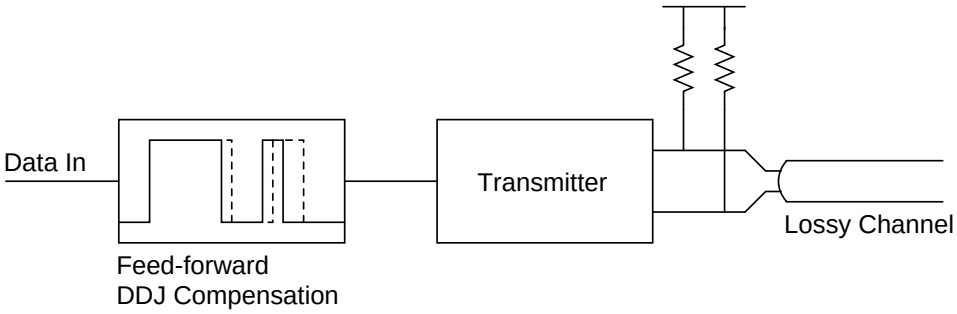

Figure 1-7: A serial link with feedforward DDJ compensation.

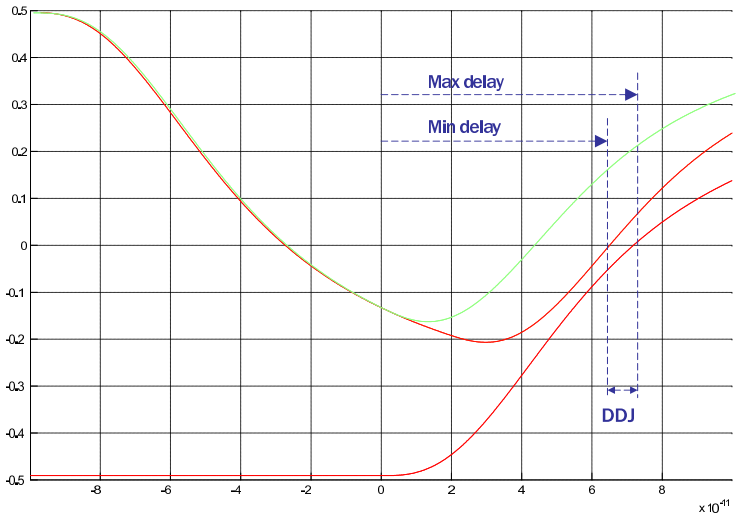

Figure 1-8: Introducing a delay at the transmitter reduces the data-dependent difference in received transition delays. The uncompensated trace from figure 1-3 (light green) is shown for comparison.

introduces data-dependent delays in the transmitted signal. In figure 1-8, the transmitted transition for the upper trace has been delayed by about 25 ps. This brings its received transition time much closer to that of the lower trace. Such a delay is an example of feed-forward jitter compensation. The effect of applying these delays over many bit periods is visible in the eye diagrams in figure 1-9.

Existing equalization techniques used to address channel loss are explained in the remainder of this section. The concept of asynchronous jitter compensation is explained in chapter 2, and the design of a digitally-controlled compensation circuit is presented in chapter 3. Simulation results and a discussion of the implications of this work follow the design review.

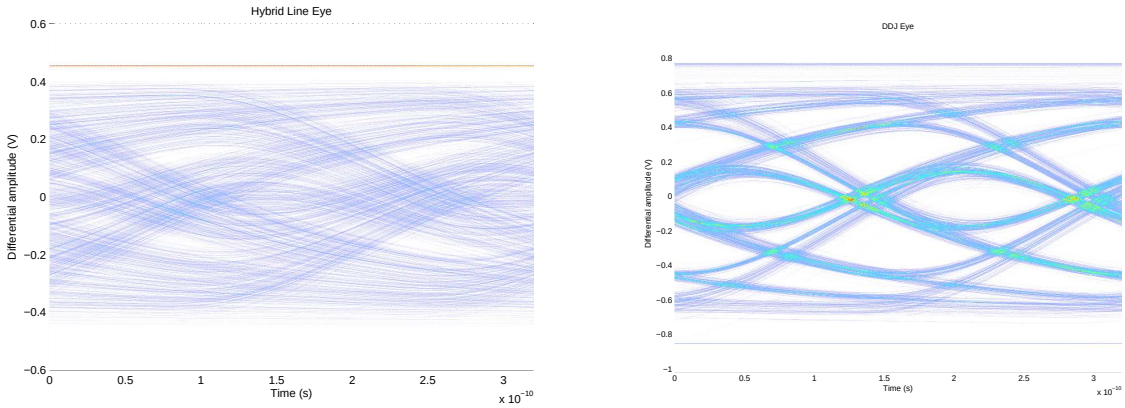

Figure 1-9: Eye diagrams for uncompensated (left) and compensated (right) 40” FR4 channels at 6.25 Gb/s.

1.3 Amplitude equalization techniques

Equalization (EQ) filters are often used to reduce jitter by introducing a high-frequency boost that compensates for the lowpass characteristic of the channel. One simple EQ is an RC shelving filter that diminishes the low-frequency component of the transmitted signal by a fixed amount, perhaps 6 dB below 3 GHz. Another is an FIR filter that subtracts a delayed version of the signal.

1.3.1 Transmit equalization

Transmitter EQ (also known as amplitude pre-emphasis) diminishes the jitter contribution of the channel by introducing exaggerated transitions. The modified pulse shape partially cancels out the ISI of closely packed bits. A typical implementation is shown in figure 1-10. These EQ circuits consume power proportional to the amount of high-frequency boost. A transmitter that steers a 16 mA tail current to swing 400 mV across a doubly-terminated 50 Ω channel would require 32 mA to do so with 6 dB of high-frequency boost. Despite this requirement, FIR transmit EQs are popular in serial links due to their simplicity and effectiveness.

1.3.2 Receive equalization

EQ can also be performed on the receive side to improve the eye opening while consuming less power than transmitter pre-emphasis. Receive EQs are generally linear filters with adjustable frequency responses.

An example of a receive EQ is shown in figure 1-11. The frequency response of the linear filter leading

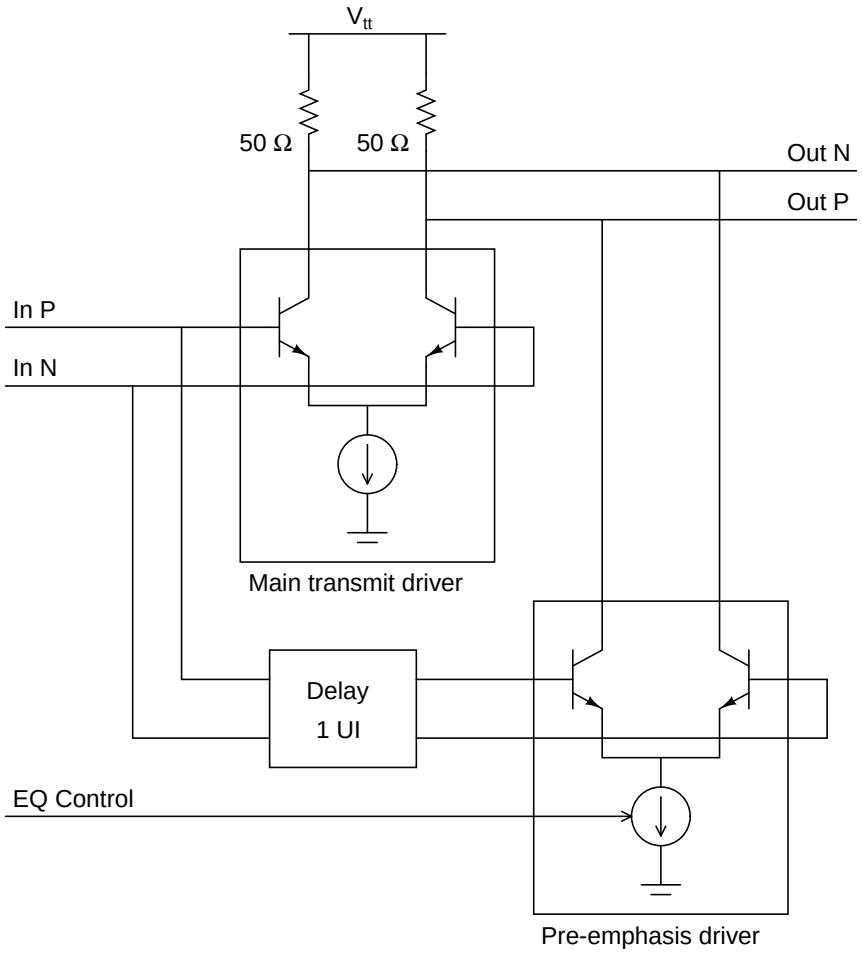

Figure 1-10: Transmit pre-emphasis using a 1-tap FIR filter.

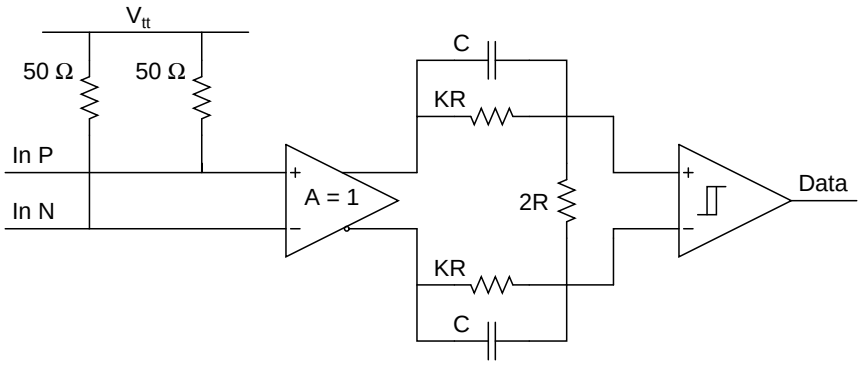

Figure 1-11: A simple buffered passive equalizer for receivers.

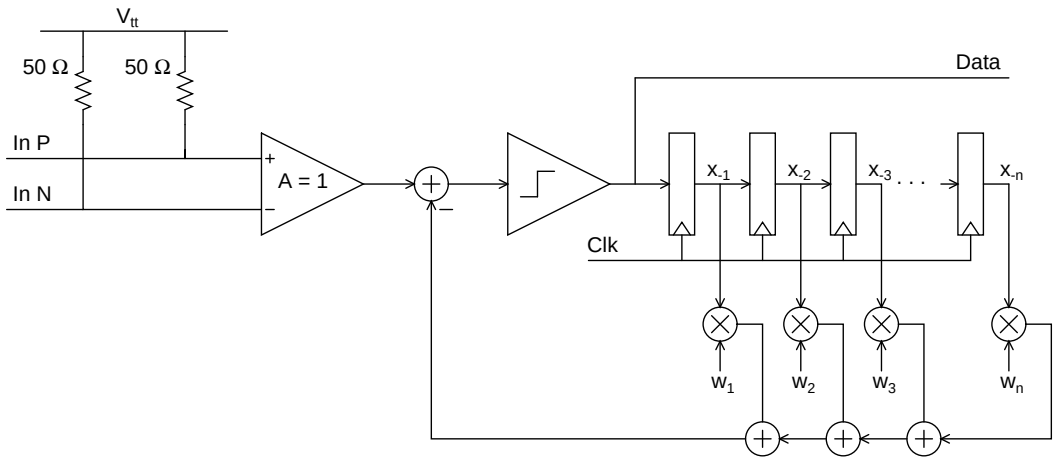

Figure 1-12: A DFE receiver.

to the comparator is

$$H(s) = \frac{1 + sKRC}{1 + K + sKRC}$$

This filter has a zero at $s = -\frac{1}{KRC}$ and a pole at $s = -\frac{1+K}{KRC}$. The DC swing of the signal is reduced by a factor of $\frac{1}{1+K}$; this de-emphasis can be compensated with an amplifier, although noise and interference are also amplified. Nevertheless, receive EQs of varying complexity are ubiquitous. A more complex and powerful type of EQ is described below.

1.3.3 Decision feedback equalization

Decision-feedback equalization (DFE) is a receive EQ technique that dynamically adjusts the equalizer's frequency response in order to emulate and subtract out ISI introduced by the channel [20]. A DFE circuit is sketched out in figure 1-12.

The weights w_i are updated periodically based on error information (typically using the sign-sign LMS algorithm). This circuit has the potential to dramatically reduce ISI, allowing proper data recovery when the unequalized eye is closed. However, the digital circuitry needed to update filter coefficients is complex; power consumption increases with the number of filter taps; proper adaptation requires a sufficiently exciting signal [21]; and a high-speed clock is required for the registers. These drawbacks motivate the use of simpler EQ techniques whenever possible.

The existence of a proper receive EQ cannot be assumed in applications where the ICs on each side of the link are not designed to cooperate with each other (as in modular networking equipment). Even if they

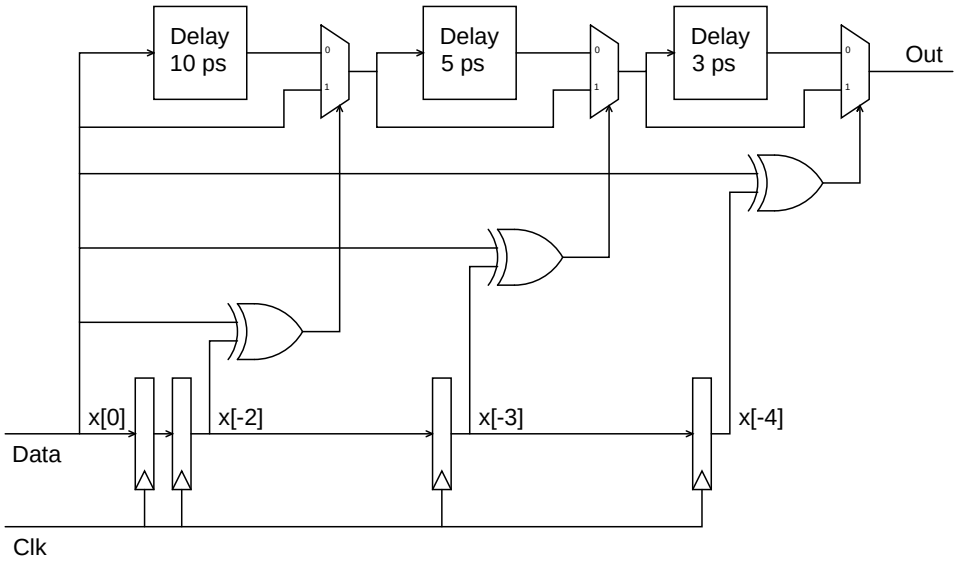

Figure 1-13: DDJ compensation device designed by Jim Buckwalter.

are, time-domain compensation techniques may still provide a useful power savings.

1.4 Phase equalization techniques

The term "phase equalization" refers to an equalization technique that does not alter the amplitude of the transmitted signal. Useful phase equalization filters are not LTI systems. It will be helpful to review the existing technique for DDJ compensation before discussing how to improve it.

1.4.1 The Buckwalter scheme

Jim Buckwalter (while a student at Caltech) contributed the bulk of the existing efforts in time-domain jitter compensation, which he has called phase pre-emphasis or deterministic jitter equalization (DJE) [5]. His work is motivated by the observation that it may take less power to adjust the time placement of transitions, instead of increasing their effective amplitude. Buckwalter noticed that the transition delay introduced by a channel is strongly dependent on the most recent bits. His DJE scheme (shown in figure 1-13) includes a chain of N programmable delay lines, each of which can be bypassed by a multiplexer. The input bitstream is fed through registers that keep track of the last $N + 1$ bits. Each of the relevant bits (from bit 2 to bit $N + 1$) is XORed with the current bit (bit 0) in order to determine whether the corresponding delay line should be engaged. The delays are scaled to reflect the diminishing importance of bits transmitted in the past.

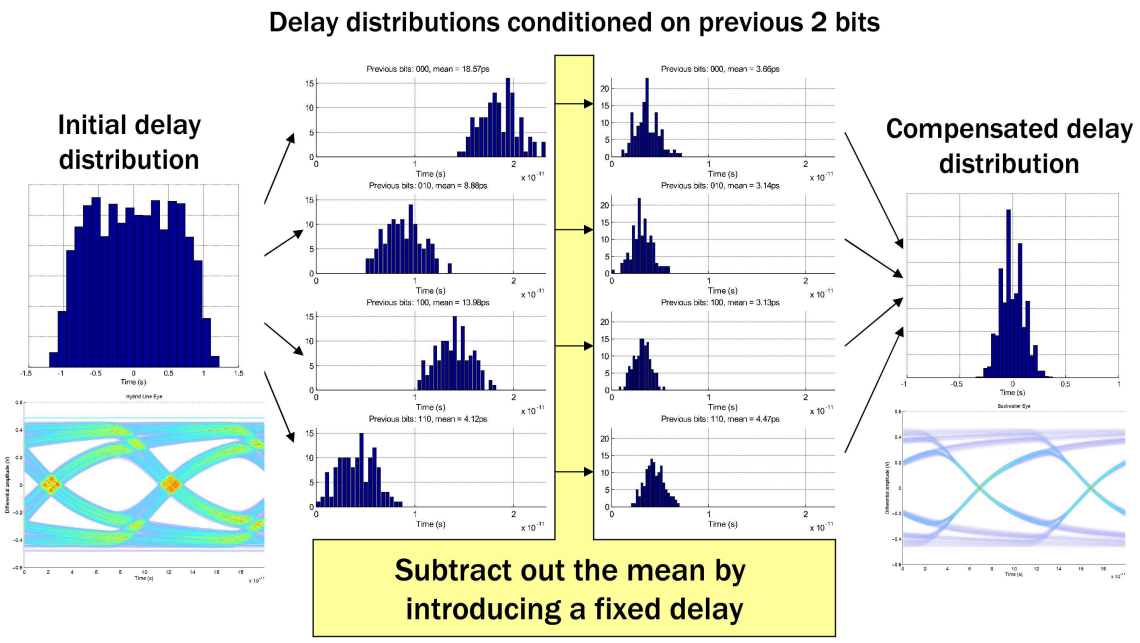

Figure 1-14: Jitter compensation viewed as an operation on jitter distributions.

1.4.2 Jitter histogram representation

Jitter can be interpreted as a probability distribution over transition delays. The goal of any jitter compensation technique is to narrow the extents of this distribution. The peak-to-peak DDJ is much more important than the variance, because low error rates are needed and DDJ is not nearly Gaussian.

The Buckwalter scheme decomposes the distribution of transition delays into 2^N narrower distributions, each representing one possible combination of previous bits. The delay lines subtract out the mean from each conditional distribution. When those conditional distributions are added back together, the resulting delay distribution may be narrower than the original, indicating a reduction in jitter. This process is shown in figure 1-14. Increasing N increases the number of conditional distributions and improves the potential cancellation accuracy, at a cost of circuit complexity and power dissipation.

1.4.3 Reported performance results

The Buckwalter scheme has been employed in several published circuit designs. Table 1.1 summarizes the measured performance of those circuits.

We will see if similar results can be achieved using an asynchronous, analog approach to DDJ compensation. The goal is to come up with an improved tradeoff between jitter, vertical eye opening, and power consumption in a variety of link scenarios.

			Jitter performance			
Date	**Process**	**Bit rate**	**Before EQ**	**After EQ**	P_D	**Source**
Oct. 2004	SiGe BiCMOS	10 Gb/s			35 mW	[3]
Sep. 2005	0.13 μm CMOS	5 Gb/s	86 ps p-p	41.33 ps p-p	40 mW	[4], [7]
Sep. 2005	0.13 μm CMOS	10 Gb/s	50 ps p-p	35 ps p-p	40 mW	[4], [7]
Jun. 2006	90 nm CMOS	6 Gb/s	16.15 ps RMS	10.29 ps RMS	6 mW	[6]

Table 1.1: Reported DDJ compensation circuit parameters and performance.

Chapter 2

A DDJ Compensation Scheme

This chapter proposes an architecture for asynchronous DDJ compensation. Before examining the theory behind this architecture, let us define several variables of interest.

- x_i: A sequence of bits, where each $x_i \in \{0, 1\}$.
  x_0 will be referred to as the current bit, whereas x_{-1}, x_{-2}, ... are the previous bits.
- $\mathcal{A}$: An alphabet of symbols mapping bit sequences to voltage values, e.g. $\mathcal{A}(0) = -1$, $\mathcal{A}(1) = 1$.
- $x_u(t)$: An uncompensated digital signal (the continuous-time version of x_i) with uniform transition times:

$$x_u(t) = \sum_{i=-\infty}^{\infty} \mathcal{A}(x_i) \left[u(t - iT) - u(t - (i + 1)T)\right]$$

- $h(t)$, $H(j\omega)$: The impulse response and frequency response of the channel between the transmitter and receiver. The step response is $s(t)$.
- d_i: A sequence of transition delays caused by the channel.
  If $x_u(t)$ is transmitted, d_i is the difference between the ith bit transition times of $x_r(t)$ and $x_u(t)$.
  Estimates of the delays are denoted by $\hat{d}_i$.
- $d(t)$: The transition delay caused by the channel (a continuous-time analog of d_i).
- $x_c(t)$: A digital signal with DDJ compensation applied to alter the transition times:

$$x_c(t) = \sum_{i=-\infty}^{\infty} \mathcal{A}(x_i) \left[u(t - iT + \hat{d}_i) - u(t - (i + 1)T + \hat{d}_{i+1})\right]$$

- $x_r(t)$: The received voltage signal:

$$x_u(t) * h(t) \qquad \text{(without compensation)}$$
$$x_c(t) * h(t) \qquad \text{(with compensation)}$$

The key to *asynchronous* DDJ compensation is maintaining a continuous-time estimate $\hat{d}(t)$ of the channel's transition delay for a transition at any given time. This delay is cancelled by a variable delay line placed between $x_u(t)$ and $x_c(t)$.

2.1 Revisiting the Buckwalter scheme

The Buckwalter approach to jitter compensation is to introduce transition delays which are linearly dependent on the previous bits. These transition delays are controlled by digital logic. Two observations allow significant improvements to that approach:

1. A linear filter may be used to accumulate the appropriate delay for the entire history of the bitstream with no additional power consumption.
2. The desired transition delay depends on the continuous-time history of the bitstream, so the system can be run asynchronously. No clock or clock-recovery circuit is necessary.

In his thesis [5, p. 86], Buckwalter noticed a possibility: "Analog feedback could also be implemented without actually sampling the data to compensate the DDJ." It is possible that he did not pursue the analog approach because of circuit implementation issues. We will attempt it here after developing a correspondence between the digital and analog methods.

2.1.1 Linear system interpretation

Buckwalter's deterministic jitter equalizer (DJE) predicts transition delays using a discrete linear model. For each incoming bit x_0, the corresponding transition delay is estimated:

$$\hat{d_0} = \mathbf{d}^\top (x_i \oplus x_0) + D$$

where $\mathbf{d}$ is a vector of delay coefficients and D is a constant propagation delay. The $\oplus$ symbol refers to an XOR operation: the delays in $\mathbf{d}$ are introduced into $x_c(t)$ for each previous bit that differs from the current bit.

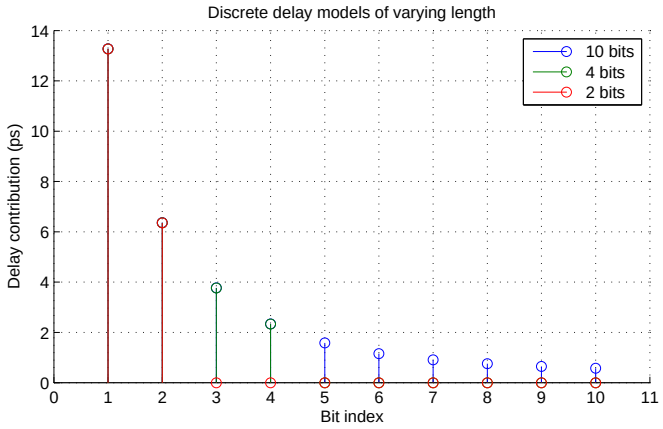

Figure 2-1: Delay coefficient vectors of varying length for a 15" FR4 channel at 10 Gb/s.

The coefficients in $\mathbf{d}$ can be estimated through SPICE transient simulations using a pseudorandom binary sequence (PRBS) for x_i. After thresholding $x_r(t)$, the sequence of delays d_i can be computed and regressed against x_i. The result of this operation is shown in figure 2-1. The indices i are plotted in reverse order; coefficients shown farther to the right on the graph refer to bits farther in the past. The coefficients are independent of the model length. Implementing each coefficient requires additional circuitry, which is traded off against the diminishing returns in compensation accuracy.

The delay coefficients change when the channel's frequency response changes. To model the frequency response of typical FR4 traces using SPICE simulation tools, a hybrid line model [18] splits the incident and reflected waves at each end and uses RLC ladders to approximate skin effect and dielectric loss. Figure 2-2 shows the delay coefficients for a few different channels represented by this model. The coefficients vary significantly, so all of the delay lines in a Buckwalter DJE need to be adjustable. (This can be accomplished by capacitively loaded inverters with an adjustable tail current.)

2.1.2 Interpolating delay coefficients

Figures 2-1 and 2-2 showed delay coefficients computed from a 10 Gb/s transient simulation. The estimated transition delay is based on recent bits x_i; given that $\mathcal{A}$ is linear, it is also a linear function of the uncompensated voltage signal $x_u(t)$ at regularly spaced time intervals like $x_u(iT)$, $x_u((i+\frac{1}{2})T)$, etc. These coefficients could conceivably be recomputed for different values of T, as the DDJ distribution varies with bit rate.

Passing any signal $x(t)$ through a linear system with impulse response $h(t)$ results in the convolution of

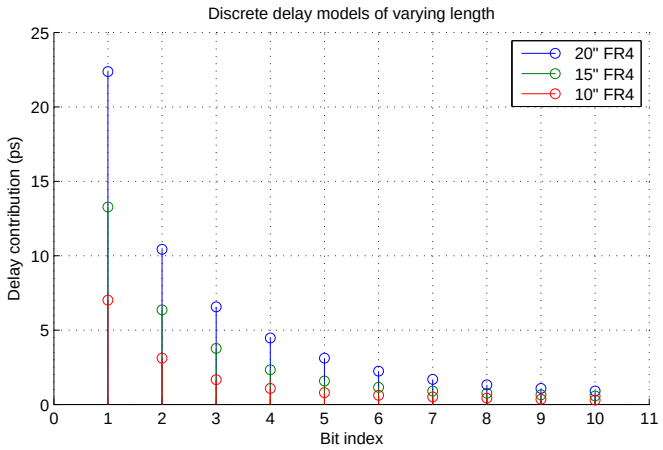

Figure 2-2: Delay coefficients compared for 10”, 15”, and 20” long FR4 channels at 10 Gb/s.

the two functions:

$$\begin{aligned} y(t) &= x(t) * h(t) \\ &= \int_{-\infty}^{\infty} x(\tau)h(t-\tau)d\tau \end{aligned}$$

If $x_u(t)$ is an input and the transition delay of the channel ($d(t)$) is a desired output, then the delay coefficients suggest the impulse response of the linear system that we need to calculate $d(t)$. Our attention now shifts to computing this continuous-time function, along with a parameterized set of approximations that can be implemented using analog circuits.

2.2 Characteristic delay

The *characteristic delay* function defined here is a measure of the transition delay introduced into a digital bitstream by fixed-amplitude impulses in the past. It is a continuous-time coefficient vector for the linear model given above. The frequency response of a channel can be transformed into the characteristic delay, creating a useful abstraction for simulations and discussions of DDJ behavior.

In [11], Hajimiri et al. invoked a similar concept to explain the phase noise of oscillators in terms of their impulse sensitivity function (ISF). The ISF was defined as the phase deviation in an oscillator output due to an impulse at some input node. Unlike ISFs, characteristic delay functions are not periodic; they represent the sensitivity of a single transition time to the entire history of a bitstream. Also, the delay is not integrated over a series of transitions. Instead, the characteristic delay function models the channel’s

"memory" of previous transitions.

2.2.1 Definition

The characteristic delay of a PAM2 serial link is a function that can be convolved with a bitstream to obtain the transition delays $d(t)$. Typical channels are symmetrical: rising and falling transitions behave identically. This means that the transition delays on rising transitions (denoted by $d^+(t)$) and falling transitions ($d^-(t)$) can be computed using the same function. This function is the characteristic delay $c(t)$, which satisfies

$$d^+(t) = D - x(t) * c(t)$$
$$d^-(t) = D - \overline{x}(t) * c(t)$$

where $x(t)$ is a digital signal at the input end of the channel and $\overline{x}(t)$ is its complement. From now on we will refer to a single delay function $d(t)$, which has the value of $d^+(t)$ when the current bit is 0 and $d^-(t)$ when the current bit is 1.

The discrete series of transition delays imposed on a bitstream with clock period T is $d_i = d(iT)$. In a DDJ compensator, we start with the uncompensated bitstream $x_u(t)$ and complement the estimated delays:

$$x_c(t) = x_u(t - (D - \hat{d}(t)))$$

If $d(t) \approx d(t + d(t))$, then the transition delay estimate $\hat{d}(t)$ can be computed accurately from the uncompensated bitstream $x_u(t)$, even though the compensated bitstream $x_c(t)$ is the one seen by the channel. The important implication for DDJ compensator design is that it is possible to run the compensator open-loop. The delay errors are mild when the delays are small relative to the decay time of the characteristic delay function.

2.2.2 Computation and fitting

In order to calculate the characteristic delay of a channel, assume that the transition delay is a linear function of the transmitted signal.[1] Also assume that there are only 2 possible symbols ("0" and "1") and that a threshold is placed halfway between the symbols without hysteresis. If a step in the input occurs at time $t = 0$, the threshold crossing time is $D = s^{-1}(\frac{1}{2})$, where $s(t)$ is the channel's unit step response. When an impulse at time $-t$ is added to this input, the tail of the channel's impulse response will bump up the

[1] This is not true, but we will show in section 2.4 that the nonlinearity is usually negligible.

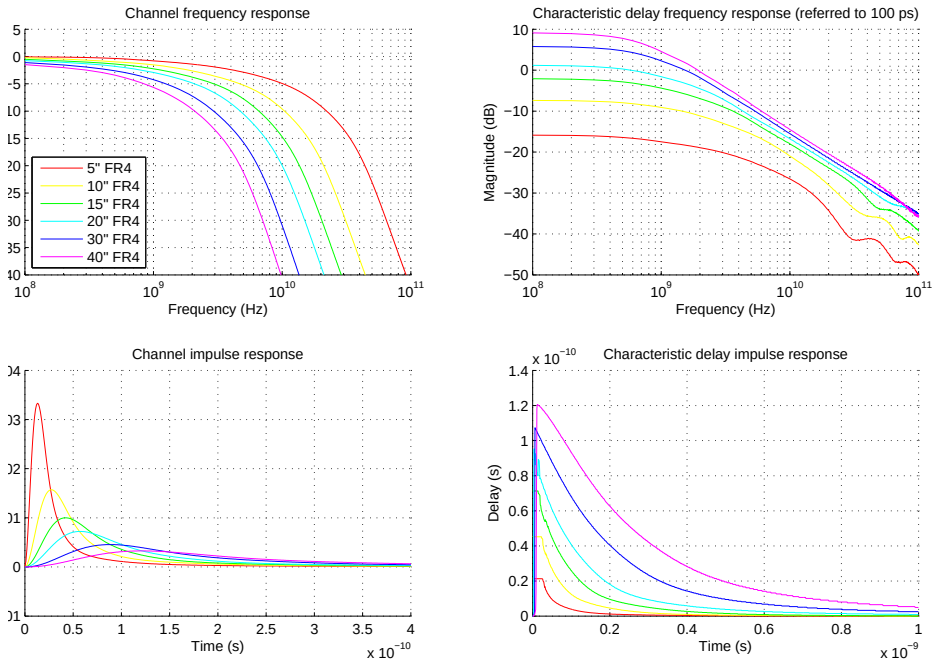

Figure 2-3: Channel responses (left) and the corresponding characteristic delay responses (right); in the frequency domain (top) and time domain (bottom).

step portion of its output, reducing the transition delay to $D - c(t)$. As the impulse recedes into the past ($t \to \infty$), its contribution to the transition delay will diminish: $\lim_{t\to\infty} c(t) = 0$.

Within this space of stimulus signals, the function c(t) satisfies

$$c(t) = s^{-1}(\tfrac{1}{2} - h(t + c(t)))$$

It can be computed numerically using a simple iterative algorithm:

$$c_0(t) = 0$$
$$c_n(t) = s^{-1}(\tfrac{1}{2} - h(t + c_{n-1}(t)))$$

where, again, $s^{-1}()\dot{}$ is the inverse of the channel's step response.

The characteristic delay depends only on the frequency response of the channel. Examples of the correspondence between frequency response and characteristic delay function are shown in figure 2-3. As the channel becomes longer, the characteristic delay becomes larger and is weighted to lower frequencies, indicating that a longer segment of the bitstream history is relevant to each transition delay.

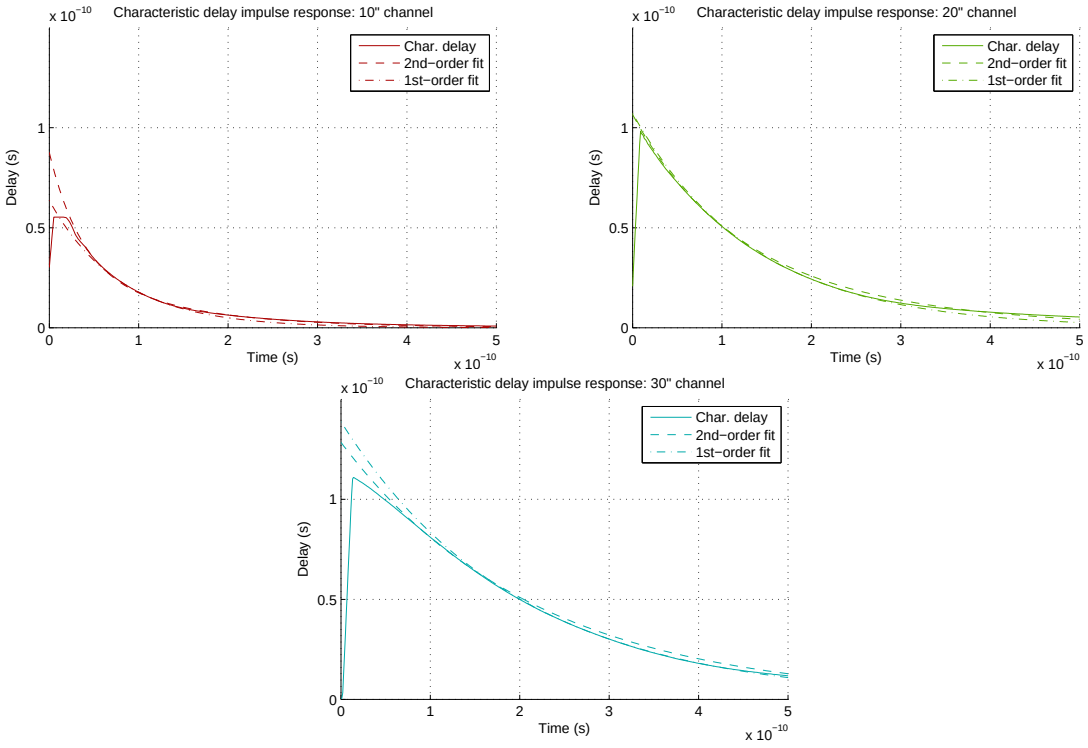

Figure 2-4: Characteristic delay functions for 10”, 20” and 30” FR4 channels. 1st- and 2nd-order fits to the impulse responses are also shown.

If represented as a voltage, the characteristic delay function is appropriate for controlling a voltage-controlled delay line operating on the bitstream. The characteristic delay function of an FR4 PCB trace appears to be well-approximated by a mixture of two exponential decays. Figure 2-4 demonstrates the use of RC filters to emulate the characteristic delay responses for a few common channel lengths.

2.3 Using a continuously variable delay line

The next challenge is to implement a transition delay proportional to the output of a characteristic delay emulator. If the sign of proportionality is positive, the delay line will introduce a jitter distribution similar to that of the channel. If the sign is negative, the jitter introduced by the delay line will cancel the jitter introduced by the channel.

Very accurate delay lines have been described in the literature, but the time needed to adjust the delay can be significant. In a DDJ compensator, the delay has to be adjusted within a single bit period. While several delay lines could be interleaved to avoid settling issues, it would be preferable to have a continuously variable delay line with a very fast adjustment capability.

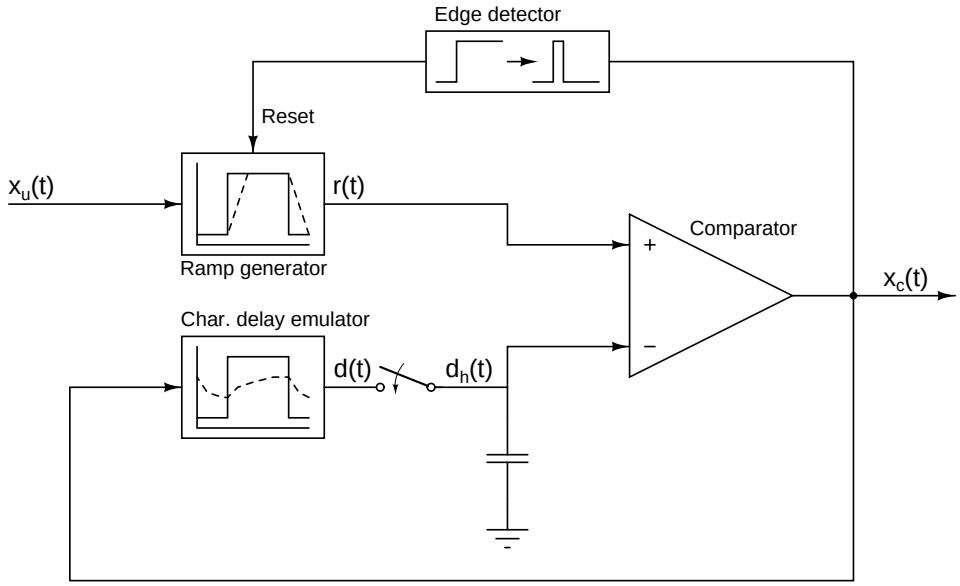

Figure 2-5: An architecture for asynchronous DDJ compensation.

2.3.1 Ramp-based implementation

One way to introduce delays in a digital signal is to limit its slew rate and threshold it again. This is the mechanism that causes propagation delays in digital circuits. The delays depend on the threshold voltage; offsetting the threshold causes duty-cycle distortion. Furthermore, a time-varying threshold can be used to provide a time-varying delay. If the slew rate is constant (as it is for a ramp signal), then the delay introduced is proportional to the difference between the threshold and input voltages. This technique can be used to generate very precisely adjustable delays [16].

Figure 2-5 shows an architecture for DDJ compensation based on this concept. A characteristic delay emulator (CDE) watches the transmitted signal $x_c(t)$ and produces the continuous-time delay estimate, $\hat{d}(t)$. When a transition arrives at time t_0, this function sampled and held at $d_h(t) = \hat{d}(t_0)$. The input bitstream is fed into a slew rate limiter, or ramp generator. The output of this ramp generator $r(t)$ is compared to the delay control signal $d_h(t)$ in order to generate delayed transitions.

Figure 2-6 shows an idealized transient simulation demonstrating how this architecture generates the appropriate delays for DDJ compensation. The delay control signal follows the input bitstream. The desired XOR function is accomplished because the comparator thresholds the difference $d_h(t) - r(t)$, where $r(t)$ carries the bitstream.

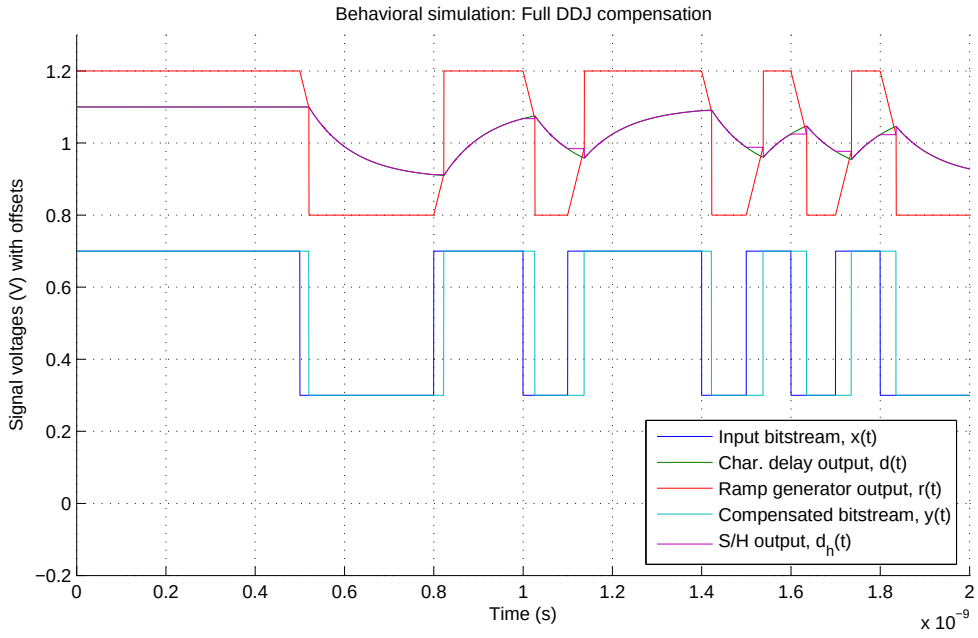

Figure 2-6: Plots of voltage signals within ramp-based DDJ compensator.

2.3.2 Simplifications

Implementing a circuit using the architecture of figure 2-5 would be daunting because of the very fast feedback that it requires:

1. The rise times of the signals must be very short (perhaps 30-50 ps). This makes it difficult to detect and act on edges.
2. The ramp generator has to be reset after each compensated transition in order to ensure that the delays are consistent.
3. Propagation delay through the comparator must be considered in the design of the characteristic delay emulator.

To avoid these complications, we try a simpler architecture (shown in figure 2-7) with the following modifications:

1. The ramp generator does not reset; instead, the output is clamped to a fixed range and the slew rate is made fast enough to sweep across this entire range in one bit period.
2. The characteristic delay emulator is driven by the uncompensated signal instead of the compensated one.

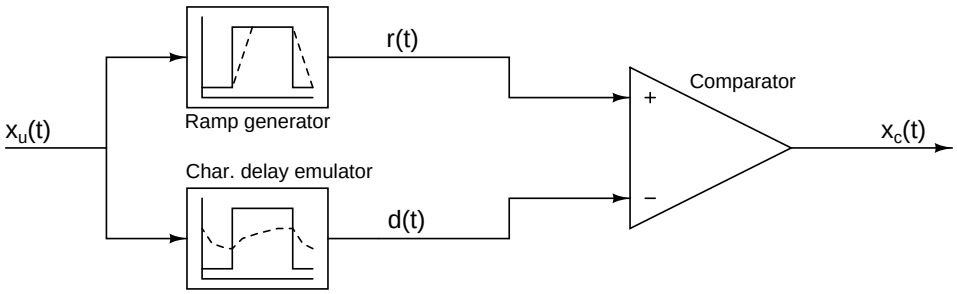

Figure 2-7: A simplified architecture for asynchronous DDJ compensation.

3. The output of the characteristic delay emulator is used as the delay control signal, and the sample-and-hold circuit is eliminated.

The first change limits the amount of delay, and hence the peak-to-peak magnitude of DDJ that can be compensated, to less than one bit period. The second and third changes reduce compensation accuracy, but the damage is minor because the delay control signal varies much more slowly than the other signals. Despite the changes, the two architectures are very similar conceptually. A behavioral simulation of the simple architecture (figure 2-8) produces a compensated output signal that is almost exactly the same as the complete architecture (figure 2-6). These simplifications were essential for a lightweight implementation of the circuitry.

2.4 Nonlinear methods

If desired, a scalar nonlinear function of the bitstream could be implemented using the scheme shown in figure 2-9, where neither "system 1" nor "system 2" is an integrator. Figure 2-10 illustrates the idea of comparing the outputs of two different filters. It will be shown below that such a scheme is not necessary even though channel-induced transition delays are not a linear function of the data being transmitted.

The PAM2 transmitted signal $x_u(t)$ has no DC offset and a rising transition at $t = 0$. We are interested in finding a way to anticipate and correct the transition delays $d(t)$ between $x_u(t)$ and $x_r(t)$. The characteristic delay has been proposed as a link between $x_u(t)$ and $d(t)$, but it might be invalid because of a nonlinear or time-varying correspondence.

Intuitively, there is no way that the transition delay could be linear for analog input signals because $d(t)$ is subject to the nonlinear shape of the channel's step response. What makes this problem much less obvious in context is the *constant amplitude* of digital signals, at least over the time intervals that matter for DDJ. We are only worried about adding signals of the same amplitude that contain pulses at different times. Even in

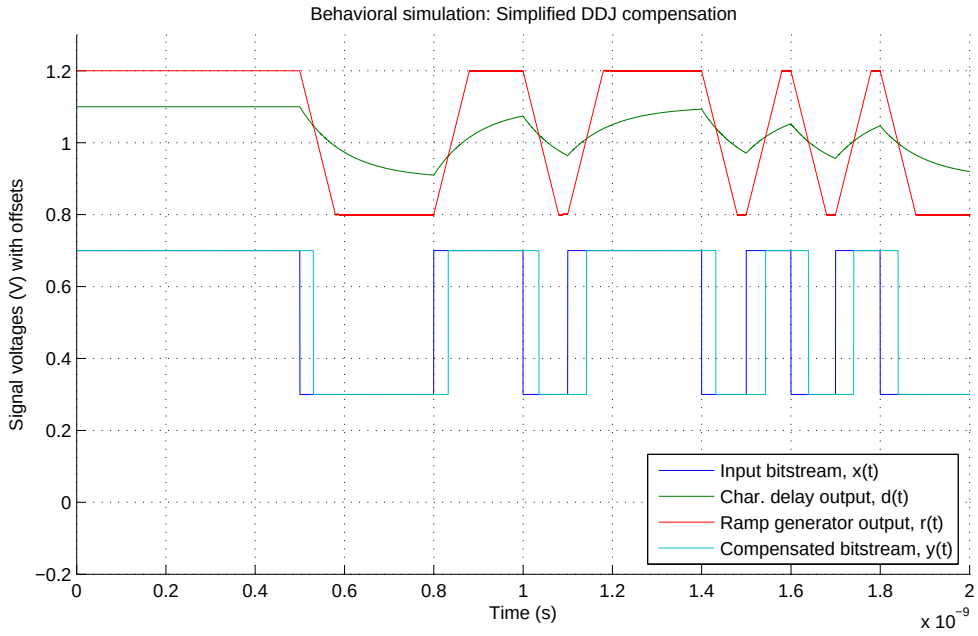

Figure 2-8: Plots of voltage signals within simplified DDJ compensator.

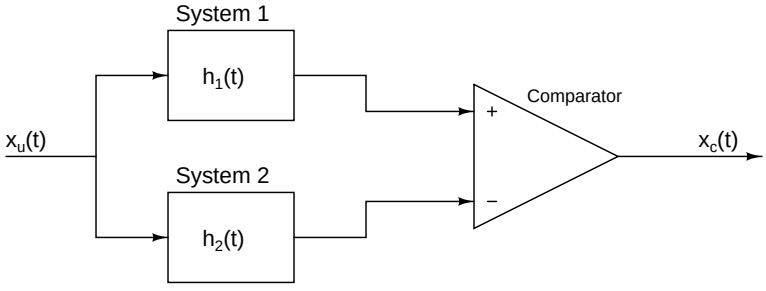

Figure 2-9: A generalized DDJ compensator to generate nonlinear delays.

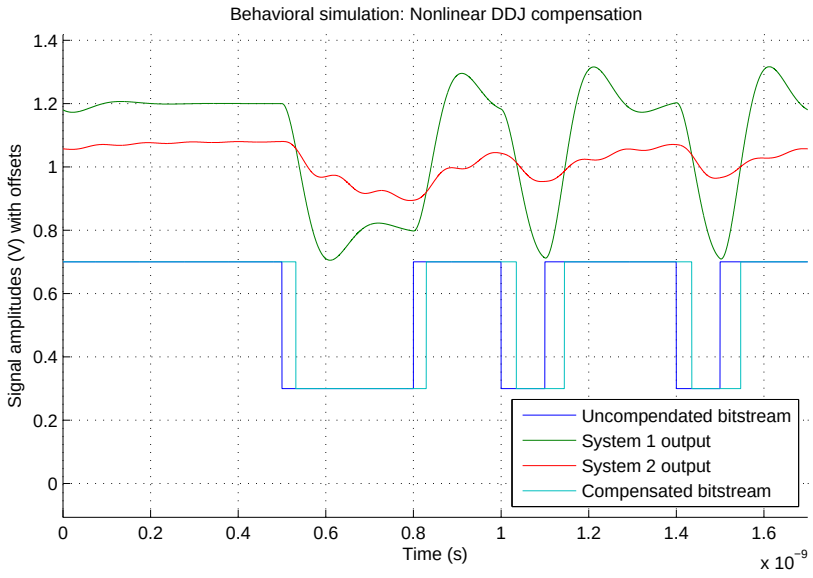

Figure 2-10: Plots of voltage signals within nonlinear DDJ compensator.

this situation the delay is nonlinear, but the error introduced by a linear approximation to $d(t)$ is acceptably small.

2.4.1 Nonlinearity in desired delays

Analytical example

Let the channel be a first-order lowpass filer: $h(t) = e^{-\frac{t}{\tau}}$. We will derive the linearity error analytically for this channel and then compute it numerically for more realistic channel models.

To test whether the first-order channel has a linear delay characteristic, try three different input histories:

$$x_{u1}(t) = u(t + T_1) - u(t + T_2)$$
$$x_{u2}(t) = u(t + T_2) - u(t + T_3)$$
$$x_{u3}(t) = u(t + T_1) - u(t + T_3)$$

Enforce $T_1 > T_2 > T_3$. This means $x_{u1}(t)$ and $x_{u2}(t)$ have non-overlapping pulses in the recent past, and $x_{u3}(t)$ is their sum.

A first-order system like an RC filter has only one state variable, which is the output voltage. Compute

the state of the channel at $t = 0^-$ in each case:

$$x_{r1}(0^-) = e^{-\frac{T_2}{\tau}} - e^{-\frac{T_1}{\tau}}$$
$$x_{r2}(0^-) = e^{-\frac{T_3}{\tau}} - e^{-\frac{T_2}{\tau}}$$
$$x_{r3}(0^-) = e^{-\frac{T_3}{\tau}} - e^{-\frac{T_1}{\tau}}$$

The transition delay in question is d_0. The threshold crossings occur when $x_r(t) = \frac{1}{2}$.

$$x_r(d_0) = 1 - \left[1 - x_r(0^-)\right] e^{-\frac{d_0}{\tau}} = \tfrac{1}{2}$$
$$\left[1 - x_r(0^-)\right] e^{-\frac{d_0}{\tau}} = \tfrac{1}{2}$$
$$d_0 = \tau \left(\ln 2 - \ln\left[1 - x_r(0^-)\right]\right)$$

The difference in delay time relative to the maximum of $D = \tau \ln 2$ is:

$$d_r = D - d_0$$
$$= \tau \ln\left[1 - x_r(0^-)\right]$$

It should be clear from this expression that while $x_r(0)$ is a linear function of $x_u(t)$, the relative transition delay is not. The exact relative delays are:

$$d_{r1} = \tau \ln\left[1 - e^{-\frac{T_2}{\tau}} + e^{-\frac{T_1}{\tau}}\right]$$
$$d_{r2} = \tau \ln\left[1 - e^{-\frac{T_3}{\tau}} + e^{-\frac{T_2}{\tau}}\right]$$
$$d_{r3} = \tau \ln\left[1 - e^{-\frac{T_3}{\tau}} + e^{-\frac{T_1}{\tau}}\right]$$

Numerical example

The three cases considered above were simulated with a 15" FR4 channel in addition to an RC filter. They are shown in figure 2-11 along with the step response. The delays are summarized in table 2.1.

If the transition delay were linear, then d_{r_3} would equal $d_{r_2}+d_{r_1}$, corresponding to $x_3(t) = x_2(t)+x_1(t)$ before the transition. The difference $\Delta t = d_{r_3} - (d_{r_2} + d_{r_1})$ is the linearity error. The simulated error of 0.15 ps is quite small. This analysis shows that a linear estimator based on the characteristic delay may be very accurate.

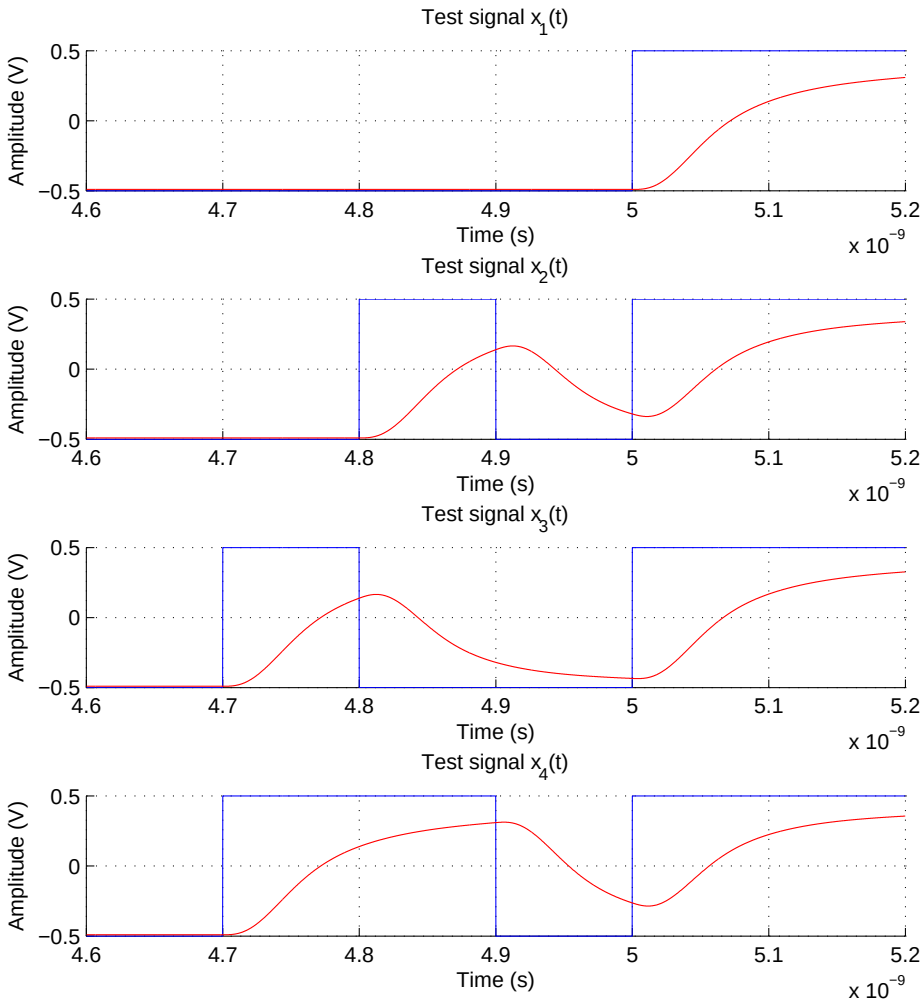

Figure 2-11: Test cases for determining the nonlinearity of the channel-induced transition delay.

Case	Signal	Transition delay	Relative delay
0	Step	71.8 ps	0 ps
1	Step + Pulse 1	61.2 ps	−10.53 ps
2	Step + Pulse 2	66.5 ps	−5.18 ps
3	Step + Both pulses	56.2 ps	−15.56 ps
	Add delays for cases 1 and 2	63.6 ps	−15.71 ps
Difference between expected and actual delays in case 3			*−0.15 ps*

Table 2.1: Results of simulating test cases using 15" FR4 channel.

It is conceivable that linearity errors could grow rapidly with DDJ magnitude. To compute an upper bound on this error, we will simplify the expressions by imposing a uniform clock. Let $x_{u1}(t)$ have a pulse two bit periods in the past, and let $x_{u2}(t)$ have a pulse three bit periods in the past. (The most recent bit must be 0 in order to have a rising edge.) To apply these changes, substitute $T_1 = 3T$, $T_2 = 2T$, $T_3 = T$ into the above formula. T only appears in exponents, so we can also let $\alpha = e^{-\frac{T}{\tau}}$.

$$\begin{aligned}
\Delta t = d_{r_3} - (d_{r_2} + d_{r_1}) &= \tau \ln \frac{1 - e^{-\frac{T_3}{\tau}} + e^{-\frac{T_1}{\tau}}}{\left[1 - e^{-\frac{T_3}{\tau}} + e^{-\frac{T_2}{\tau}}\right]\left[1 - e^{-\frac{T_2}{\tau}} + e^{-\frac{T_1}{\tau}}\right]} \\
&= \tau ln \frac{1 - \alpha + \alpha^3}{\left[1 - \alpha + \alpha^2\right]\left[1 - \alpha^2 + \alpha^3\right]} \\
&= \tau \ln \frac{1 - \alpha + \alpha^3}{1 - \alpha + 2\alpha^3 - 2\alpha^4 + \alpha^5} \\
&= \tau \ln \left[1 - \frac{\alpha^3 - 2\alpha^4 + \alpha^5}{1 - \alpha + 2\alpha^3 - 2\alpha^4 + \alpha^5}\right]
\end{aligned}$$

The above result is exact for a first-order channel, but still complicated. Introducing the approximations $\ln(1 + x) \approx x$ and $\alpha \ll 1$ (discarding higher order terms in α):

$$\begin{aligned}
\Delta t &\approx -\frac{\alpha^3 - 2\alpha^4 + \alpha^5}{1 - \alpha + 2\alpha^3 - 2\alpha^4 + \alpha^5} \\
&\approx -\frac{\alpha^3}{1 - \alpha} \\
&= -\frac{e^{-\frac{3T}{\tau}}}{1 - e^{-\frac{T}{\tau}}}
\end{aligned}$$

To help interpret this result, figure 2-12 shows the analytically computed error in unit intervals with respect to $\frac{T}{\tau}$, the ratio of the bit period to the channel time constant. The first-order approximation to a 15" hybrid line model has a -3 dB point of 2 GHz and $\tau = 80$ ps. At 10 Gb/s, $\frac{T}{\tau} = 1.26$ ($\alpha = 0.28$) and the linearity error for the first-order channel is $0.012T$, or 1.25 ps. This matches the linearity error computed by

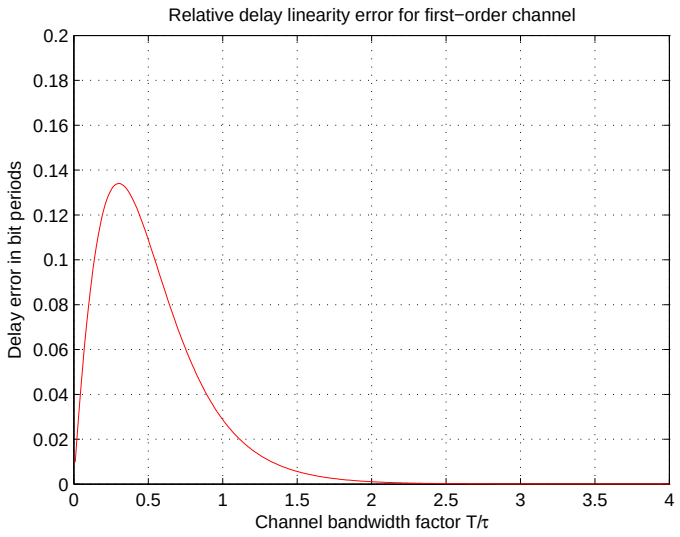

Figure 2-12: Deviation from transition delay linearity for a first-order channel.

a numerical simulation of that channel (1.37 ps). The simulated linearity error for the hybrid line, 0.15 ps, is even smaller because of the inertial characteristics of the line.

Note that the errors can become large if the channel is grossly bandlimited ($\frac{T}{\tau} < 1$). This is the regime of operation that could benefit most from DDJ compensation. The error reaches 5% of a bit period at a relatively low channel bandwidth: -3 dB at 1.3 GHz (corresponding to a 20" FR4 trace) for 10 Gb/s data. Linear DDJ compensation is still useful in this case due to the large overall DDJ magnitude.

2.4.2 Mitigating linearity errors

The linearity error is always negative if the step response is monotonic. This means that a system designed to compensate jitter using a linear transition delay estimate will always overcompensate transitions that require a lot of delay. Passing the estimated delay through a nonlinear function could help, because the most negative error will be incurred for the largest relative delays.

Figure 2-13 is a scatterplot of the exact versus approximated relative delays for a 25" long channel at 10 Gb/s. Note the positive curvature, indicating that edges expected to propagate down the channel more quickly are overcompensated. If a simple nonlinear function were applied to the delay, the general trend of the error could be flattened out. There is some variance in the actual delays; even an arbitrary pair of nonlinear systems (as in figure 2-9) could not eliminate all delay errors. Because of the recursive nature of the transition delay calculation, doing so would be akin to looking into the future.

The linear models (e.g. characteristic delay) for transition delay are accurate in most situations. Trying

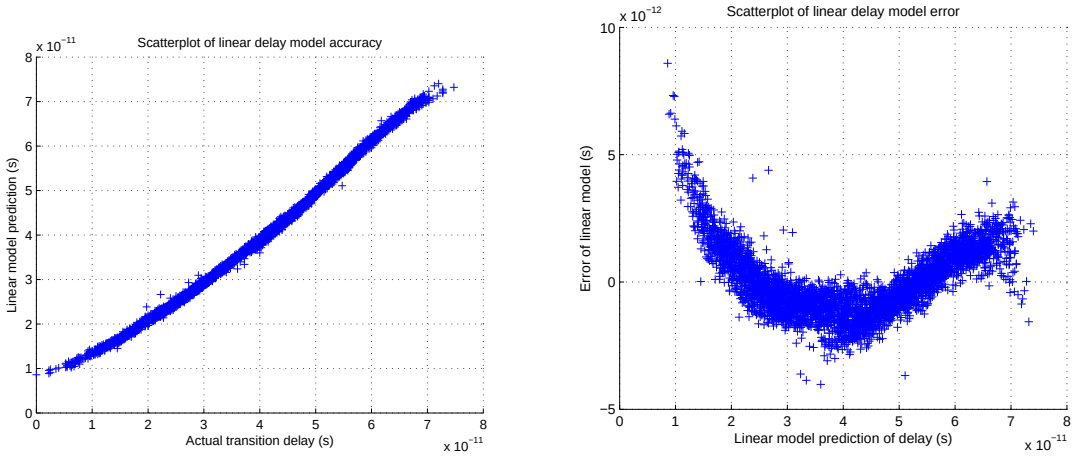

Figure 2-13: Scatter plots of the actual vs. predicted transition delays (left) and errors vs. predicted delays (right) for 25" FR4 channel at 10 Gb/s.

to implement an appropriate nonlinear CDE would likely result in diminishing returns, so we will defer them to future work.

2.5 Discussion

2.5.1 Compensating transmitter jitter

Investigations of DDJ in serial links led to some uncertainty over the exact meaning of "channel." At microwave frequencies the frequency response of the transmitter circuit, as well as the package parasitics, deviates noticeably from 1. Because the DDJ distribution caused by a channel depends on the frequency response, these components undoubtedly influence the received DDJ distribution. These effects are visible in the characteristic delay function. Figure 2-14 shows channel frequency responses and characteristic delays simulated with and without the addition of a second-order rolloff at 8 GHz.

In these simulations, the transmitter's output settles much more quickly than the channel's. This explains why its effect on the characteristic delay is much more pronounced in the first few unit intervals. To compensate the additional DDJ caused by a bandlimited transmitter, the high-frequency component of the CDE response would need to be boosted. This may be a useful technique for increasing fanout ratios, reducing power consumption, or otherwise extending the useful bit rates of slower circuit technologies (e.g. 0.35 μm). To maintain some generality in the more detailed simulations that follow, the transmitter will be considered ideal.

In general, jitter caused by any linear element in the channel can be compensated by adjusting the CDE.

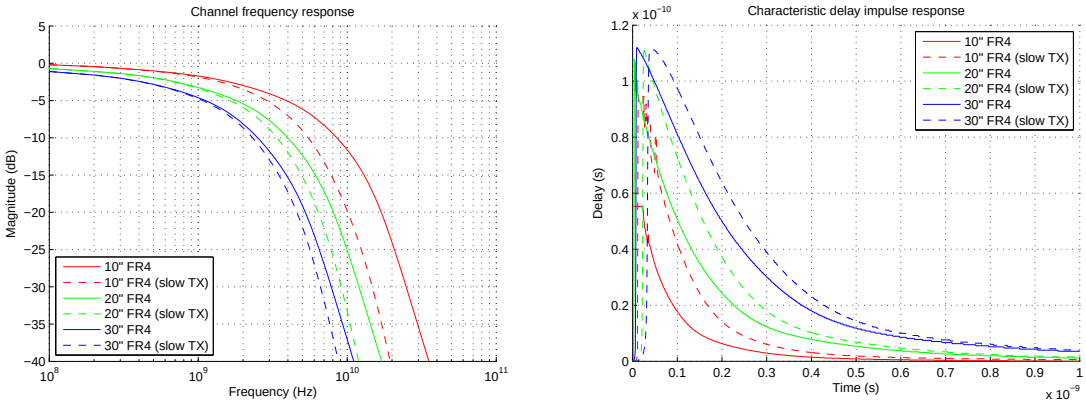

Figure 2-14: Frequency responses and characteristic delay functions for FR4 channels modeled with and without the effects of finite transmitter bandwidth.

The quality of compensation is limited by the complexity of the filters used in the emulator.

2.5.2 Summary

This chapter defined the characteristic delay function, a property of the channel which can be computed from the channel's frequency response. The characteristic delay function is the coefficient vector in a continuous-time linear model of transition delays. An architecture for DDJ compensation based on this model was presented. After observing several circuit design challenges, the architecture was simplified at some cost in theoretical compensation accuracy. Concerns about the inherent nonlinearity of DDJ motivated a more careful examination of the validity of the linear transition delay model. Analytical and numerical experiments quantified the expected compensation errors. Since those errors are acceptably small, we are prepared to proceed in implementing the compensator.

Chapter 3

Design Review

3.1 Top-level overview

A circuit block `ddj_comp`, designed for a 0.35μm BiCMOS process, performs asynchronous jitter compensation in a serial transmitter using the simplified architecture shown in figure 2-7. Its schematic is shown in figure 3-1. A differential input bitstream (`ip`, `in`) with approximately 200 mV swing is passed through an adjustable ramp generator and an adjustable CDE. The differential outputs of these two subcircuits are compared to produce a compensated bitstream (`op`, `on`). Two auxiliary subcircuits have been added to the basic architecture: a small delay cell placed in front of the CDE, and an adjustable current mirror for a set of current sources that track the delay sensitivity.

The following sections review the design of each subcircuit, explaining the tradeoffs that were needed to achieve effective compensation at 6 Gb/s and above despite the relatively slow process technology. NPN bipolar transistors have been used throughout the signal path because the other active devices are not fast enough.

The design assumes the existence of a 0.1 mA reference current into the drain of a 10 μm $\times$ 1 μm MOSFET. Current sinks driven from the `bias` line in the following schematics draw approximately 10 μA per unit $\frac{W}{L}$.

3.2 Adjustment mechanisms

As described in section 2.1.1, the characteristic delay function depends on the frequency response of the channel. While there is an infinite-dimensional space of possible frequency responses, most channels encountered in wireline applications share similar frequency response characteristics (see section 1.1.2). For

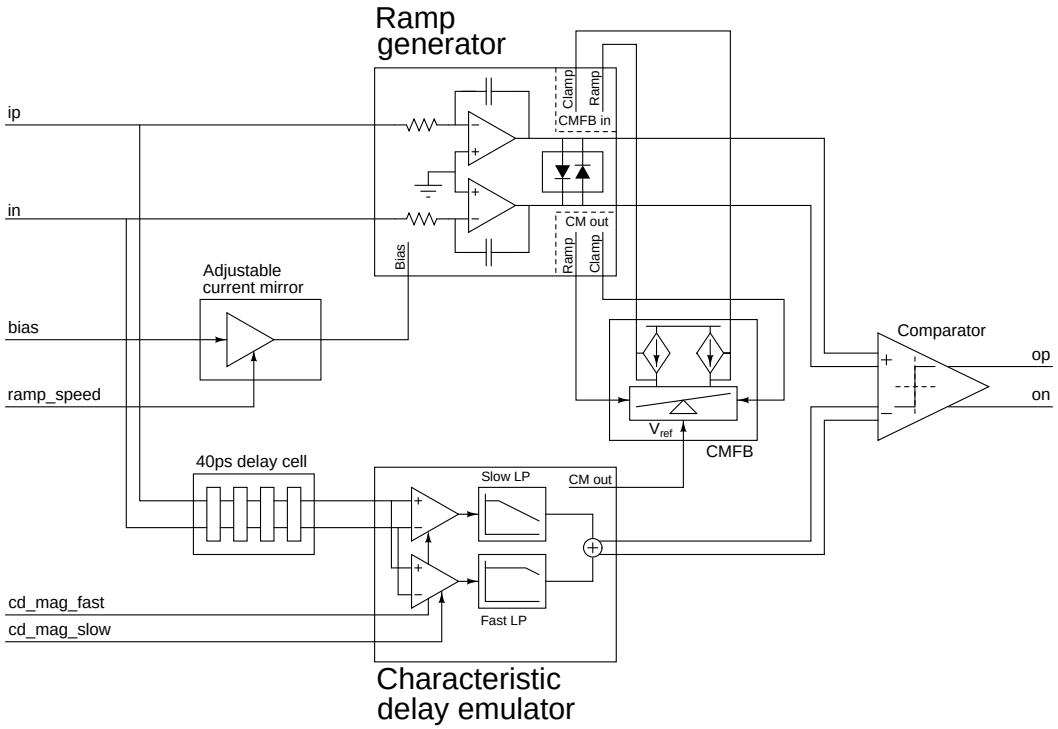

Figure 3-1: Top-level schematic of DDJ compensator.

copper traces on FR4 circuit boards, the characteristic delay function can be approximated by a sum of first-order lowpass filters. To simplify the circuitry even more, these lowpass filters have fixed corner frequencies; only their amplitudes are adjustable.

Remember that the ramp generator and comparator constitute a continuously variable delay line. The slew rate of the ramp generator output controls the sensitivity of this delay line. (If ramp generator had infinite slew rate, then the CDE output would be compared to a square wave, and no delay would be introduced on any transition.) Slower slew rates lead to larger delays, which are useful for compensating lossier channels.

The two CDE adjustments and one ramp generator adjustment are each represented by a 3-bit binary code. They are referred to as:

1. `cd_mag_slow[2:0]`: Voltage swing of the low-frequency component of the CDE output
2. `cd_mag_slow[2:0]`: Voltage swing of the high-frequency component of the CDE output
3. `ramp_speed[2:0]`: Slew rate of the ramp generator

Table 3.1 provides a rough guide for setting these digital codes based on the bit rate and channel length. As the channel gets longer, the overall amount of compensation should be increased and the CDE output

Situation		*Optimal settings*		
Bit rate	**Trace length**	`ramp_speed`	`cd_mag_fast`	`cd_mag_slow`
6.25 Gb/s	20”	5	2	1
6.25 Gb/s	30”	5	3	3
6.25 Gb/s	40”	5	5	7
10 Gb/s	15”	7	0	0
10 Gb/s	20”	7	1	1
10 Gb/s	25”	7	4	2

Table 3.1: Optimal settings for digital controls of DDJ compensator in nominal process conditions.

should be weighted towards low frequencies (matching the trend in characteristic delay shown in figure 2-3). This guide is based on simulation results; in a complete IC implementation, the adjustment settings will be stored in registers. They should be adjusted in their final application circuit with the aid of test equipment to minimize received jitter.

3.3 Characteristic delay emulator (CDE)

The CDE is a circuit providing a mixture of two first-order filters, as shown in figure 3-2. To fix the signal amplitudes at levels determined by the `cd_mag_slow` and `cd_mag_fast` settings, the input bitstream is first passed through two variable-amplitude limiters. The output of each limiter is individually filtered, then the outputs are summed. The resulting differential voltage is V_{out}:

$$h_1(t) = e^{-\frac{t}{R_1 C_1}}$$
$$h_2(t) = e^{-\frac{t}{R_2 C_2}}$$
$$V_{out} = V_0 \left[A_1 \text{ sgn } V_{in}(t) * h_1(t) + A_2 \text{ sgn } V_{in}(t) * h_2(t)\right]$$

3.3.1 Variable amplitude input limiter

The CDE’s input limiter arrangement is shown in figure 3-3. Each of the magnitude control codes is connected to a simple NMOS current DAC. The output swing of the limiter is the variable bias current multiplied by the fixed resistive load. Each DAC sinks between 20 to 160 μA. The load resistors are 900 Ω, resulting in $\pm$18 to $\pm$144 mV swing from each limiter.

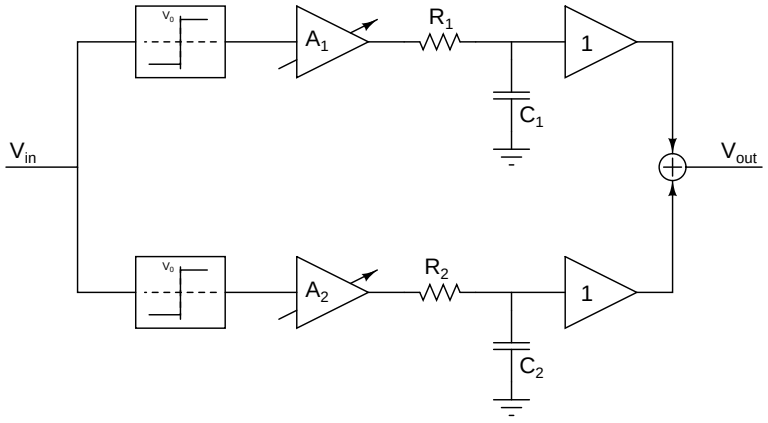

Figure 3-2: Concept of CDE filters.

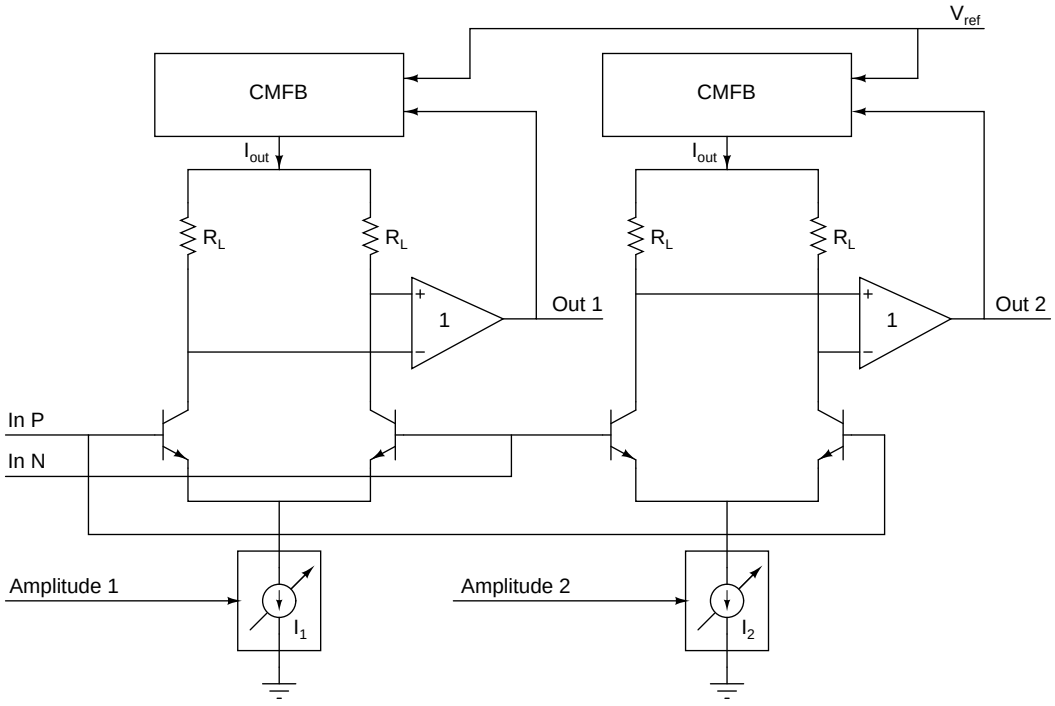

Figure 3-3: Dual variable-amplitude input limiter for CDE.

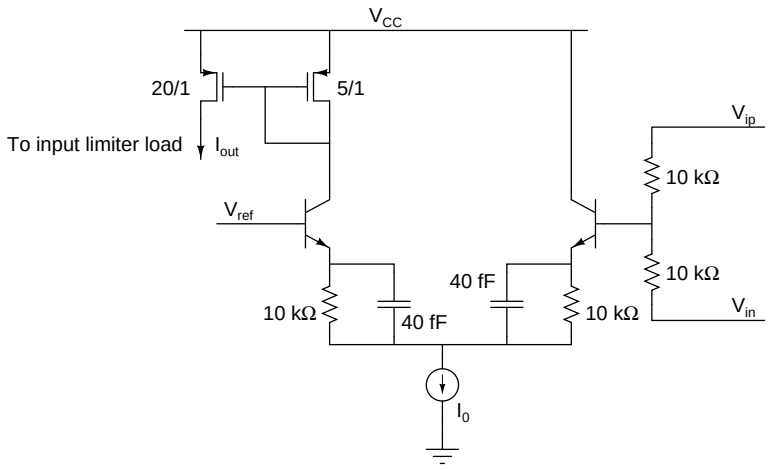

Figure 3-4: Simple common-mode feedback loop for CDE input limiters.

3.3.2 Common-mode feedback

Because the bias current varies over an eightfold range, pure resistive loading would shift the common-mode level of the limiter output significantly depending on the values of `cd_mag_slow` and `cd_mag_fast`. It would be possible to design a differential output stage to handle this common-mode swing. However, since linearity and frequency response accuracy are important here, emitter follower buffers and heavy resistive degeneration are used at the expense of voltage headroom. The output stage ends up having a narrow common-mode input range, outside of which either the amplifying transistors or the current sources will saturate.

Feedback is used to stabilize the common-mode level of the signals going into the output stage as shown in figure 3-4. This is nearly the simplest possible circuit that can be used for common-mode feedback (CMFB), with the addition of RC emitter degeneration to throw away unnecessary gain at low frequencies. CMFB challenges precipitated by the ramp generator design will be examined in more detail in section 3.5.

3.3.3 RC filters

The input limiters and output stage are configured as shown in the complete CDE schematic, figure 3-5. Each of the input limiter outputs is fed through a separate g_m stage with an RC filter at its input. The time constants of the two filters are approximately 50 ps and 300 ps. The output impedance of the buffers `qn6`, `qn7`, `qn10`, and `qn11` and the parasitic load capacitance are augmented with resistors `r25`, `r26`, `r7` and `r8`; extra capacitance (`c11` and `c14`) is needed for the slower pole. Emitter degeneration components reduce the gain of each section to approximately 1 and push the unwanted poles above 6 GHz. Resistors

r24 and r28, with opposing temperature coefficients, reduce the common-mode level of the output to suit the comparator. This level is sensed by resistors r29 and r30 so it can be used as a reference for the common-mode levels in the ramp generator.

Figure 3-6 shows a family of frequency responses for the CDE, swept across the 64 possible control codes (0 through 7 for each of the cd_mag_slow and cd_mag_fast components). There is some coupling at high frequencies due to parasitic capacitances in the layout, which is unimportant because the outputs are being mixed anyway. The filters' pole frequencies and limiter amplitudes were adjusted to cover the space of characteristic delay functions for FR4 channels 10–40" in length.

3.4 Ramp generator

3.4.1 Concept and implementation

The ramp generator, while conceptually simple, is the key to a successful analog DDJ compensator. Any jitter or nonlinearity in its output results in compensation errors. We also desire low power consumption: less than 1 mA. The desired behavior is achieved at 6 Gb/s and beyond using a circuit developed with two principles in mind:

1. Lightweight differential signal path with common-mode feedback only.
2. Very limited voltage swing.

A ramp is the integral of a step. When a step function of current is supplied to a capacitor, the capacitor's voltage follows a ramp. The differential arrangement of figure 3-7 accomplishes the desired slew-rate-limiting function of the ramp generator by simply clamping the capacitor voltage to a fixed range. The slew rate of this circuit is $\frac{dV_C}{dt} = \frac{I_0}{C_L}$. To maximize slew rate, C_L is composed only of parasitic capacitances. The current source I_0 can be adjusted to control delay line sensitivity; a typical value is 240 μA. Furthermore, the slew time is proportional to the voltage range V_W allowed by the clamp.

The output levels will drift if the source and sink currents are not matched. To prevent drift, the "CMFB" loads are PMOS current sources controlled by an external command. The circuitry that generates that command is described later in section 3.5.

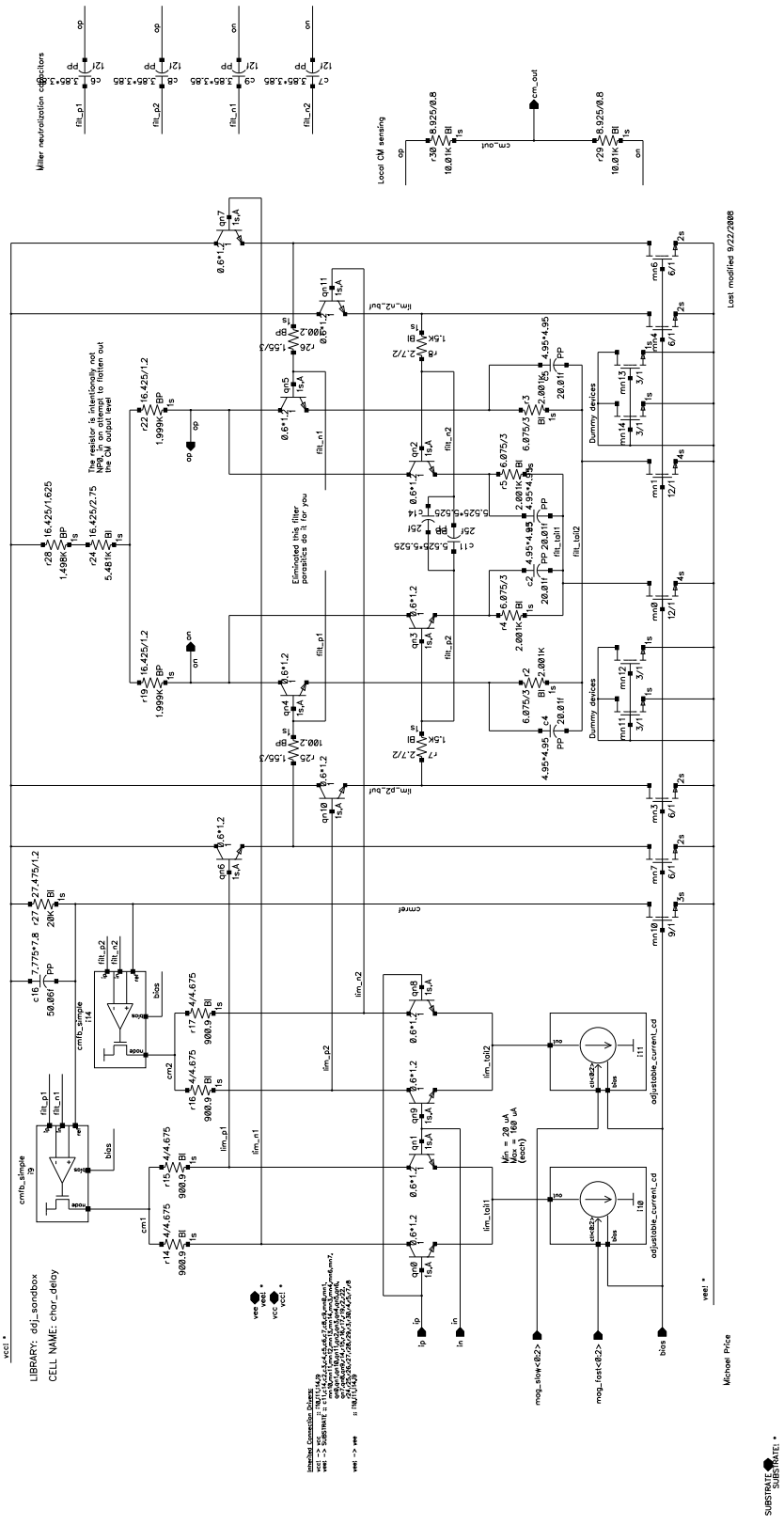

Figure 3-5: Complete schematic of characteristic delay emulator (CDE).

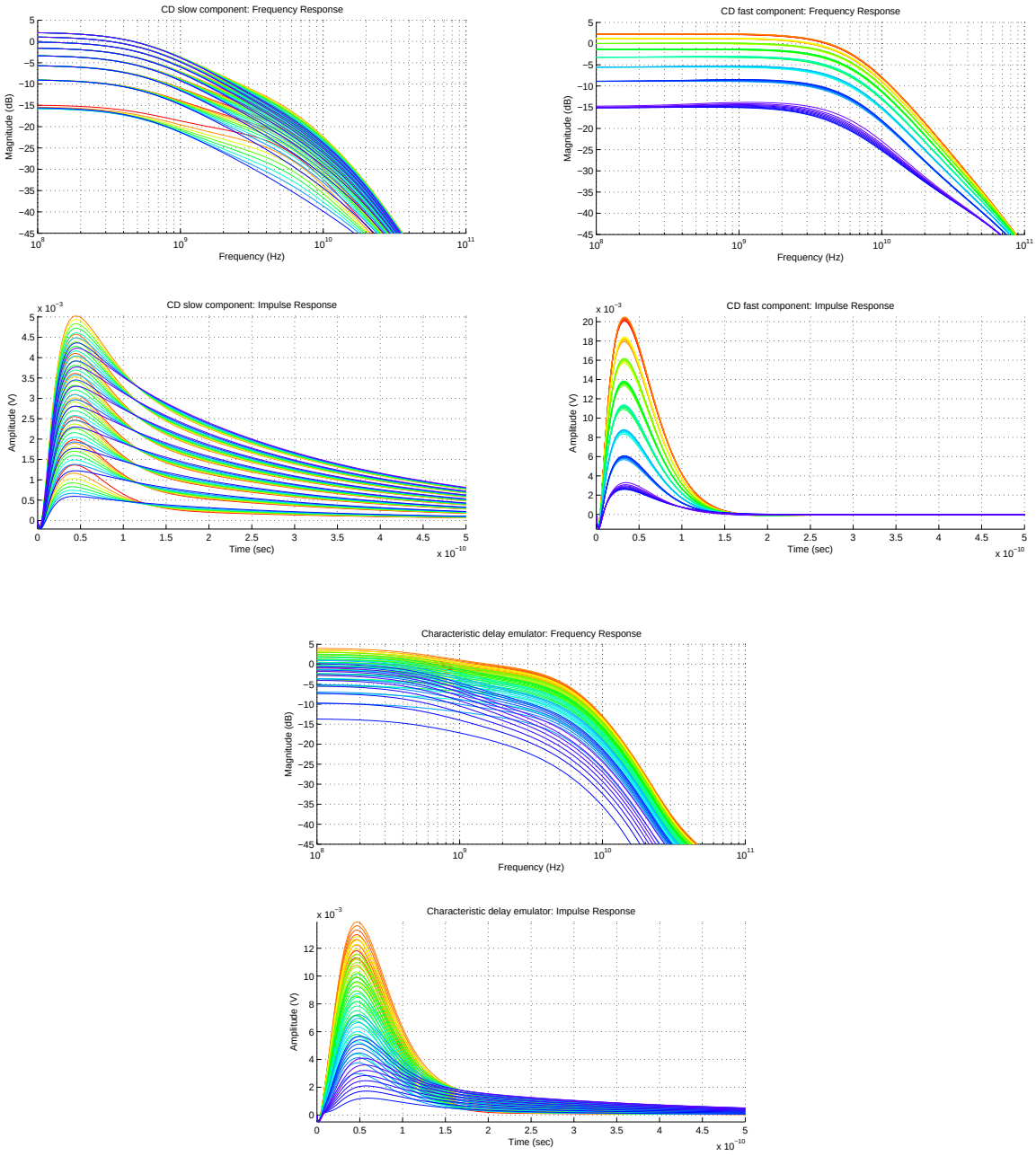

Figure 3-6: Effect of varying digital input codes on CDE response. Top left: “slow” component. Top right: “fast” component. Bottom: sum of both components.

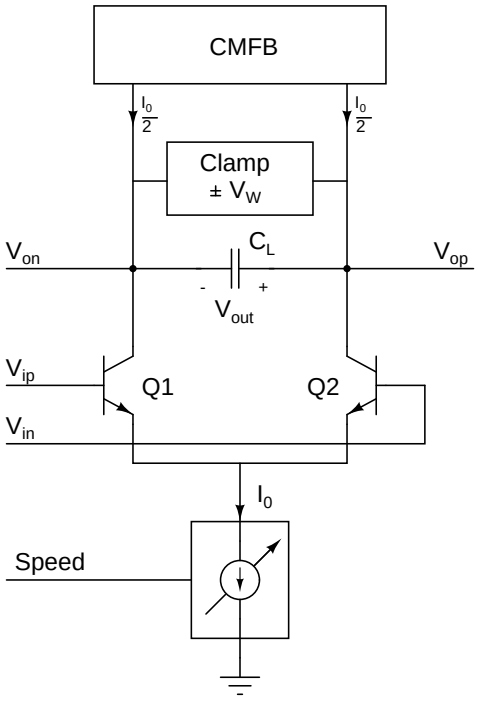

Figure 3-7: Concept of differential ramp generator.

3.4.2 Clamp circuit

The simplest differential voltage clamp is made with two diodes, as in the left side of figure 3-8. The window voltage V_W is computed as follows:

$$\begin{aligned} I_D &= I_S e^{\frac{qV_W}{kT}} \\ V_W &= \frac{kT}{q} \ln \frac{I_D}{I_S} \\ &= \frac{kT}{q} \ln \frac{I_0}{2I_S} \end{aligned}$$

Silicon diodes (or diode-connected transistors) of reasonable size would have a clamp range of around $V_W = \pm$ 700 mV. Schottky diodes and germanium diodes provide a lower voltage drop but are not available in the present IC process. This leads us to an active transistor clamp as shown in the right half of the figure. The output voltage V_{out} is amplified and level-shifted by the "clamp amplifier" devices `Q5` and `Q6`, driving the bases of the "clamp" devices `Q7` and `Q8`. `Q7` is turned on when V_{out} exceeds $+V_W$, and `Q8` is turned on when V_{out} exceeds $-V_W$. The exact value of the window voltage is determined by I_1, R_L, and the load current.

Instead of clamping to V_{BE} as diode-connected transistors would, this circuit clamps to V_{CE}. The active clamp presents an additional capacitive load, but is well worthwhile because of the reduced clamp range (window). Using the Ebers-Moll transistor model [10], we find the base [over]drive required to clamp to the desired $V_W = V_{BE} - V_{BC}$:

$$\begin{aligned}
I_C &= \alpha_F I_{SE} e^{\frac{qV_{BE}}{kT}} - I_{SC} e^{\frac{qV_{BC}}{kT}} \\
I_E &= -I_{SE} e^{\frac{qV_{BE}}{kT}} + \alpha_R I_{SC} e^{\frac{qV_{BC}}{kT}} \\
I_B &= -I_C - I_E \\
&= (1-\alpha_F) I_{SE} e^{\frac{qV_{BE}}{kT}} + (1-\alpha_R) I_{SC} e^{\frac{qV_{BC}}{kT}} \\
&= (1-\alpha_F) I_{SE} e^{\frac{qV_{BE}}{kT}} + (1-\alpha_R) I_{SC} e^{\frac{qV_{BE}}{kT}} e^{-\frac{qV_W}{kT}} \\
&= e^{\frac{qV_{BE}}{kT}} \left[(1-\alpha_F) I_{SE} + (1-\alpha_R) I_{SC} e^{-\frac{qV_W}{kT}} \right] \\
V_{BE} &= -\frac{kT}{q} \ln \left[\frac{(1-\alpha_F) I_{SE}}{I_B} + \frac{(1-\alpha_R) I_{SC} e^{-\frac{qV_W}{kT}}}{I_B} \right] \\
&= -\frac{kT}{q} \ln \left[\frac{I_{SE}}{\beta_F I_B} + \frac{I_{SC} e^{-\frac{qV_W}{kT}}}{\beta_R I_B} \right]
\end{aligned}$$

There is a negative correlation between the clamp range V_W and the base drive V_{BE}. A tight clamp range is desirable for low power consumption, but clamping the ramp output to less than 200 mV requires driving the clamp devices into hard saturation. The base charge grows rapidly in saturation, causing overshoot and settling tails on the clamped signal. A compromise clamp range of $V_W = 225$ mV avoids this problem. While the clamp range can be increased from this point if supported by proportionally higher bias current, this is not advisable because the ramp becomes more nonlinear.

There are several opportunities for nonideal behavior in the V_{CE} clamp circuit. As shown above, the V_{CE}–V_{BE} relation for a BJT in forward active operation depends on temperature and base current. In steady-state operation, the collector of `Q3` or `Q4` is effectively sandwiched between a PMOS current source and an NMOS current sink. Sweeping the base voltage upward brings V_W down through the linear regime and then into saturation; the desired V_W is close to the knee between those regimes. A difference between the source and sink currents shifts this knee around significantly, as shown in figure 3-9. This is a problem because the steady-state V_W changes drastically in the linear region, and transient performance changes drastically in the saturation region. The operating point of this circuit needs to be held steady in order for it to work.

One way to regulate the V_{CE} clamp range would be to introduce a small offset current at the base of

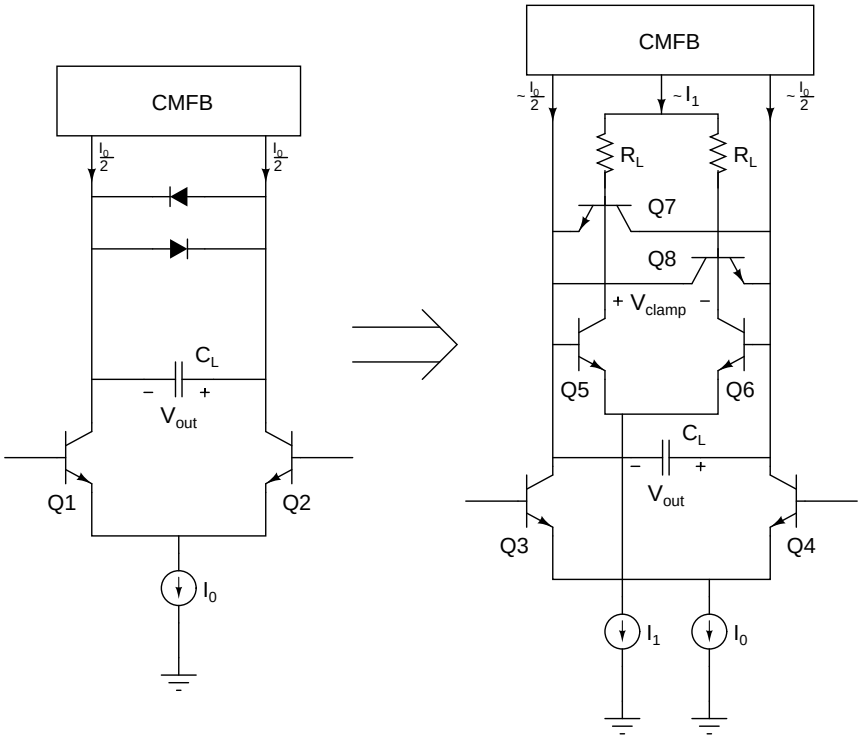

Figure 3-8: Diode-clamped (left) and actively clamped (right) ramp generator circuits.

the clamp device. The effect of this offset current would be similar to that of mismatched current source MOSFETs (see figure 3-10), providing an opportunity to cancel process and temperature variation. But, due to the sensitive nature of the clamp, its clamping range is better stabilized using common-mode hoopla.[1]

We will return to the hoopla circuitry momentarily. The complete schematic of the ramp generator is shown in figure 3-11. Note that the common-mode levels of the ramp output and the clamp base drive signals are sensed by resistors `r4`, `r5`, `r14`, and `r15` and fed to another subcircuit. As with the CDE, dissimilar resistors are placed in series to cancel the temperature dependence in the clamp amplifier's gain.

3.5 Common-mode feedback (CMFB)

CMFB is commonly used by necessity in high-gain amplifier stages [19]. The ramp generator, which is similar to a high-gain amplifier, relies on a nonstandard CMFB technique described here. The CMFB circuit `cm_force` has two tasks:

1. Keep the ramp generator output at a fixed common-mode level of approximately $\frac{V_{CC}}{2}$.

[1] Hoopla is defined by the Random House Dictionary as "bustling excitement or activity" or "commotion."

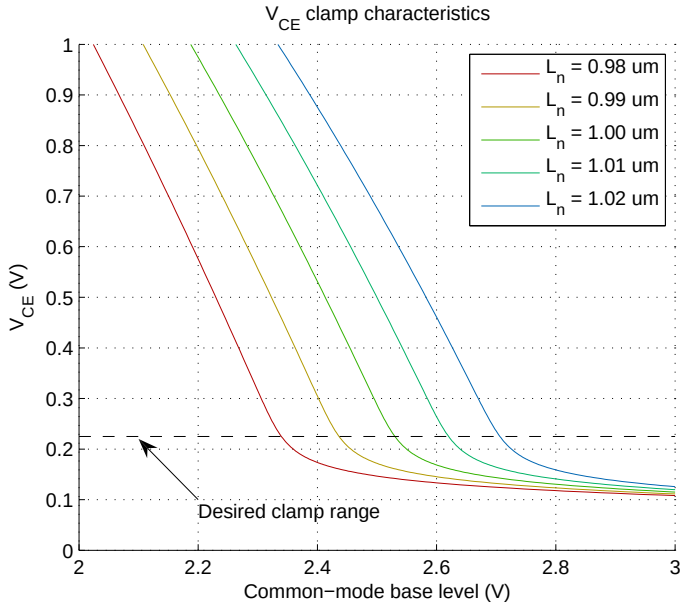

Figure 3-9: Effect of MOSFET current source length mismatch on the V_{CE} clamp range.

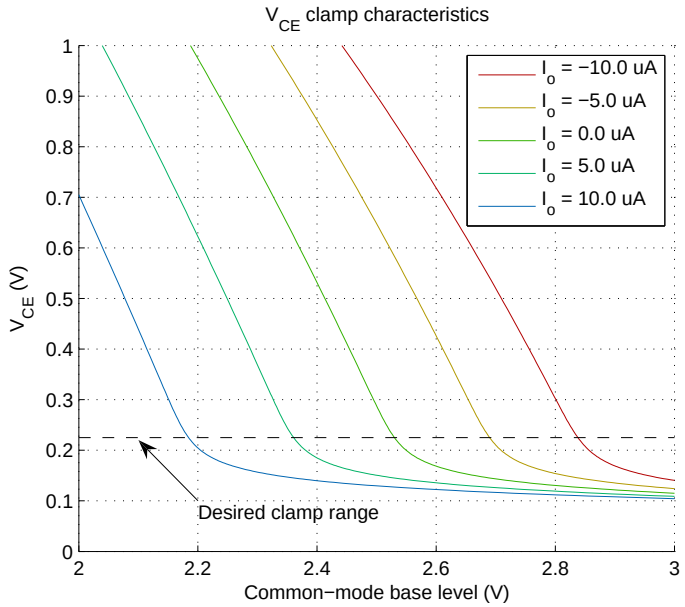

Figure 3-10: Effect of a base offset current on the V_{CE} clamp range.

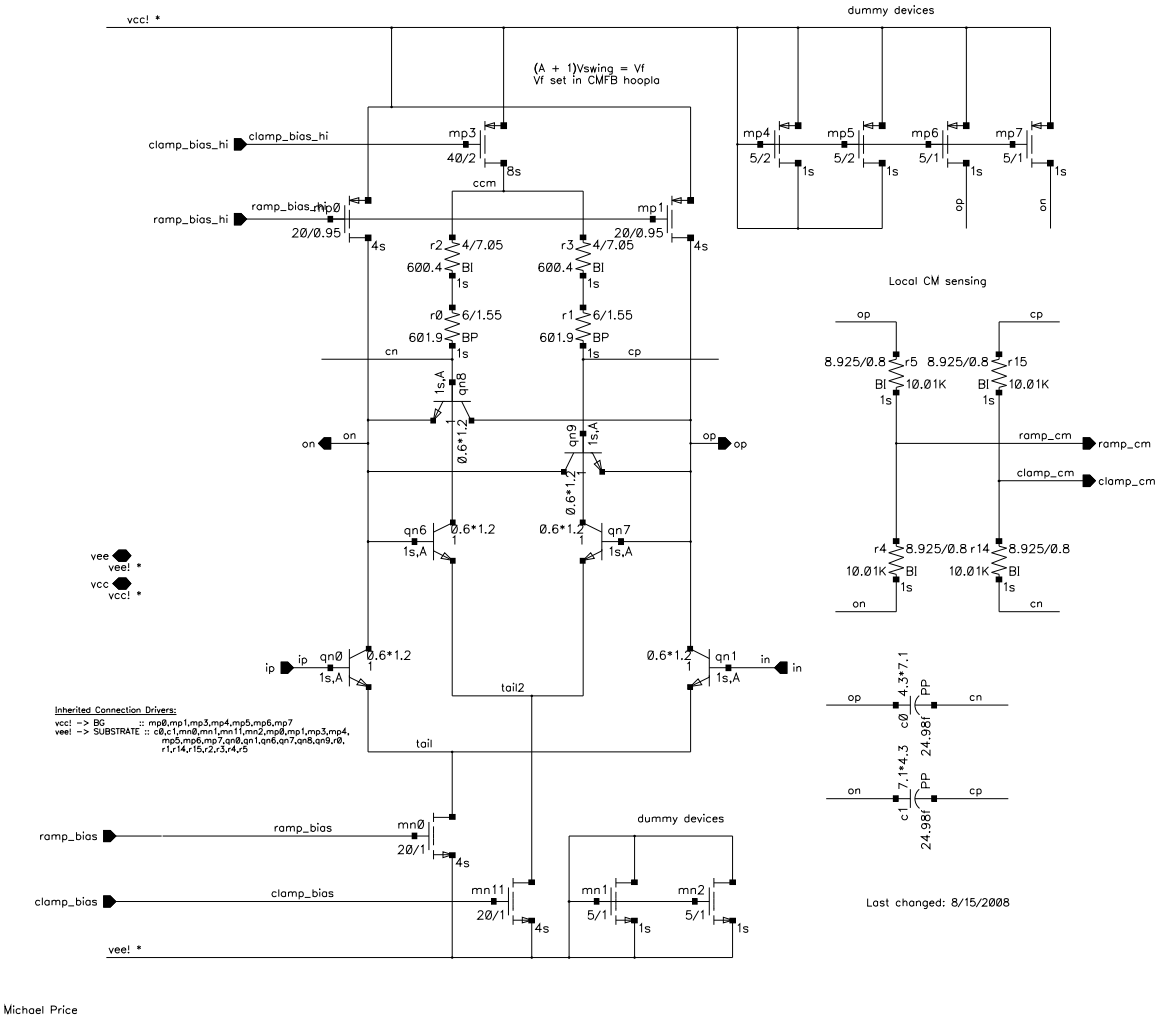

Figure 3-11: Complete schematic of ramp generator.

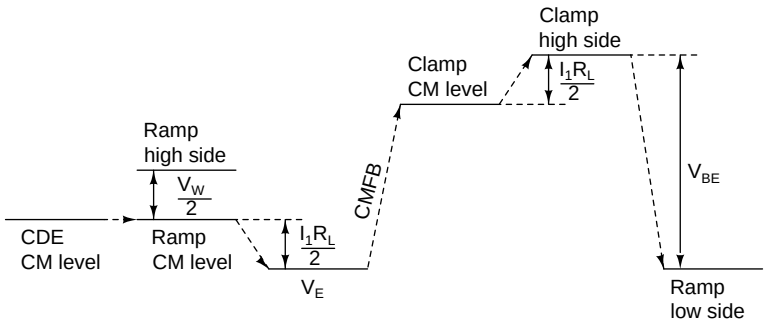

Figure 3-12: Graph showing voltage drops in CMFB scheme.

2. Keep the clamp amplifier outputs at the appropriate common-mode level so that $V_W \approx 225$ mV.

3.5.1 Technique

As noted before, the CDE output is used as a common-mode reference from which other common-mode levels are derived. This relaxes the CMRR constraint on the comparator (which has to compare the CDE and ramp generator outputs). The relationship between voltage levels in this CMFB configuration is shown in figure 3-12.

3.5.2 Compensation

A classic CMFB circuit uses a differential pair to amplify the error between some common-mode level and a reference voltage. The output current of this amplifier is mirrored around to control the common-mode level. These loops are typically dominant-pole compensated [1]. A feedback capacitor across an inverting amplifier, magnified by the Miller effect, is sufficient in most cases to push the common-mode loop crossover frequency below the other high-frequency poles in the loop transfer function. This arrangement is shown on the left side of figure 3-13. The low-frequency common-mode loop gain is:

$$A_0 = A\frac{qI_0}{2kT}\frac{r_{o1}r_l}{r_{o1}+r_l}$$

where r_{o1} is the output resistance of the MOSFET `M1` and r_l is the small-signal load resistance.

In the context of the ramp generator (and associated active clamp), the CMFB directly drives PMOS current sources. The ramp output nodes are loaded only by high-impedance current sources, resulting in high loop gain. Furthermore, PMOS devices in this process have relatively large parasitic capacitances. A SPICE simulation of common-mode loop gains (shown in figure 3-14) using 50 fF of Miller capacitance

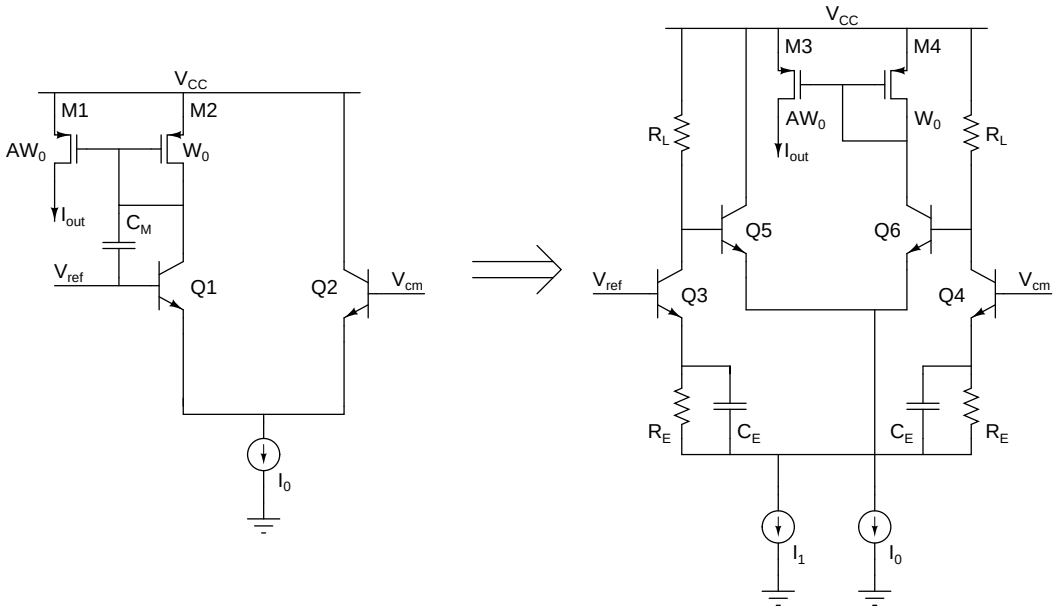

Figure 3-13: Comparison of standard Miller compensated (left) and degenerated lead compensated (right) CMFB topologies.

confirms the marginal stability associated with this configuration. This problem manifests as clamp window variations, causing significant parasitic jitter. An undesirably large Miller capacitor (on the order of 500 fF) would be needed to obtain 45° of phase margin.

Instead of slowing the loop down in order to stabilize it, maybe we could speed it up instead. A heavily degenerated differential pair lowers the DC gain by a factor of $\frac{R_L}{R_E}$; relatively space-efficient bypass capacitors add a zero at $w = \frac{1}{R_E C_E}$ that can cancel the 150 MHz parasitic pole. This more space-efficient scheme is on the right side of figure 3-13. It is used in error amplifiers for both the ramp output level and the clamp amplifier output level. However, we still need an algorithm for determing what the clamp amplifier output level should be.

3.5.3 Clamp range control

Making the clamp range robust to manufacturing variation and operating conditions is challenging. The simplest solution is to implement a fixed offset between the common-mode levels of the ramp output and the clamp amplifier output. The V_{BE} temperature dependence of the clamp devices could be compensated with temperature-dependent resistors, or even by including a V_{BE} drop in the offset voltage. Extensive experiments with these CMFB arrangements led to the development of a more robust control scheme pictured in figure 3-16. This scheme indirectly controls the clamp window V_W.

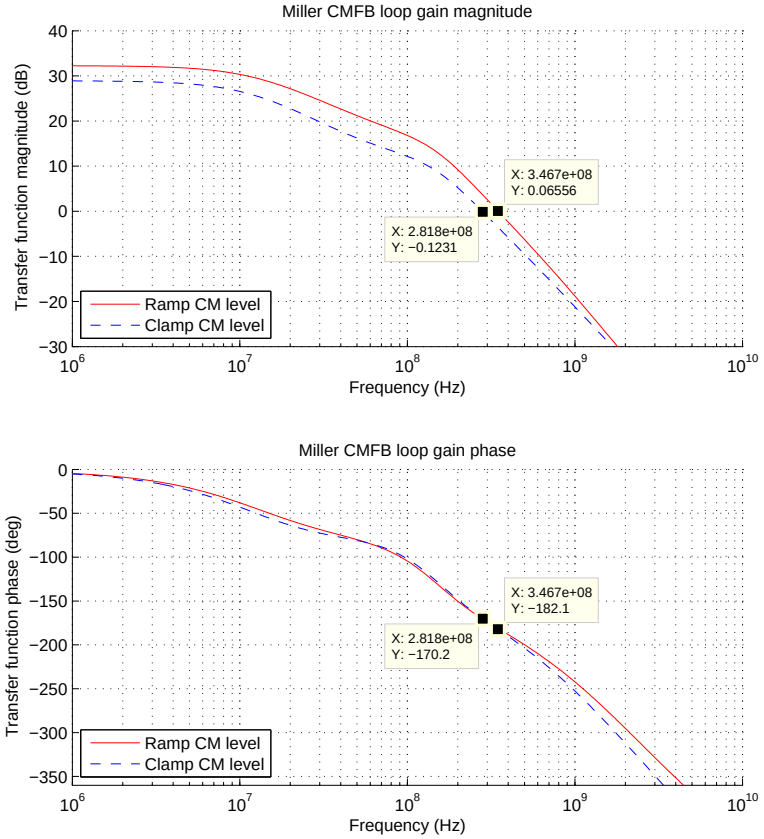

Figure 3-14: Open-loop frequency response of a typical CMFB loop with 50 fF Miller compensation capacitors.

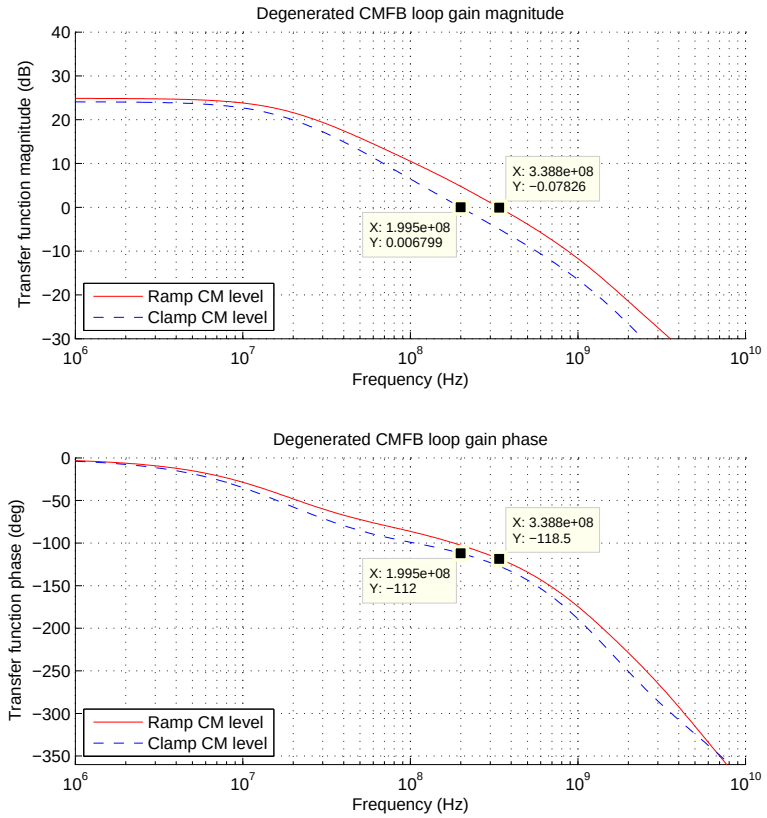

Figure 3-15: Open-loop frequency response of heavily degenerated lead compensated CMFB loop.

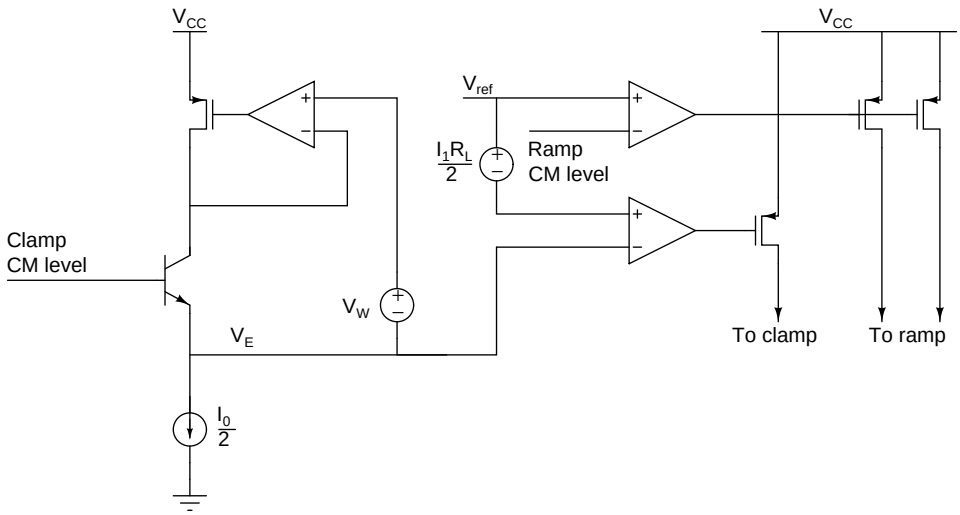

Figure 3-16: Nested feedback arrangement for clamp V_{CE} and common-mode level control.

An inner feedback loop is used to stabilize the V_{CE} of a replica transistor, operated at the same current as the clamp devices. When one of the clamp devices is active, its emitter is connected to the more negative of the ramp outputs. Hence the emitter voltage of the clamp device (labeled V_E in figure 3-16) should be equal to the ramp's common-mode level minus $\frac{V_W}{2}$. A second error amplifier forces the clamp amplifier to satisfy this constraint. We find that $I_1 R_L = V_W$, i.e. the swing of the clamp amplifier should equal the clamp range.

The aforementioned pieces are assembled in figure 3-17, the schematic of the `cm_force` circuit. The inputs of this circuit are the common-mode levels sensed in the CDE (`ref_cm`) and ramp generator (`cm1`, `cm2`). Common-mode level shifting devices `qn6`, `qn10`, and `r22` set up inter-stage biasing for the error amplifiers.[2] The gates of the current mirror devices (`mp0` and `mp10`) are connected to the gates of the PMOS current sources (`mp0` and `mp3` for the ramp, `mp1` for the clamp) in the ramp generator.

It is possible for this CMFB circuit to stabilize at a large value of V_W when the lower current sources `mn7` and `mn18` are driven into the triode regime. The helper device `qn24` prevents this by supplying extra current to `mn7` and `mn18` when their drain voltages fall significantly below the reference common-mode level. Once the current sources are in saturation again, the circuit provides the desired negative feedback.

A simulation of the crucial window range (figure 3-18) shows that this feedback arrangement should result in consistent behavior up to 85 °C despite the multitude of variables involved.

3.6 Comparator

All of the circuitry described above is dedicated to producing two data-dependent signals, $r(t)$ (ramp) and $\hat{d}(t)$ (delay estimate). If everything went well, those two signals will be differential voltages at the outputs of the ramp generator and CDE. Recall from section 2.3 and figure 2-7 that a comparison of those two signals generates jitter-compensated edges.

Speed is the main consideration for this comparator, which can generate parasitic DDJ if its settling time extends beyond one bit period. The fastest practical topology is an open-loop limiting amplifier without hysteresis.

[2] The transistors here are simply used to obtain voltage drops that would otherwise require very large resistances.

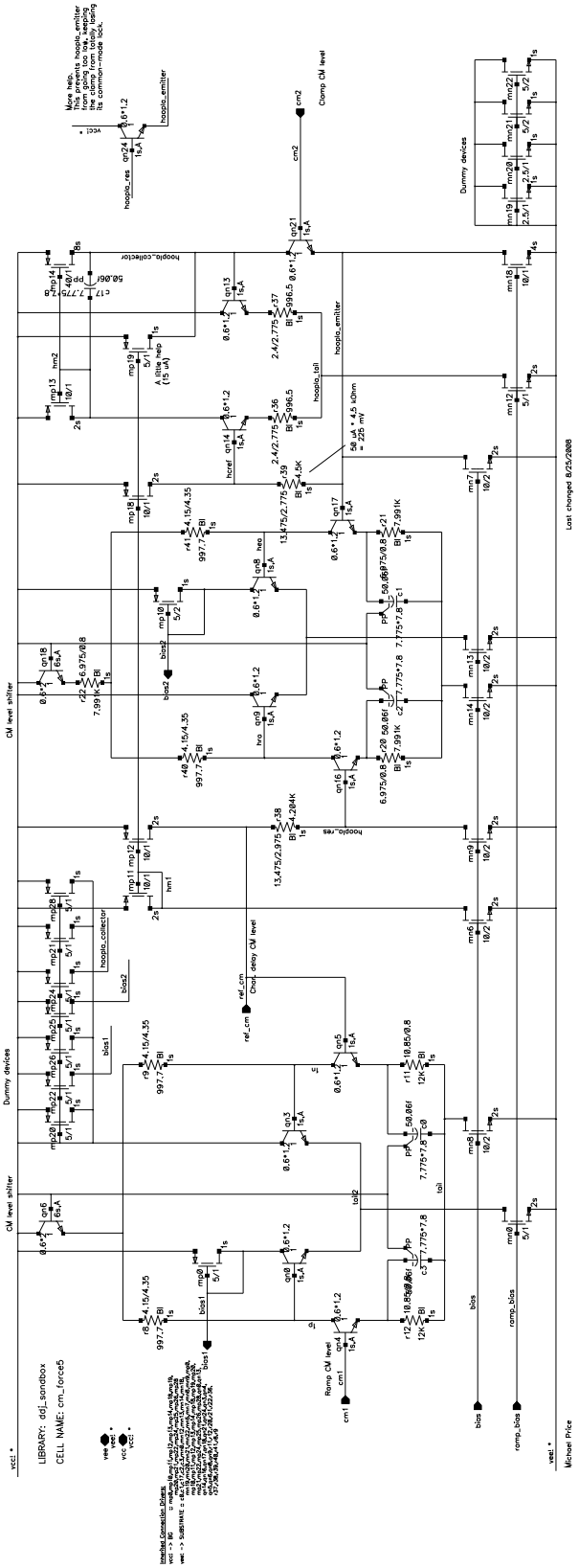

Figure 3-17: Complete schematic of CMFB network.

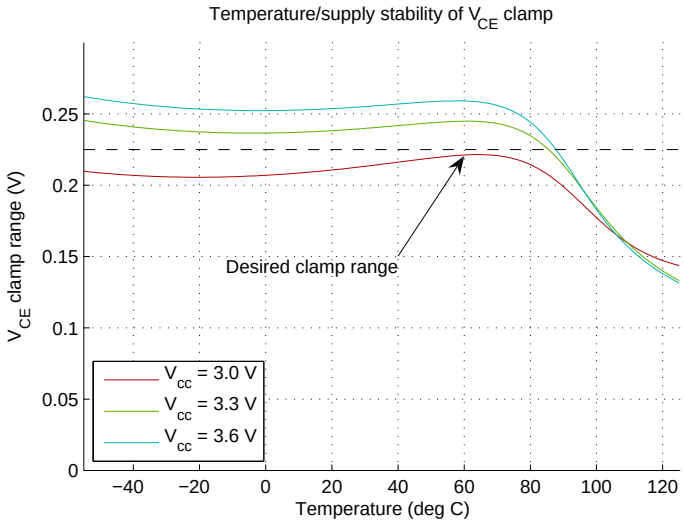

Figure 3-18: Sweep of V_{CE} clamp range across supply voltages and temperatures.

3.6.1 Differential input stage

The circuit of figure 3-19 is used to reduce two differential signals to one. Assuming that the resistors are large enough to linearize the transconductance characteristic of the transistors,

$$\begin{aligned} V_{op} &= V_{CC} - \frac{R_L}{2R_E}\left[(V_{1p} - V_{1n}) + (V_{2n} - V_{2p})\right] \\ V_{on} &= V_{CC} - \frac{R_L}{2R_E}\left[(V_{1n} - V_{1p}) + (V_{2p} - V_{2n})\right] \\ V_{out} &= V_{op} - V_{on} \\ &= \frac{R_L}{R_E}\left[(V_{1p} - V_{1n}) - (V_{2p} - V_{2n})\right] \end{aligned}$$

The resistors R_E are required to linearize the stage across a differential input voltage range of 225 mV. Without emitter degeneration, the stage would not be able to resolve any difference between (for example) $V_{1p} - V_{1n} = 120$ mV and $V_{2p} - V_{2n} = 100$ mV. Here R_E is made small enough to the input stage a limiting characteristic.

3.6.2 Modified Cherry-Hooper amplifier

A modified Cherry-Hooper topology [12] was used in a simple differential gain stage in this comparator. This amplifier has excellent high-frequency performance. To understand why, consider the block diagram in figure 3-20. The amplifier is divided into an open-loop stage followed by a closed-loop stage. The

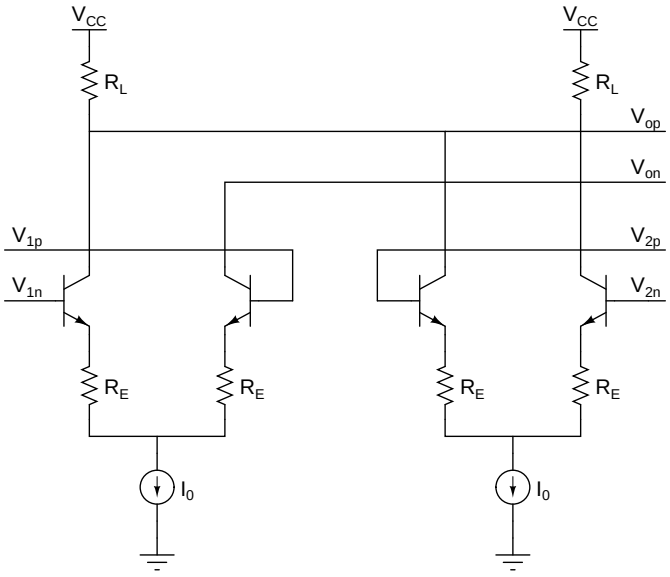

Figure 3-19: Dual differential input stage for comparator.

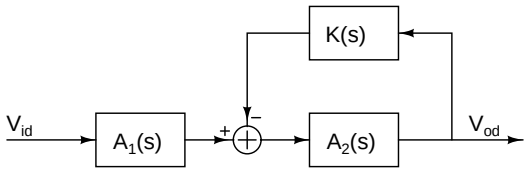

Figure 3-20: Block diagram for Cherry-Hooper amplifier topology.

closed-loop transfer function is

$$A(s) = \frac{A_1(s)A_2(s)}{1 + A_2(s)K(s)}$$

Introducing premature rolloff in the feedback transfer function $K(s)$ creates a high-frequency boost in the second stage that cancels the dominant pole of the first stage. By properly allocating bias currents and adjusting resistor values, the bandwidth of the amplifier can be maximized as the various pole frequencies are brought closer together.

Two negative capacitance techniques, shown in figure 3-21, were considered in efforts to further improve bandwidth. The left-hand approach is used to cancel the Miller capacitances, including the amplifying devices' c_μ, by supplying charge from the opposite input.[3] The right-hand circuit synthesizes a negative capacitance load as follows. When `Q3` turns on, it begins to discharge the load capacitance. At the same

[3]This is a form of high-frequency positive feedback, so the capacitors must not be made as large as the actual Miller capacitance.

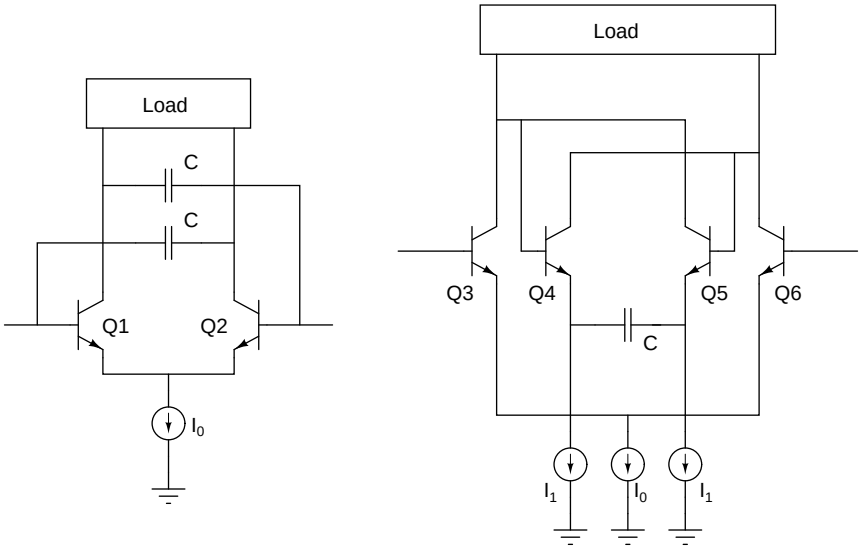

Figure 3-21: Circuits for synthesizing negative differential capacitance loads.

time, the collector of `Q6` floats upward, turning on `Q5`. `Q5` pulls its collector current from the opposite output (`Q3`'s collector) in order to charge `C`. This speeds up the discharge of load capacitance.

The second method is limited by the bandwidth of the "followers" `Q4` and `Q5`. In this particular design, the parasitic load capacitance of the Cherry-Hooper is small enough that this negative capacitance scheme diminishes gain above 4 GHz. Partial Miller capacitance nulling was beneficial, however.

Figure 3-22 shows how the input and gain stages are implemented in the complete comparator circuit. Emitter followers `qn8` and `qn9` buffer the inputs to the gain stage. The feedback network around the second gain stage consists of `qn26` and `qn27`, each preceded by a 1:2 voltage divider (setting the closed-loop gain of that stage to 2). The parasitic pole at the bases of `qn26` and `qn27` is essential.

This circuit consumes 960 μA and has a small-signal gain of 20 dB. Simulations of its performance including interconnect parasitics are shown in figures 3-23 and 3-24. The small-signal -3 dB frequency is 6.5 GHz, and the output slews completely across its range when stimulated by a 160 ps input pulse. This indicates very low parasitic jitter at 6.25 Gb/s. The comparator introduces more jitter as the bit rate is increased.

3.7 Auxiliary circuit blocks

This section describes two additional subcircuits that were added to the original architecture (figure 2-7) in order to simplify those in the signal path. Adding a fixed delay at the CDE input lets us get away without a

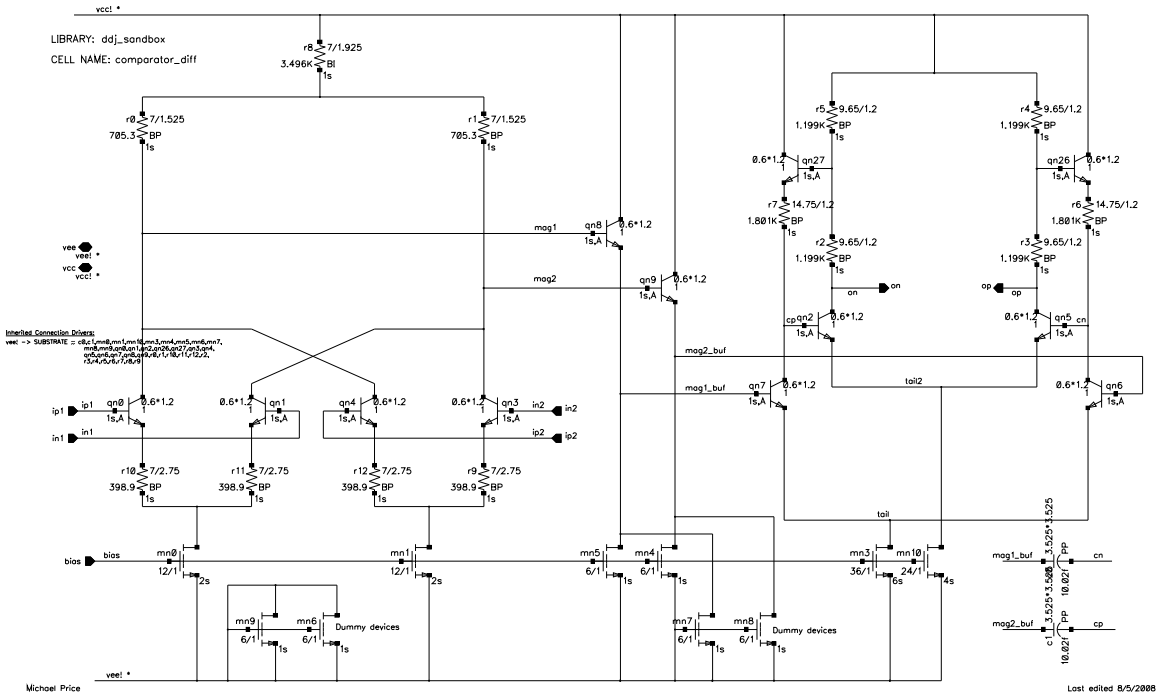

Figure 3-22: Complete schematic of differential comparator.

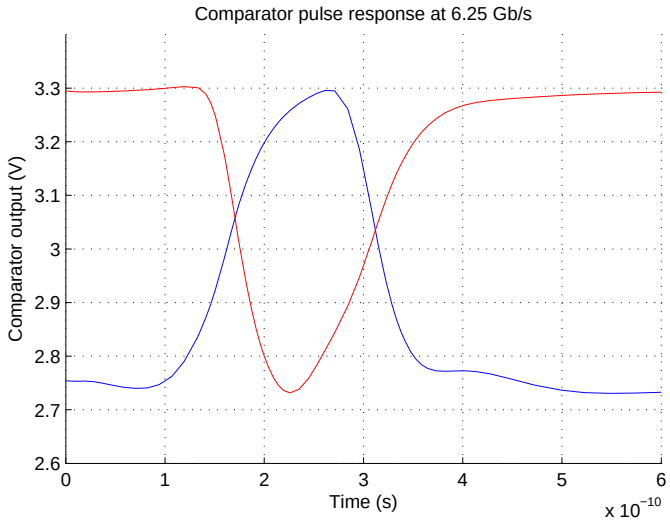

Figure 3-23: Transient simulation of differential-input comparator.

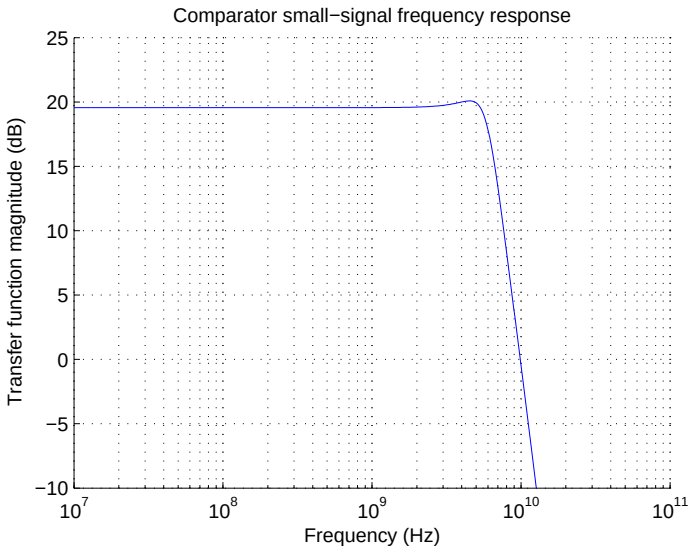

Figure 3-24: AC simulation of differential-input comparator.

sample-and-hold at the CDE output. A global reference current generator for the ramp obviates the need for multiple local current mirrors.

3.7.1 Delay cell for CDE input

The delay cell (figure 3-25) allows the use of the uncompensated bitstream as a CDE input. It uses a cascade of two CML inverters to provide a fixed 40 ps delay, in place of the data-dependent delay that would be introduced by a sample-and-hold at the CDE output. Diode-connected transistors provide compact level shifting. The first inverter provides most of the delay; about two-thirds of the 300 μA bias current is directed to the second inverter, setting its output swing at $\pm$160 mV.

3.7.2 Joint current mirror for CMFB tracking

Current sources within the CMFB circuit must be locked in proportion with those in the ramp generator. Because the ramp current is adjustable, the current DAC was moved out from the ramp generator into a global `joint_mirror` block shown in figure 3-26. This circuit mirrors the DAC output around to a diode-connected N-channel MOSFET so that a gate bias line for ramp-related current sources can be distributed.

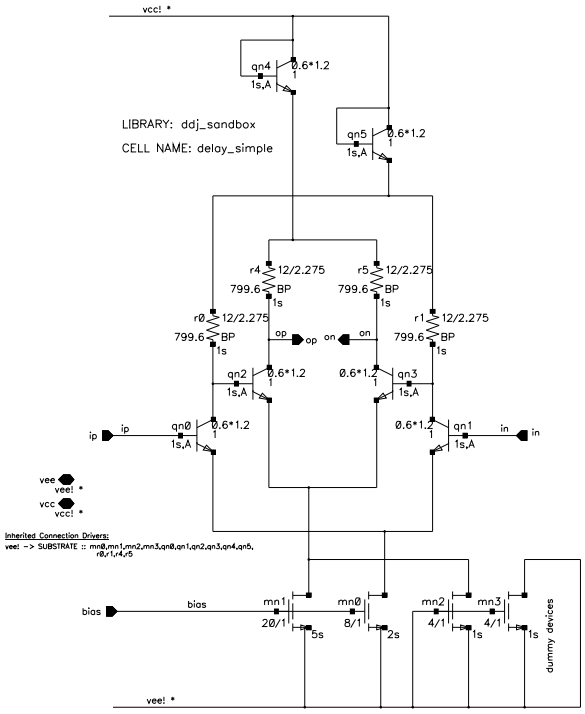

Figure 3-25: Complete schematic of 40ps delay cell.

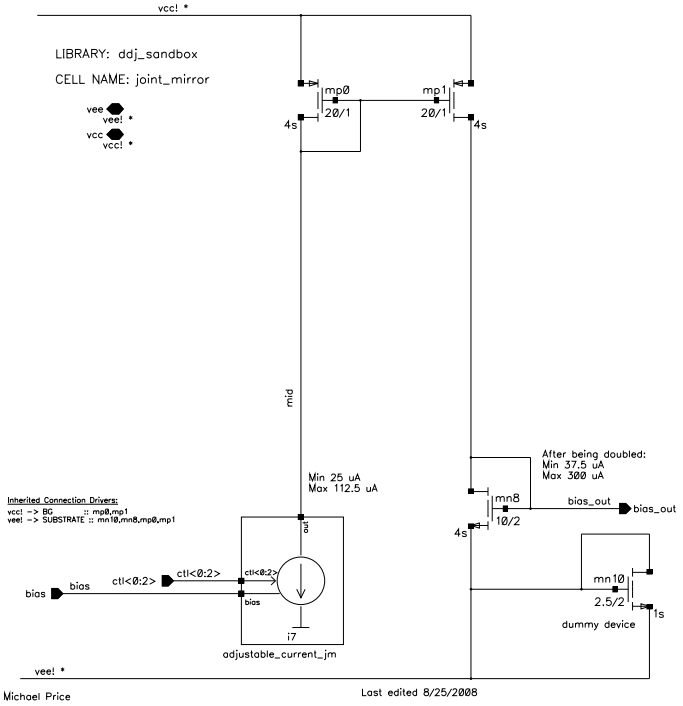

Figure 3-26: Schematic of adjustable current mirror.

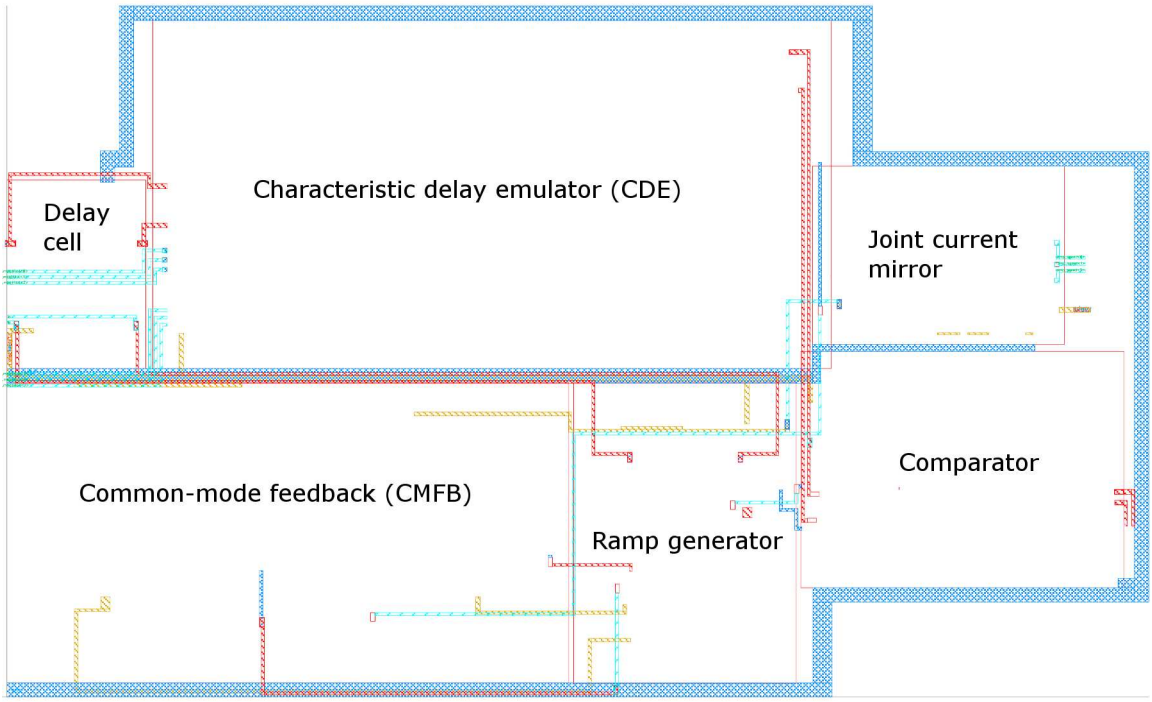

Figure 3-27: Top-level floorplan of DDJ compensator layout.

3.8 Layouts

This DDJ compensation circuit is intended for use in the transmitter of a serial link IC. Its layout was designed for easy integration into an existing chip made using the same process technology. The 240 $\times$ 140 μm block fits alongside the transmitter's pre-emphasis driver and is divided into subcircuit blocks as shown in figure 3-27. The signal flow is from left (uncompensated input) to right (compensated output).

A complete layout is shown for reference in figure 3-28, providing some additional detail as to how each subcircuit was arranged. The design incorporates sensible analog layout techniques: symmetrical layout of differential circuits, dummy MOSFETs placed alongside current sources, and wire routing optimized to minimize capacitance on the crucial nodes within the ramp generator and comparator.

3.9 Summary

The proposed DDJ compensation architecture has now been wrapped up into a single BiCMOS circuit block. The design reviewed in the preceding pages includes a characteristic delay emulator (CDE) and ramp generator. The low parasitic jitter of the ramp generator is made possible by a high-speed transistor clamp circuit with a narrow window of $\pm$ 225 mV. The CDE and ramp outputs are compared by a dual-differential

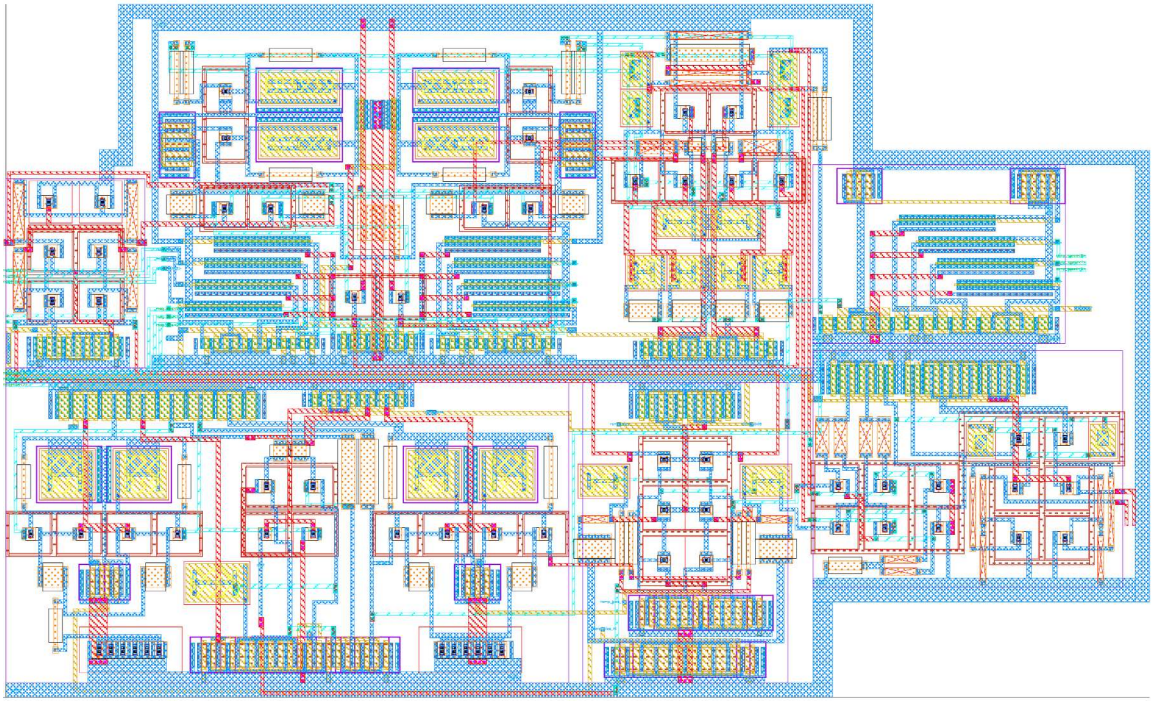

Figure 3-28: Layout of DDJ compensator.

amplifier with relatively low gain. These lightweight circuits can be digitally adjusted to compensate DDJ caused by the high-frequency loss of FR4 channels between 10–40” in length. The compensator draws 3.4 mA from a 3.3 V power supply in typical conditions.

The simulations presented along with the circuit designs verified that each piece of the compensation scheme works as intended. Now we need to step back and take a system-level view of the compensator’s behavior.

Chapter 4

Simulation Results

4.1 Methodology

A distributed transistor-level simulation and data analysis system was used to predict the performance of the DDJ compensation cell, `ddj_comp`, in a variety of situations. Several variables were considered:

- Application variables
  - Channel length and geometry
  - Bit rate
  - Additional equalization circuitry
- Controlled variables
  - Ramp speed
  - CDE slow component magnitude
  - CDE fast component magnitude
- Uncontrolled variables
  - Temperature
  - Power supply voltage
  - Systematic process variation (skew)
  - Random device variation (mismatch)

While these results are no substitute for measurements, they incorporate commonly accepted models of uncontrolled real-world variables. Parasitic interconnect resistances and capacitances within the DDJ compensation block were incorporated into all simulations.

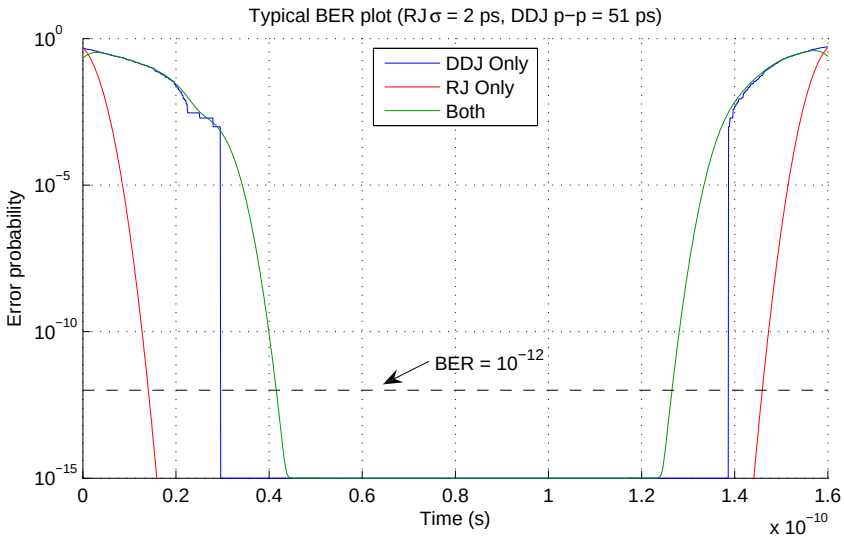

Figure 4-1: A "bathtub" plot showing the sampling window as a function of desired BER.

The compensator is clock-agnostic and will attempt to operate on any input signal. The effects of jitter are more evident at higher bit rates; 6.25 Gb/s (160 ps UI) was selected since it is a relatively common serial link speed that can be achieved using readily available 0.35μm BiCMOS technology. Several tests were also run at 10 Gb/s (100 ps UI) to demonstrate the speed limitations of the compensator. For each bit rate, three different lengths of FR4 stripline were chosen to introduce mild, significant, and severe DDJ.

In many backplane applications, DDJ dominates the jitter distribution at the receiver. Since the sampling window is defined by the edges of the jitter distribution, peak-to-peak DDJ is the most meaningful performance metric reported below. Random jitter (RJ) and crosstalk-induced jitter (BUJ) are excluded; duty-cycle distortion caused by the compensator is included. The FR4 trace is assumed to be the only lossy component of the channel. The complete jitter distribution is the convolution of the DDJ distribution with all other types of jitter (including contributions from crosstalk and random noise).

Figure 4-1 shows the BER as a function of sampling time across a unit interval in a typical case. DDJ dominates near the edges, and RJ effectively "extends" the jitter distribution towards the center of the sampling window. At a BER of 10^{-12}, the RJ threshold is 28.5 ps; the peak-to-peak DDJ is 50.9 ps; and the total jitter threshold is 75.1 ps. The horizontal eye opening can be approximated conservatively by subtracting the peak-to-peak value of all deterministic jitter components and the BER-defined RJ limit from the length of one bit period.

4.2 Nominal conditions

In some cases, asynchronous DDJ compensation reduces jitter to acceptable levels without any amplitude pre-emphasis. Table 4.1 documents the peak-to-peak DDJ, before and after compensation, with the compensator operating at $T = 40$ °C, $V_{CC} = 3.3$ V, and nominal process conditions.

		Uncompensated		Compensated	
Channel length	**Bit rate (Gb/s)**	**Jitter p-p (ps)**	**Jitter p-p (UI)**	**Jitter p-p (ps)**	**Jitter p-p (UI)**
20”	6.25	44.3	0.277	20.5	0.129
30”	6.25	98.8	0.618	46.4	0.290
40”	6.25	Bit error	N/A	94.4	0.590
15”	10.0	31.9	0.319	20.0	0.200
20”	10.0	63.9	0.639	32.0	0.320
25”	10.0	Bit error	N/A	Bit error	N/A

Table 4.1: Peak-to-peak jitter before and after compensation in six nominal cases.

4.3 Nonideal effects

Although the compensation circuit was designed to withstand expected variations in process, voltage and temperature (PVT) conditions, its performance can be degraded by several factors. The results are presented below and then discussed in section 4.5.

4.3.1 Process skew

Manufacturing irregularities lead to systematic variations in bandwidth due to incorrect device sizing. A simple skew model that scales all resistors and capacitors (including parasitic capacitors) by a multiplicative factor can be used to quickly simulate worst-case circuit behavior. The DDJ compensation circuit is not intrinsically sensitive to the exact values of its passive components, although process skew creates error in the emulation of the channel’s characteristic delay. The results of several simulations, similar to those in table 4.1 but incorporating process skew, are shown in table 4.2. The emulation errors can be mitigated to some extent by changing the adjustment settings.

Using “fast” N-channel and “slow” P-channel MOSFETs with nominal resistors and BJTs increased the peak-to-peak parasitic jitter of the ramp generator output by 2.0 ps to 13.6 ps.[1] The differences were caused by a mismatch of sink and source currents in the clamp amplifier that reduced the window voltage from 230

[1]The jitter increase of 0.4 ps in the opposite scenario (slow NMOS and fast PMOS devices) is negligible.

mV to 198 mV. This mismatch cannot be eliminated completely by CMFB because of the finite loop gain. Simple bandwidth limitations due to BJT and resistor sizes have much more significant implications for the compensator's jitter performance.

Process corner	Channel	Bit rate (Gb/s)	Jitter p-p (ps)	Jitter p-p (UI)
Slow	20”	6.25	47.0	0.294
Nominal	20”	6.25	20.5	0.128
Fast	20”	6.25	36.2	0.226
Slow	30”	6.25	64.0	0.400
Nominal	30”	6.25	46.4	0.290
Fast	30”	6.25	74.9	0.468
Slow	40”	6.25	Bit error	N/A
Nominal	40”	6.25	94.4	0.590
Fast	40”	6.25	117.8	0.590
Slow	15”	10.0	Bit error	N/A
Nominal	15”	10.0	20.0	0.200
Fast	15”	10.0	32.2	0.322
Slow	20”	10.0	Bit error	N/A
Nominal	20”	10.0	32.0	0.320
Fast	20”	10.0	48.4	0.484
Slow	25”	10.0	Bit error	N/A
Nominal	25”	10.0	Bit error	N/A
Fast	25”	10.0	61.6	0.616

Table 4.2: Compensated peak-to-peak jitter in process corners.

The increased parasitic capacitances witnessed in the slow process corner hamper the slew rate of the ramp generator, introducing a scale factor to the strength of jitter compensation and introducing additional jitter in the ramp signal itself. As a result, compensation is no longer effective at 10 Gb/s in the slow corner.

4.3.2 Temperature and supply voltage

By far the most common variations in real-world usage are those of temperature (due to the ambient temperature and device self-heating) and power supply voltage (due to imperfect regulation and on-chip IR drop). The signal swing of the ramp generator were plotted against temperature and supply voltage in figure 3-18, indicating a wide safe operating area. Numerical results extracted from PRBS transient simulations are displayed graphically in figure 4-2; a summary of the corner cases is provided in table 4.3.

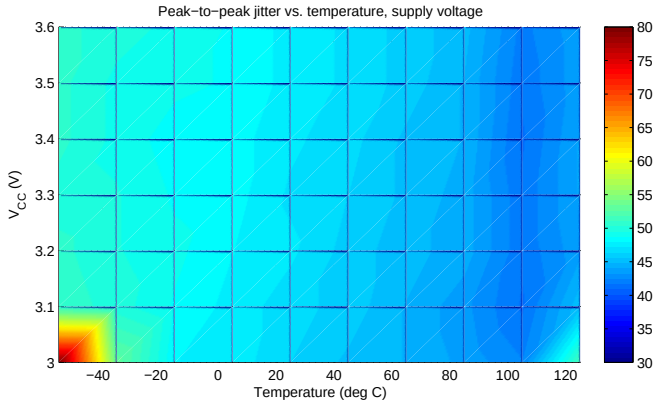

Figure 4-2: Peak-to-peak jitter swept against temperature and supply voltage.

T (°C)	V_{CC} **(V)**	**Jitter p-p (ps)**	**Jitter p-p (UI)**
-55	3.0	50.6	0.316
40	3.0	44.8	0.280
125	3.0	50.6	0.316
-55	3.3	48.6	0.304
40	3.3	46.1	0.288
125	3.3	43.5	0.272
-55	3.6	49.3	0.308
40	3.6	46.1	0.288
125	3.6	44.2	0.276

Table 4.3: Peak-to-peak jitter in temperature and voltage corners at 6.25 Gb/s over 30” FR4 trace.

4.3.3 Improper adjustment

The DDJ compensator cannot exactly “invert” the jitter characteristic of the channel, but its delay error is small when the settings are chosen correctly. For each channel, there is an optimal combination of settings for which the CDE output closely matches the characteristic delay of the channel (see figure 4-3). In this case, most of the jitter introduced by the compensator (visible in the transmit-side eye diagram) is nulled by the jitter caused by the channel. Guidelines for choosing the correct digital control codes were presented in section 3.2.

As the CDE transfer function and delay sensitivity vary from the optimal settings, additional jitter is introduced into the bitstream, as shown in figure 4-4. Figure 4-5 shows how the CDE settings and ramp speed setting affect the jitter of the received signal across a 30” long FR4 trace at 6.25 Gb/s. For this channel model, the optimal control codes are 101 (ramp speed), 011 (CDE slow magnitude) and 011 (CDE fast magnitude).

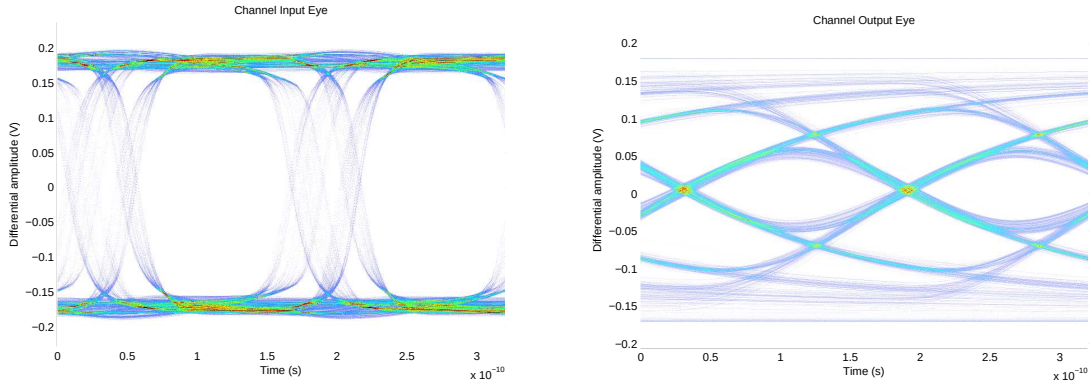

Figure 4-3: Predistorted (transmitted) and received signal eyes when compensator is properly adjusted.

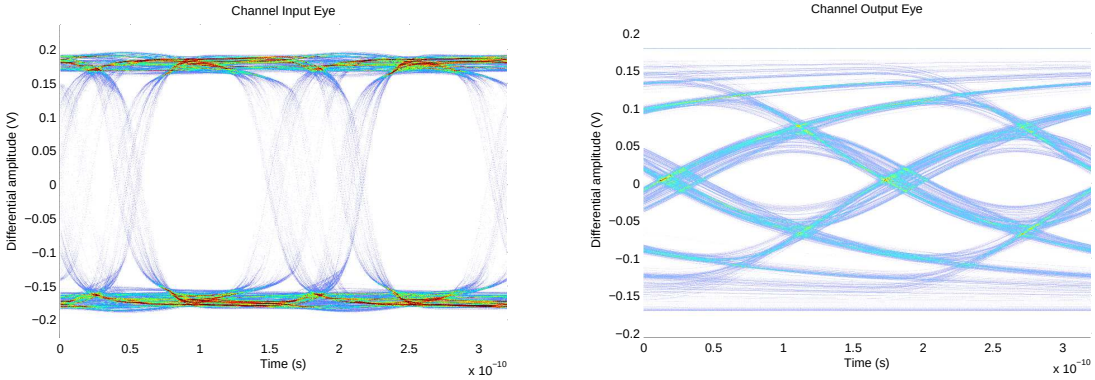

Figure 4-4: Predistorted (transmitted) and received signal eyes when compensator is improperly adjusted.

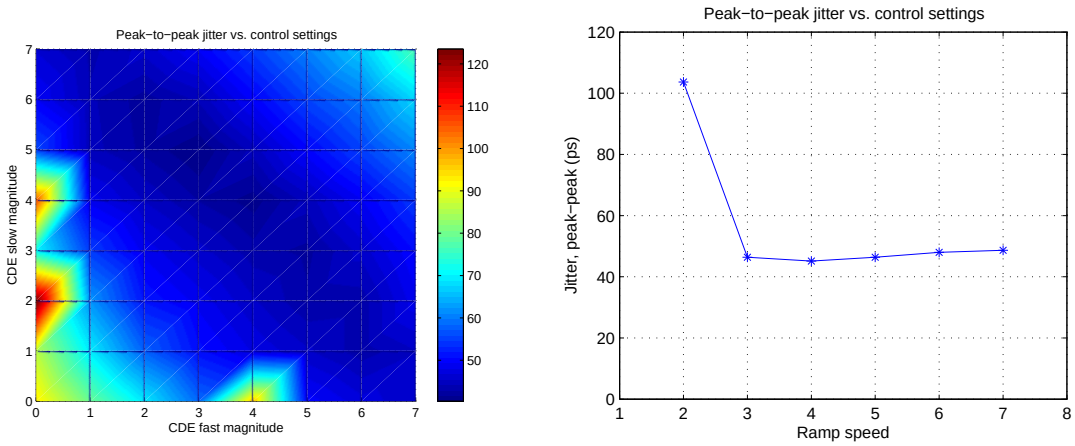

Figure 4-5: Jitter as a function of the control settings: characteristic delay (left) and ramp (right).

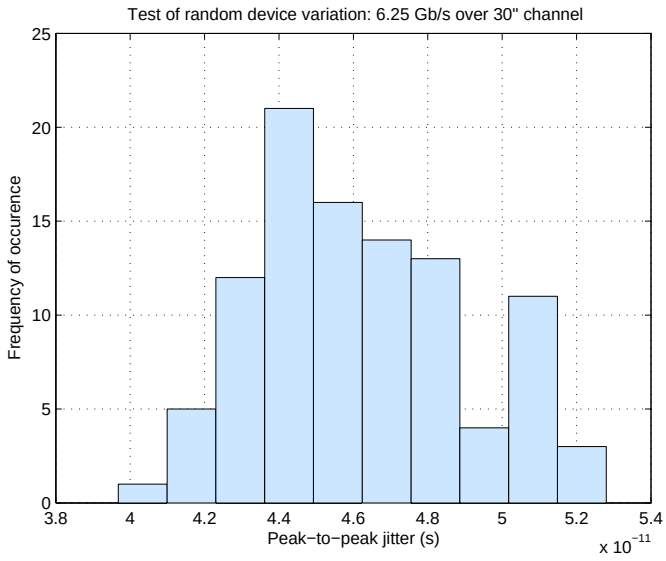

Figure 4-6: Distribution of received peak-to-peak jitter due to random device variations.

Using slower ramp speeds saves power, but the ramp cannot reset itself within one bit period if the slew rate is too slow. At 6.25 Gb/s, the minimum feasible ramp speed setting is 011. At this setting, the ramp tail current is 218 μA and its output slew rate is 2.78 V/ns. At the maximum ramp speed setting of 111, the tail current is 427 μA and slew rate is 4.93 V/ns. Due to matched biasing in the CMFB network, this increase in ramp current increases the total current consumption of the compensator from 3.13 mA to 3.63 mA.

4.3.4 Random device variation

Monte Carlo simulations using process-specific statistical mismatch models for BJTs, MOSFETs and resistors were used to evaluate the sensitivity of this implementation to relative device dimensions. Figure 4-6 demonstrates that mismatch creates mild delay errors at 6.25 Gb/s. The maximum peak-to-peak jitter encountered in an ensemble of 100 trials was 52.8 ps, compared to the 46.2 ps ensemble mean and 98.8 ps without any jitter compensation over a 30" FR4 trace.

Performance degradations due to device variation were especially significant at 10 Gb/s. At this bit rate, the differential swing allowed by the V_{CE} clamp in the ramp generator (see section 3.4.2) influences jitter because the slew rate of the ramp output is limited. The middle eye diagram in figure 4-7 shows that jitter is minimized when the clamp range is set to between 200–250 mV. Above 250 mV, jitter is introduced because the slew rate of the ramp is insufficient to traverse the clamp range within one bit period. Below 200 mV, the limited speed of the clamp introduces settling tails. Only 40 of the 100 trials resulted in a reduction in

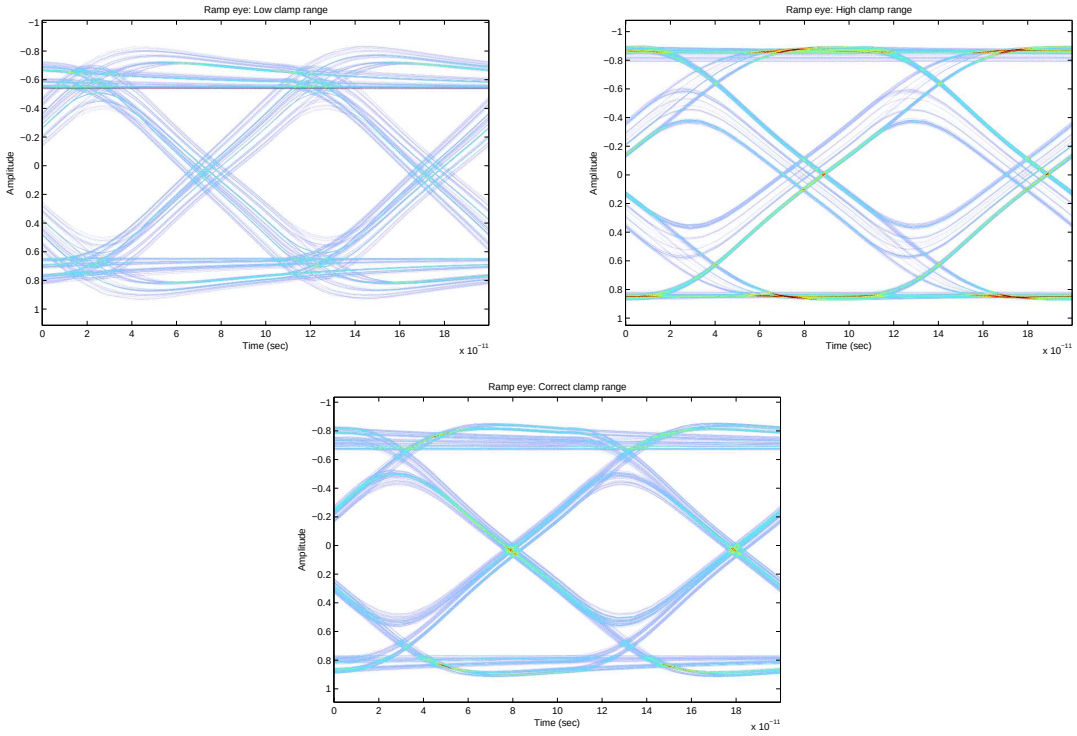

Figure 4-7: Eye diagrams of ramp output at 10 Gb/s: overly clamped (top left), insufficiently clamped (top right), and normal (bottom).

jitter; bit errors were encountered in 45 of the trials.

While these problems do not appear significant at 6.25 Gb/s and below, it would be prudent to investigate further. Extra care should be taken to ensure that the clamp range is stable in order to prevent mismatch-induced jitter. Future implementations of this circuit could employ digitally controlled offset currents in the CMFB block to tweak the clamp range in situ.

4.4 Cooperative equalization

Numerous pre-emphasis techniques for compensating jitter already exist, but DDJ compensation is still a useful addition. It can be used in conjunction with a 1-tap FIR equalizer to achieve any desired horizontal eye opening, while reducing the amount of high-frequency boost (and hence power consumption) needed by the equalizer. Sometimes, the need for amplitude pre-emphasis is eliminated entirely. An example of this strategy is shown in figure 4-8.

The plots below demonstrate the changes in the design space for a doubly-terminated 50 Ω link driven with $\pm$400 mV differential swing. The tail current in the output stage of the transmitter is 16 mA in the

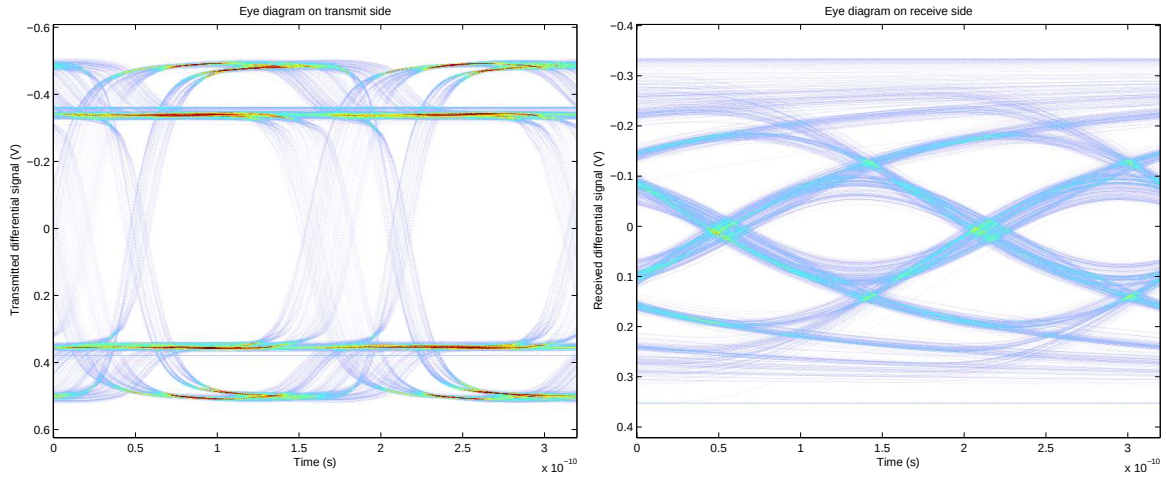

Figure 4-8: Eye diagrams simulated at transmitter (left) and receiver (right) for 40” FR4 link equalized with 3 dB of FIR pre-emphasis plus DDJ compensation.

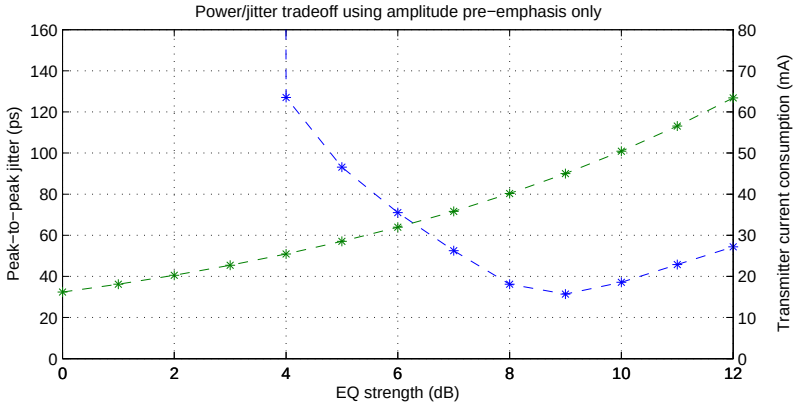

Figure 4-9: Transmitter current draw (green trace) and jitter (blue trace) for varying amounts of amplitude pre-emphasis (40” of FR4 trace at 6.25 Gb/s).

absence of DDJ compensation or pre-emphasis.

Figure 4-9 shows the power–jitter tradeoff for a 1-tap FIR pre-emphasis transmitter driving a 40” long channel at 6.25 Gb/s. The eye is closed when pre-emphasis is turned off. As pre-emphasis gain is increased, the eye opens gradually and the transmitter’s power consumption increases. 6 dB of gain is enough to open the eye and reduce peak-to-peak jitter to 71.0 ps, but requires 16 mA of additional current. The best jitter performance (31.4 ps p-p) is achieved with 9 dB of pre-emphasis.

DDJ compensation is useful because its power consumption does not scale with the amount of desired jitter compensation. As shown in figure 4-10, the current draw of the `ddj_comp` block is always between 3.28–3.49 mA. This is less than the power needed for 2 dB of pre-emphasis boost.

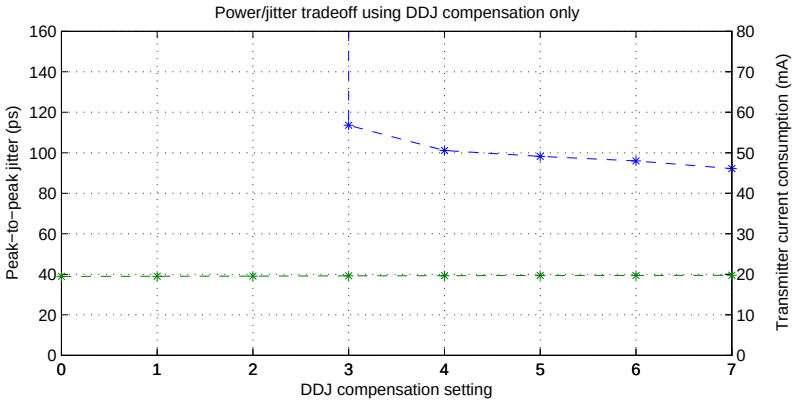

Figure 4-10: Current/jitter tradeoff for varying amounts of DDJ compensation.

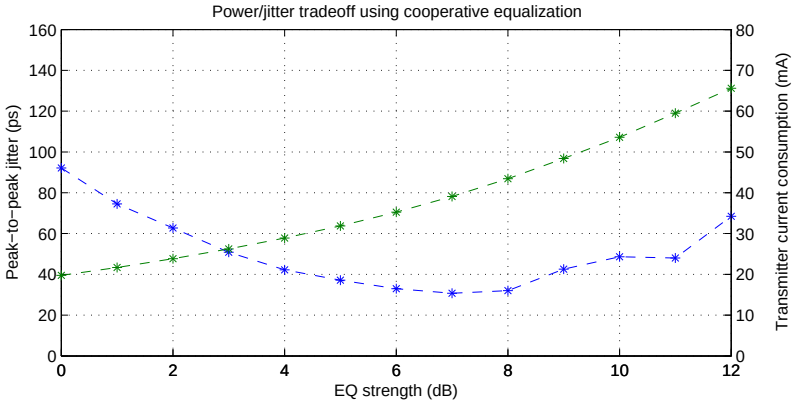

Figure 4-11: Current/jitter tradeoff for combined use of amplitude pre-emphasis and DDJ compensation.

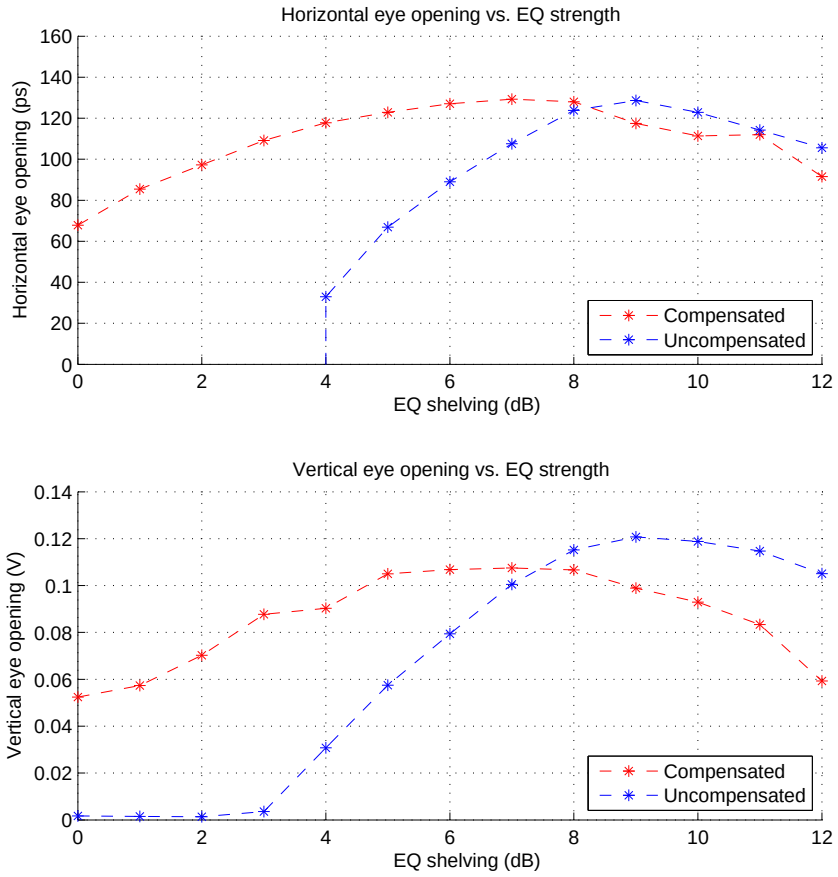

Figure 4-12: Eye openings of received signals over 40" of FR4 trace at 6.25 Gb/s, with transmitter current draw (including DDJ compensator) capped at 20 mA.

A combination of amplitude and phase pre-emphasis (as in figure 4-11) can be used to equalize very lossy channels while using less power than amplitude pre-emphasis alone. With jitter compensation, 3 dB of pre-emphasis boost is required to reduce DDJ to 50 ps at 6.25 Gb/s over a 40" long FR4 trace. This results in a savings of 9.8 mA over the 7 dB of pre-emphasis that would be required to achieve the same horizontal eye opening without DDJ compensation.

A transmitter using amplitude pre-emphasis can be configured for constant current consumption by reducing the signal swing as pre-emphasis boost is increased. Figure 4-12 shows horizontal and vertical eye openings at 6.25 Gb/s for a 40" FR4 channel when the transmitter supply current is fixed at 20 mA. The 3.4 mA draw of the DDJ compensator reduces the available drive current and hence the vertical eye opening (red trace, lower graph). However, acceptable jitter performance can be achieved over a wide range of pre-emphasis levels.

4.5 Discussion

4.5.1 Benefits

The essential benefit of DDJ compensation is that it introduces another degree of freedom in serial link configurations. Behavioral simulations predicted that an asynchronous compensation scheme could practically eliminate the DDJ introduced by any given link. This is possible because, as shown in section 2.2.2, the transition delays computed by a linear filter can closely match those introduced by the channel. The `ddj_comp` circuit is unable to completely eliminate DDJ, but provides a reduction of at least 50% at 6.25 Gb/s when adjusted properly. It can be used to open up a closed eye, eliminating the need for receive equalization in some links. Another application is reducing the amount of boost needed from a conventional 1-tap FIR equalizer.

4.5.2 Limitations

The results presented above demonstrate both circuit-level and system-level drawbacks. Two sources of error detract from compensation accuracy:

- Imperfect emulation of the channel's characteristic delay; and
- Parasitic jitter introduced by the ramp and comparator circuits.

In the results reported above, emulation errors are more significant at 6.25 Gb/s, whereas parasitic jitter is more significant at 10 Gb/s. Slew rate limits, preventing the ramp and comparator outputs from settling before a transition, are responsible for much of the increase at 10 Gb/s. These limitations are worsened in cases where process variation pushes the compliance range of the V_{CE} clamp beyond 250 mV, as seen in section 4.3.4. Practical applications of this circuit will involve lower bit rates relative to the bandwidth limits of the process, reducing the impact of parasitics.

Testing combinations of amplitude pre-emphasis and DDJ compensation revealed that this circuit cannot break from the fundamental limiting factors in serial link performance. Figure 4-12 shows that with sufficient boost, amplitude equalization can achieve all of the same benefits as phase equalization. Note that the horizontal and vertical eye opening are not mutually exclusive; and, with the channel models simulated above, pre-emphasis introduces very little jitter. Real-world channels may exhibit non-monotonic equalized pulse responses, causing increased jitter when strong pre-emphasis is used. These channels may benefit more from the substitution of transmit EQ with DDJ compensation.

Chapter 5

Conclusion

5.1 Summary

This research was motivated by the simple challenge of transmitting digital data over a low-bandwidth channel. In many serial links DDJ is a major constraint on the data rate and BER, and the equalizers used to mitigate DDJ consume substantial amounts of power. We defined the characteristic delay function of a channel, which is the impulse response of a linear filter mapping fixed-amplitude symbols to expected delay times. It was found that the channel-induced delay on each transition in a bitstream was accurately predicted by the output of this filter. The appropriate frequency response was emulated by an adjustable filter circuit.

While it would have been difficult to design circuitry applying the linear DDJ model exactly, a simplified architecture turned out to work well enough. This architecture compared the output of a characteristic delay emulator to a slew-rate-limited version of the uncompensated bitstream. A complete set of circuits implementing the DDJ compensation scheme was designed for a 0.35 μm BiCMOS process, and simulated in many different situations. The maximum practical data rate of the circuit is somewhere between 6.25 and 10 Gb/s, so it is unlikely to be a bottleneck relative to other signal processing circuits fabricated using the same process. Simulations revealed that the circuit could reduce the jitter received over 20", 30", and 40" FR4 channels by more than 50% at 6.25 Gb/s, while consuming up to 32 mW less power than a typical amplitude pre-emphasis circuit. Common-mode feedback techniques were employed to make this performance robust to the expected temperature, power supply, and manufacturing variations.

The result is another degree of freedom for serial link designers. Asynchronous links are relatively lightweight—their equalization circuits are often limited to an adjustable boost at the Nyquist frequency of the fastest expected bitstream. These linear equalizers can use increasing amounts of power to improve horizontal and vertical eye openings at the receiver. DDJ compensation, which alters the placement of

bit transitions without emphasizing them, improves the horizontal eye opening while using a nearly fixed amount of power. When adjusted correctly, it makes the jitter distribution of the received signal less sensitive to the amount of amplitude pre-emphasis.

The DDJ compensation block reported above was designed for a 0.35 μm BiCMOS process used in many Analog Devices serial link products. These products are designed to operate at speeds of up to 6.25 Gb/s. With few exceptions, the standard device types used in the above circuits can easily be ported to other BiCMOS processes.

Test circuits will need to be fabricated and characterized before the value of this DDJ compensation scheme can be assessed. Such testing is beyond the scope of this work, but still essential.

5.2 Directions for future research

The goals of high-speed link research are to eliminate bottlenecks in communication systems and improve their energy efficiency. DDJ compensation represents progress towards both goals: it allows higher bit rates to be used with lossy channels, and it can be used as a lower-power substitute for amplitude pre-emphasis. The intention here was to provide an initial example of the asynchronous approach while leaving improvements in characteristic delay emulation (including adaptive controls) to future work. Further research should refine asynchronous DDJ compensation and develop other techniques to accommodate channel impairments.

5.2.1 DDJ improvements

Behavioral simulation models of DDJ compensation circuits would be very helpful to future studies. The proper simulation of jitter through a complicated analog circuit is very computationally intensive; collecting the data presented above required the use of a computer cluster. To make the design process faster, we need a model that is simpler than the transistor-level circuit but produces nearly identical results. The time-domain behavior of the circuitry should be characterized and condensed into a parameterized subcircuit model that can be used in transient SPICE simulations.

Assuming that the architecture described above continues to be used for DDJ compensation, the procedure for improving jitter compensation accuracy is straightforward. The majority of received DDJ can be attributed either to characteristic delay emulation errors or parasitic jitter. The parasitic jitter at high bit rates can be addressed by cleaning up the transient performance of the ramp generator and comparator. The emulation errors can be addressed by improving the CDE—making its frequency responses more closely match the characteristic delay of the relevant channels, including transmitter and receiver circuits. Implementing

a nonlinear CDE as described in section 2.4.2 could shave a few picoseconds from the DDJ distribution in lossy situations. The deterministic component of the parasitic jitter could theoretically be compensated as well.

Future work may consider power and size reductions in addition to accuracy improvements. Comparing a control signal to a ramp was initially proposed in section 2.3.1 as a method for introducing transition delays. Section 2.4 showed that signal shapes other than a ramp could be used to implement delays that are a nonlinear function of the control signal. This could be useful because the transition delay caused by the channel is also a nonlinear function of the transmitted signal. But since the errors caused by a linear delay are small, the errors caused by undesired nonlinearities may also be small. This means that ramp output's linearity is not critical as long as its parasitic jitter remains low. In an extreme case, the ramp generator could be discarded entirely. The output of a CML buffer (with inherently limited slew rate) would connect to the positive terminal of the comparator. This approach may result in a favorable exchange of circuit complexity for compensation accuracy.

The V_{CE} clamp circuit developed in section 3.4.2 requires more attention. This circuit essentially allows a comparator-based delay line to function at higher speeds than would be possible with a more compliant (i.e. diode-clamped) ramp output. But the behavior of this circuit is very sensitive to process variation. After testing initial samples, the sources of clamp window variation and parasitic jitter should be more carefully studied and resolved.

5.2.2 Effects on DFEs

Transmitters with DDJ compensation may be used along with DFE receivers, but the interaction of these technologies has not yet been studied. A DFE maintains coefficients w_i that estimate uniformly spaced samples of the channel's single-bit pulse response. Introducing data-dependent delays into each pulse creates uncertainty in the underlying parameter values. The sign-error LMS technique used in many DFEs will force w_i to converge to the mean value of each coefficient. However, cycle-to-cycle variations in duty cycle prevent the DFE from accurately cancelling ISI when DDJ compensation is used. This potential problem is illustrated in figures 5-1 and 5-2, which were generated by a behavioral 4-tap DFE simulation.

The uncompensated 30" line responds well to DFE; the DFE output samples (figure 5-1, left plot) are confined to narrow bands once the coefficients have converged. However, the samples derived from a compensated bitstream (figure 5-1, right plot) are not. The eye diagrams in figure 5-2 demonstrate that the DFE appears to eliminate the jitter caused by ISI, but not the jitter introduced by the DDJ compensator. It will be important to characterize the effects of DFE on received jitter distributions and investigate how DDJ

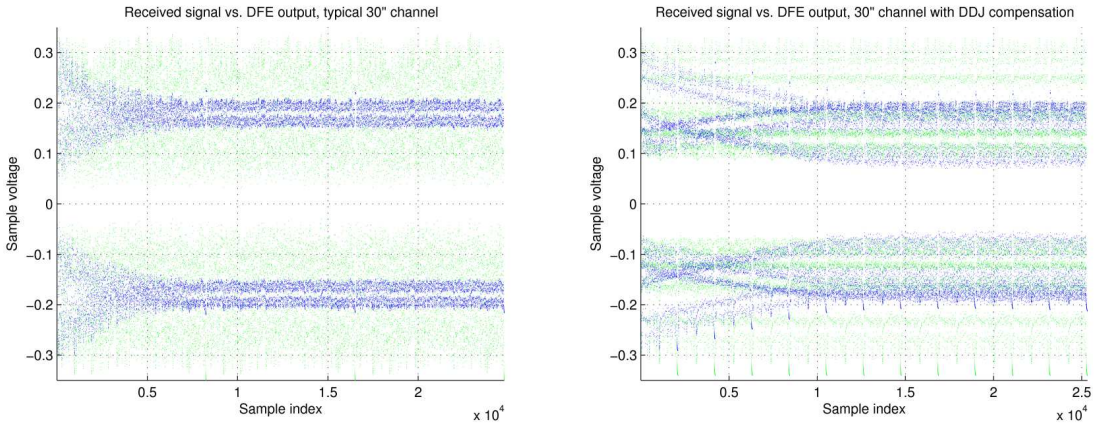

Figure 5-1: Sampled voltages from a DFE input (light green) and DFE output (blue) for uncompensated (left) and compensated (right) bitstreams.

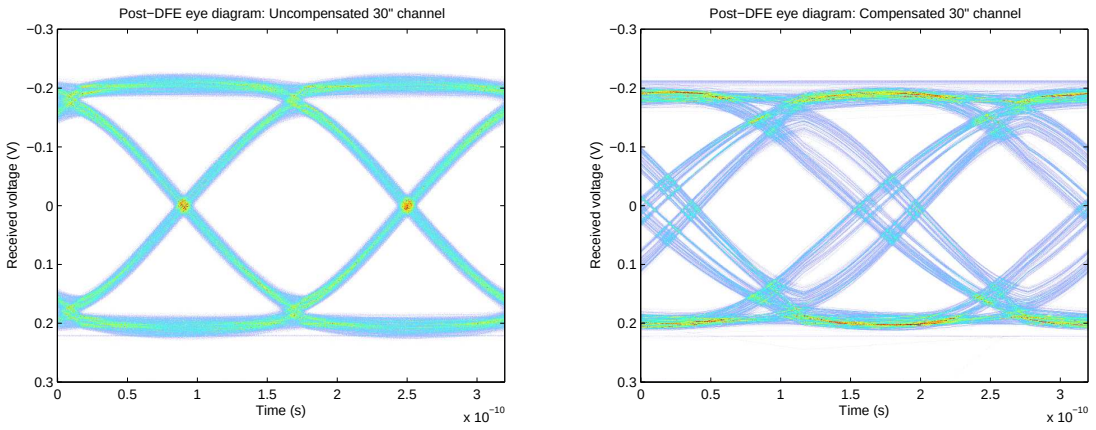

Figure 5-2: Eye diagrams of ideal DFE outputs for uncompensated (left) and compensated (right) bitstreams.

compensation settings can be jointly optimized with adaptive filters in the receiver.

5.2.3 Automatic adaptive pre-emphasis

Regardless of which pre-emphasis scheme is used, the transmitter in a serial link should be aware of the loss characteristics of the channel it is driving. Current state-of-the-art links rely on a backchannel: the receiver sends its sign-error signal back to the transmitter, which uses the information to adapt equalization coefficients using a least-mean-squares (LMS) algorithm much like a DFE [25]. Adaptive transmit pre-emphasis requires a standardized protocol between the chips on either end of the link. In existing backplane systems where modular components may be upgraded one at a time, the upgrade process to this technology will be very slow.

Instead of relying on the receiver, transmitters ideally would be able to sense the channel frequency response directly. One possible approach would be to introduce common-mode pulses and watch for reflections using an undersampled on-chip ADC [15]. The channel length could be estimated from the propagation delay or frequency content of the reflections from the far end.

5.2.4 Other channel types

It will also be important to extend this work to other types of channels. The simulation studies presented above were limited to an idealized model of FR4 backplane traces. Defects caused by vias and connectors need to be included in simulations in order to determine the appropriate settings for jitter compensation, and their consideration will likely result in changes to the compensator architecture. Also, while copper traces on FR4 PCBs are the most common channels in use, some modern equipment employs higher-performance dielectrics [13]. Lower-frequency serial links may use cables, whose transmission line characteristics differ from those of PCB traces. These differences may lead to the development of new characteristic delay approximations.

Multicore CPUs require extreme bandwidth for communications between the individual cores and between the CPU and memory, motivating the application of serial link technology to on-chip interconnects [14]. Optical interconnects are starting to be used for asynchronous serial links [8], which may also benefit from DDJ compensation. Future studies should explore these alternative system-level design problems once the appropriate behavioral models have been developed.

Finally, the meaning of DDJ compensation in PAM4 and other modulation schemes is not yet clear. We look forward to work that generalizes or replaces the characteristic delay approach presently applied to PAM2 systems.

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