Integrated Circuit Control of Resonant and Hard Switched dc/dc Converters for Industrial and Educational Applications

by

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B.S., Massachusetts Institute of Technology (2008)

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of
Master of Engineering in Electrical Engineering and Computer Science

at the
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2009

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Abstract

This thesis presents an integrated secondary side synchronous rectification controller, designed on a modern industrial silicon IC process, for use in the LLC resonant converter topology. The controller is intended to function in systems with output power levels up to 500 W and switching frequencies up to 1 MHz. Simulation data for this controller indicates high degrees of performance over a input voltage range of 12-48 V and an operating temperature range of -50° C to 150° C. Significant improvement over existing synchronous rectification controllers is observed.

In addition, a simulation and written exercise framework, intended to couple with circuits in a pre-existing discrete hardware kit, has been developed for a proposed class on power IC design. SPICE schematics of important circuit modules as well as relevant coursework is presented and explained. The course itself is motivated by the challenges of the industrial design process, and goals include teaching students about practical power IC design techniques and developing their intuition for high level circuit function. The end result is student construction of a working controller for a traditional hard-switched dc/dc converter.

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Acknowledgments

I would first like to thank Robert Neidorff for his patient tutelage and experienced and kind mentoring. Without his help, much of this project would have been impossible. Additionally, everyone in the power supply control group at Texas Instruments deserves my deepest gratitude for accepting me into their family and providing me with the resources and expertise I needed to succeed.

Next, I would like to thank Professor Steven Leeb, my thesis advisor, for exposing me to the world of power electronics and helping me find my passion in life. Working in his lab for the past few years has been an unforgettable experience.

Thank you to all those in LEES, and especially to Al-Thaddeus Avestruz, for providing me with excellent guidance and advice.

I would also like to thank my parents, Irene and Jack, for their unconditional love and support in all my endeavors. Without their devotion to my happiness and education, I would not be who I am today. I owe them more than I can ever express.

To my friends, thank you for knowing what I needed during this process.

Finally, to my wonderful girlfriend Felecia, the thought of you keeps me going.

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Chapter 1

Introduction

Across almost every engineering discipline, efficient system operation dominates the design process. This fact is especially true for those involved in the power electronics world, where every extra percentage point of efficiency significantly affects the performance and success of a given power converter. Recently, great strides in high frequency topology design have resulted in a variety of systems that are optimized for both power density and efficiency. These *resonant* converters are the backbone of the modern consumer electronics industry, and require intricately complex control circuitry to ensure proper operation. This thesis investigates integrated circuit design methodologies as they apply to modern power converter control.

The first part of this document details the actual design of a control IC fabricated using an industrial mixed signal silicon process. Specifically, Chapter 3 presents relevant schematics and performance data for a secondary side synchronous rectification controller for use in an LLC resonant converter. The majority of the work on this IC was carried out at Texas Instruments. Given that this controller is intended to be a competitively marketable product, heavy emphasis has been placed on accurate, low power operation over a wide input voltage and temperature range. Proper implementation of synchronous rectification (SR) also requires immediate response to specified control signals, thus the controller must be rated for gate drive switching on the order of 20 ns. Balancing all of these different design criteria has resulted in a novel and robust integrated circuit, which serves as an exemplary frame to discuss

the challenges associated with industrial IC design. As a relevant background section, Chapter 2 presents a review of the basic concepts of resonant conversion and synchronous rectification.

Motivated by the intricacies of the mixed signal design noted above, the second part of this document explores methods for teaching power IC design techniques to students in a university level electrical engineering program. Real world issues, such as temperature fluctuation, non ideal input voltage, and process variation are seldom covered in an academic setting. This fact leads to a significant gap between the knowledge base of a graduating analog IC designer and that required by standard industrial practice.

Currently, a hardware kit exists that allows students to build common IC modules out of discrete components, and then hook them together to create a working power supply control circuit [1]. The intention is for students to develop the intuition and skills that uniquely arise from building and testing complete circuit systems. Although certain aspects of discrete design are fundamentally different from integrated design, the circuits in this kit mostly avoid any technology dependent quirks [1]. In a classroom setting, students will learn about basic analog building blocks, review relevant control techniques, and then customize reference circuit topologies by individually picking component values based on applied theory and appropriate hand calculations. As with real IC design, students will need to verify their design choices with calculation and simulation. Chapter 4 of this thesis presents the SPICE and written exercise framework that has been developed for student design evaluation. Relevant circuit blocks, important simulations, and potential classroom/homework assignments are explained, and sample waveforms from circuits with *stock* component values are shown. This work, along with the preexisting hardware kit, provides the foundation for a power IC design laboratory course at any upper level institution.

Chapter 5 concludes this document with closing remarks and relevant summaries.

Chapter 2

Review of Resonant Conversion and Synchronous Rectification

This chapter presents the background necessary to understand the operation of the LLC resonant converter, and explains the motivation behind using synchronous rectification in power output stages. Section 2.1 details the fundamentals of resonant conversion and concludes with a description of the LLC converter. Section 2.2 develops the concept of synchronous rectification and its application to the LLC converter. Finally, section 2.3 discusses the challenges of designing an integrated secondary side synchronous rectification controller on a modern industrial silicon process.

2.1 Resonant Conversion

With the demand for smaller, more powerful electronic devices increasing daily, a common trend in power supply design has been to attempt to maximize both power density and efficiency. High power density requires that the energy storage elements used in the conversion process be as small as possible. In traditional DC-DC converters, such as the buck converter in Fig. 2-1, the size of the energy storage elements is determined by the fundamental switching frequency f_{SW} [6]. To understand this

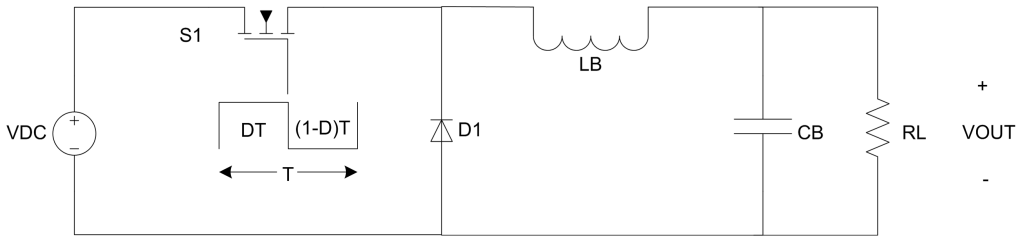

Figure 2-1: Buck Converter Schematic

statement, consider the voltage conversion relationship of the buck converter:

$$V_{out} = DV_{DC} \tag{2.1}$$

where D is the fraction of the switching period that switch S_1 conducts. This equation is derived from the steady state requirement that the current through the buck inductor L_B must start and end each switching cycle with the same value [6]. An important feature of the actual calculation of (2.1) is that the buck capacitor voltage is assumed to be constant throughout an entire switching period. While this assumption is never entirely accurate, it holds to a first order as long as the switching period is significantly less than the time constant of the system. Expressed mathematically, this requirement is

$$\tau \gg \frac{1}{2\pi f_{sw}} \tag{2.2}$$

Given that $\tau = \sqrt{LC}$, (2.2) can be expressed in terms of the energy storage elements of the system as follows:

$$LC \gg \frac{1}{(2\pi f_{sw})^2} \tag{2.3}$$

Thus, as the switching frequency of the converter increases, the constraint on the sizes of L and C decreases.

Unfortunately, increasing f_{sw} has significant negative effects on the efficiency of the buck system. In traditional converters, an important mechanism of efficiency degradation is the switching loss of the power semiconductor devices [6]. Consider the energy lost in the transition between on and off states of the switch S_1 in Fig.

2-1:

$$E_{LOSS} = \int_0^{t_{off}} V_{S1} I_{S1} \mathrm{d}t \tag{2.4}$$

where V_{S1} is the voltage across the switch, I_{S1} is the current through the switch, and t_{off} is the rise and fall time of both quantities. Typical switching waveforms for such a transition are illustrated in Fig. 2-2. As can be seen, V_{S1} starts at zero and ramps

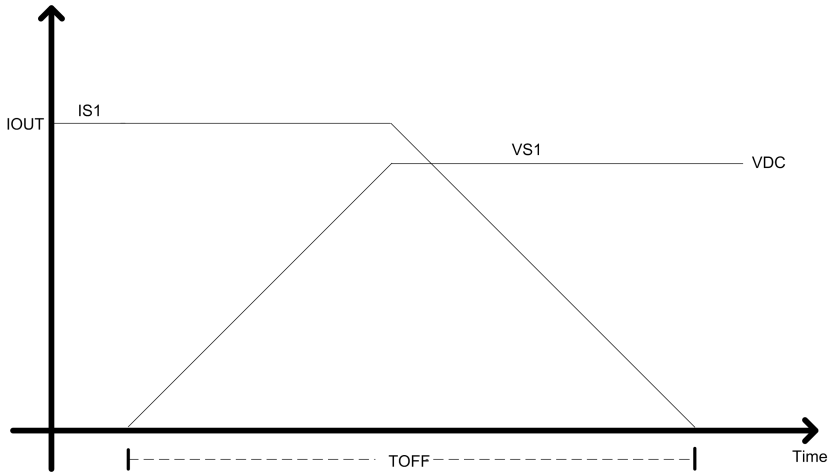

Figure 2-2: S_1 Turn Off Waveforms

up as more and more voltage builds across S_1. I_{S1} remains constant until $V_{S1} = V_{DC}$, at which point it ramps down to zero as the output current commutates to D_1. This process is called a *hard* transition. Energy is lost because both switch voltage and current are non-zero for a finite amount of time, due to the speed limitations inherent to all field effect devices and the diode commutation period. Using (2.4), the total calculated energy loss for one transition is

$$E_{LOSS} = \frac{1}{2} V_{DC} I_{out} t_{off} \tag{2.5}$$

Assuming that $t_{on} = t_{off}$, the same amount of energy is lost when S_1 turns on. Thus, the total power dissipation due to semiconductor switching loss is [6]

$$P_{LOSSswitch} = V_{DC} I_{out} t_{off} f_{sw} \tag{2.6}$$

Noting that this value is directly proportional to the switching frequency of the system, traditional DC-DC converters, such as the buck converter, cannot be optimized for both power density and efficiency. Therefore, a different type of power converter must be used to allow for simultaneous improvement of multiple figures of merit.

Recently increasing in popularity, resonant converters are an excellent replacement, and feature significantly enhanced performance statistics over the *hard* switched converters discussed above [6]. All resonant converters share a set of common attributes. First, a network of switches creates a square wave AC waveform from one or more DC sources. This square wave is applied to a reactive filter to remove unwanted harmonics from the signal, leaving only the fundamental component. Given that the difference between the fundamental and the lowest order harmonic in a square wave is so small, a highly selective LC resonant tank, tuned to the switching frequency of the system, is used as the filter [6]. From here the name *resonant converter* is derived. Second, power is controlled by varying the switching frequency about the resonant frequency of the tank, such that the impedance of the tank changes and more or less of the fundamental voltage drops across the load. Third, the semiconductor devices in a resonant converter can have much lower switching loss as compared to those in a high frequency traditional converter. Considering equation (2.4), a resonant converter can be designed to ensure that either V_S or I_S remains near zero during a switching transition, thereby minimizing the value of E_{LOSS}. This feature will be more throughly discussed in section 2.1.2, and allows for efficient system operation at much higher frequencies than would otherwise be possible. High f_{sw} implies small values for L and C, thus power density improves as well [6].

The resonant converter, however, is not without its drawbacks. Specifically, the internal currents and voltages that the switches and the energy storage elements must endure are more severe than in traditional converters [6]. These higher stress parameters imply the need for more expensive devices and raise the cost of the entire system. Despite these issues, resonant conversion still yields vastly superior performance over traditional high frequency conversion.

2.1.1 Second Order Systems

In general, the implementation of a resonant converter is fundamentally a second order system. Before discussing specific topologies, the following section reviews the behavior of second order circuits. Consider the series RLC circuit presented in Fig. 2-3. As derived in [6], the complex admittance of the network in terms of frequency

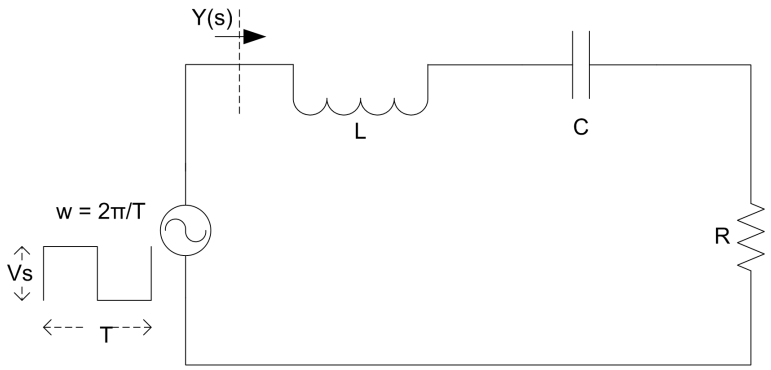

Figure 2-3: Series RLC Circuit with Square Wave Drive

is:

$$Y(s) = \frac{sC}{s^2LC + sRC + 1} \tag{2.7}$$

where $s = j\omega$, and $\omega = 2\pi f$. At a certain frequency, where $\omega = \omega_0$, the admittance of the inductor and capacitor perfectly cancel, and the resulting value is a purely resistive admittance:

$$Y(j\omega_0) = \frac{1}{R} \tag{2.8}$$

The quantity ω_0 is equal to $\frac{1}{\sqrt{LC}}$, and is called the resonant natural frequency of the system. A graph of the admittance of the network versus ω is shown in Fig. 2-4. As can be seen, the peak of the admittance function occurs at ω_0. The points at which the magnitude of the admittance is less than its maximum value by $\frac{1}{\sqrt{2}}$ are called the *half power* points, and occur at $\omega_0 \pm \alpha$. The ratio $\frac{\omega_0}{2\alpha}$ is a standard measure of the selectivity of the system and is referred to as the *quality factor*, or Q. The higher the value of Q, the better the system's ability to select one frequency and reject all others

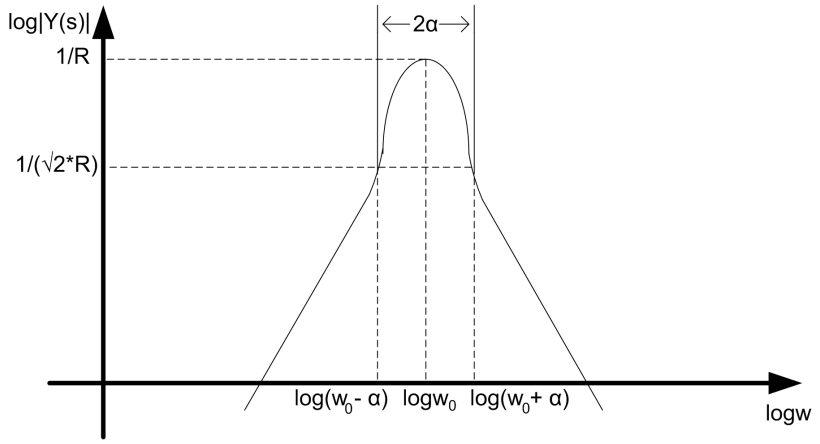

Figure 2-4: Admittance vs. ω for the Series RLC Circuit

[6]. In terms of Q, (2.7) becomes:

$$Y(s) = \frac{1}{R}\frac{(\frac{1}{Q})(\frac{s}{\omega_0})}{(\frac{s}{\omega_0})^2 + (\frac{1}{Q})(\frac{s}{\omega_0}) + 1} \tag{2.9}$$

where $Q = \frac{1}{R}\sqrt{\frac{L}{C}}$. If Q is sufficiently large, it becomes evident that

$$|Y(n\omega)| \ll |Y(\omega)| \tag{2.10}$$

for $\omega \geq \omega_0$. Therefore, for a square wave drive, only the fundamental sinusoidal component, with magnitude $\frac{4V_S}{\pi}$, needs to be considered in the circuit analysis [9]. This idea is called the first harmonic approximation, and is useful for simplifying calculations of power transfer in resonant converters [6].

As a final note, consider the peak voltage across the capacitor in fig. 2-3 as derived in [6]:

$$|\frac{V_C}{V_S}| = Q \tag{2.11}$$

Unfortunately, the more selective the RLC system, the higher the peak voltage magnitude across the capacitor. Similar analysis shows that the peak magnitude of the current in the inductor is also proportional to Q. Thus, equation (2.11) exemplifies the costly disadvantage of employing second order techniques to power conversion: L,

C, and the semiconductor switches must be expensive components with high stress tolerances.

With this brief overview of second order systems complete, specific resonant topologies are presented below.

2.1.2 The Series Resonant Converter

Consider the series resonant converter schematic presented in Fig. 2-5. By lumping

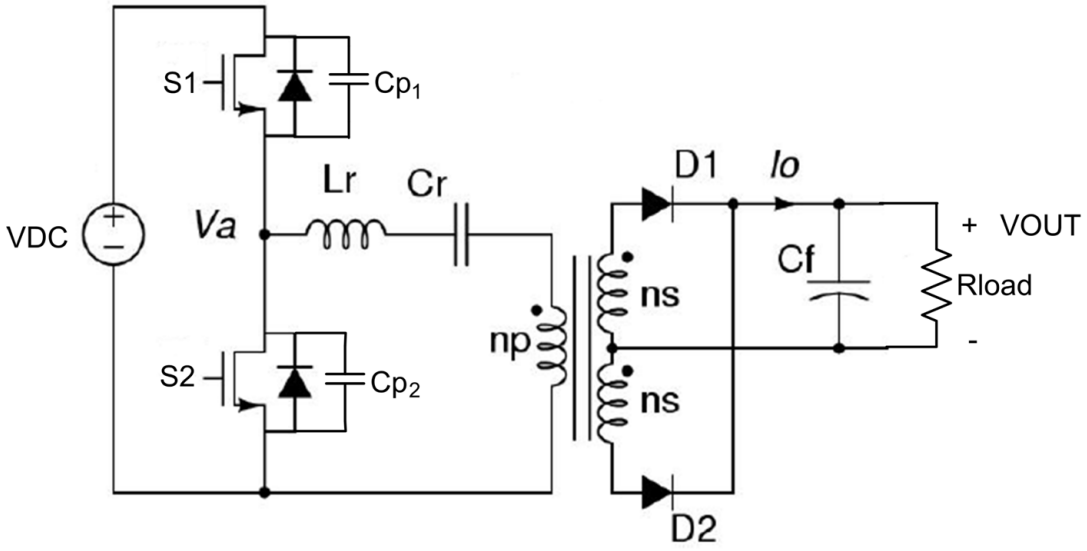

Figure 2-5: Half Bridge Series Resonant Converter

the transformer, output rectification diodes, and resistor R_{load} into one primary side impedance, R_{eff}, this system can be modeled as a series RLC circuit with square wave drive at node V_a. L_r and C_r form a resonant tank, with $\omega_0 = \frac{1}{\sqrt{L_r C_r}}$, and are in series with the effective load. Thus, the admittance relation of (2.7) holds for this converter topology [6].

Given the results of the previous section, the full fundamental component of the drive voltage waveform appears across the resistor R_{eff} at resonance, and, therefore, maximum power is transferred to the load at this frequency. Running the converter off of resonance introduces finite tank impedance, reducing the output voltage magnitude, and the power delivered to the load.

Fig. 2-6 shows a graph of output voltage gain versus normalized switching frequency for various values of Q. As expected, the maximum gain is 1. This converter is

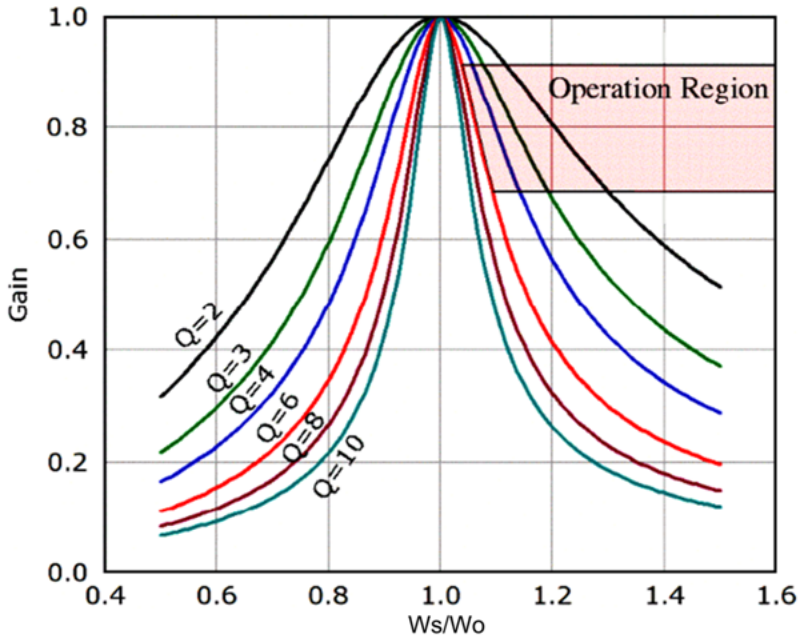

Figure 2-6: Gain Characteristics for the Series Resonant Converter [12]

designed to nominally operate above resonance, such that variations in input voltage can be compensated for by increasing or decreasing the switching frequency.

The chosen operating region also ensures that the LC tank impedance always looks inductive, i.e. the current will lag the voltage at node V_a. This is one of the most important design considerations for a resonant converter, for when the drive current lags the drive voltage, switches S_1 and S_2 can transition with no voltage across them. The switching loss in the converter, therefore, will be roughly eliminated [6].

To further understand the notion of zero voltage switching, a detailed review of one switching period is presented below. Assume first that S_2 is off and S_1 has not yet turned on. The circuit corresponding to these conditions is shown in Fig. 2-7. Notice that the primary side current, I_p, is negative. With S_2 off, I_p forward biases the body diode of MOSFET switch S_1, and leaves the device free to turn on with minimal voltage across it. Sometime later, the current I_p reverses direction and becomes positive. When S_1 turns off, I_p commutates to C_{p1}, and the switch voltage

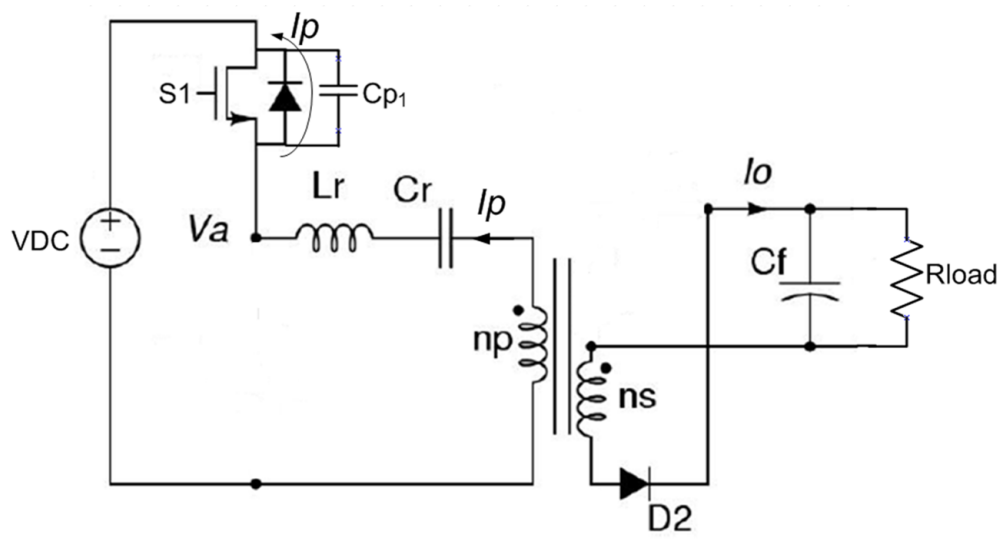

Figure 2-7: SRC Equivalent Circuit: S_1 and S_2 Off, I_p Negative

slowly charges up to V_{DC}, implementing another transition where switch voltage is negligible.

Once C_{p1} is fully charged, I_p begins to flow through the body diode of S_2, allowing that switch to turn on with minimal voltage. This situation is presented in Fig. 2-8. At the end of the S_2 conduction cycle, I_p has reversed again, and is now flowing in

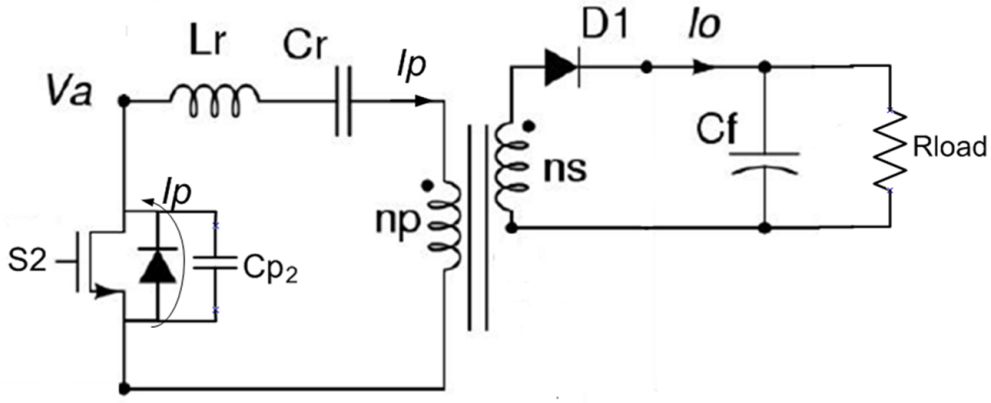

Figure 2-8: SRC Equivalent Circuit: S_1 and S_2 Off, I_p Positive

the negative direction. When S_2 turns off, I_p commutates to C_{p2}, and yields a final

lossless transition as described above. I_p then begins to flow through the body diode of S_1, and the entire cycle repeats.

In summary, the series resonant converter can control power delivered to a load by varying its switching frequency about the resonant frequency of its LC tank. If the converter is run nominally above resonance, all of the switch transitions will be lossless. This fact allows operation at very high frequency without an appreciable loss of converter efficiency, and, consequently, yields a converter with very high power density.

Certain inherent flaws, however, render this converter unsuitable for many applications. Primarily, as the quality factor of the system decreases, the converter must run at higher and higher frequencies to properly regulate its output voltage. Thus, in situations where the load and input voltage are variable, the series resonant converter will have an extremely wide switching frequency range. Given that more current circulates in the energy storage elements the further away from resonance the converter operates, more power will be dissipated in the parasitic components of those elements [12]. Therefore, efficient regulation over a wide input and load range is impossible, and the need for a more robust topology is clearly evident.

2.1.3 The Parallel Resonant Converter

A schematic of a parallel resonant converter is presented in Fig. 2-9. This topology places the load in parallel with resonant capacitor C_r, rather than in series with it. The filter inductor L_f is used to match impedances between the primary and secondary sides of the transformer, and does not affect the resonant frequency of the system [12]. A graph of the output voltage gain versus normalized switching frequency is given in Fig. 2-10. As shown, the operating region for this converter is above resonance. Much like in the series resonant converter, this frequency range ensures the ability to regulate against input voltage variation, and yields zero voltage switching for both S_1 and S_2.

When examining light load regulation, it is important to note that Q for this system increases in proportion to the value of load resistance. Thus, as the converter

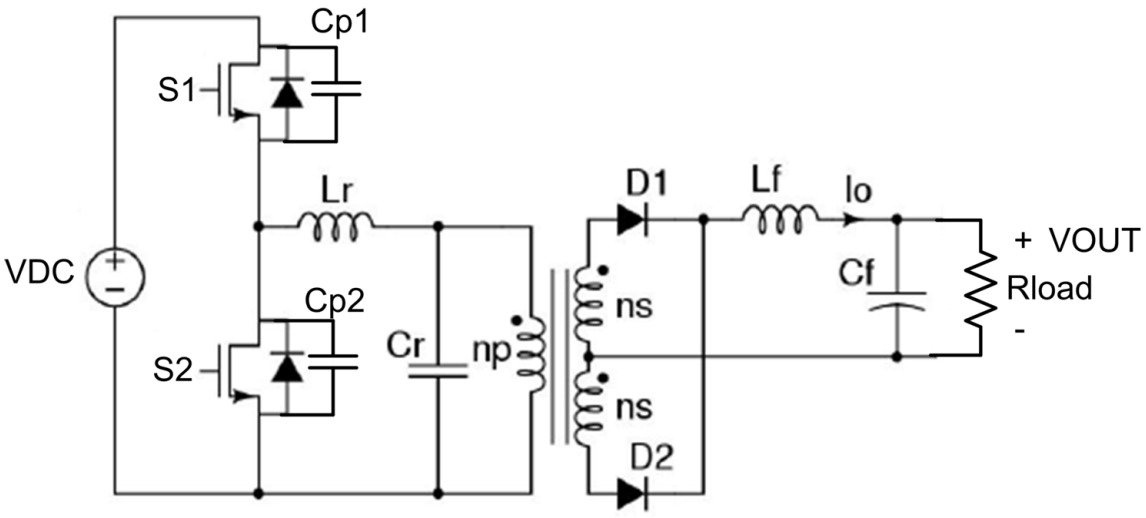

Figure 2-9: Half Bridge Parallel Resonant Converter [12]

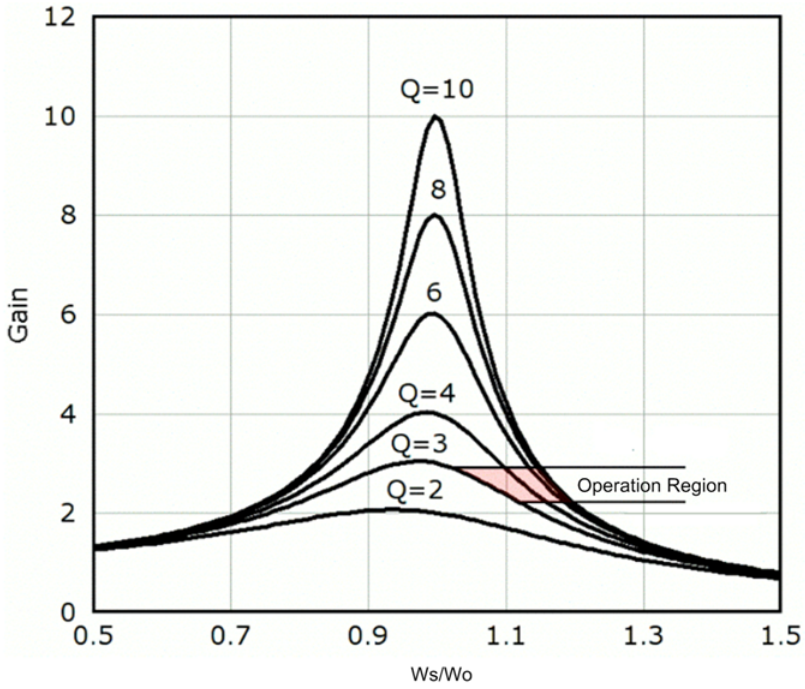

Figure 2-10: Gain Characteristics for the Parallel Resonant Converter [12]

load lightens, the gain curve in Fig. 2-10 steepens, and less frequency shift is necessary to regulate the output voltage. The circulating current in the resonant tank, however, increases dramatically with decreasing load, and results in significant power dissipation in the parasitic components of the energy storage elements. As derived in [12], the energy lost due to circulating current in a parallel resonant converter is higher than the corresponding energy loss in a series resonant converter. This converter, therefore, is not suitable for efficient operation in applications with widely varying loads and input voltages.

2.1.4 The LLC Resonant Converter

As just described, the series and parallel resonant converter topologies are unideal choices for power systems without stable loads and input voltages. Deviations from their nominal operating points lead to noticeable efficiency degradation. Additionally, both of these converters are designed to operate above their respective resonant frequencies (to ensure ZVS and bidirectional output voltage control), which inherently imposes finite circulating energy loss [12].

Consider now the LLC resonant converter topology presented in Fig. 2-11. This

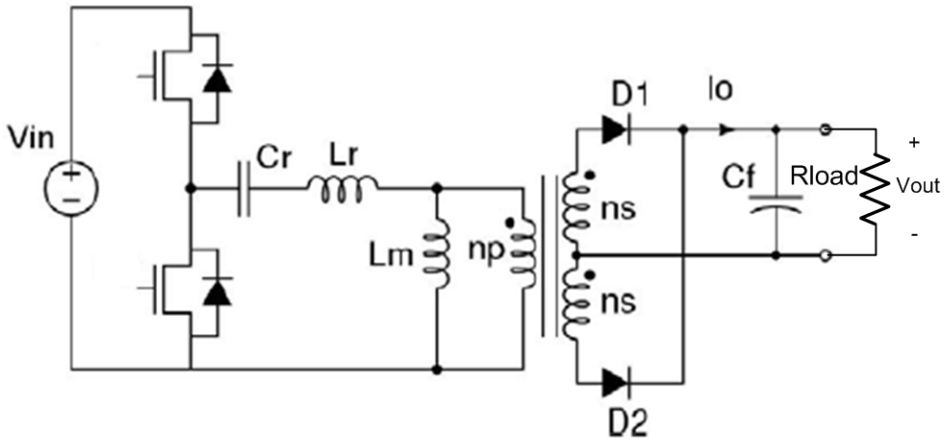

Figure 2-11: Half Bridge LLC Resonant Converter [12]

schematic looks much like that of the SRC, but an additional inductor has been placed in series with the load. A relatively simple addition, this inductor has significant

effects on the dynamics of the system. Specifically, two resonant frequencies now exist, and are given by [12]

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.12}$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2.13}$$

A graph of the DC gain characteristics of this converter is shown in Fig. 2-12. In this graph, f_{r1} occurs at $\frac{f_s}{f_r} = 1$. Note that Q for this system is equal to

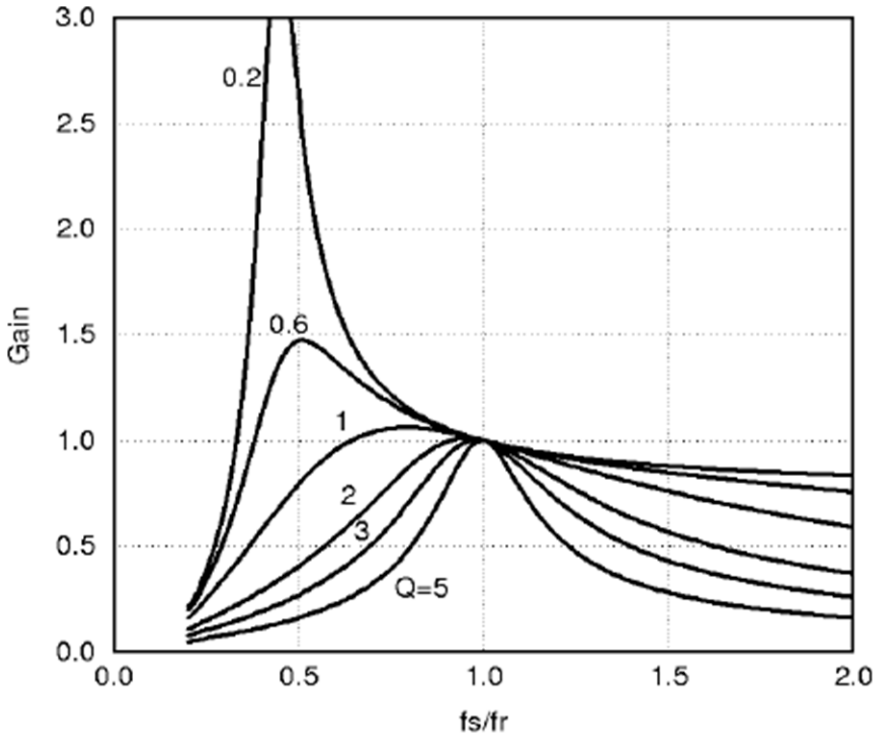

Figure 2-12: Gain Characteristics for the LLC Resonant Converter [12]

$$Q = \frac{1}{R_p}\sqrt{\frac{L_r}{C_r}} \tag{2.14}$$

where R_p is the reflected load impedance on the primary side of the converter. After quick inspection, fig. 2-12 looks much like a combination of the DC gain characteristics of the SRC and PRC. At the lower resonant frequency, f_{r2}, the dynamics of the

PRC dominate, while at the higher resonant frequency, f_{r1}, the dynamics of the SRC dominate [12]. Thus, this converter can both step up and step down its input voltage by switching below or above f_{r1}.

As evident, a load independent operating point exists at the upper resonant frequency. Designing the converter to nominally operate at this frequency yields the ability to regulate the output voltage down to zero load without switching off of resonance. Loss due to circulating energy, therefore, is minimized, for the impedance of the resonant tank goes to zero and no net current reactively flows between the energy storage elements [4]. Additionally, for careful balancing of load conditions and allowable input voltage range, this converter can remain in the inductive region for regulative switching above and below f_{r1} [9]. This fact enables ZVS for all designed operating conditions and minimizes the semiconductor switching losses. A final benefit is a boost in power density achievable by magnetically integrating L_r and L_m as the leakage and magnetizing inductances of the transformer.

In summary, the LLC converter does not suffer from the same limitations that plague the SRC and PRC. Energy lost due to circulating current in the resonant tank is minimized by the load independent operating point at f_{r1}. Variations in allowed input voltage can be efficiently regulated against by switching above *or* below f_{r1}, while still maintaining ZVS conditions for the power semiconductor devices. Also, power density increases beyond that of a general resonant converter when magnetic integration techniques are used.

This topology, therefore, is very popular for use as the primary power conversion stage for systems requiring up to 500 W. Efficiencies as high as 93% have been reported for implementations of the system as drawn in fig. 2-11 [4]. Topologies that employ synchronous rectification techniques, however, report efficiencies up to 96% [4]. These extra few percentage points can make the difference between a system that receives government mandated efficiency certification and one that does not. Thus, synchronous rectification controllers for this topology are extremely valuable, and the design of one such controller is the subject of the first part of this thesis document. Before going through the design and operation of this LLC secondary side

synchronous rectification controller, a brief discussion of synchronous rectification itself is appropriate.

2.2 Synchronous Rectification

The concept of SR is best understood by going back to the buck converter of fig. 2-1. In the previous section, the efficiency degradation associated with the switching transitions of S_1 was explained, but the power loss due to diode conduction was neglected, as the diode was assumed to be ideal. In a real system, however, a conducting diode has a forward voltage drop given by

$$V_f = V_T \ln \frac{I_f}{I_0} \tag{2.15}$$

where I_f is the forward biased current through the device, V_T is the thermal voltage, and I_0 is a device specific parameter that depends on the doping, diffusion coefficient, and physical length of the actual diode [10]. Noting that the power dissipated in any device is equal to the voltage across the device times the current through the device, average diode power loss in the buck converter can be expressed as

$$P_{diode} = (1 - D)V_T I_{out} \ln \frac{I_{out}}{I_0} \tag{2.16}$$

where I_f in (2.15) has been replaced by the average converter output current I_{out}. Thus, as the load demand on the system increases, so does the conduction loss of D_1.

Now consider replacing D_1 with MOSFET switch S_2. Assume the proper circuitry exists such that S_2 is off whenever S_1 is on, and vice versa. This control scheme is called synchronous rectification. The corresponding average conduction loss due to S_2 is

$$P_{s2cond} = (1 - D)I_{out}^2 R_{DSon} \tag{2.17}$$

where $R_{DS,on}$ is the on state resistance of the switch.

In order to compare these two loss mechanism, we must first define some reference

parameters. For a diode, typical values of the saturation current I_0 for a power device are on the order of 10^{-12} A. For a power MOSFET, a respectable value for $R_{DS,on}$ is roughly 20 mΩ, assuming a cost conscious design methodology [10]. Using these values, the following table compares the conduction losses of the two different rectification devices in the buck converter for increasing values of load current.

I_{load} [A]	R_{DSon} Loss [W]	Diode Loss [W]
1	.02	.68
5	.5	3.6
25	12.5	19
50	50	39

As can be seen, synchronous rectification yields vast improvements over diode rectification at low current levels. As the demand for power increases, however, the benefit of using SR quickly diminishes, and above a certain output power level, vanishes altogether. A graph of these results is presented in fig. 2-13, where the shaded region indicates conduction loss savings by using SR.

It is important to understand that the analysis above neglects the additional switching loss introduced by S_2 turn off transitions in the buck converter system. For this reason, SR is not an extremely useful tool in the design of *hard* switched converters. In the LLC resonant converter, on the other hand, no additional switching loss is added to the system by the inclusion of synchronous rectification MOSFETs. Turn on transitions are lossless given that the control circuitry waits until the body diode of the proper SR FET is forward biased before applying power to its gate. Turn off transition are similarly lossless, given that the current in the SR FET decays to zero at the turn off instant, assuming discontinuous conduction mode. Thus, for the power levels where R_{DSon} conduction loss is lower than diode conduction loss, SR directly improves the efficiency of an LLC resonant converter.

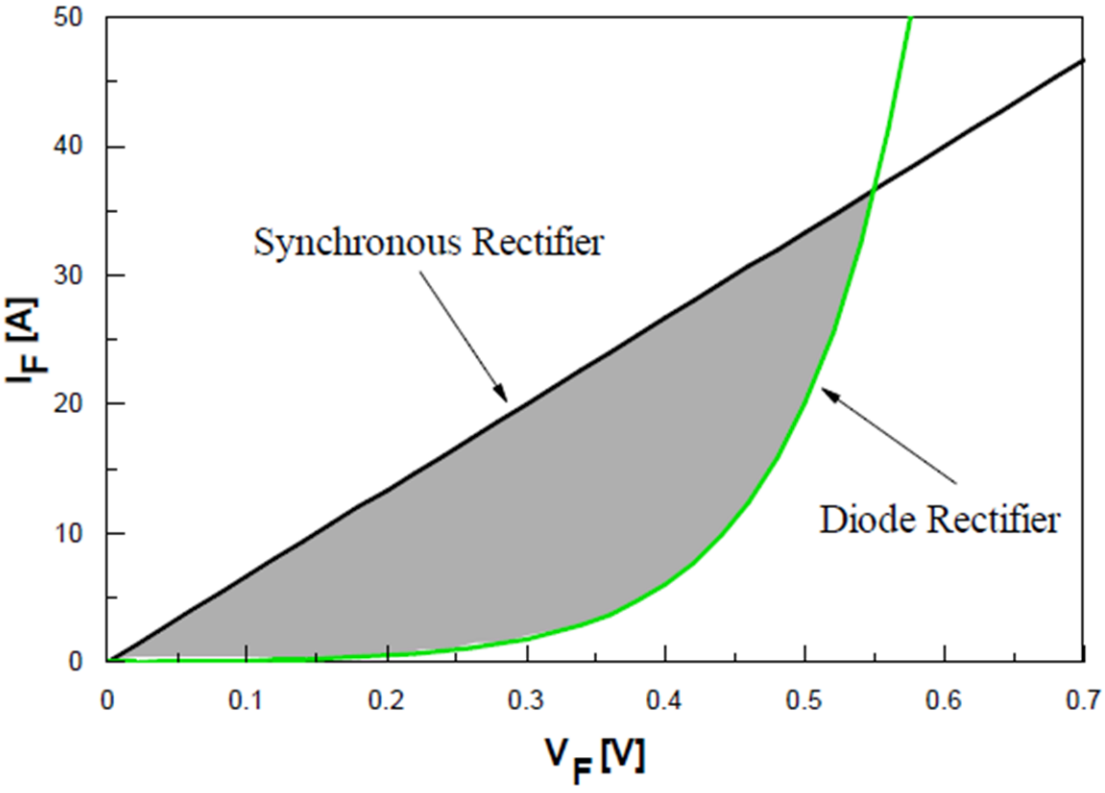

Figure 2-13: Forward Voltage to Current Comparison of an SR FET and a Diode [12]

2.3 Integrated Controller Challenges

While the concept of synchronous rectification (SR) is relatively simple to understand, designing an integrated circuit that accurately and efficiently implements the proper secondary side control scheme is non-trivial. Additionally, for a chip to be accepted in the industrial marketplace, it must function over a wide variety of different operating conditions, further complicating the design process.

The first major hurdle involves sensing when to turn off the SR FET. Given that most LLC converters nominally operate in the discontinuous conduction mode, the gate of the SR FET must be immediately brought low once the current flowing through the device decays to zero. If the SR FET is turned off too soon, an inefficient body diode will complete the conduction cycle and negate any potential power savings. If the SR FET is turned off too late, output current will begin to flow through the converter in reverse, potentially damaging system components and decreasing overall efficiency. A common solution to this problem involves accepting the lesser of two evils by sensing the voltage from source to drain across the SR FET, and turning off the device before current has completely decayed. This method of control is sub-optimal.

The second challenge involves possible system operation in continuous conduction mode. Here, signals from the primary side must be coupled into the secondary side controller to dictate proper operation of the SR FETs. Very few industrial SR solutions include the option for primary synchronization, thus CCM performance is extremely weak.

The third challenge involves designing an IC that will function over a very wide range of supply voltages. Given that the most efficient way to power a secondary side controller is from the converter output itself, an IC must be rated for operation at all possible system output voltages in which it will be used. Additionally, packaging constraints do not allow for an internal power bypass pin, thus the on-chip power buffer must be designed to reliably operate without the aid of bypass capacitors.

The fourth challenge relates to the design of accurate IC timing circuitry. A voltage mode SR controller must generate timing pulses that blank the internal detection

circuitry for a specific amount of time to prevent false turn on and turn off events. The details of this requirement will be discussed in the next chapter, but due to the variation in component values introduced by the manufacturing process, design of high accuracy timers and pulse generators is a difficult task [3].

The final criteria is true of any industrial integrated circuit used in a power system, specifically, the need for low standby current and minimal steady state power consumption.

All of these aforementioned concerns are addressed by the LLC secondary side SR controller presented in Chapter 3 of this document. Unlike any other commercially available SR controller, this chip consistently implements a complete SR FET conduction cycle for converters switching at frequencies of up to 1 MHz, thereby maximizing the theoretical efficiency gains of systems in DCM [6]. Additionally, this controller provides a primary synchronization input pin, enabling high performance operation in the continuous conduction mode. Note that power consumption in standby and normal modes is also kept at a minimum. Schematics, operational statistics, and simulation data for all the circuit blocks in this converter are discussed next.

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Chapter 3

LLC Secondary Side Synchronous Rectification Controller

To address the difficulties associated with implementing a synchronous rectification scheme, an integrated secondary side controller for the LLC converter has been designed using a proprietary Texas Instruments silicon process technology. Target output power levels for systems using this controller are in the range of 90 - 500 W (depending on the end application), with output voltages ranging from 12 - 48 V at switching frequencies up to 1 MHz.

These broad specifications introduce unique challenges into the IC design process that are seldom discussed in an academic setting. Most notable is the construction of circuits that produce exact reference currents and voltages that are independent of supply variation. Additionally, in order meet industrial and consumer product standards, this controller must reliably function over a temperature range of -50 - 150 $^{\circ}C$. Thus, the temperature dependence of every device included in a given design schematic must be carefully considered, and methods to assure temperature independence of critical quantities become essential.

Variation due to the manufacturing process presents yet another design variable that is normally ignored in the classroom. Specifically, slight drift in the prescribed dimensions of semiconductor devices can yield noticeable inaccuracies between calculated and experimental circuit parameters. Care must be taken, therefore, to intelli-

gently hook up and size devices so as to minimize the effects of process variation on a particular circuit. Layout techniques, such as including dummy devices and using common centroid configurations [5], can be useful to help match critical devices, but the overall benefits are limited.

When verifying a particular design using simulation, it is vital to consider the effect of process variation on circuit performance. This fact motivates the use of Monte Carlo simulation, a method that randomly varies system parameters based on a predetermined statistical distribution [8]. If enough sequential simulations are performed, relevant output statistics can be computed for quantities of interest, and performance over manufacturing process variation can be assessed. In this way, Monte Carlo simulation can help hone particular topological choices, such that the number of real ICs that meet certain standards is maximized. Given that every chip sold must conform to the specifications laid out in its data sheet, it is desirable to maintain the ratio of marketable to unmarketable chips per silicon wafer as high as possible. The use of Monte Carlo simulation techniques helps maximize the functional device yield, reducing wasted resources and increasing overall profitability.

This chapter is dedicated to the exploration of the particular design choices involved in the creation of the secondary side SR controller mentioned above. Schematics of essential circuit blocks and simulated data on the chip's performance are presented. As implied, individual circuit evaluation relies heavily on Monte Carlo generated data. The discussion proceeds logically, beginning with an overview of the system level operation, proceeding to the specifics of the internal circuitry, and concluding with top level simulation results. Due to a binding non-disclosure agreement, however, specific component values and device sizes have been omitted from all the figures found below.

3.1 System Level Operation

Fig. 3-1 shows a typical application diagram of the aforementioned controller in an LLC resonant converter. Note that the designation UCC24600 is the Texas Instru-

ments part number for this IC. As evident, both secondary side FETs require their

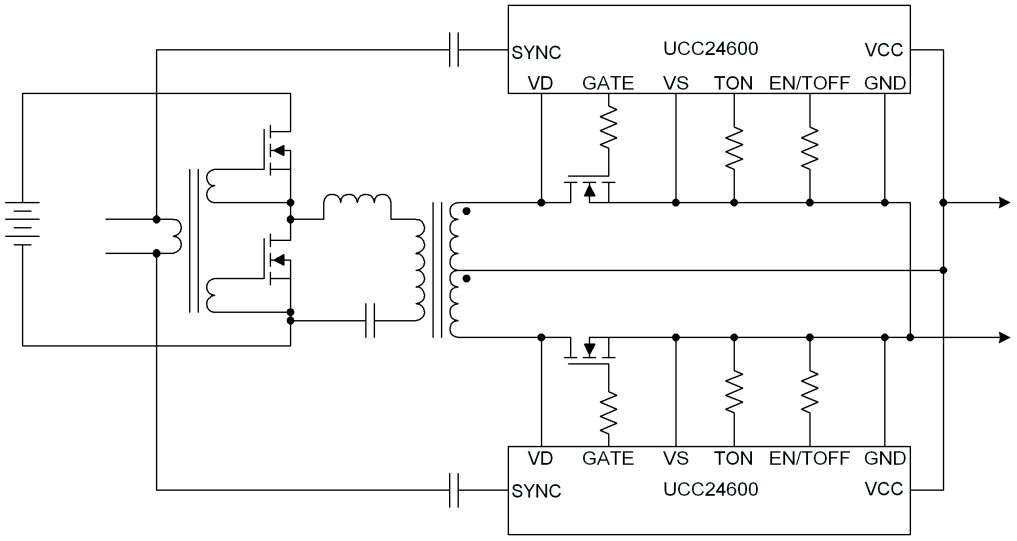

Figure 3-1: Typical Application Diagram

own controllers, thus two chips are necessary for each desired output stage. Additionally, this controller uniquely allows for converter operation in the continuous conduction mode, using primary side signals received on the *sync* pin to coordinate proper switching.

To better understand the operation of this controller, consider the block level diagram, shown in Fig. 3-2, and the typical timing waveforms, shown in Fig. 3-3. Assuming first discontinuous conduction mode, steadily increasing current flow forward biases the body diode of one of the secondary side FETs at the beginning of its conduction cycle. The corresponding voltage drop from source to drain is enough to trigger the -100 mV comparator, which instructs the controller to bring the gate drive output high, turning on the synchronous rectification (SR) FET. Given that the magnitude of voltage across the SR FET immediately drops, the minimum on timer (MOT) is also triggered by the -100 mV comparator, ensuring that the gate drive signal remains high for a user programmable amount of time. After the MOT expires, the controller waits for the output current to decay such that the voltage from source to drain across the SR FET is roughly $V_{th,off}$. At this threshold, the -3 mV comparator is triggered, and the gate drive signal is brought low. Due to parasitic voltage ringing

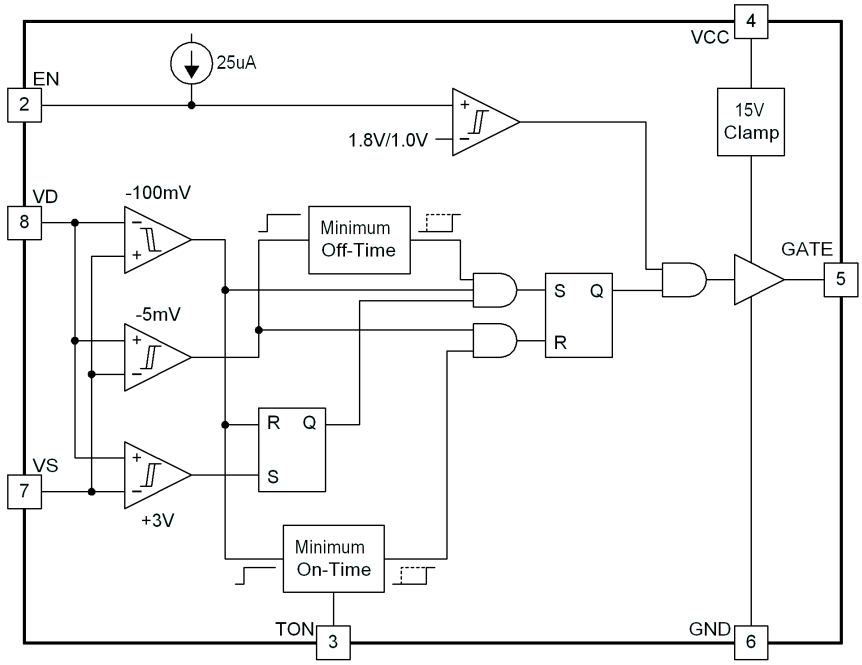

Figure 3-2: Synchronous Rectification Controller Block Diagram

on the drain of the SR FET after turn-off, a user programmable minimum off timer (MOFFT) is initiated to prevent spurious turn-on signals. Only after the MOFFT has expired *and* the drain voltage has risen above $V_{th,reset}$ (implying the other SR FET is conducting) is the system armed and ready for another conduction cycle.

In continuous conduction mode, the current in the SR FET never decays to zero. Turn off, therefore, is dictated by the coupling of the primary side switching signal to the secondary side controller through the sync pin and an AC coupling capacitor. Otherwise, operation is identical to the process described above.

The following is an overview of the function of each pin on the IC:

SYNC (CCM Turn-off Synchronization) - A falling edge on SYNC forces GATE low, turning off the SR MOSFET without regard to the voltage across its drain and source. When a power converter is operated in CCM, it is necessary to turn off the SR MOSFET under command of the primary control circuit. SYNC must be connected, therefore, to a control signal on the primary side of the converter using a high-voltage isolation capacitor or transformer. This pin is not shown in Fig. 3-2 due

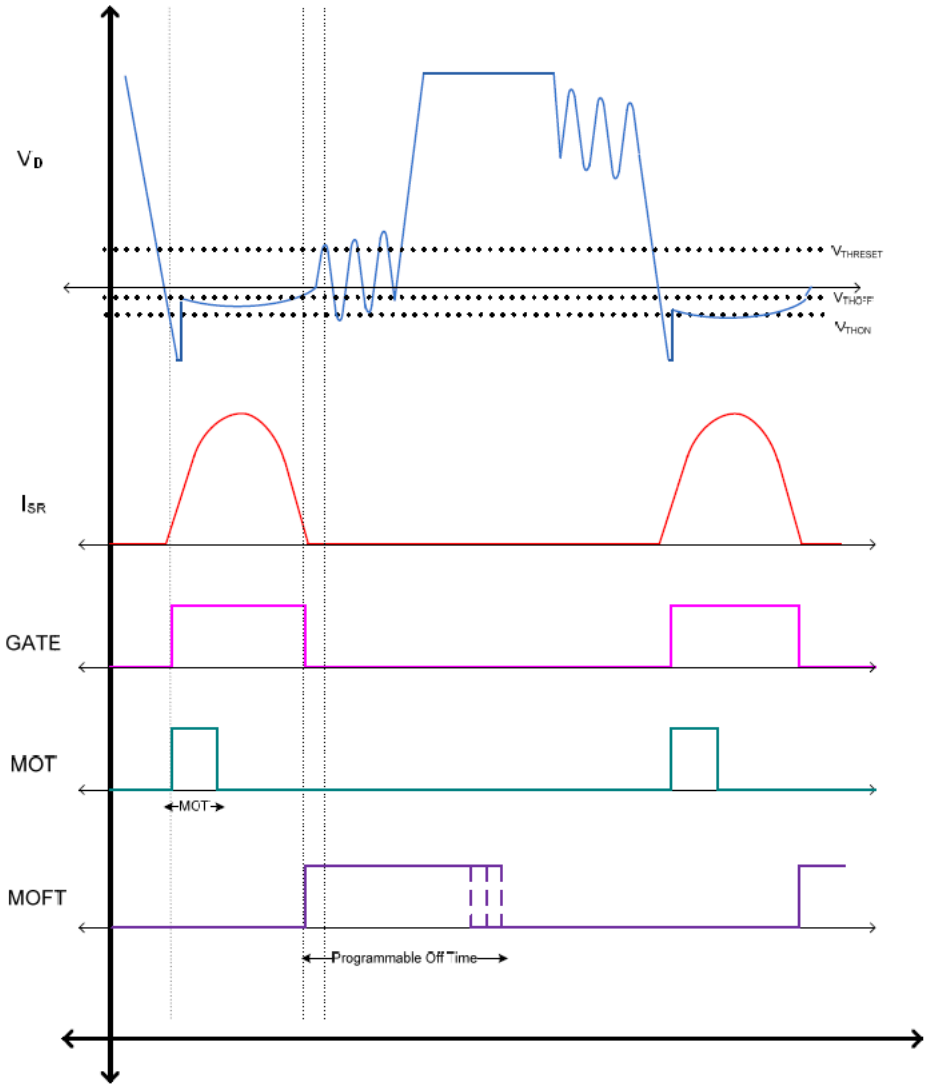

Figure 3-3: Conduction Cycle Timing Waveforms

to intellectual property concerns.

EN (Enable, Programmable Off Time) - When EN is low, the UCC24600 is in sleep mode. When EN is above its turn on threshold, and V_{CC} is greater than $V_{CC,on}$, the UCC24600 is in run mode. The voltage level on EN also programs the minimum off timer, as will be discussed later. EN is internally pulled high by a 25 μA current source, so the voltage level on this pin can be set by connecting a resistor from EN to GND.

T_{on} **(Programmable On Time)** A resistor from T_{on} to GND programs the minimum on timer, as will be discussed later.

V_{CC} **(Positive Power Input)** - V_{CC} supplies power to all circuits in the UCC24600. Comparators in the under-voltage lock out (UVLO) block prevent operation until V_{CC} rises above $V_{CC,on}$. V_{CC} can be used to safely turn off the UCC24600 by pulling it below $V_{CC,off}$, in which case GATE immediately falls.

GATE (SR MOSFET Gate Drive) - GATE is a high current output port used to quickly turn on and off the SR MOSFET. It is internally clamped to 15 V.

GND (Analog, Digital and Power Ground) This pin serves as the reference potential for all the circuitry inside the IC.

V_S **(Source Voltage Sense)** - This pin is used as the potential reference for the voltage across the SR MOSFET.

V_D **(Drain Voltage Sense)** - This pin is used to determine the switching operation of the SR MOSFET. In a steady state LLC resonant converter, this pin fluctuates between ground and twice the converter output voltage [6].

Having briefly discussed the system level operation of the chip above, individual circuit blocks are presented in the subsequent sections.

3.2 Under Voltage Lock Out

An intelligent interface with the external converter system, this block determines whether or not enough voltage has been applied on the V_{CC} pin to reliably run all of the internal circuitry, and makes sure the EN pin voltage is above the proper threshold

for normal operation. A full schematic of this block can be seen in Fig. 3-4. Given the number of devices that comprise this circuit, however, the UVLO block has been divided into two sub-blocks, which are discussed in detail below.

3.2.1 Supply Independent Current Source

In order to supply power to those devices that operate when the system is in sleep mode, a low overhead, supply independent current source is necessary. Fig. 3-5 shows a schematic of this current source as it is implemented in the UVLO block. This circuit develops a stable, temperature and supply insensitive reference current, I_{out}, that is used to bias the rest of the startup circuits in the IC.

To find an analytical value for I_{out}, consider KVL around the loop comprised of R_3 and the four bipolar transistors:

$$V_{R3} + V_{be3} + V_{be0} = V_{be1} + V_{be2} \tag{3.1}$$

Rearranging terms and noting that

$$V_{bex} = \frac{KT}{q} ln \frac{I_{CX}}{I_{SX}} \tag{3.2}$$

where $\frac{KT}{q}$ is the thermal voltage, and Icx and Isx are the collector and saturation currents respectively of device x, the voltage across R_3 can be expressed as

$$V_{R3} = \frac{KT}{q}[ln\frac{I_{out}}{I_{S1}} + ln\frac{I_{in}}{I_{S2}} - ln\frac{I_{in}}{I_{S0}} - ln\frac{I_{out}}{I_{S3}}] \tag{3.3}$$

By collapsing the ln terms and dividing by R_3, I_{out} becomes

$$I_{out} = \frac{KT}{qR_3} ln \frac{I_{S0}I_{S3}}{I_{S1}I_{S2}} \tag{3.4}$$

Thus, the output current of the circuit is dependent only on the device geometries of Q_0 - Q_3 and the value of R_3. As long as there is enough voltage headroom to bias all of the devices in their active regions, the supply voltage has no effect on I_{out}.

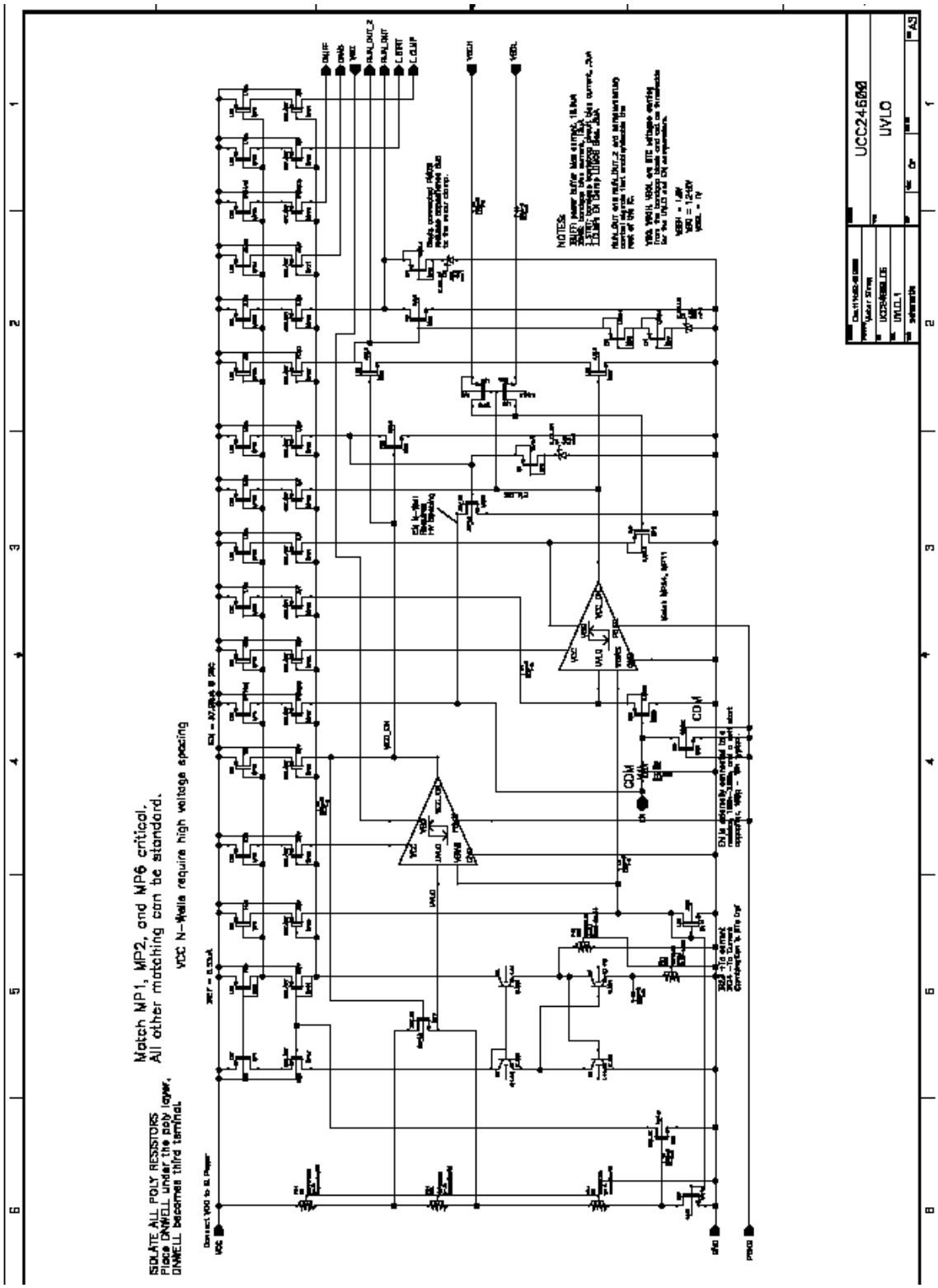

Figure 3-4: Full UVLO Schematic Diagram

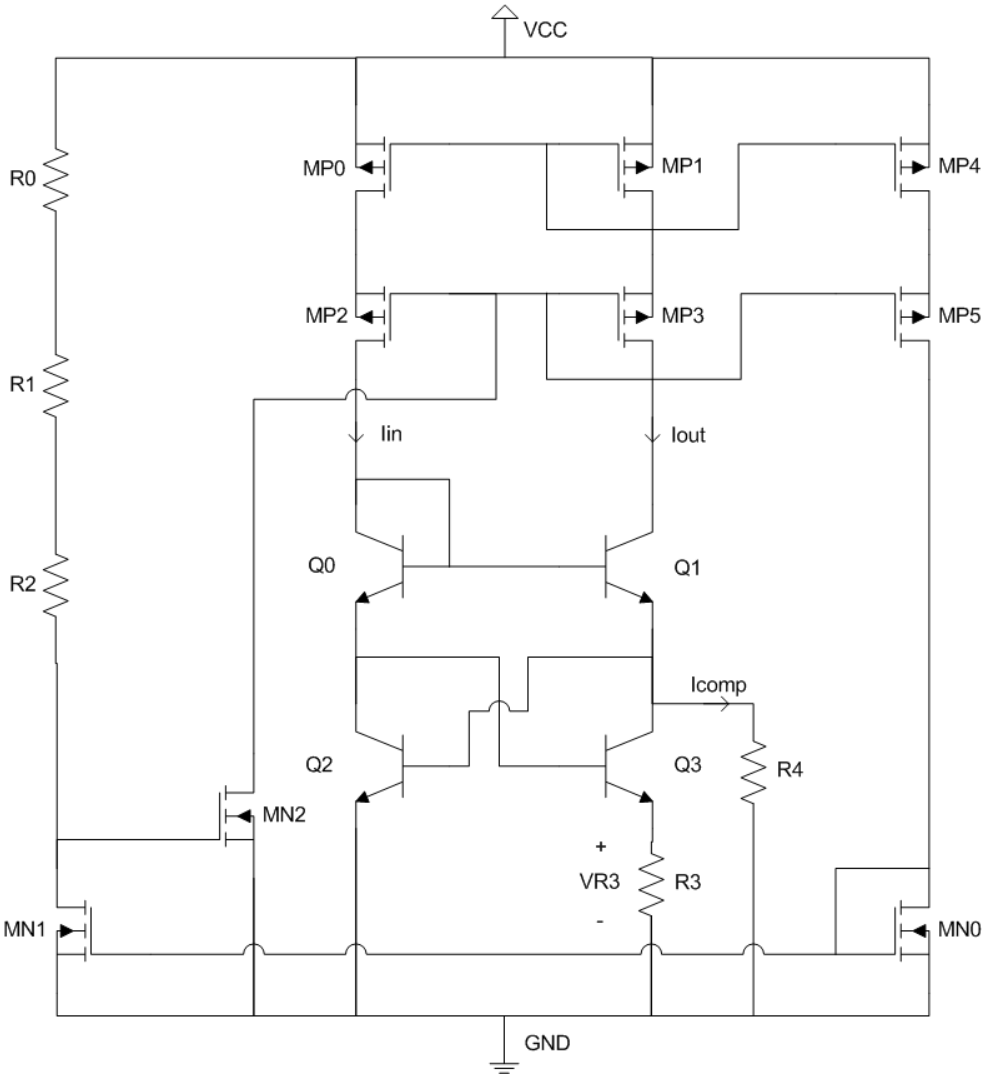

Figure 3-5: Supply Independent Current Source Schematic

In terms of temperature, I_{out} is evidently proportional to absolute temperature (PTAT), as shown in (3.4). To counteract this effect, the resistor R_4 is placed from the base of Q_2 to ground. Given that the base-emitter drop of a bipolar transistor has a negative temperature coefficient [2], as temperature increases, I_{comp} will decrease while I_{R3} increases. For the proper weighting of R_3 and R_4, I_{out} will remain unaffected by variations in temperature. It is important to note that this analysis ignores the temperature dependence of the resistors themselves, however, if they are made of the same material and carefully matched, their individual temperature coefficients will tend to cancel.

As can also be seen in Fig. 3-5, the current source is loaded by a p-channel cascoded current mirror. This construction yields two stable operating points for the circuit. The first is where the desired values of I_{out} and I_{in} flow in the proper legs, and the second occurs when no current flows in any of the devices. To avoid the zero current state, transistors M_{N0}, M_{N1}, M_{N2}, M_{P4}, and M_{P5} are used to form a "kick start" circuit.

Consider the case when V_{CC} starts at zero and slowly ramps up to a higher voltage. Initially, no current flows through the system, and all transistors in the circuit are cutoff. When V_{CC} rises above the threshold voltage of M_{N2}, however, the drain of that transistor pulls down on the gates of M_{P2} and M_{P3}, allowing current to start flowing through the primary mirror. The circuit quickly breaks away from the zero current state, and regenerates itself until the second stable operating point is reached. To prevent M_{N2} from interfering with the steady state operation of the system, the current from M_{P1} and M_{P3} is mirrored to M_{P4} and M_{P5}, and then again to M_{N1} through M_{N0}. As M_{N1} starts to draw current, it pulls down on the gate of M_{N2}, turning off the transistor and effectively removing it from operation. Thus, the "kick start" circuit ensures that the current source never settles into the zero current state and does not interfere with normal function.

As mentioned previously, the current source supplies power to those blocks that operate when V_{CC} is below the turn-on threshold of the IC, specifically the UVLO comparators, the bandgap voltage reference, the internal power buffer, and the EN

node pull up current source. It is essential to accurately control how much current these circuits draw in sleep mode ($V_{CC} < V_{CC,on}$) in order to minimize system power consumption when the IC is disabled. This goal is achieved by using scaled versions of I_{out} to power the blocks.

Simulated data on the performance of the current source over temperature is now presented in the form of the EN node pull up current. This current is merely an amplified version of I_{out}. Fig. 3-6 is generated using centered process values, while Fig. 3-7 is generated using 100 Monte Carlo simulation runs where process parameters are allowed to vary.

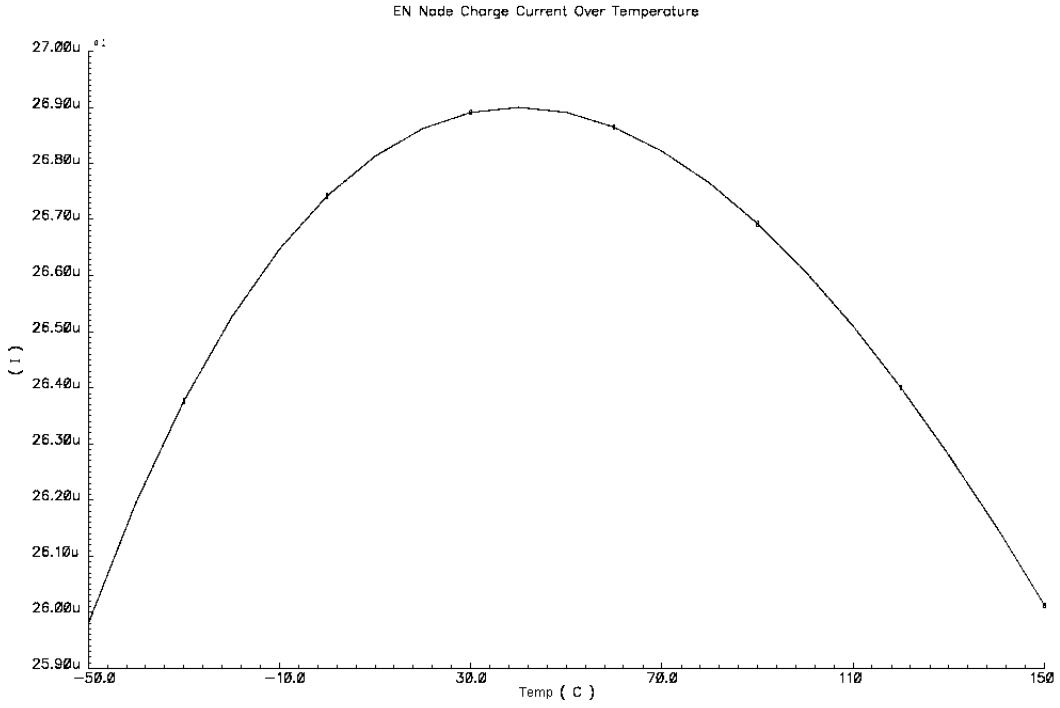

Figure 3-6: EN Node Pull Up Current Over Temperature; $V_{CC} = 20$ V

As evident, the temperature dependence is not completely zero, but specific design choices yield an average value of 25 μA over an extremely wide temperature range.

The remaining devices in this circuit, specifically R_0, R_1, and R_2, are used to generate the $V_{CC,on}$ and $V_{CC,off}$ thresholds for the one of the UVLO comparators discussed below.

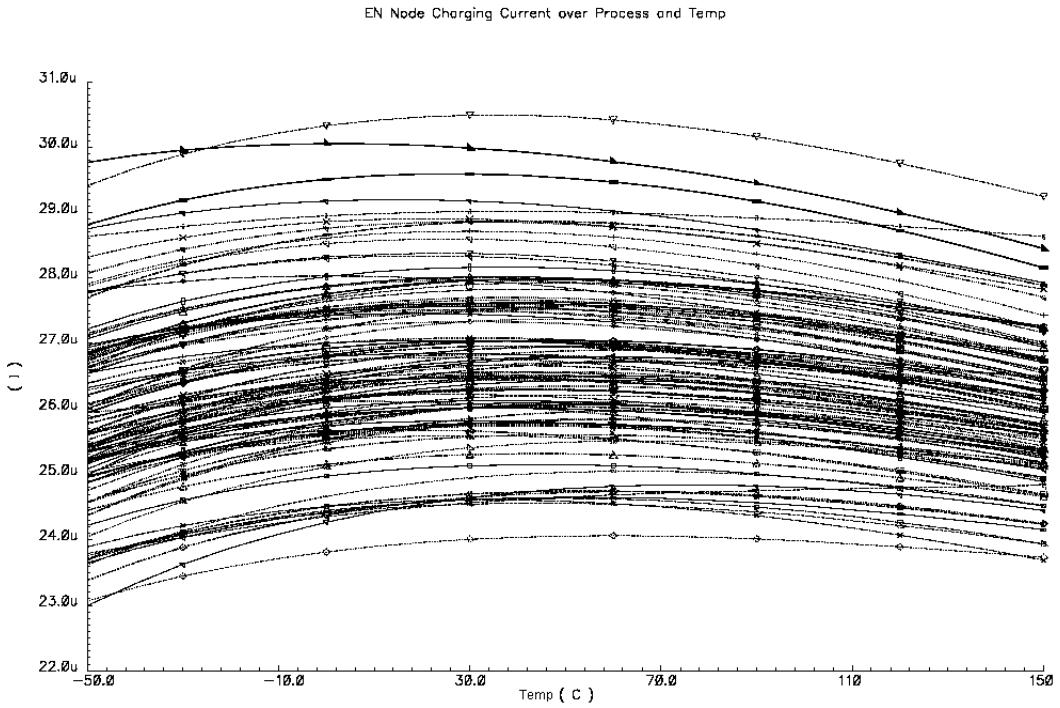

Figure 3-7: EN Node Pull Up Current Over Temperature; $V_{CC} = 20$ V; Monte Carlo

3.2.2 UVLO Comparator

To determine when the proper conditions for normal operation exist in the external converter system, the UVLO block has two identical comparators that monitor the voltages on the V_{CC} and EN pins respectively. A simplified schematic of the comparator system is presented in Fig. 3-8. As shown, $Comp_1$ and $Comp_2$ are fed with current sources derived from the supply independent source described above. Each comparator has a $Thrsh$ input against which the voltage on the In pin is compared. Run and Run_z are complementary output signals, generated by the two comparators and additional logic, that control the function of the rest of the IC, and V_{BG}, V_{BGH}, and V_{BGL} are voltages produced by the bandgap voltage reference. Not shown in the diagram are the transistors that keep the EN node grounded until V_{CC} rises above the $V_{CC,on}$ threshold.

To understand the operation of this sub-block, consider when V_{CC} is lower than $V_{CC,on}$. In this case, $V_{CC,ok}$ and EN_{ok} are both low, while Run and Run_z are inverted.

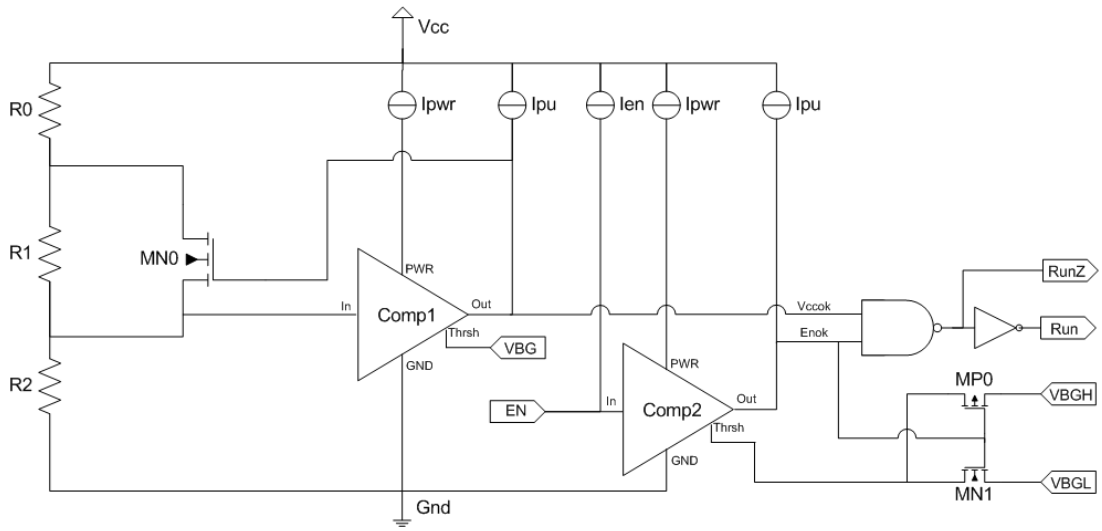

Figure 3-8: Simplified UVLO System Diagram

Noting that the gate of M_{N0} is connected to $V_{CC,ok}$, the V_{CC} turn-on threshold is given by:

$$V_{CC,on} = \frac{R_0 + R_1 + R_2}{R_2} V_{BG} \tag{3.5}$$

The turn-on threshold for the EN pin is dictated by the voltage on the $Thrsh$ pin of $Comp_2$, and is equal to V_{BGH}.

When V_{CC} rises above $V_{CC,on}$, $V_{CC,ok}$ transitions high, and allows the EN pull up current to begin charging the EN node. When the voltage on EN exceeds V_{BGH}, EN_{ok} also transitions high. These two events trigger Run and Run_z to be properly asserted, and the controller awakens from sleep mode and begins to draw its rated quiescent current from V_{CC}. Note that hysteresis is implemented differently for $Comp_1$ and $Comp_2$. When $V_{CC,ok}$ goes high, M_{N0} turns on, and the switching threshold for $Comp_1$ drops to

$$V_{CC,off} = \frac{R_0 + R_2}{R_2} V_{BG} \tag{3.6}$$

When EN_{ok} goes high, the voltage on the $Thrsh$ pin of $Comp_2$ is directly modulated through a complementary transmission gate, and the switching threshold drops to

$$EN_{off} = V_{BGL} \tag{3.7}$$

The actual schematic of the comparator that implements $Comp_1$ and $Comp_2$ is shown in Fig. 3-9, and consists of an NMOS differential input stage followed by two inverting common source gain stages. The comparator is fed by two current sources,

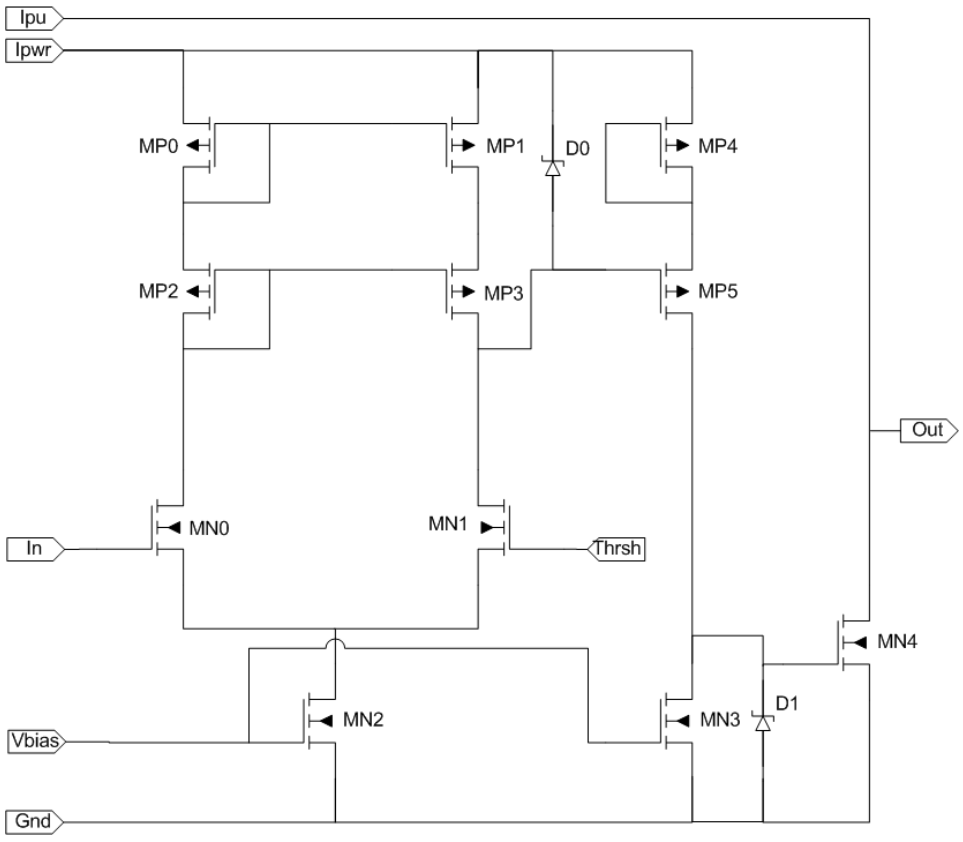

Figure 3-9: UVLO Comparator Schematic

where I_{pwr} supplies bias current to the input and intermediate gain stages, and I_{pu} supplies pull up current to the output gain stage. M_{N2} and M_{N3} are each biased with the same gate voltage, derived from the supply independent current source network, and split the current supplied by I_{pwr} between the first and second stages. Zener diodes D_0 and D_1 limit the voltage swing on the gates of M_{P5} and M_{N4} to protect the gate oxides of those devices, and to increase the turn-on speed of the entire comparator by decreasing the slewing time of those nodes.

Simulated performance data of this comparator is shown below. Note that R_0, R_1, and R_2 are sized such that $V_{CC,on} = 10.2$ V and $V_{CC,off} = 8.8$ V. V_{BGH} and V_{BGL} are designed such that $EN_{on} = 1.8$ V and $EN_{off} = 1$ V.

Fig. 3-10 is a graph of $V_{CC,on}$ and $V_{CC,off}$ at 25° Celsius, generated by 100 Monte Carlo simulation runs of the UVLO block. The average $V_{CC,on}$ and $V_{CC,off}$ thresholds are 10.19 V and 8.79 V respectively, and the standard deviations are .047 V and .040 V respectively. These values do not appreciably change as temperature is varied.

Fig. 3-11 is a graph of EN_{on} and EN_{off} at 25° Celsius, also generated by 100 Monte Carlo simulation runs of the UVLO block. The average EN_{on} and EN_{off} thresholds are 1.81 V and .988 V respectively, and the standard deviation is .009 V for both. These values do not appreciably change as temperature is varied.

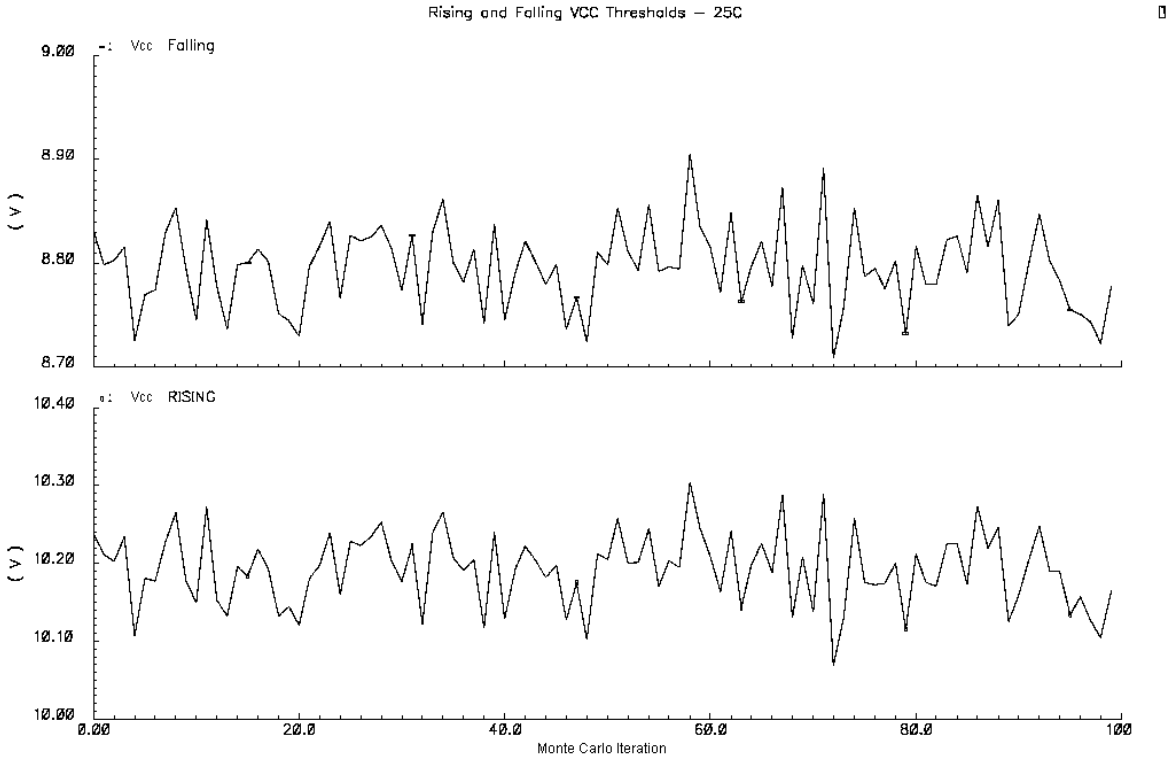

Figure 3-10: VCC Switching Thresholds over Process Variation at 25C

As a final note, any devices found in Fig. 3-4 and not explicitly discussed above are used as biasing elements or are not fundamental to the understanding of the UVLO block operation.

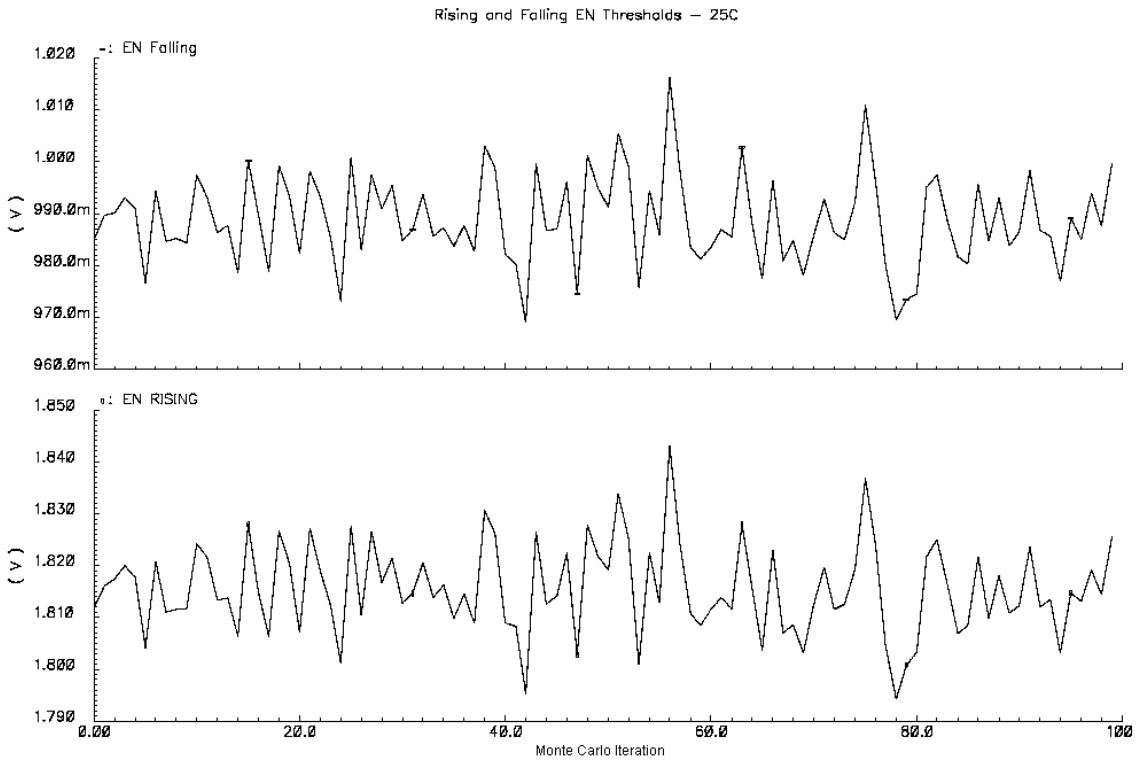

Figure 3-11: EN Switching Thresholds over Process Variation at 25C

3.3 Bandgap Voltage Reference

An important building block in any modern integrated circuit is a stable voltage reference. Using the fact that $V_{be,on}$ and V_T have opposite voltage temperature coefficients [2], it should be possible to construct a circuit that weights these two values to yield a temperature insensitive reference.

3.3.1 Canonical Bandgap Voltage Reference Operation

In order to understand the operation of such a reference, consider the hypothetical circuit shown in Fig. 3-12.

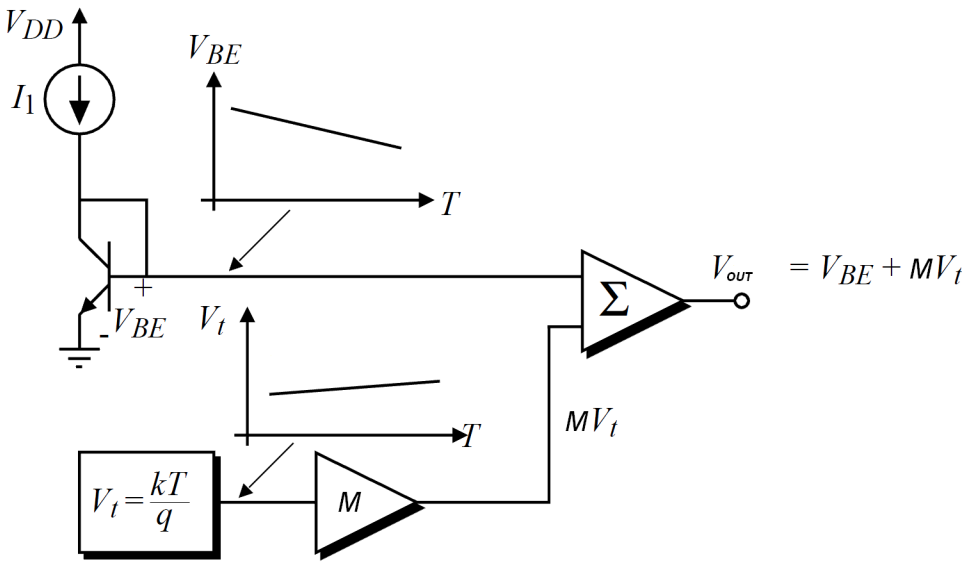

Figure 3-12: Ideal Bandgap Circuit

As shown, the output voltage is

$$V_{out} = V_{be,on} + MV_T \tag{3.8}$$

From the derivations carried out in [2], the quantities in (3.8) are given by

$$V_{be,on} = V_{G0} - V_T[(\gamma - \alpha)\ln T - \ln(EG)] \tag{3.9}$$

$$V_T = \frac{KT}{q} \tag{3.10}$$

where V_{G0} is the bandgap voltage of silicon at 0 K, γ and E are device specific parameters, and α and G are bias specific parameters. From these two equations, the negative temperature dependence of $V_{be,on}$ and the positive temperature dependence of V_T are evident. Thus, proper weighting of these two quantities should yield a temperature insensitive value. If (3.9) and (3.10) are substituted back into (3.8), the result as given in [2] is

$$V_{out} = V_{G0} + V_T(\gamma - \alpha)(1 + ln\frac{T_0}{T}) \tag{3.11}$$

Thus, the temperature dependence of the output voltage is heavily dependent on the quantity T_0, which is determined by the circuit parameters M, E, and G [2].

When (3.11) is differentiated with respect to T, the slope of V_{out} as a function of temperature is

$$\frac{\mathrm{d}V_{out}}{\mathrm{d}T} = (\gamma - \alpha)\frac{V_T}{T}(ln\frac{T_0}{T}) \tag{3.12}$$

As shown by (3.12), the temperature coefficient of the output voltage is zero only at T $= T_0$. Assuming that $(\gamma - \alpha)$ is a positive quantity, the slope of the output is positive when $T < T_0$, and negative when $T > T_0$. This result can be understood by examining (3.9) and (3.10). Given that MV_T can only be used to cancel linear temperature dependence, the variation of $\frac{\mathrm{d}V_{out}}{\mathrm{d}T}$ with temperature is due to the uncompensated non-linear term in the equation describing $V_{be,on}$.

Even with the aforementioned non-linear effects, it is still possible to build a reference based on the hypothetical circuit presented above with extremely small variations in output voltage over a wide range in temperature. For the purposes of most power supply control chips, higher order temperature cancellation is unnecessary [6].

The next challenge is designing a circuit that practically implements the output voltage relationship in (3.8). Consider the circuit in Fig. 3-13. Looking at the voltage

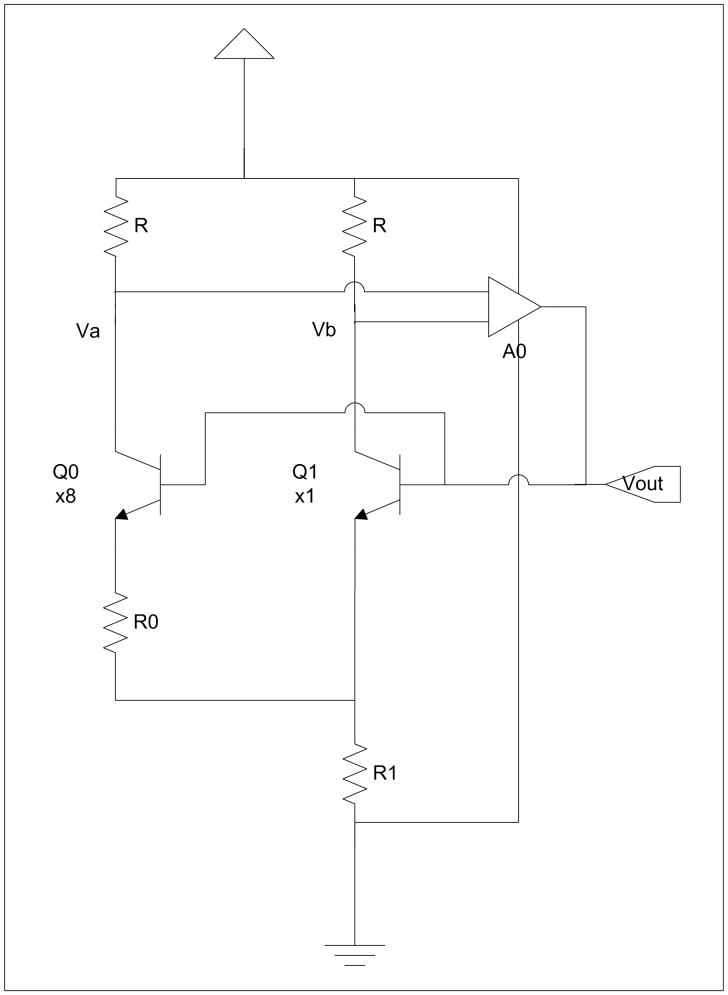

Figure 3-13: Simple Bandgap Voltage Reference

across R_0, the value is determined to be the difference between two base-emitter voltage drops.

$$V_{R0} = V_{be1} - V_{be0} \tag{3.13}$$

As noted in [2]

$$V_{bex} = V_T ln \frac{I_{CX}}{I_{SX}} \tag{3.14}$$

where I_{CX} and I_{SX} are the collector and saturation currents respectively of device X.

Plugging (3.14) into (3.13) yields the following equation for the voltage across R_0:

$$V_{R0} = V_T ln \frac{I_{C1} I_{S0}}{I_{C0} I_{S1}} \tag{3.15}$$

Given that the amplifier A_0 regulates V_a and V_b to the same voltage, the collector currents running through Q_0 and Q_1 must be the same. Also, assuming that Q_0 is a parallel combination of transistors identical to Q_1, the ratio $\frac{I_{S0}}{I_{S1}}$ is equal to the ratio of the emitter areas of Q_0 and Q_1 [2]. Thus, the voltage across R_0 and the current through R_0 are

$$V_{R0} = V_T ln8 \tag{3.16}$$

$$I_{R0} = \frac{V_T ln8}{R_0} \tag{3.17}$$

Since double the current that flows through R_0 flows through R_1, the voltage across R_1 must be

$$V_{R1} = 2 \frac{R_1}{R_0} V_T ln8 \tag{3.18}$$

This equation shows that the voltage across R_1 is linearly proportional to temperature, because of the direct temperature dependence of the thermal voltage V_T. Now, considering the location of the output terminal, the output voltage is the sum of the voltage across R_1 and the base-emitter drop of Q_1:

$$V_{out} = V_{be1} + 2 \frac{R_1}{R_0} V_T ln8 = V_{be1} + M V_T \tag{3.19}$$

Therefore, this circuit behaves exactly as the hypothetical circuit presented in Fig. 3-12 with the value of M set by a constant times the ratio of $\frac{R1}{R0}$.

While many other bandgap voltage reference topologies exist, the fundamental output voltage relation for this group of circuits is as presented in (3.19) [2]. Thus, a general design philosophy can be employed:

1. Model bipolar transistor characteristics to extract process specific parameters.

2. Choose a temperature at which V_{out} will have zero temperature coefficient, i.e.

T_0.

3. Using (3.11), calculate the value of V_{out} at this temperature.

4. Run design simulations at $T = T_0$, and adjust the value of M to yield the desired $0T_C$ output voltage.

3.3.2 Specific IC Implementation

Using the structure of Fig. 3-13 as a foundation, the actual circuit constructed for the LLC secondary side controller is shown in Fig. 3-14. As can be seen, Q_0, Q_1, R_0,

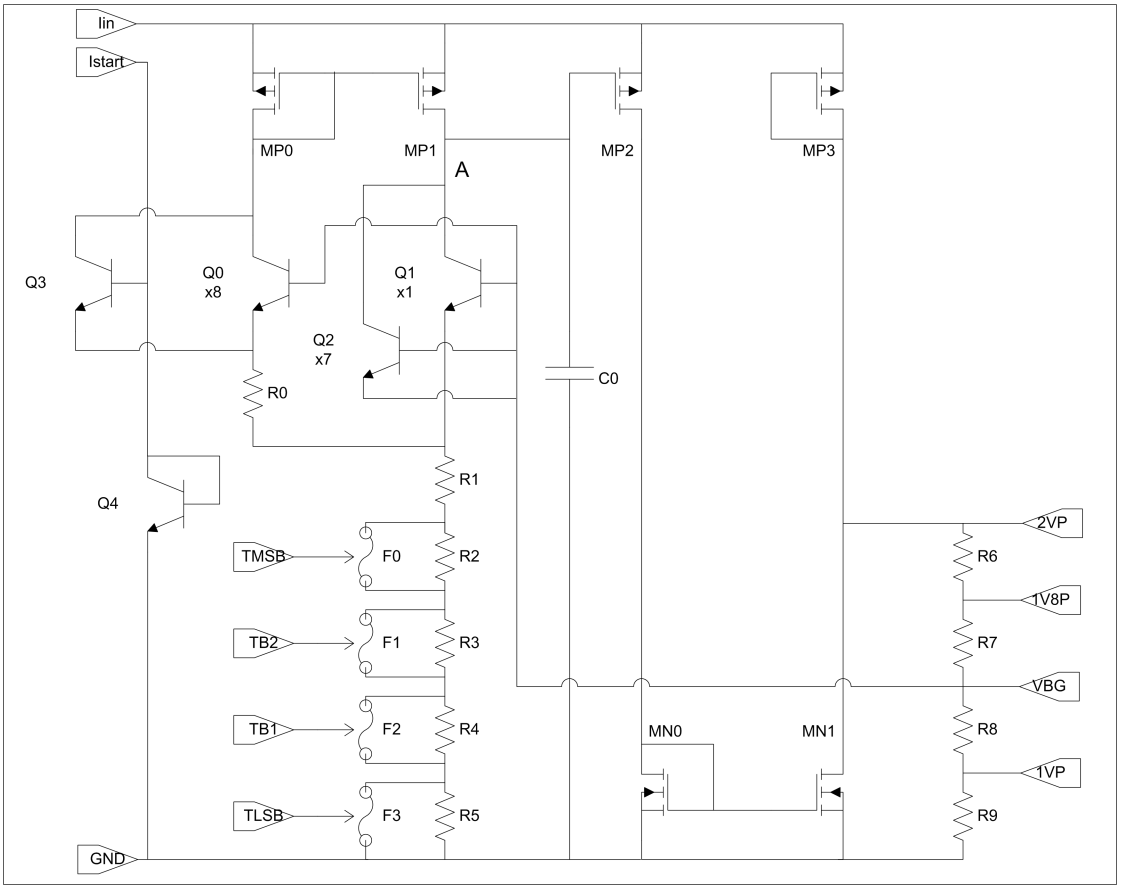

Figure 3-14: Complete Bandgap Voltage Reference

and R_1 still form the bandgap cell that yields the output voltage relationship given in (3.19). Where resistors were used to load the collectors of Q_0 and Q_1, a current mirror now exists. It is important to note that the results of (3.13) - (3.19) imply that

when V_{out} equals the desired $0T_C$ value, the currents flowing through Q_0 and Q_1 will be the same. If V_{out} is too high, or too low, the collector current of Q_1 will not match the drain current of M_{P1}, and node A will fluctuate in voltage. Thus, a single ended inverting amplifier, composed of M_{P2}, M_{P3}, M_{N0}, and M_{N1}, is used to regulated the output voltage to the proper value. Steady state is reached when $I_{DMP1} = I_{CQ1}$ and V_{BG} equals the value calculated in (3.11).

The operation of the regulation loop can be understood in the following manner. Assuming that the output voltage on the V_{BG} node is too high, more current will flow through Q_1 than Q_0 [2]. This has the effect of pulling down the voltage on node A, and raising the current flowing out of the drain of M_{P2}. This current is mirrored around through M_{N0} and M_{N1}, and pulls down on the top of the output divider, effectively lowering the voltage on the V_{BG} node back down to its nominal value. The opposite process occurs if the output voltage starts off too low, which results in V_{BG} being pulled up. C_0 is placed between the high impedance node of the amplifier and ground, implementing dominant pole compensation and ensuring overall loop stability.

A few other devices in this circuit are also worth mentioning, specifically Q_2, Q_3, and Q_4. Q_2 functions as a matching device for the collector-base junction area of Q_1 with Q_0. Q_3 and Q_4 are startup devices. While operation in steady state was previously explained, another stable operating point exists when no current runs in all the circuit legs. Q_3 and Q_4 prevent this condition from occurring. Driven by a small current source, I_{start}, Q_4 biases the base of Q_3 at roughly a diode drop above ground. If no current is flowing through R_0, then the emitter of Q_3 will be sitting at ground. Thus, Q_3 will be forward biased, and the collector of the device will draw current through M_{P0}. This process breaks the reference away from its zero current state, and begins the output regulation cycle. As more current flows through R_0, the base-emitter voltage of Q_3 drops, and the device removes itself from the steady state operation of the circuit.

The remaining components of the circuit in Fig. 3-14 will be discussed in the next section. As a final remark, note that the supply node for this circuit is connected

to a current source derived from the supply independent source in the UVLO block, rather than a voltage source. This choice limits the maximum current consumed by this block, and isolates the circuit from variations in V_{CC}.

3.3.3 Silicon Process Concerns

As with any industrial integrated circuit process, variations in the manufacturing process can result in undesirable effects, most notably device and component mismatch. Many layout techniques exist to mitigate these effects, such as including dummy devices to help match important components, but a higher level of control is necessary when exact precision is required. Thus the inclusion of trim resistors R_2 - R_5. This binary weighted array is used to adjust the effective value of R_1 in (3.19) to yield the proper $0T_C$ output voltage at T_0, post-production. Without any of the fuses blown, the voltage across R_1 is designed to be 46 mV below its desired value, indicating that it is smaller than required. Adding the MSB trim resistor into the string by blowing fuse F_0, however, increases the output voltage by 46 mV. Therefore, the ideal value of R_{1eff} is equal to $R_1 + R_2$. If the value of V_{be1} drifts higher or lower than expected due to process variation, different combinations of the binary weighted resistors in the array can be added together to yield the proper output voltage. In such a manner, the circuit as implemented at Texas Instruments can correct for variations in V_{be1}, or any other parameter affecting V_{out}, that would results in an uncompensated voltage error of $\pm$46 mV. Using Monte Carlo simulation techniques, the standard deviation of the untrimmed output voltage, over process variation, was calculated to be 4 mV, implying that the trim range is more than sufficient.

Other process specific design choices include:

1. Using transistors with large gate lengths as mirrors to minimize the effect of threshold voltage mismatch on current mirror accuracy [2].

2. Using combinations of unit sized resistors when constructing important resistor ratios to ensure ratio insensitivity to process and temperature.

3.3.4 Simulated Results

The simulation results for the circuit described above are shown in Figs. 3-15 and 3-16.

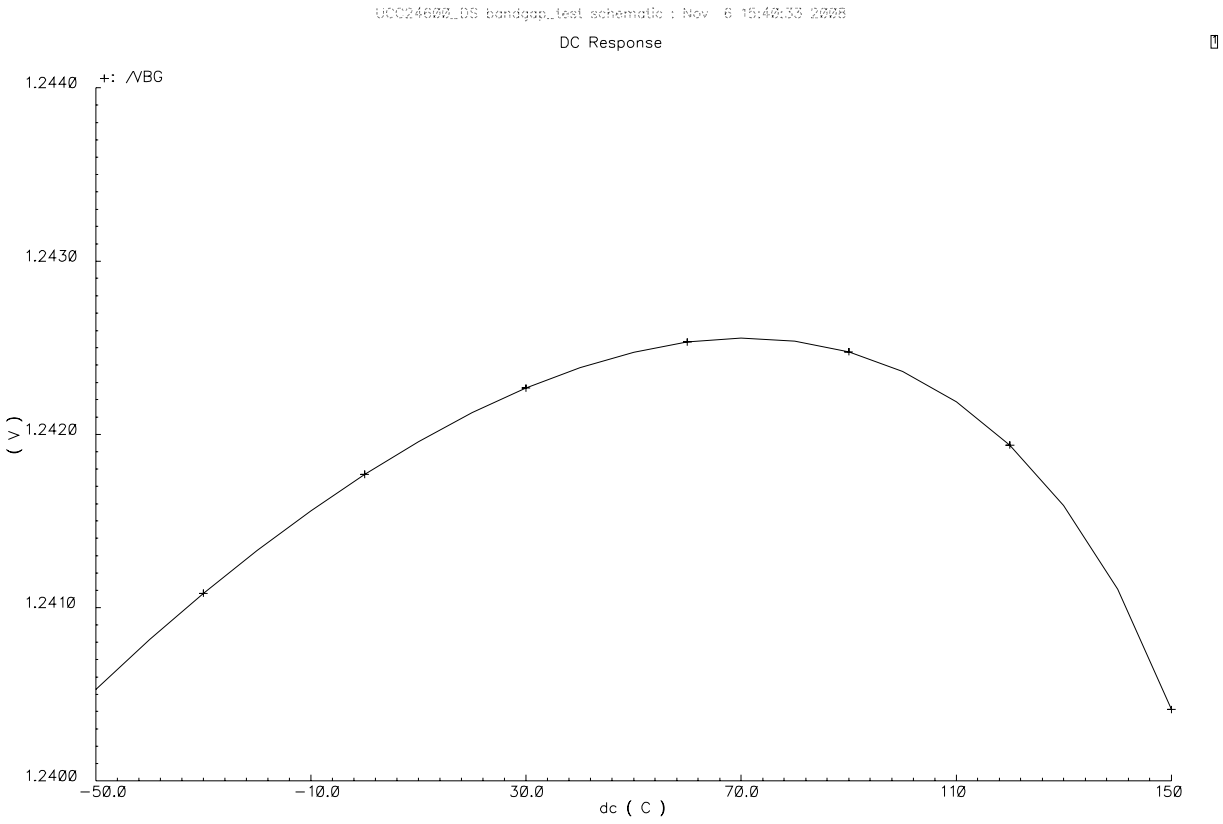

Figure 3-15: V_{BG} for $-50C \leq T \leq 150C$, Centered Process

As evident, the peak to peak voltage variation over an extremely wide operating range is limited to ≈ 1.5 mV, assuming standard parameters. The previously mentioned standard deviation of 4 mV over process was calculated from the Monte Carlo generated distribution in Fig. 3-16. Given the generous trim range provided by R_2 - R_5, any process variation can be compensated by trimming one or more resistors. Thus, a precise and robust voltage reference has been developed.

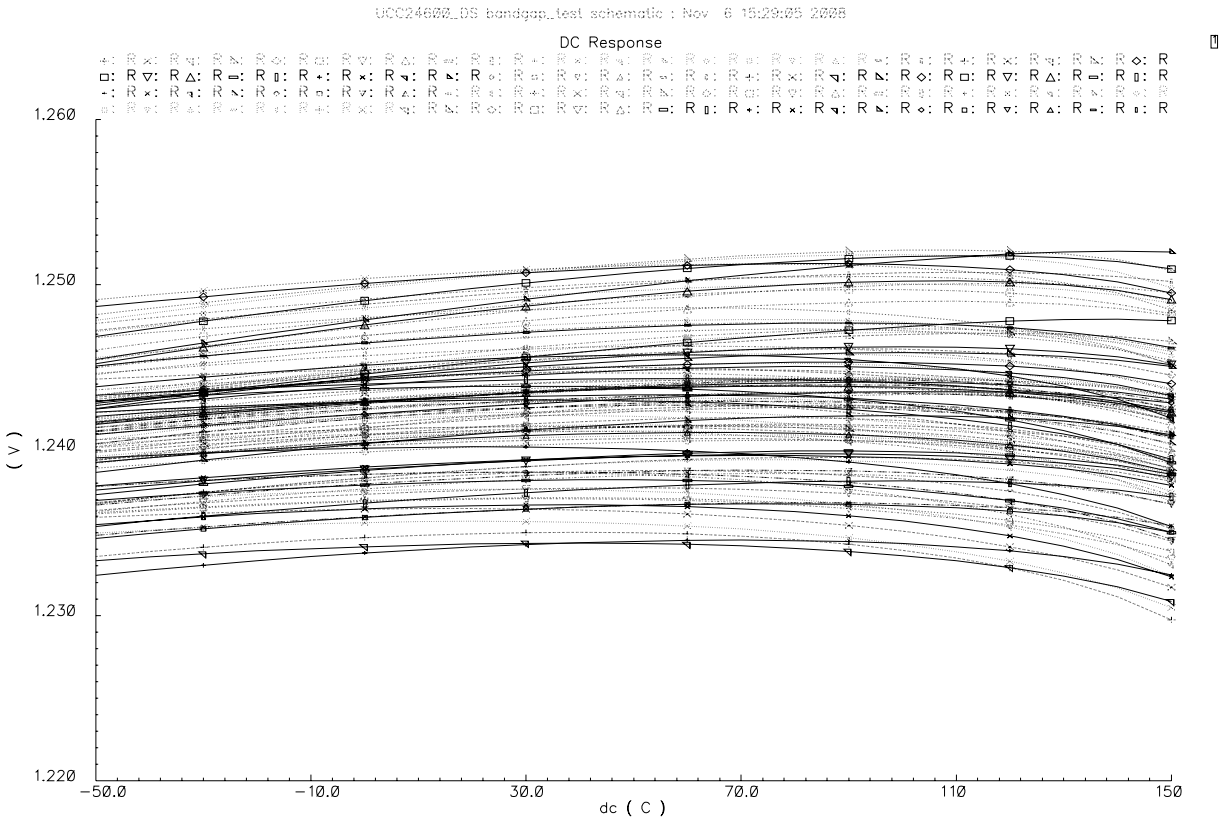

Figure 3-16: V_{BG} for $-50C \leq T \leq 150C$, Montecarlo Simulation - 100 Runs

3.4 Power Buffer

In the frequency range of interest for the converter system (150 KHz - 1 MHz), low voltage, high speed transistors are necessary to implement the desired analog signal processing. Thus, an on chip power buffer is required to convert V_{CC} into two lower voltage power rails, from which the remainder of the circuit blocks in the IC draw their current. Using the bandgap voltage as a reference, the power buffer is basically a non-inverting feedback amplifier coupled with a unity gain open loop buffer, as shown in Fig. 3-17. The output of the amplifier is designed to be 5 V, with a current

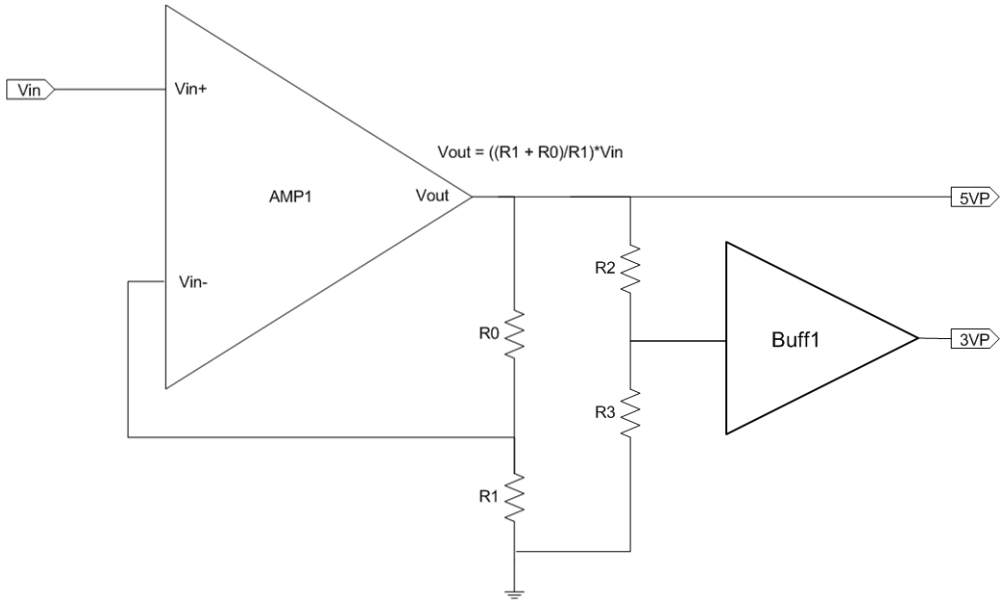

Figure 3-17: Power Buffer System Diagram

sourcing capability of 10 mA. The output of the unity gain buffer is designed to be 3 V with a current sourcing capability of up to 2 mA. A full, detailed schematic of the entire power buffer is shown in Fig. 3-18. Note that discussion of this block is split into two subsections regarding the 5 V and 3 V circuitry respectively.

3.4.1 5V Amplifier

A schematic of the 5 V power amplifier is shown below in Fig. 3-19. This circuit is a single stage, differential amplifier hooked up in a non-inverting feedback configura-

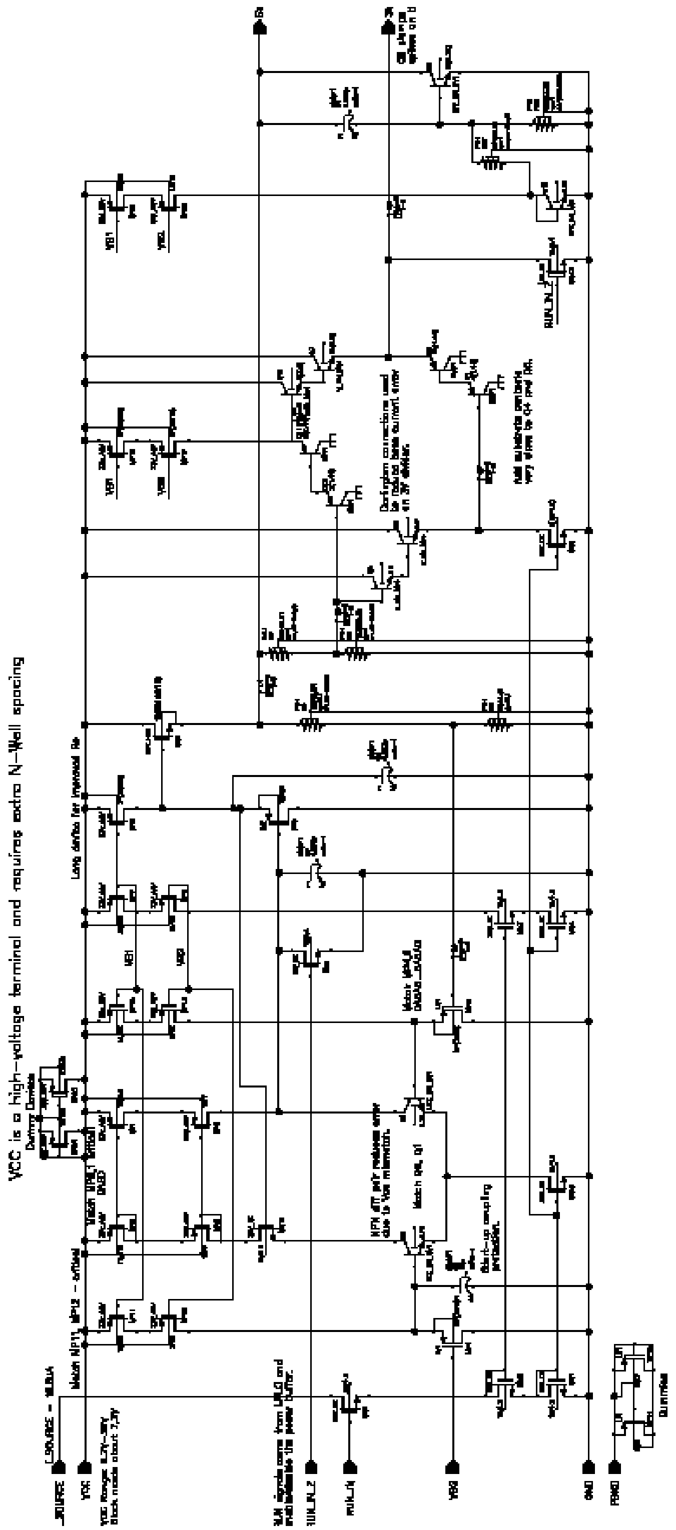

Figure 3-18: Full Power Buffer Schematic

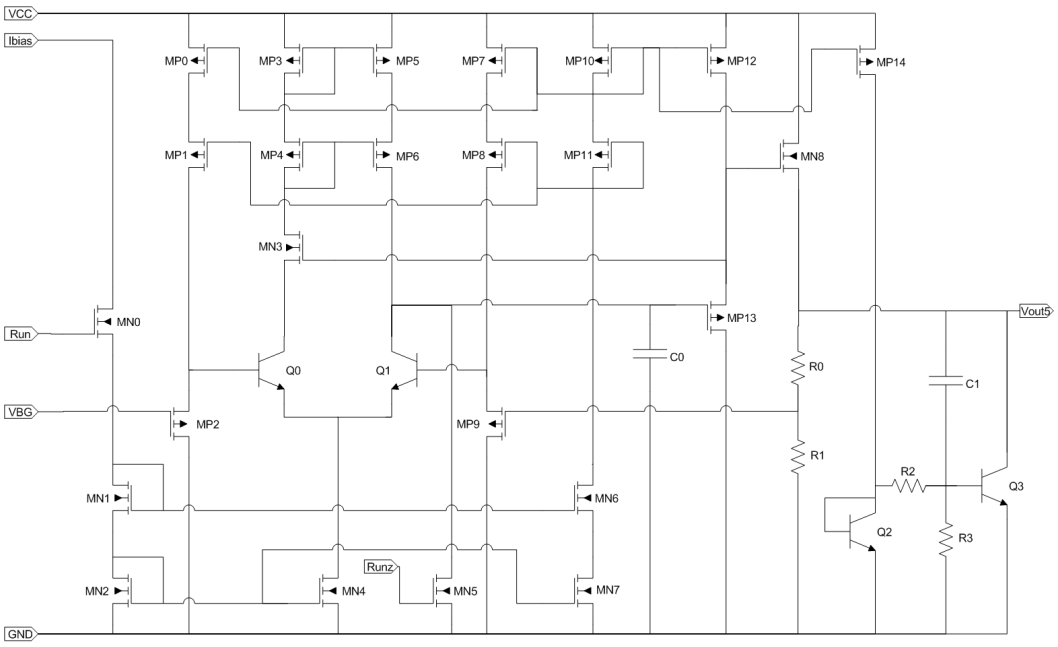

Figure 3-19: 5V Power Amplifier Schematic

tion. Q_0 and Q_1 form the emitter coupled differential input pair. Bipolar transistors are chosen as input devices for their high transconductance and output resistance for a given bias current level relative to MOS transistors [2]. A cascoded current mirror load ensures accurate current matching between input legs and presents a high incremental output impedance on the drain of M_{P6}. Given that the differential gain of the amplifier is roughly

$$A_v = g_{m1}(r_{o1} \| r_{o6}) \tag{3.20}$$

where g_{m1} is the transconductance of Q_1, and r_{o1} and r_{o6} are the incremental output resistances of Q_1 and M_{P6} respectively, the configuration described above is optimal for high amplifier gain [2]. The inclusion of C_0 from the high impedance node to ground implements dominant pole compensation, and guarantees closed loop stability.

The output stage of the amplifier is formed by two unity gain followers, comprised of M_{P13} and M_{N8}. Noting that the load current of the buffer must flow through M_{N8}, the gate to source voltage of this device at full load is

$$V_{GS8,max} = \sqrt{\frac{2LI_{D8,max}}{kW}} + V_t \tag{3.21}$$

where L and W are the length and width of M_{N8}, k is a process dependent parameter, V_t is the threshold voltage, and $I_{D8,max}$ is the maximum load current of the buffer [2]. In order for the entire circuit to function properly, all MOS devices must be biased in their saturation regimes, implying that $V_{DS} \geq V_{GS} + V_t$ for all devices, and consequently V_{CC} must be higher than a certain value. Given that $I_{D8,max}$ is orders of magnitude larger than any other current in the circuit, the limiting factor in the V_{CC} overhead requirement is $V_{GS8,max}$. Thus, to ensure the controller reliably operates at the minimum allowable value of V_{CC}, M_{N8} must be designed to be as wide as possible.

Moving on to biasing, M_{N1} and M_{N2} form the reference leg of all the current mirrors used to supply bias current to the various circuit elements in the buffer. I_{bias} is fed into this leg from the UVLO block, and is derived from the supply independent source discussed earlier. R_0 and R_1 serve dual purpose as biasing elements for M_{N8}, and as the voltage divider feeding the output signal back to the inverting terminal of the amplifier.

There are several other peripheral devices in this circuit that are worth mentioning. First, M_{N0} and M_{N5} are two transistors that form an effective on/off switch. When Run is low, M_{N0} prevents I_{bias} from flowing through M_{N1} and M_{N2}, stopping the flow of all bias current in the system. Similarly, when Run_z is high, M_{N5} ensures that the output voltage of the buffer remains at GND. Both of these precautions avoid the possibility of false gate triggers when the controller is disabled. As soon as Run and Run_z are properly asserted, however, the buffer is free to operate normally.

Second, M_{N3} is used to reduce the input offset voltage of the amplifier by matching the collector-emitter voltages of Q_0 and Q_1. To a first order, V_{GS} of M_{P13} roughly matches that of M_{N3}, thus V_{C1} will equal V_{C0}, and the effect of base-width modulation on the collector currents of Q_0 and Q_1 will be the same.

Finally, Q_2, Q_3, R_2, R_3, and C_1 are used to implement a transient output voltage spike suppression circuit. Without these components, the amplifier can effectively regulate its output voltage in the presence of positive load current spikes, as the current through M_{N8} merely increases by design. Negative going spikes, however, will result in dangerously high voltage transients, perhaps large enough to damage the

transistors connected to the output node. To understand how the above mentioned devices prevent this situation from occurring, consider steady state operation where the output voltage is 5 V, and, assuming $R_2 = R_3$, the base of Q_3 is biased at $\frac{1}{2}V_{beon}$. If the load current suddenly drops from I_{load} to zero, the induced voltage spike on the output node will couple through C_1 and strongly forward bias Q_3, allowing this device to absorb the excess transient current and suppress the voltage spike on the output. Given a load step from 10 mA to zero in 10 ns, the maximum voltage seen on the output of the buffer without spike suppression is roughly 7.4 V. With spike suppression, this value drops to 5.6 V. Both of these voltages were attained with simulation at 25° Celsius. At -50° Celsius, the value of the peak decreases to 5.3 V, while at 150° Celsius, the peak increases to 5.9 V. It is important to note that the slew rate of the load current used in these simulations is significantly higher than any expected slew rate in the physical controller system, thus the values reported above will never actually be observed.

Simulated data on the steady state performance of the 5 V buffer will be presented alongside that of the 3 V buffer in section 3.4.3.

3.4.2 3V Buffer

A schematic of the open loop 3 V buffer is shown below in Fig. 3-20. Note that the feedback amplifier discussed above has been abstracted into a block labeled $Buff5$, with an input voltage equal to the bandgap reference, and an output voltage equal to 5 V. The 3 V buffer itself is comprised of Q_4 - Q_{11}, which form two Darlington followers and a Darlington push pull output stage. Tracing the signal path from the input to the output of the buffer, V_{out3} can be expressed as

$$V_{out3} = V_{Q4b} + 2V_{be,onp} - 2V_{be,onn} \tag{3.22}$$

Assuming that the base-emitter voltage drops of a pnp and npn transistor are equal, the output voltage will roughly equal the voltage on the base of Q_4. For proper choices of the values of R_4 and R_5, this voltage can be set to 3 V. To ensure accuracy of the

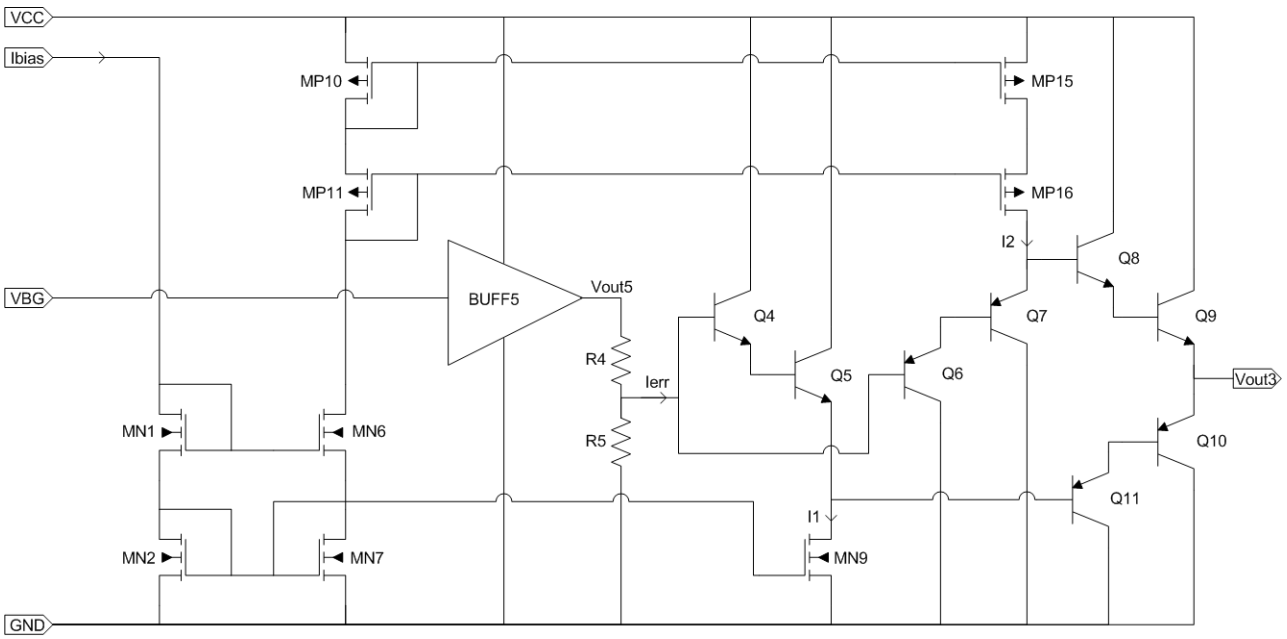

Figure 3-20: 3 V Power Buffer Schematic

buffer over process and temperature variation, it is essential that the ratio of R_4 to R_5 remain constant. Thus, these devices must be made from the same resistive material, and constructed from the same unit sized blocks to minimize possible sources of error.

Now, given that the current gain of a composite Darlington transistor is β^2 [2], where β is the base to collector current gain of one bipolar device, the configuration of this buffer allows for significant output load current with minimal requirements on the bias currents I_1 and I_2. In fact, as long as the following two expressions are satisfied,

$$I_1 > \frac{I_{C10max}}{\beta^2} \tag{3.23}$$

$$I_2 > \frac{I_{C9max}}{\beta^2} \tag{3.24}$$

the buffer will reliably produce its desired output voltage for any value of rated load current.

Of interest in the system is the magnitude of output voltage error. This value is proportional to the current I_{err}, which is equal to the difference between the base

currents of the npn and pnp Darlington followers. Assuming that I_1 and I_2 are set to their minimum values, as defined above, I_{err} can be expressed as

$$I_{err} = \frac{1}{\beta^4}((I_{C10max} - I_{C10}) - (I_{C9max} - I_{C9})) \tag{3.25}$$

with the important simplification that $\beta_{npn} = \beta_{pnp}$. Thus, the benefit of using Darlington connected transistors is extremely evident, for the error current and output voltage error become inversely proportional to β^4. For even moderate values of β, this error negligibly effects the performance of the system. Please note that in the real circuit, I_{c10} will nominally equal zero, as the buffer is not designed to function as a current sink in steady state. Also, β_{npn} will not equal β_{pnp} in practice, hence, the above analysis is slightly inaccurate.

3.4.3 Simulated Results

The following two figures display simulation results for the entire power buffer system. Fig. 3-21 is a graph of the steady state values for V_{out3} and V_{out5} with zero load over 50 Monte Carlo simulation runs where process parameters are randomly varied. Fig. 3-22 shows the same data, but the buffer is under full load, with 2 mA drawn from V_{out3} and 10 mA drawn from V_{out5}. Both simulations are done at 25° Celsius.

For the no load case, the average output voltages are 3.008 V and 5.004 V, and the standard deviations are .018 V and .007 V respectively. Over temperature, V_{out5} does not noticeably change, while average V_{out3} drifts $\mp$20 mV with increasing and decreasing temperature. For the full load case, the statistical values for V_{out5} are unchanged, while average V_{out3} drops to 2.851 V at 25° Celsius, and drifts $\mp$40 mV with increasing and decreasing temperature. Given that V_{out3} functions only as a power source, the slight degradation observed with increasing load does not affect system performance. In fact, this result is expected, as the 3 V buffer is strictly an open loop system.

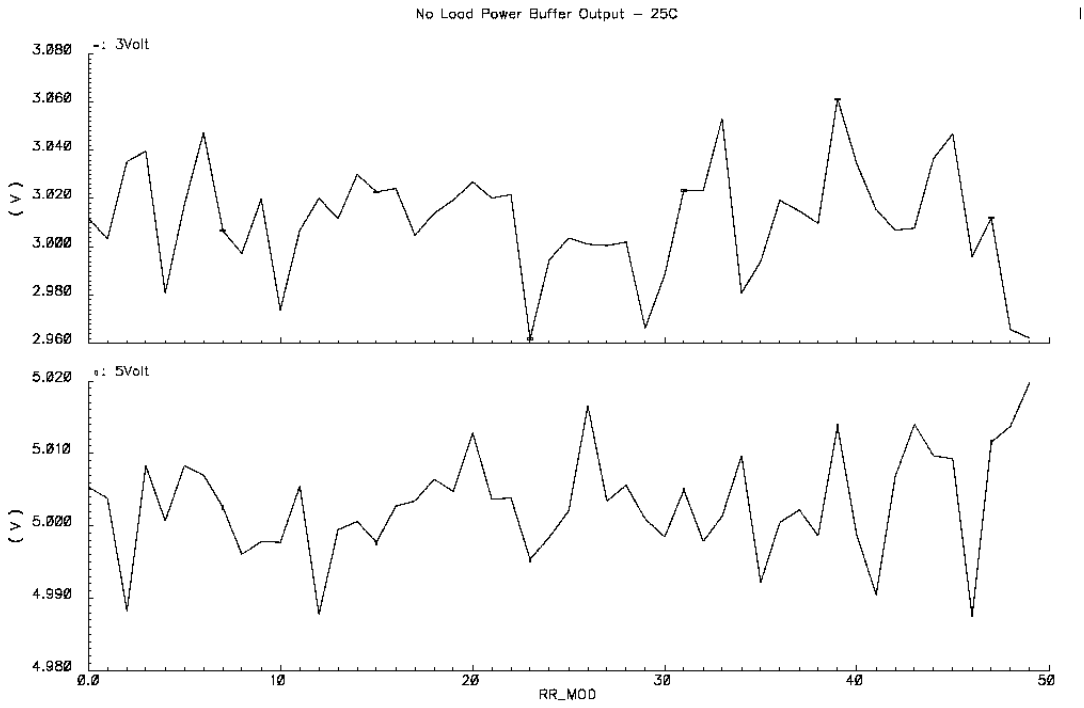

Figure 3-21: No Load Power Buffer Output Voltages Over Process Variation

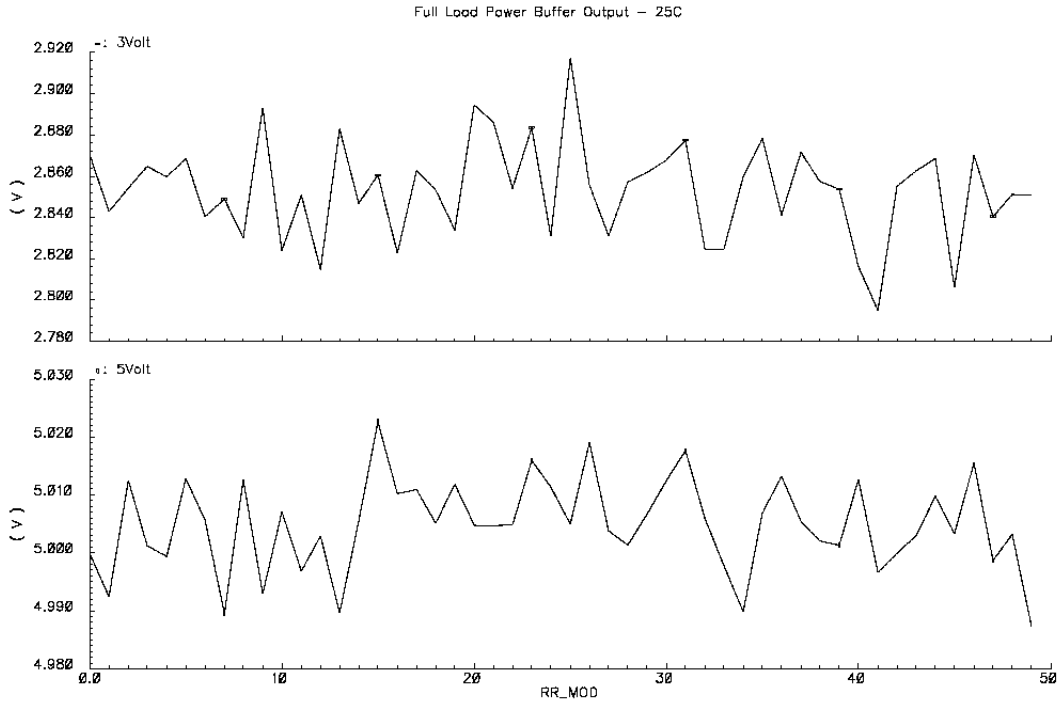

Figure 3-22: Full Load Power Buffer Output Voltages Over Process Variation

3.5 Minimum On Timer

When current begins to flow through the body diode of the SR FET, the internal -100 mV comparator detects the induced voltage drop, and instructs the controller to bring its gate drive output high. As the SR FET turns on, the magnitude of V_{DS} across the FET can drop below the turn off threshold. To prevent false triggering of the -3 mV comparator, and thus spurious turn off of the SR FET, all external signals are ignored by the controller after turn-on for a user programmable length of time, given by the minimum on timer (MOT). This block generates a variable width pulse that blanks control signals produced by the internal detection circuitry and maintains the gate drive output high. The following subsection goes through the operation and structure of the timer.

3.5.1 MOT Operation and Structure

A high level schematic of the MOT is shown in Fig. 3-23. Note that the variable width output pulse mentioned above occurs on the MOT_{on} node. To understand

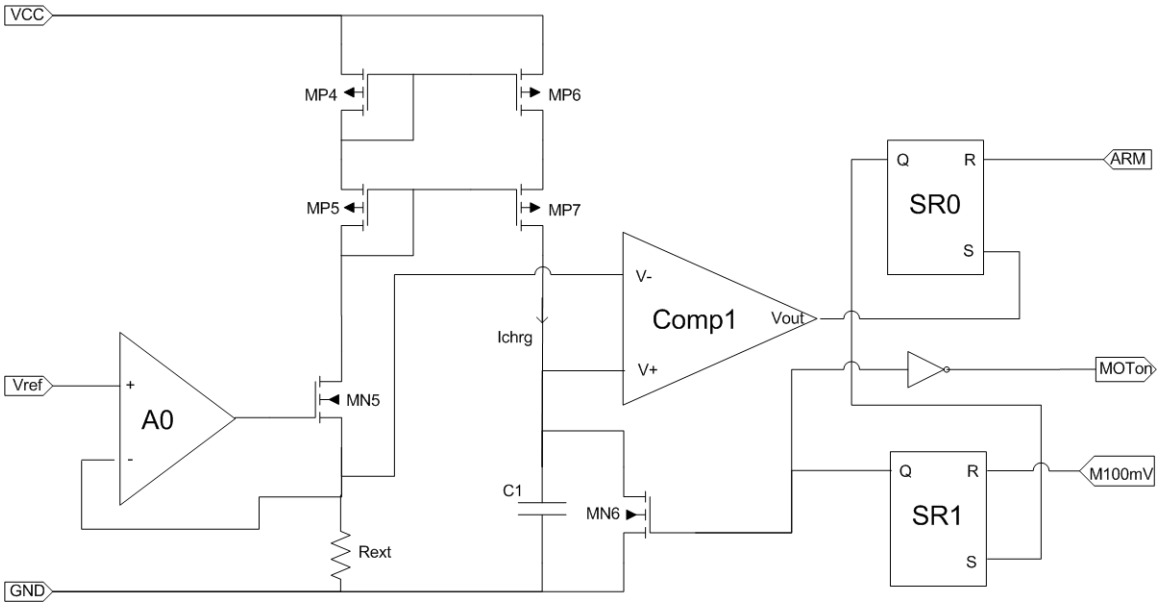

Figure 3-23: Simplified MOT System Schematic

the operation of this circuit, assume that ARM, $M100mV$, and MOT_{on} are initially

low, and that the V_+ input of $Comp_1$ is actively held at ground by M_{N6}. When the conduction cycle of the SR FET begins, $M100mV$ transitions high, triggering MOT_{on} and turning off the gate of M_{N6}. I_{chrg} now begins to charge up the V_+ node through C_1. Once $V_+ = V_-$, the output of $Comp_1$ inverts, forcing the Q outputs of SR_0 and SR_1 high. This terminates the MOT_{on} pulse and shorts the V_+ node back to ground. Given that the SR latches are both set dominant, the system will remain in this state until a positive transition on the ARM pin is detected, bringing the S input of SR_1 low, and allowing the $M100mV$ signal to dictate the latch's behavior.

The length of the MOT_{on} pulse is thus determined by the charging time of C_1 from ground to the voltage on the V_- input of $Comp_1$. Using the fundamental voltage to current relationship of a capacitor, the pulse duration can be expressed as

$$t_{MOT} = C_1 \frac{V_-}{I_{chrg}} \tag{3.26}$$

Given that V_- is hooked to the inverting terminal of amplifier A_0, and noting that A_0 is configured as a unity gain buffer, the voltage on V_- equals V_{ref}. To find I_{chrg}, assume that M_{P4} - M_{P7} form a 1:1 current mirror. The charge current then becomes

$$I_{chrg} = \frac{V_{ref}}{R_{ext}} \tag{3.27}$$

Now, if the expressions for V_- and I_{chrg} are substituted back into (3.26), t_{MOT} can be written as

$$t_{MOT} = C_1 R_{ext} \tag{3.28}$$

The pulse width of MOT_{on} now only depends on the values of C_1 and R_{ext}, where R_{ext} is a user supplied resistor from the T_{on} pin of the controller to ground. The limits on R_{ext} result in $t_{MOT,min} = 250$ ns and $t_{MOT,max} = 3$ μs. This configuration, therefore, yields a robust, programmable timer that is immune to variations in V_{ref} and amplifier offset voltage.

A full schematic of the MOT is shown in Fig. 3-24. $Comp_1$ is left as an abstract block and will be discussed in detail in the next subsection. As can be seen, the

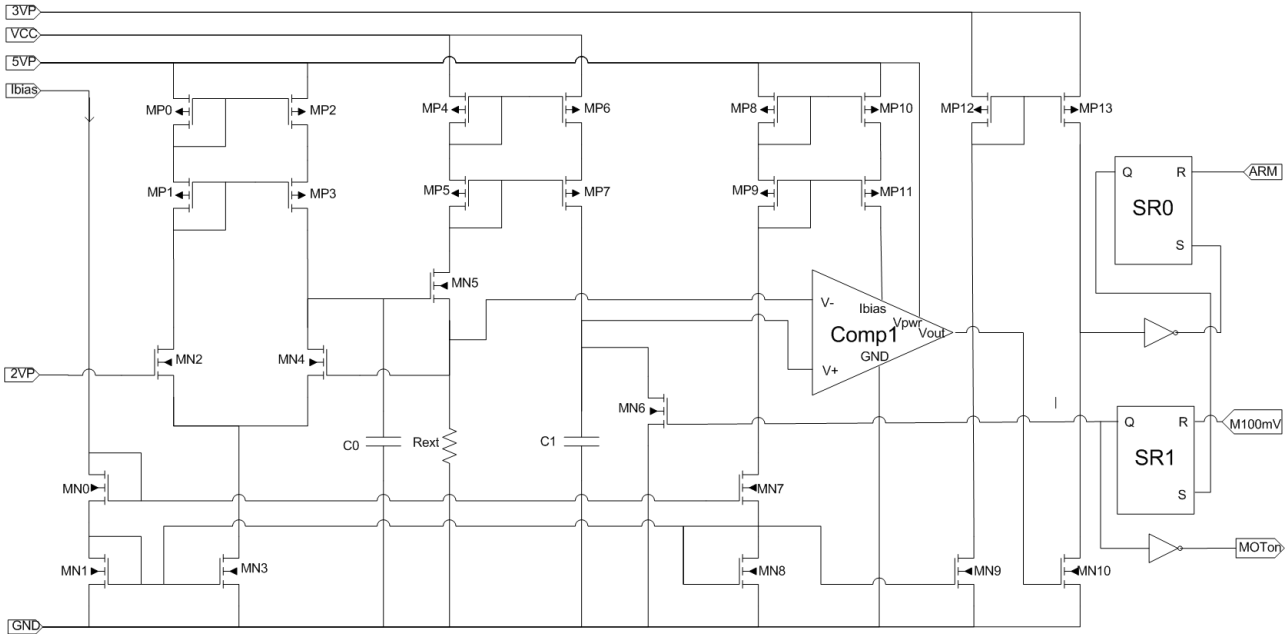

Figure 3-24: Full MOT System Schematic

signal processing and timing circuitry draw current from the 5 V power rail, whereas the logic blocks draw current from the 3 V power rail. This design choice guarantees that logic gate switching events do not perturb the 5 V rail, and consequently disturb the accuracy of the timing circuits. M_{N10} and M_{P13} have been included to interface between the 0-5 V comparator output and the 0-3 V logic input. V_{CC} supplies I_{chrg} to ensure that the devices in the leg comprised of M_{P4}, M_{P5}, M_{N5}, and R_{ext} have enough voltage headroom to operate in their respective active regions.

A_0, from Fig. 3-23, is implemented as a single stage, dominant pole compensated, NMOS differential amplifier with PMOS cascoded current mirror load. Transistors M_{P0} - M_{P3}, M_{N2} - M_{N4}, and capacitor C_0 form this sub-circuit. The reference voltage on the gate of M_{N2} comes from the bandgap voltage reference, and is nominally equal to 2 V. Bias current for this, and the rest of the circuits in the MOT block, comes from mirrors of the injected current I_{bias}.

In the next subsection, the design of the timing comparator is discussed, after which simulated results for the entire block are presented.

3.5.2 Timer Comparator

Accurate timing requires a comparator with fast response time and low offset voltage. If either of these parameters is sufficiently skewed, the t_{MOT} analysis performed above no longer models the behavior of the system. Thus, $Comp_1$ in Figs. 3-23 and 3-24 is essential to the performance of the MOT.

A full schematic of this comparator is presented in Fig. 3-25 below. The most

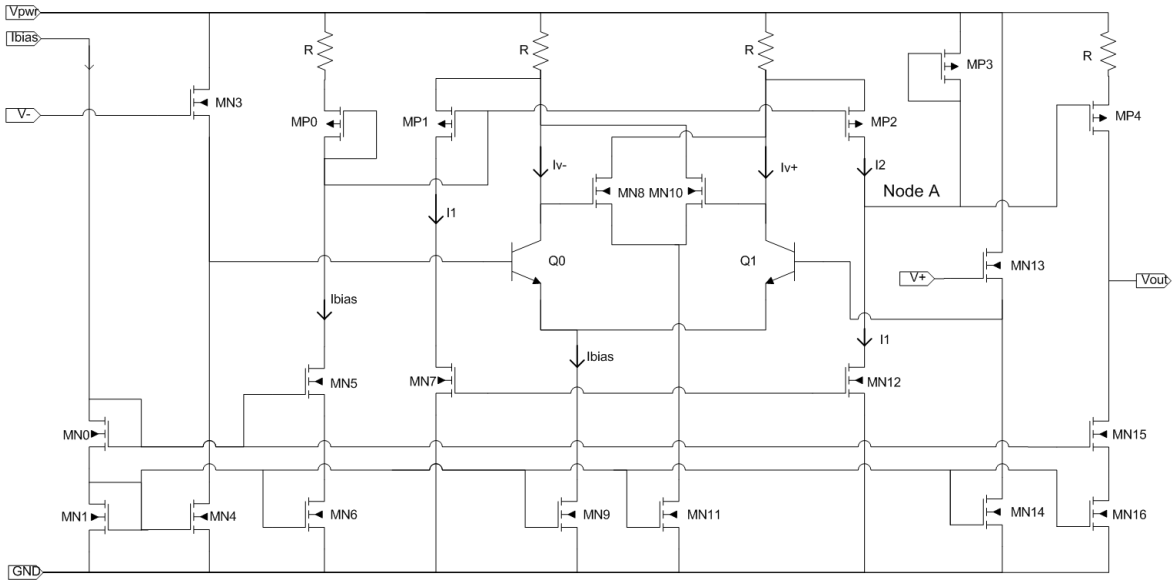

Figure 3-25: Timing Comparator Schematic

important feature of this circuit is the design of the input gain stage. To ensure high transconductance and low offset, bipolar transistors are chosen as the primary input devices. To mitigate the detrimental effect of base current on the input resistance of the comparator, M_{N3} and M_{N13} are used as input voltage buffers.

Note that Q_0 and Q_1 are both resistively loaded such that at maximum differential input, neither transistor saturates, guaranteeing optimal switching characteristics for the entire block [2]. This construction requires the use of folding legs to steer the input currents, I_{v+} and I_{v-}, to node A. These legs are formed by M_{P1}, M_{P2}, M_{N7}, and M_{N12}. To understand their function, consider the following relationship for the current I_2:

$$I_2 = k[I_{bias}R - (I_2 + I_{v+})R + \sqrt{\frac{1}{2k}I_{bias}}]^2 \tag{3.29}$$

where I_{bias} is the current flowing out of the drain of M_{P0}, I_{v+} is the current flowing through the collector of Q_1, and k is a process dependent parameter [2]. It is important to realize that the above equation was derived assuming that M_{P0} is twice the width of M_{P2}. A similar relation for I_1 exists where I_2 and I_{v+} in (3.29) are replaced by I_1 and I_{v-} respectively. At balance, when $V_+ = V_-$, $I_{v+} = I_{v-} = \frac{I_{bias}}{2}$, and equation (3.29) reduces to

$$I_2 = \frac{I_{bias}}{2} \tag{3.30}$$

Similar analysis yields the same value for I_1, thus no net voltage change is induced on node A for these conditions. As soon as the system moves away from balance, however, I_1 increases in proportion to the quantity $(V_+ - V_-)$, while I_2 increases in proportion to the quantity $-(V_+ - V_-)$. Therefore, for positive differential input voltages, node A falls and the output of the comparator goes high, while for negative differential inputs, the opposite occurs.

The topology described above results in extremely fast comparator response times, largely due to the low impedances on each node in the signal path. High current biasing of the input and output stages contributes as well. M_{P13} functions as a speed enhancing device by limiting the maximum negative voltage swing of node A, and consequently decreasing the slewing time required to bring the comparator output low. The average delays between V_+ crossing V_- and the output of the comparator changing are summarized in the table below.

Temp	Rising Delay	Falling Delay	Power Consumption
-50 C	5.86 ns	19.9 ns	700 μW
25 C	6.95 ns	19.2 ns	729 μW
150 C	8.84 ns	19.25 ns	734 μW

These numbers were calculated from 100 Monte Carlo simulations of the timing comparator block. For each run, V_- was held at 2.5 V, while V_+ was a 0-5 V, 2.5 μs pulse with 10 ps rise and fall times. Given that the lowest allowable value of t_{MOT} is 250 ns, the comparator dynamics do not negatively affect the performance of the greater MOT system.

3.5.3 Simulated Results

Simulated data for the MOT block is presented below. Fig. 3-26 is a graph of the minimum t_{MOT} pulse width over 100 Monte Carlo simulations runs. Fig. 3-27 shows the same data, but for the maximum t_{MOT} pulse width.

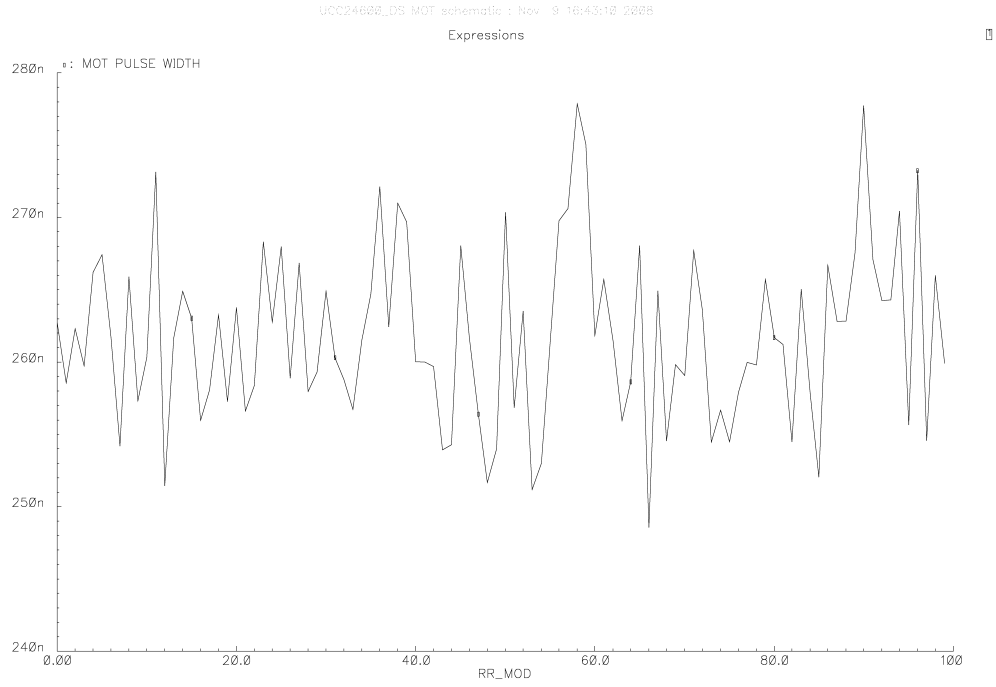

Figure 3-26: Minimum t_{MOT} Over Process Variation

Both of these graphs were generated at room temperature, and their respective averages are 261.9 ns and 2.93 μs, with respective standard deviations of 1.2 ns and .021 μs. Over temperature, none of these statistics noticeably change, due to timer insensitivity to fluctuations in V_{ref} (see eqn (3.28)), and careful comparator design. The primary source of pulse width variation comes from capacitor C_1, whose value deterministically drifts over process.

These results are extremely promising, for while most power IC timing circuits are rated at $\pm 20\%$ of their nominal values [5], the MOT output only varies $\pm 5\%$, assuming a maximum process variation of 6σ.

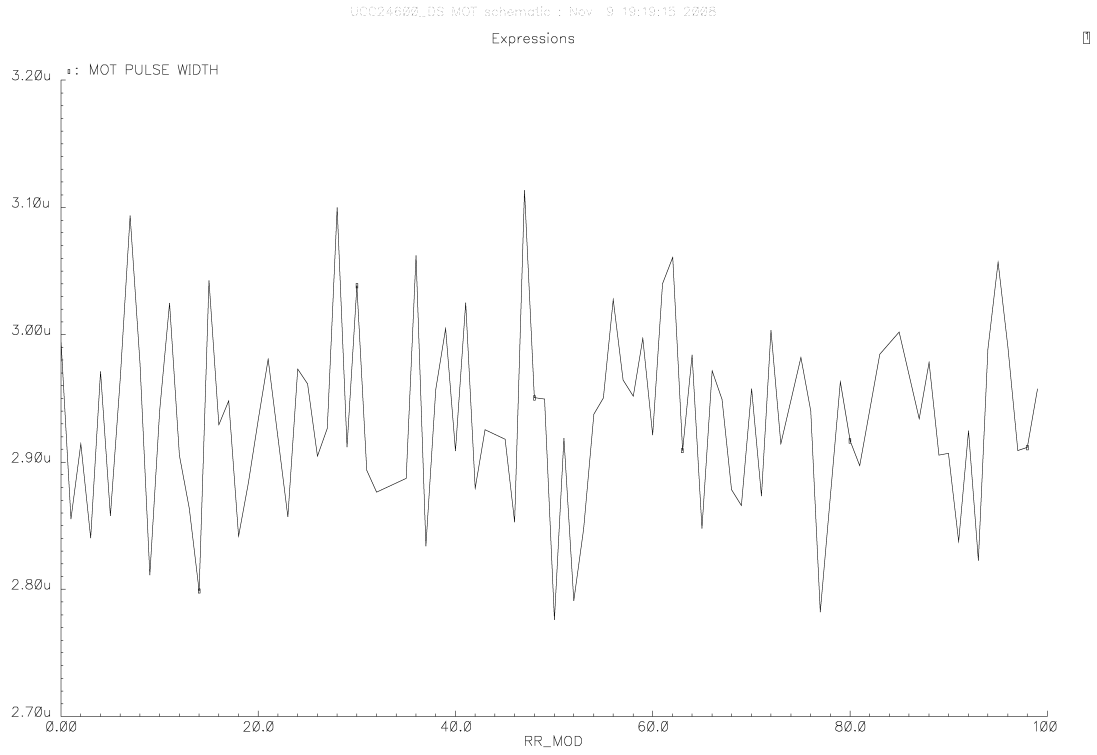

Figure 3-27: Maximum t_{MOT} Over Process Variation

3.6 Minimum Off Timer

The logical dual of the MOT, the minimum off timer (MOFFT) generates a low going, variable width pulse that blanks the internal detection circuitry and ensures the gate drive output remains low for a user programmable length of time. This function is necessary to prevent false turn on signals from being generated by the parasitic voltage ringing on the drain of the SR FET after current decays to zero. The following section details the function of this timer.

3.6.1 MOFFT Operation and Structure

A schematic of the MOFFT system is shown below in Fig. 3-28. This timer is very

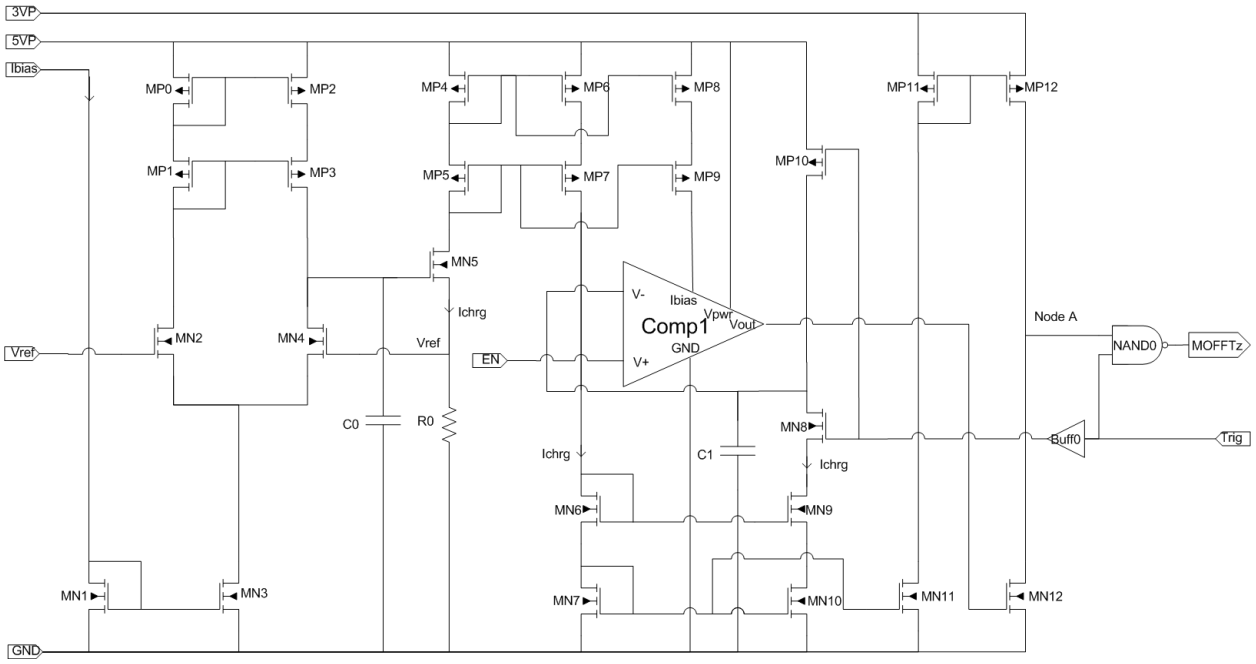

Figure 3-28: MOFFT Schematic

similar in construction to the MOT discussed above. Specifically, amplifier $A0$ and timing comparator $Comp_1$ are identical to the circuits previously described. The differences are as follows. First, I_{chrg} is given by $\frac{V_{ref}}{R_0}$, where R_0 is an internal, rather than external, resistor. Immediately, this timer will be subject to greater output

variation than is the MOT, for integrated resistors drift roughly ±10% over process, while discrete resistors have tighter variation statistics.

Second, the duration of the low going output pulse is given by the discharge time of C_1 from the 5 V rail, to the voltage on the V_+ pin of $Comp_1$. This threshold is given by the voltage on the EN node, and is equal to $I_{EN}R_{EN}$, where I_{EN} is the pull up current on the EN node described earlier, and R_{EN} is a user supplied resistor from the EN node to ground. The range of this resistor is chosen such that the ideal minimum and maximum pulse widths are 500 ns and 5 μs respectively. Unfortunately, this setup decouples the charge current from the comparator threshold voltage, and subjects the MOFFT pulse to variations in both V_{ref} and I_{EN}.

The final difference is that no latches are involved with the operation of this timer. One 3 V NAND gate, one 3-5 V level shifting buffer ($BUFF_0$), and one 5-3 V level shifting inverter (M_{P13} and M_{N13}) are the only logic gates. Nominally, the output of $Comp_1$ is low and the $Trig$ input is low, thus $MOFFT_z$ is high and C_1 sits charged up to the 5 V rail. When $Trig$ transitions high, $MOFFT_z$ drops low and I_{chrg} begins to discharge C_1. When $V_{C1} = V_{EN}$, the output of the comparator goes high, node A falls to zero, and the $MOFFT_z$ low going pulse is terminated. C_1 does not charge back up to 5 V until $Trig$ goes low, which happens at the beginning of the next SR FET conduction cycle.

In terms of pulse width variation, consider the following equation:

$$t_{MOFFT} = R_0 C_1 \frac{5 - V_{EN}}{V_{ref}} \tag{3.31}$$

Noting that all the terms in the above equation have process dependent parameter distributions, the total variation in pulse duration will be significantly higher than that of the MOT.

3.6.2 Enable Node Voltage Clamp

Given that the user is allowed to float the EN pin, a circuit that clamps the maximum voltage on this node is necessary to ensure that $t_{MOFFT,min}$ is a deterministic value.

A schematic of such a circuit is shown in Fig. 3-29. Here, V_{clamp} is equal to $\frac{R_1}{R_0+R_1}5$,

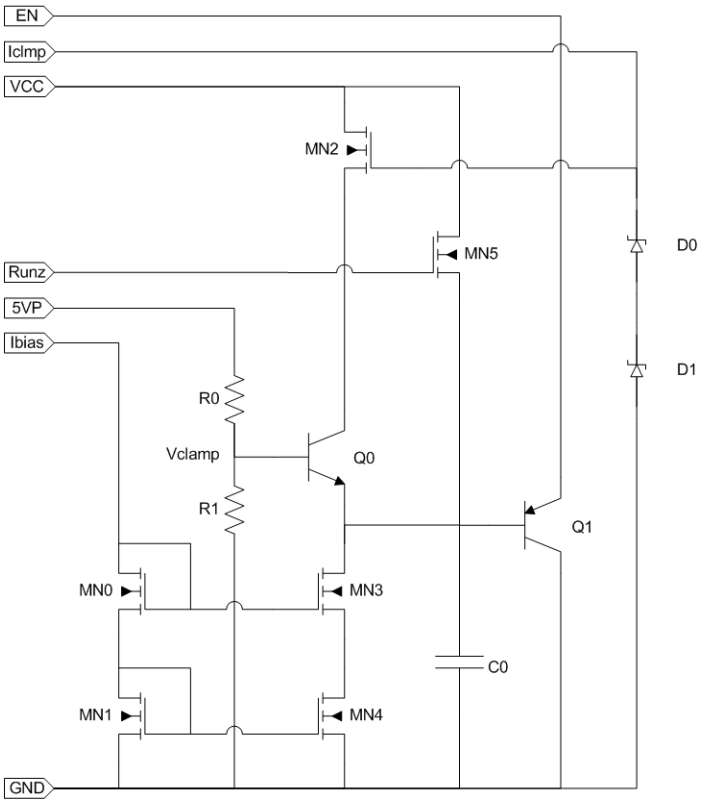

Figure 3-29: EN Node Voltage Clamp Schematic

and the voltage on the base of Q_1 in steady state is

$$V_{Q1b} = V_{clamp} - V_{be,onn} \tag{3.32}$$

where $V_{be,onn}$ is the base-emitter voltage drop of Q_0. Once the voltage on the EN node reaches $V_{clamp} - V_{be,onn} + V_{be,onp}$, Q_1 starts to draw current through its emitter, and actively limits the EN node to this voltage. Given that the base-emitter drops of a npn and pnp transistor are not exactly equivalent, iterative simulations can yield the proper sizing of R_0 and R_1 for the desired clamp output voltage.

The remainder of the devices in this circuit supply bias current to Q_0, and ensure that the EN clamp does not affect the operation of the system during startup. Consider when V_{CC} is below $V_{CC,on}$ and the 5 V rail is at zero. Without M_{N5}, the base of Q_1 would be at ground, and the EN node would be clamped to roughly $V_{be,onp}$,

preventing the circuit from ever coming out of sleep mode, for the power buffer only turns on if $V_{EN} \geq V_{EN,on}$. With the inclusion of M_{N5}, however, the base of Q_1 sits roughly at the value of Run_z, which is significantly higher than $V_{EN,on}$ when the controller is in sleep mode. As soon as normal operating mode is reached, Run_z drops low, the power buffer turns on, and the desired value of V_{clamp} controls the voltage on the base of Q_1. Note that I_{clamp}, D_0, D_1, and M_{N2} are included to limit the operating voltage on the collector of Q_0 to safe levels for this particular device.

3.6.3 Simulated Results

This section presents the simulated performance data for the MOFFT block. Fig. 3-30 is a graph of the minimum low going output pulse duration over 100 Monte Carlo simulation runs at 25° Celsius. Fig. 3-31 is a graph of the same data, but for the maximum pulse width.

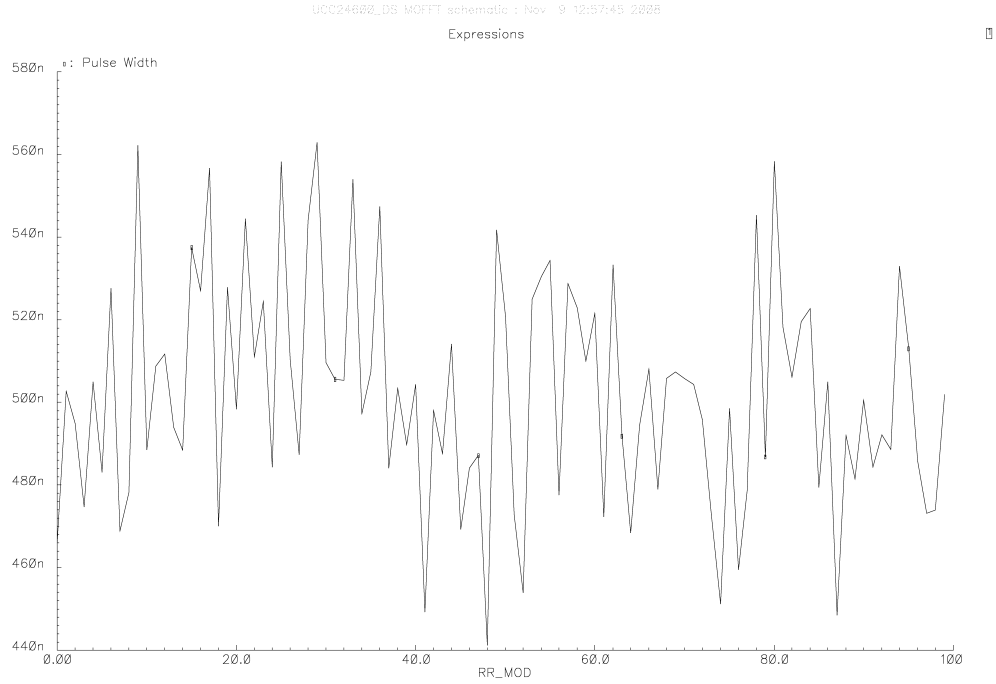

Figure 3-30: Minimum t_{MOFFT} Over Process Variation

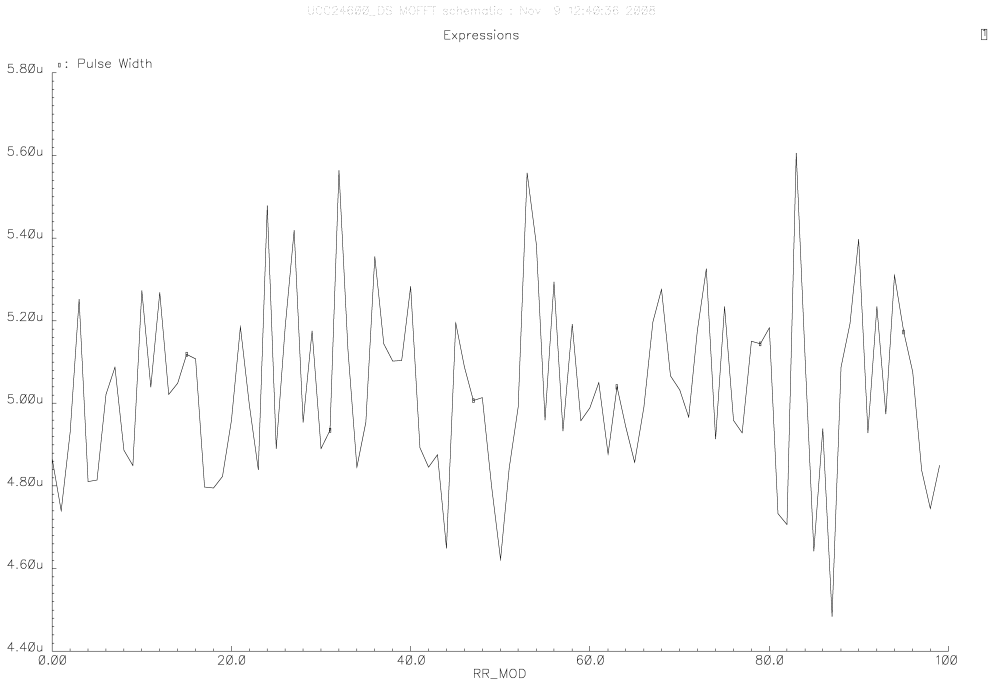

Figure 3-31: Maximum t_{MOFFT} Over Process Variation

The average calculated pulse widths for the two data sets above are 498.1 ns and 4.988 μs respectively. Assuming maximum process variation of 6σ, the total pulse width is accurate to within $\pm 12\%$ of these averages. Over temperature, the standard deviations do not change, but the averages drift $\pm 1\%$. It is important to note that this data does not include variation due to the EN node pull up current, which brings total pulse width accuracy to within $\pm 20\%$ of the averages.

3.7 Detection Circuitry

The final circuits of interest inside this secondary side controller are the three external signal comparators that sense the voltage across the SR MOSFET and detect primary side switching events. These circuits were designed by Robert Neidorff, an engineer at Texas Instruments, and thus the schematics cannot be reproduced in this document. A brief discussion of the specifications of these circuits is presented below.

3.7.1 -3 mV Comparator

Turn off of the SR FET in discontinuous conduction mode is triggered by the current in the device decaying to zero. This condition is detected by the system when the magnitude of voltage from drain to source of the SR FET falls below 3 mV. An additional requirement is that the gate of the SR FET must begin to fall 20 ns after this threshold is reached. Given the difficulty in detecting such low voltage levels, and the stringent speed requirements of the system, a robust comparator with extremely fast transistors is necessary.

A block level view of this comparator is shown in Fig. 3-32. Taking advantage of the minimum time between successive conduction cycles (500 ns), the comparator includes an offset trimming circuit to ensure consistently accurate threshold voltage. As soon as the MOFFT block is activated, the *Compare* signals go low, and the *Zero* signals go high. This event places the comparator in "trim" mode, where the V_+ input is shorted to ground and the V_- input is tied to 3 mV. M_{P1} and M_{P2} then regulate the output of the comparator to half way between its supply voltage and ground

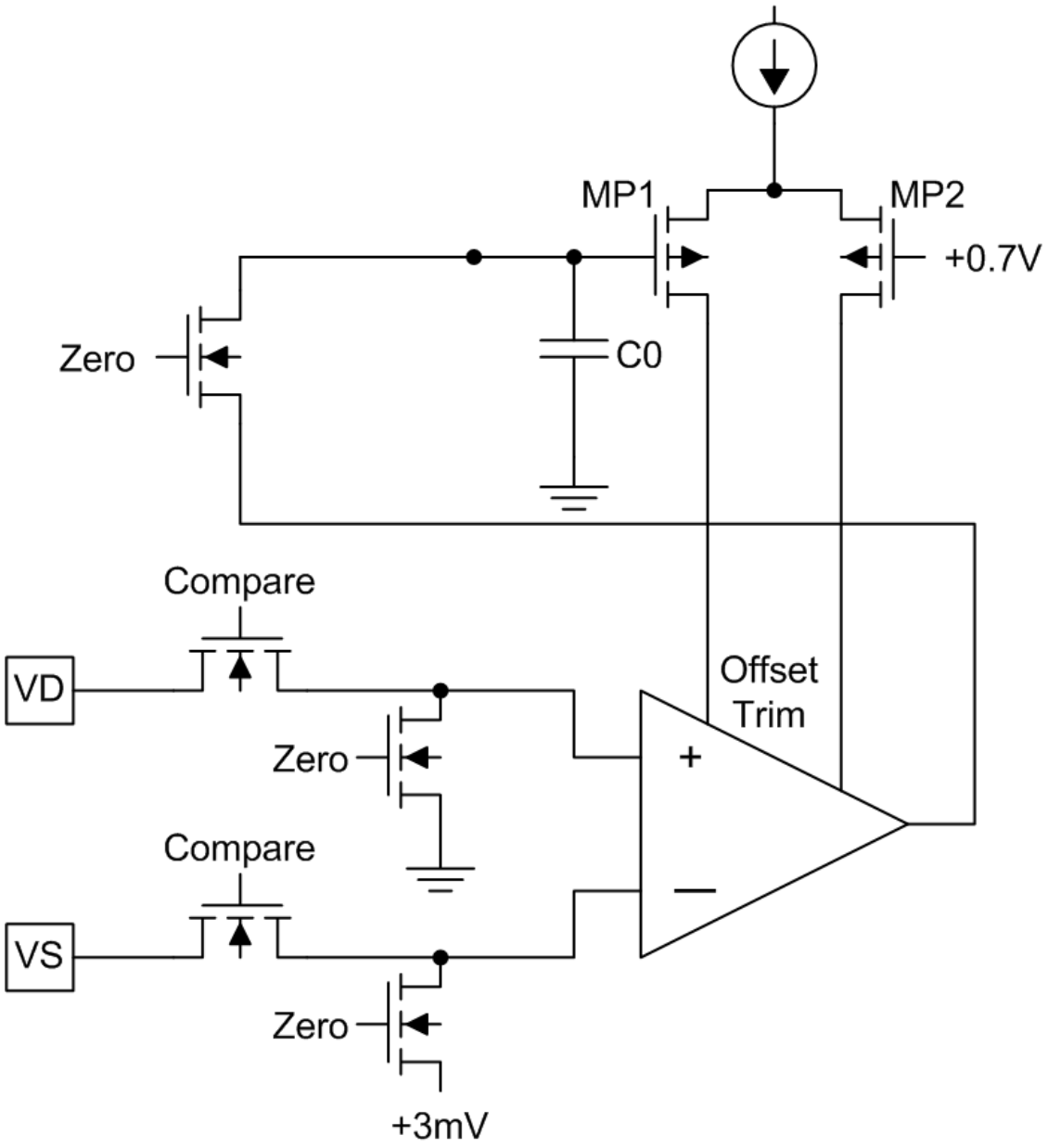

Figure 3-32: -3 mV Comparator Functional Diagram

by injecting differential current into the system. This process forces the switching threshold of the comparator to occur when V_+ is 3 mV below V_-, regardless of any process shifts and input offset voltages. Once the $Zero$ signals go low, the comparator is back to normal operating mode, and the voltage induced on the gate of M_{P1} during "trim" mode is stored on C_0. Thus, every conduction cycle, the -3 mV comparator always trips at the proper threshold. As long as the "trim" mode lasts less than $t_{MOFFT,min}$, the system is never adversely affected by this operation.

Simulation of this block yields typical switching voltages of -3.7 mV at 150° Celsius and -5.15 mV at -50° Celsius. Typical comparator delays are on the order of 12 ns, as will be shown in the top level simulation section.

3.7.2 -100 mV and Primary Synchronization Comparators

The -100 mV comparator is responsible for detecting when current begins to flow through the body diode of the SR FET, and thus when to apply power to its gate. Given that the drop across a typical MOSFET body diode is roughly 1 V [6], the requirements on the accuracy of this comparator are not particularly rigid. Even if the threshold drifts ±50 mV, the overdrive on the inputs will still be sufficient to trigger turn on at the right instant.

The primary synchronization comparator detects switching events on the primary side of the converter system. When the appropriate primary switch turns off, a negative pulse couples through to the $SYNC$ pin of the controller. This pulse triggers the primary synchronization comparator, and the SR MOSFET gate is immediately shut off if the current in the SR FET has not already decayed to zero. This block is subject to the same speed requirements as the -3 mV comparator, namely that the gate drive output must begin to fall 20 ns after a triggering event. Supporting simulation data can be found in the next section.

3.8 Top Level Simulation Results

This section presents simulation data for the entire controller system. All of the blocks described above are hooked together as shown in Fig. 3-33. Note that the block labeled V_{ds} $Comp$ includes the -3 mV and -100 mV comparators and all of the control logic for the chip. Additionally, all simulations include a 100 pF load capacitor placed from the $GATE$ pin to ground representing the gate capacitance of a typical SR FET.

Fig. 3-34 shows the steady state room temperature switching waveforms of the controller in a converter system designed to operate at 170 KHz. The voltage on the V_d pin of the controller (DRAIN) is a piecewise linear waveform meant to simulate discontinuous conduction mode operation. As evident, the gate drive signal is high during the conduction period of the SR FET, and the MOT and MOFFT timer pulses are triggered at the proper times. The resistances on the EN and T_{on} pins to ground are sized for minimum pulse widths. Additionally, no significant voltage spikes are noticeable on the 3 V and 5 V power rails during internal logic switching events.

The next two figures exemplify the important voltage thresholds and propagation delays of the controller. Fig. 3-35 shows the delay between -100 mV detection and the gate drive output rising at room temperature. As can be seen, the -100 mV comparator trips at roughly the correct threshold, and the delay before the gate drive starts to rise is 27 ns. The rising delay limit is 40nS, thus the system outperforms the design specification. Fig. 3-36 shows the delay between -3 mV detection and the gate drive falling. The detection point for this graph is $V_{DS} = -3.9$ mV and the propagation delay to the gate driver is 13.7 ns. Both of these values are well within the required limits.

Finally, Fig. 3-37 shows the delay between the detection of a primary side turn off event, and the gate drive output being driven low. The magnitude of V_{DS} is assumed to be instantaneously greater than the -3 mV threshold, thus the converter is operating in continuous conduction mode. As demonstrated, the delay is 18.6 ns at room temperature. This value is also acceptably below the design specification.

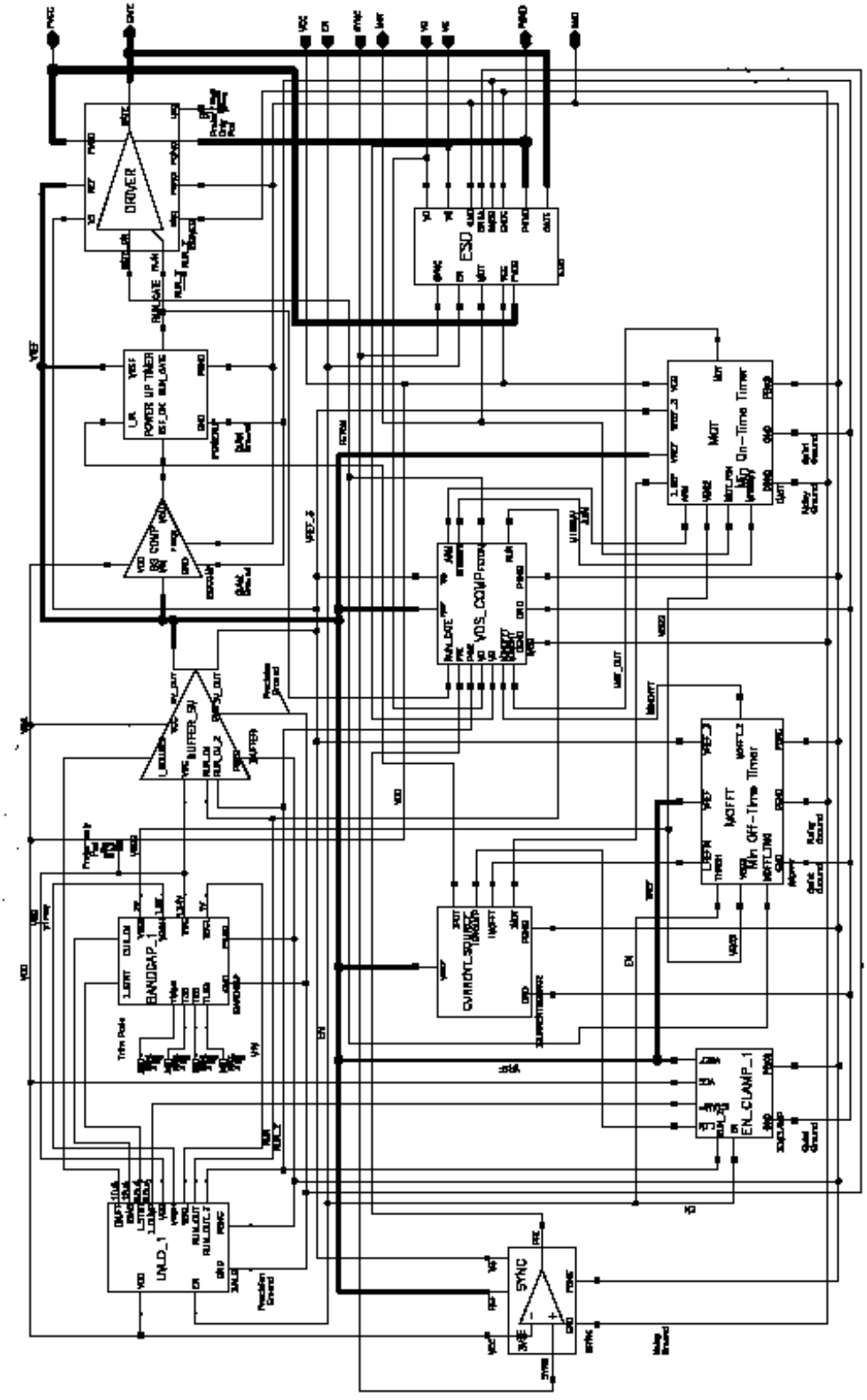

Figure 3-33: Top Level System Schematic

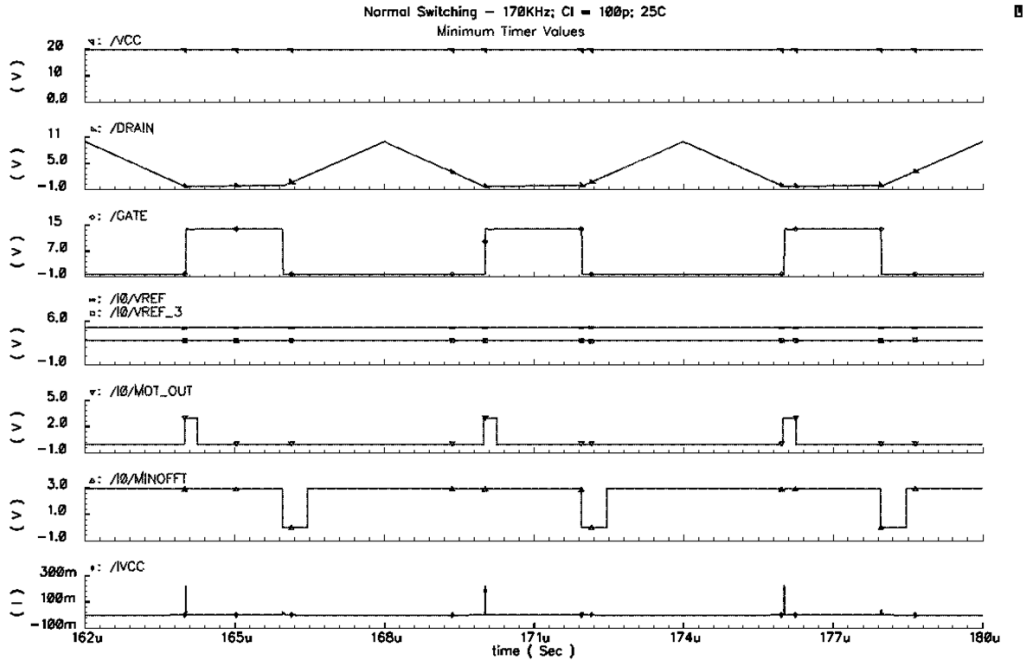

Figure 3-34: Simulated Steady State Controller Switching Waveforms

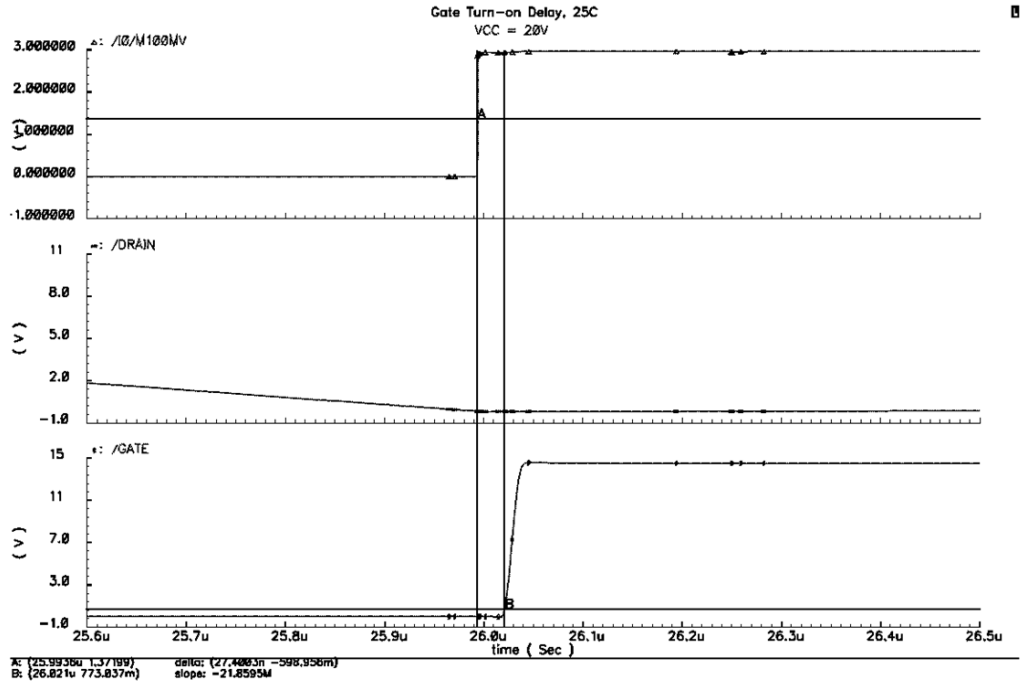

Figure 3-35: Simulated Gate Drive Turn On Waveforms

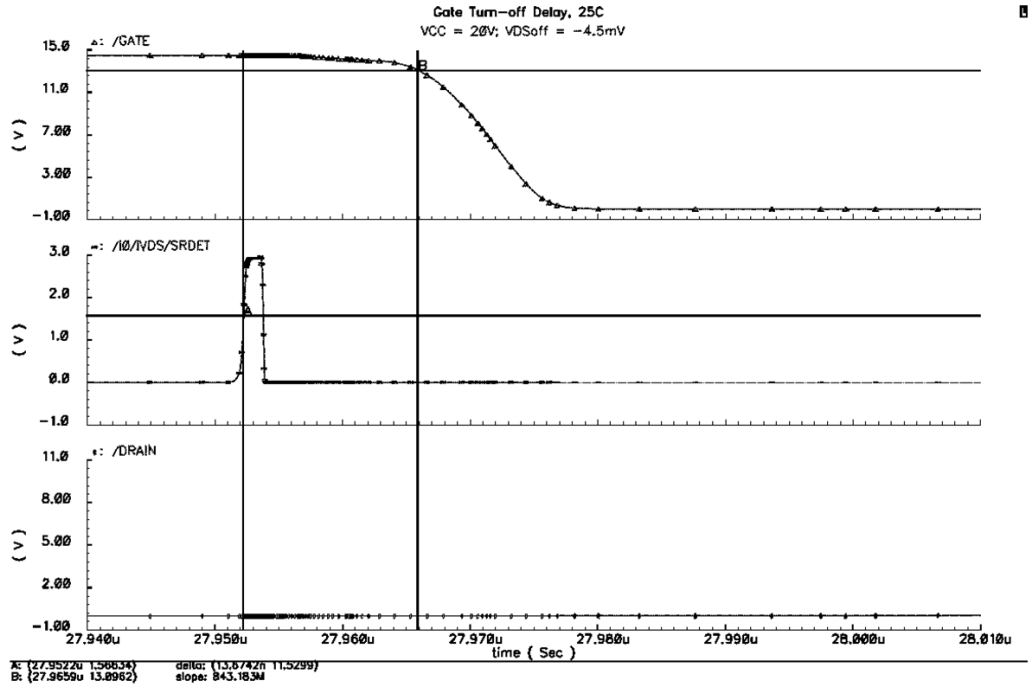

Figure 3-36: Simulated Gate Drive Turn Off Waveforms

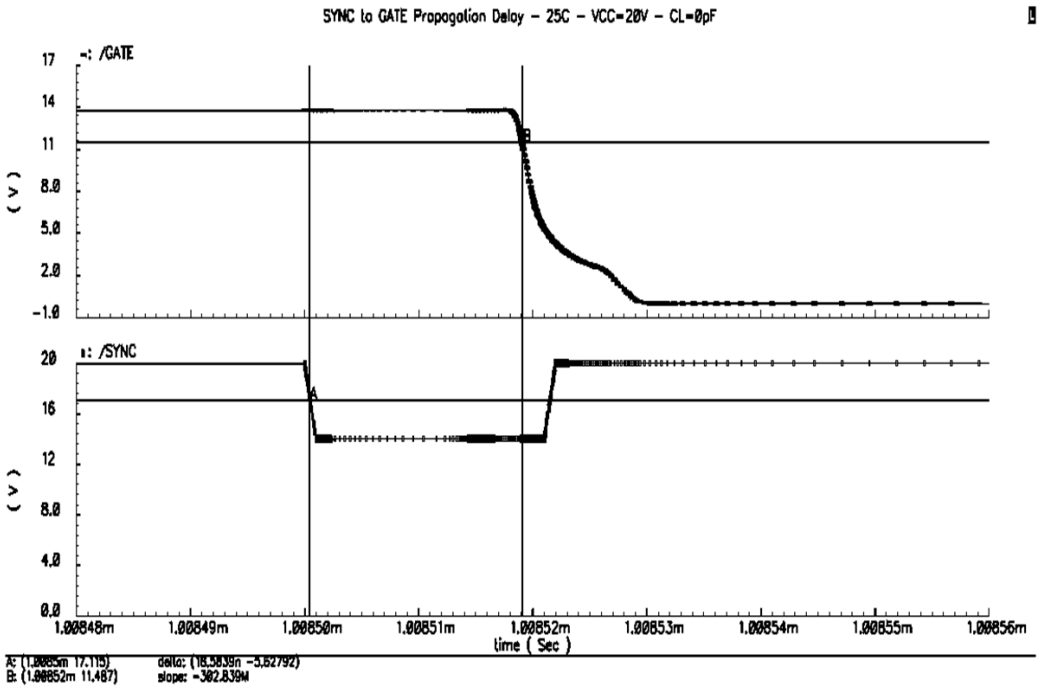

Figure 3-37: Simulated Primary Synchronization Turn Off Waveforms

3.9 Summary

This chapter has explored the design and simulated performance of an integrated secondary side synchronous rectification controller for use in an LLC resonant converter. This chip was designed on a proprietary Texas Instruments silicon IC process, and is meant to be sold as a competitive product. As exemplified by the previous discussion, the performance of this chip far exceeds its aggressive design targets. Additionally, the broad applicable converter frequency range, inclusion of primary synchronization capability, and accurate detection and timing circuitry, uniquely identify this chip as an industry leading SR controller.

I would also like to briefly mention that the practical experience gained from participating in the industrial design process is invaluable. As will be discussed in the next chapter, it is exceedingly difficult to address many real world IC design issues given the inherent limitations of a classroom environment. Working in industry, even briefly, is an excellent method for expanding upon one's skill set and abilities as an IC designer.

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Chapter 4

Simulation and Exercise Framework for a Power IC Design Course

More and more, companies are discovering that new electrical engineering graduates have limited applicable experience with integrated circuit (IC) design. Issues such as thermal behavior, manufacturing process variation, practical circuit construction, and layout considerations are overlooked in a typical curriculum due to resource and time constraints. Additionally, instructing students about modern IC fabrication is difficult, considering that industrial techniques are continually evolving [1].

A new laboratory course has been developed for advanced undergraduate or beginning graduate students that intends to fill in this knowledge gap that has been growing between educational and industrial power IC design realms. The specific objectives of this course include the following:

1. Introduce students to the fundamentals of power converter control theory.

2. Teach students to design analog control circuitry block by block.

3. Teach students to simulate models of their circuit designs.

4. Instruct students on how to build and debug their circuits and compare exper-

imental results with their simulated results [1].

As mentioned in Chapter 1, a hardware kit exists that allows for the construction of a complete power electronic controller. The kit consists of individual functional modules that plug into a motherboard. Each module is a predesigned printed circuit (PC) board meant to mimic a common IC building block, such as a bandgap reference, error amplifier, or clock. Students populate these boards with components of their choosing, and then fit them all together on the motherboard to form customized controllers. Ideally, the overall experience is foundationally similar to that of integrated circuit design, while still enabling the use discrete components [1].

Important distinctions do exist, however, between integrated and discrete circuits. Most notable is the use of resistors. In the discrete world, resistors are small, two terminal devices that take up less room on a printed circuit or bread board than do transistors, which are larger, three terminal devices [1]. On an integrated circuit, however, resistor are fabricated from various types of silicon, poly-silicon, and metal constructs, and take up orders of magnitude more die area than do bipolar or MOS devices. Thus, on an IC, resistors are only used if absolutely necessary, and are normally replaced by transistor equivalents whenever possible [5]. Another important difference is that discrete thermal and geometric matching is only available on an extremely limited basis [1]. Therefore, when matching is critical in a given module, pairs of transistors fabricated on the same die are used.

This chapter presents the simulation and written exercise framework, intended to couple with the preexisting hardware kit discussed above, that allows students to verify their potential designs. SPICE schematics of each PC board module with *stock* component values are shown, along with typical simulation results and potential classroom/homework exercises. Given its ease of use, strong convergence likelihood, and free academic license, LTSPICE has been chosen as the ideal simulation environment for this course.

Before individual modules are presented, however, a review of the course design methodology is appropriate.

4.1 Design Methodology

Without a doubt, simulation is an essential tool in integrated circuit design. In fact, the speed and ease with which particular topological criteria can be verified is essential to the industrial community, as discussed in Chapter 3. Unfortunately, designs that are based on simulation alone suffer consequences resulting from the hidden assumptions and inherent limitations of most simulation environments. SPICE, for example, does not predict the effects of thermal runaway on un-degenerated bipolar current mirrors, thus, a design that is functional in simulation may destroy itself once constructed [1].

Given that SPICE should not be thought of as a primary design media, students are instructed to begin with hand calculations, where order-of-magnitude quantities prevail over exact numbers [1]. This is the stage where true engineering intuition is developed. Students must choose appropriate approximations, such as small signal and linear equivalent circuit models, in order to properly estimate useful component values. From an enormous array of concepts, students learn to identify and employ those that will roughly predict the operation of their circuits. In so doing, they are assured to fundamentally *understand* the circuits they design, and are able to foresee simulated outcomes. It can be argued that one does not simulate unless one has a prediction of the result [1].

Once the component calculations are complete, SPICE simulation is useful in verifying the legitimacy of the values. On the occasion that the simulated answers disagree with expected ones, students must revisit their initial assumptions and revise their hand calculations. In this way, simulation works to illuminate circuit design concepts, rather than obscure them, and is thus an essential part of this power IC laboratory course.

The following Sections detail the simulation framework developed for each IC module to enable the design verification process.

4.2 Regulator and Reference Board

This Section presents relevant information about the voltage regulator and bandgap reference board. It is split into two subsections, where each part of the board is discussed separately.

4.2.1 Voltage Regulator

A linear voltage regulator is an essential block of any integrated power controller, and serves as an important starting place in the study and motivation of power conversion techniques. A PC board module exists upon which students build a linear regulator based on a single stage operational amplifier and output driver. The SPICE schematic for this circuit is shown in Fig. 4-1. Note that two regulators exist on each PC board module, and their respective outputs are meant to function as the internal power rails for the remainder of the controller circuitry.

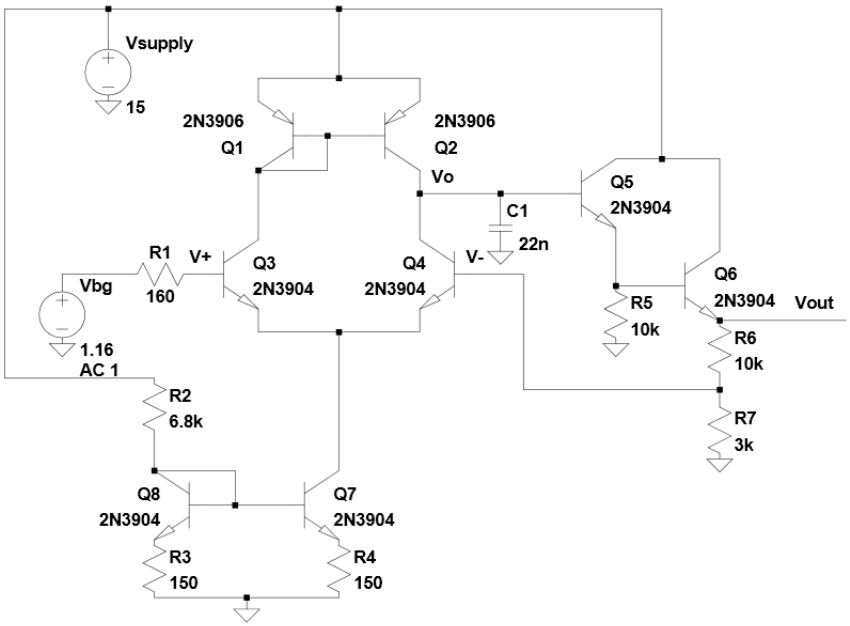

Figure 4-1: Discrete Linear Voltage Regulator Schematic

Transistors Q_1 - Q_4 form the differential input stage to the regulator, where Q_3 and Q_4 are an NPN emitter coupled pair, and Q_1 and Q_2 are a PNP current mirror

load. This configuration results in a low frequency differential voltage gain of

$$|\frac{V_o}{V_{id}}| = g_m r_o \tag{4.1}$$

where V_{id} is the magnitude of differential input voltage, g_m is the transconductance of one of the input transistors, and r_o is the parallel combination of the incremental output resistances of Q_2 and Q_4 [2]. Q_5 and Q_6 form a Darlington output follower stage where the small signal gain from the base of Q_5 to the emitter of Q_6 is one [2]. The base of Q_4 is connected to the tap of the output voltage divider formed by R_6 and R_7, while the base of Q_3 is connected to the bandgap reference voltage, which will be explained shortly. The result of this entire topology is a circuit that functions as a canonical non-inverting feedback amplifier, like the one shown in Fig. 4-2. A_0

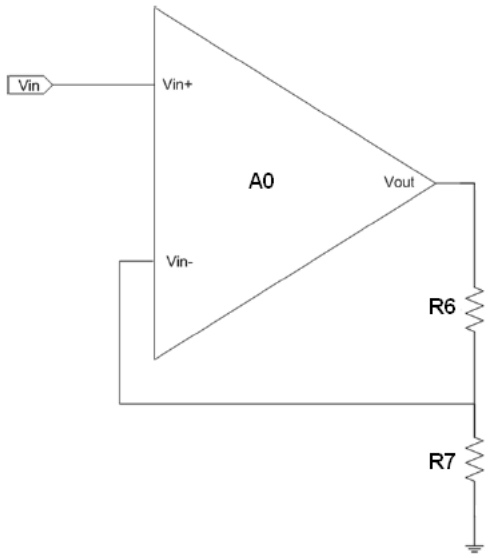

Figure 4-2: Canonical Non-Inverting Feedback Amplifier

represents the single stage differential amplifier and Darlington output stage discussed above, while R_6 and R_7 function as the feedback voltage divider. The output voltage

of such a circuit is given by

$$V_{out} = \frac{R_7 + R_6}{R_7} V_{in} \tag{4.2}$$

assuming that the gain of amplifier A_0 approaches infinity. While unrealistic, this assumption simplifies the general analysis of this circuit and is largely accurate if the gain is adequately high [2]. The meaning of *adequately* is left as an exercise to the student, and is discussed later.

When the circuit of Fig. 4-1 is compared to a functionally similar circuit used in a real IC, (see Fig. 3-19 from Chapter 3) certain differences can be observed. Aside from a MOS implementation, the use of input followers, and extra control signals, the most important topological distinction between the two circuits is the lack of degeneration resistors in the biasing current mirrors of the IC regulator. For a well designed mirror, the output current will almost exactly match the input current, a characteristic that heavily relies on the geometric matching of the two (or more) transistors involved [2]. On a given IC, modern fabrication and layout techniques can yield high degrees of matching between devices on the same silicon die, thus, current mirror linearity is quite high. With discrete devices, however, direct geometry matching is nearly impossible [1]. Emitter degeneration resistors are used in lieu of device matching to achieve the linearity required in a discrete mirror.

To understand the effect of these resistors, consider the case when R_3 and R_4 in Fig. 4-1 are not present. As derived in [2], the output current of such a mirror equals

$$I_{out,m} = \frac{I_{s7}}{I_{s8}} I_{in,m} \tag{4.3}$$

where $I_{out,m}$ is the collector current of Q_7, and $I_{in,m}$ is the collector current of Q_8. If the mirror is designed to have unity gain, the saturation currents of both devices, I_{s7} and I_{s8}, must be equal. Note that these two parameters are linearly dependent on the emitter areas of their respective devices. If Q_7 and Q_8 are implemented as two discrete transistors, a deterministic value for the ratio of their saturation currents is impossible to attain, thus the resulting current mirror will not function as intended [2].

Consider what happens, however, when R_3 and R_4 are added back into the circuit analysis. The base voltage of Q_8 becomes

$$V_{b8} = I_{in,m}R_3 + V_{be,on} \tag{4.4}$$

where $V_{be,on}$ is roughly equal to .6 V [10]. Given that the $V_{b7} = V_{b8}$, the voltage across R_4 is

$$V_{R4} = V_{b8} - V_{be,on} = I_{in,m}R_3 \tag{4.5}$$

where we have assumed that the base-emitter drops of both Q_7 and Q_8 are equal to $V_{be,on}$. Finally, the output current of the mirror is

$$I_{out,m} = I_{R4} = \frac{R_3}{R_4}I_{in,m} \tag{4.6}$$

As evident, the current gain only depends on the ratio of $\frac{R_3}{R_4}$. For discrete precision resistors, the tolerance on stated device values is $\pm$ 1%, thus the worst case current mirror error is limited to $\pm$ 2%. When compared to the enormous error incurred without degeneration [2], the inclusion of R_3 and R_4 is more than justified.

Such comparative analysis is essential for the success of this laboratory course. Every circuit block *must* be framed in IC domain for students to gain a true intuitive understanding of the design process. By highlighting technology dependent asymmetries, buried intricacies become apparent, and topics that are not explicitly part of discrete circuit design, such as device layout and matching, can be effectively taught.

After the hand calculation design stage is complete, students are instructed to simulate their circuits in SPICE. For the linear voltage regulator, students use the schematic in Fig. 4-1, where the *stock* component values are replaced by their own. Hopefully, the simulated performance of the student's circuit will match or exceed some base metric set by the instructor. An open-loop bode plot of the input to output characteristics of the *stock* circuit is shown below in Fig. 4-3. As can be seen, the circuit is dominant pole compensated, resulting in a crossover frequency of 293 KHz and a phase margin of 90°. From this plot, all closed loop dynamics can be

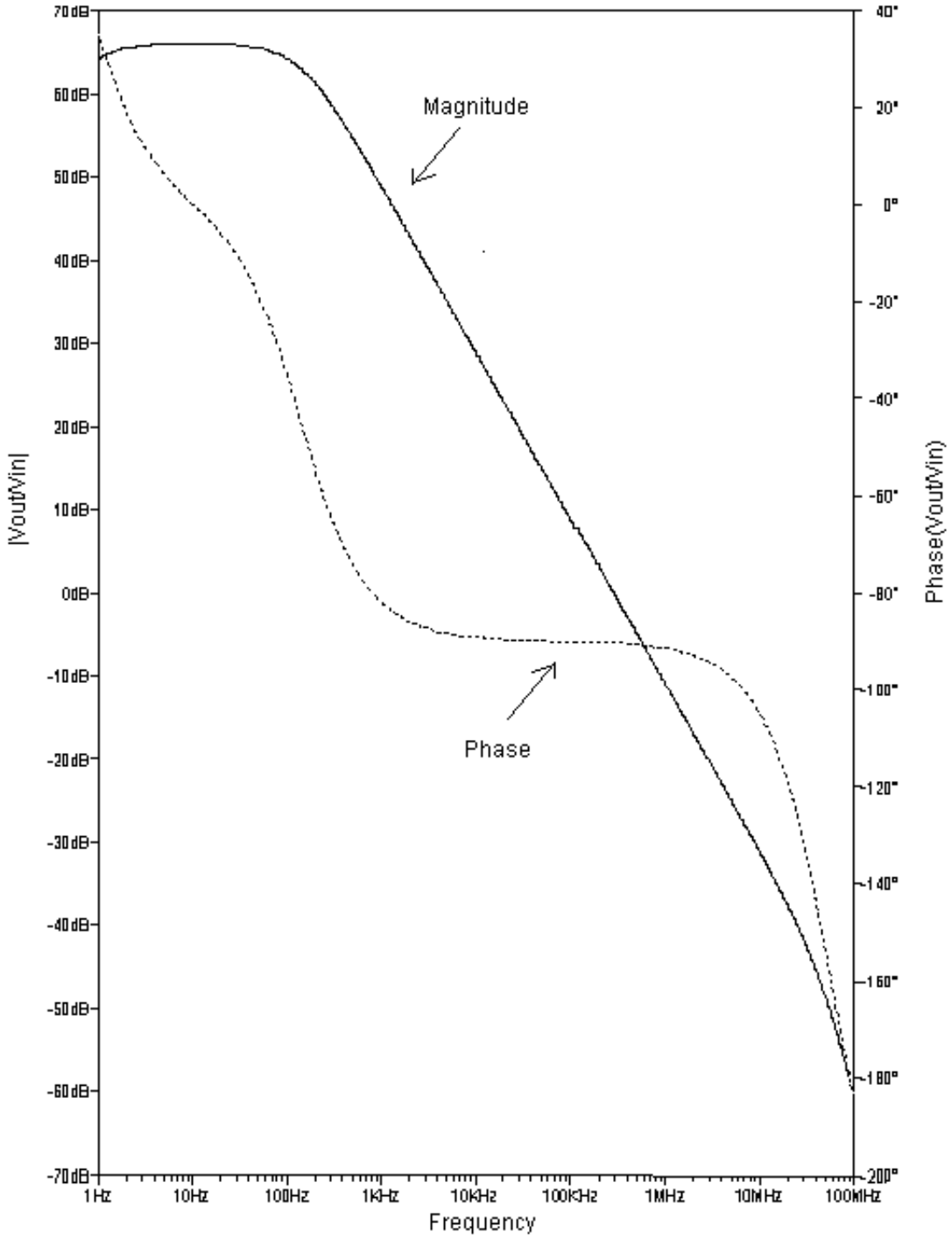

Figure 4-3: Bode Plot of $\frac{V_{out}}{V_{in}}$ Magnitude and Phase for the Open-Loop Stock Regulator

2N3904	**MAT03**
Q_5 Q_6 Q_7 Q_8	Q_1 Q_2
LM394	**Passives**
Q_3 Q_4	Remaining components

Table 4.1: Bill of Materials for Voltage Regulator Module

found [7].

The bill of materials for one of the actual discrete voltage regulator modules can be found in Table 4.1.

Coupled with each laboratory module are corresponding homework problems, intended to further illustrate associated design concepts. Referencing Figs. 4-1 and 4-3, several potential problems are discussed below. Note that some of the answers should result from hand calculations, and not blind simulation.

1. *What is the open-loop, dc gain of the regulator op-amp circuit?* This question helps students to understand the difference between an ideal and real op-amp, where gain is no longer infinity. This should be done without simulation.

2. *What effect does finite gain have on the desired output voltage of the regulator?* This question results in a steady state error calculation, and explains why high op-amp gain is desirable. Any lingering concerns about what *adequate* amplifier gain implies should be alleviated.

3. *Come up with an approximate transfer function for the open-loop operation of the amplifier.* This directive should get students thinking about the frequency response and stability of the regulator. Several sub-questions are now necessary.

    - *Based on this function, what is the unity gain crossover frequency?*
    - *What is your estimation for the phase margin? Larger than 45° ? Smaller? Why?*
    - *What would happen without capacitor C_1 ?*

Students should be able to use their calculated answers, and compare them to simulated results. Ideally, this will reinforce an understanding of amplifier stability metrics, methods for compensation, and gain/bandwidth tradeoffs. It will also allow them to revise their designs and approximations if simulation and calculation disagree.

4. *What accounts for the differences between your estimations and SPICE's results?* Even if hand calculation and simulation yield similar results, some difference will always be evident. Students must realize that the circuit models they use for analysis are approximate. Additionally, this question could potentially lead into exploration of the SPICE algorithm, if an instructor so desires.

4.2.2 Bandgap Voltage Reference

Much like the power buffer block in the SR controller of Chapter 3, the voltage regulator discussed above requires a stable, temperature invariant voltage reference from which its output voltage is derived. A high level schematic of this reference circuit is shown below in Fig. 4-4. Assuming that A_0 has adequately high gain, the voltage on the inverting and non-inverting terminals of the amplifier will be equal. The output voltage of the reference, therefore, is equal to

$$V_{BG} = V_{be9} + V_{R6} \tag{4.7}$$

To find V_{R6}, look at the voltage across R_7:

$$V_{R7} = V_T ln \frac{I_{C9} I_{S8}}{I_{C8} I_{S9}} \tag{4.8}$$

Assuming Q_8 and Q_9 are implemented as a matched pair, and realizing that $\frac{I_{C9}}{I_{C8}} = \frac{R_6}{R_5}$, V_{R7} can be written as

$$V_{R7} = V_T ln \frac{R_6}{R_5} \tag{4.9}$$

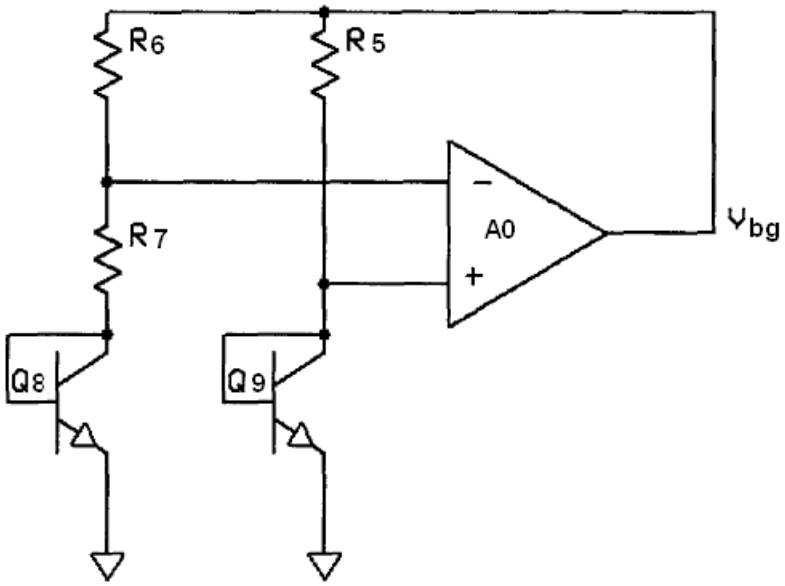

Figure 4-4: High Level Bandgap Voltage Reference Schematic

By finding the current flowing through R_7, and multiplying by the value of R_6, V_{R6} can be expressed as

$$V_{R6} = V_T \frac{R_6}{R_7} ln \frac{R_6}{R_5} \tag{4.10}$$

The final expression for the output voltage is now

$$V_{BG} = V_{be9} + (\frac{KT}{q}) \frac{R_6}{R_7} ln \frac{R_6}{R_5} \tag{4.11}$$

where the thermal voltage, V_T, has been replaced by its constituent relationship. Thus, the output voltage of this circuit is of the same form as that of the hypothetical bandgap voltage reference presented in Section 3.3.1, Fig. 3-12:

$$V_{out} = V_{be} + M(\frac{KT}{q}) \tag{4.12}$$

where the positive temperature coefficient gain, M, is given in this case by

$$M = \frac{R_6}{R_7} ln \frac{R_6}{R_5} \tag{4.13}$$

The actual discrete implementation of this circuit is shown below in Fig. 4-5. A_0 is almost the dual of the amplifier in the voltage regulator discussed above, where the input stage is comprised of a PNP differential pair and an NPN current mirror load. For reasons discussed earlier, Q_5 and Q_6 must be a matched pair to ensure current mirror linearity. This amplifier also contains a common emitter output stage to increase the overall dc gain and minimize the input offset voltage [2].

Students are required to reduce this circuit into the system schematic shown in Fig. 4-4. A similar strategy to that presented at the end of Section 3.3.1 can be used to choose a nominal temperature where the slope of the output voltage vs temperature is 0, calculate the required value of M, and then size R_5 - R_7 appropriately.

Once the initial calculations are complete, students must simulate their own designs using a supplied SPICE schematic with initially blank values. Results for the sample bandgap reference shown in Fig. 4-5 are presented below. In this implementa-

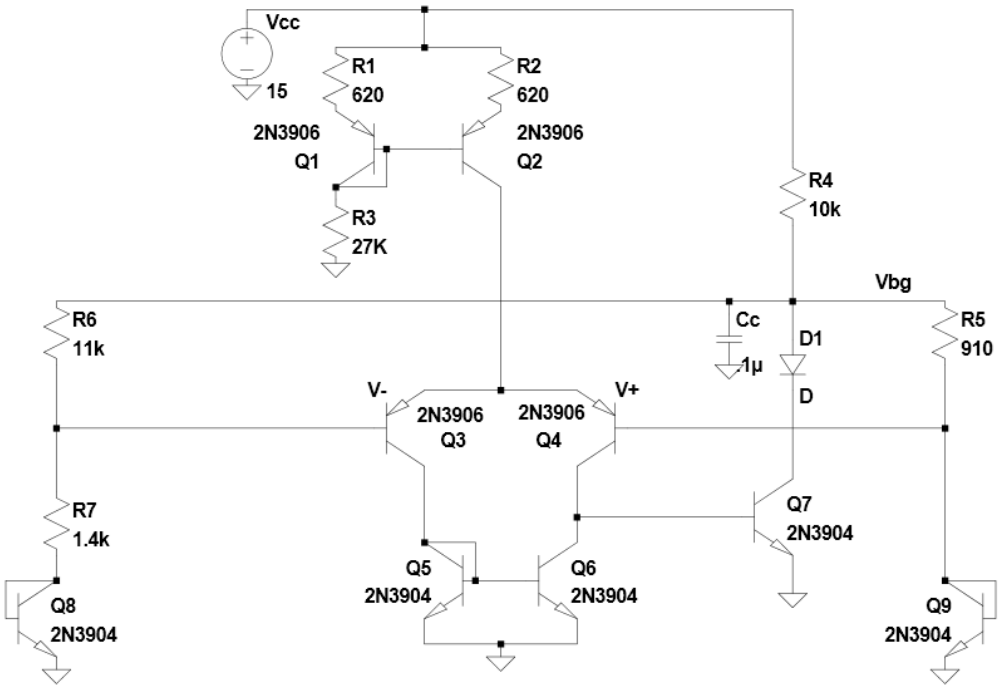

Figure 4-5: Discrete Bandgap Voltage Reference Schematic

tion, the output voltage varies 100 mV peak to peak over a 200 °C range. While still acceptable for most power controller applications [6], the output swing is two orders of magnitude greater than that of the integrated bandgap reference in Section 3.3.2. This discrepancy helps to exemplify the performance limitations of discrete circuits.

The bill of materials for the actual discrete bandgap reference module can be found in Table 4.2.

2N3904	**2N3906**
Q_7 Q_8 Q_9	Q_1 Q_2
LM394	**MAT03**
Q_5 Q_6	Q_3 Q_4
1N4148	**Passives**
D_1	Remaining components

Table 4.2: Bill of Materials for Bandgap Reference Module

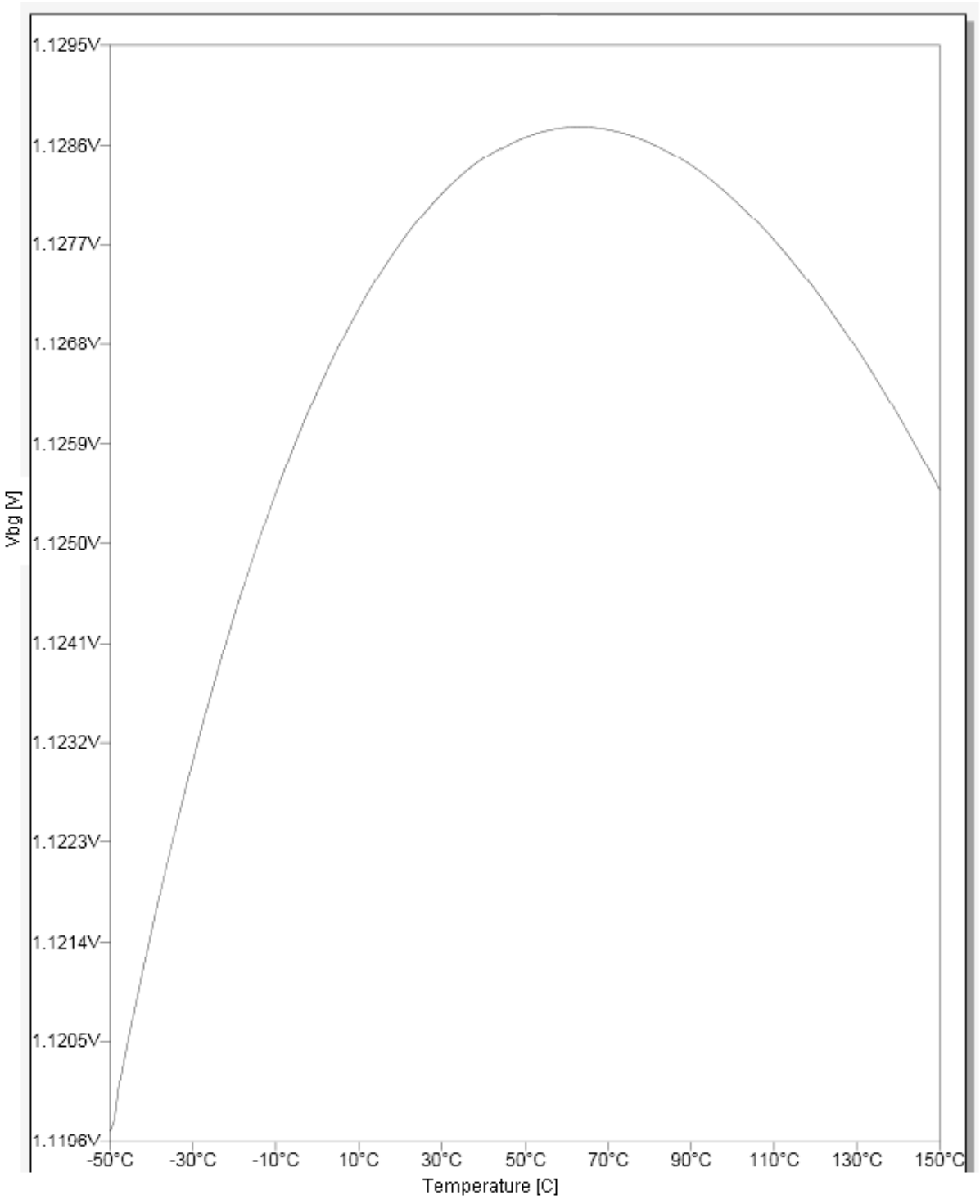

Figure 4-6: Simulated Discrete Bandgap Output Voltage for a DC Temperature Sweep $-50 \leq T \leq 150C$

Corresponding homework problems for this laboratory module are as follows:

1. *Consider Fig. 4-4.*

   - *What are the voltages at the inverting and non-inverting terminals of A_0?*
   - *What is the voltage across R_7? Reduce this value to an expression linearly dependent on temperature.*
   - *What is the value of the current running through R_6?*
   - *Derive an expression for the output voltage, V_{BG}? What is the temperature dependence of this quantity?*

   This series of questions directs students towards deriving the temperature dependence of the output voltage. While the operation and theory of bandgap references will most likely have been covered in the classroom, personal derivation is essential to complete understanding.

2. *What are the requirements for A_0?* After learning about the non-ideal characteristics of real op-amps, this question forces students to think about the strict regulation requirements for proper bandgap function.

3. *Why is it essential that Q_5 and Q_6 be implemented as a matched pair? What effect on system performance would Q_5 and Q_6 have if they were instead two discrete transistors?* This question reinforces important discrete design concepts, and can be used to bring up IC matching and layout issues.

4. *How do the open-loop dynamics of A_0 differ from those of a single gain stage amplifier? What do closed-loop stability requirements imply about the location of the crossover frequency and the size of C_C?* Another op-amp question, students should be able to identify the increased difficulty of compensating a system with two low frequency poles, and calculate the dependence of the unity gain crossover frequency on C_C.

5. *Why does the simulated bandgap output voltage look parabolic over temperature? At what temperature does the $\frac{dV_{BG}}{dT}$ go to zero?* Connecting

simulation with calculation, students need to realize that the circuit as constructed can only suppress the linear temperature dependence of the output voltage. The resultant parabolic curve exemplifies the parasitic effect of higher order temperature coefficients on the system. Ideally, the temperature at which 0 T_c is observed coincides with the student's target design value.

6. *Why is a startup circuit for this reference necessary?* As a final question, students are asked to explain the need for some kind of startup circuit that keeps the reference out of its stable 0 current state. It is important to note that this operating condition is an example of something that could be missed if the entire circuit design is based only on simulation.

4.3 Clock Board

An accurate clock is a vital piece of any power supply control circuit, and is used primarily to set the switching frequency of a given converter system. In this course, students are exposed to various clock topologies, however only one is actually constructed.

4.3.1 Exponential Relaxation Oscillator

In order to teach the basics of clock operation, the exponential type relaxation oscillator of Fig. 4-7 is presented to students first. The operation of this timer is very straightforward. Assume the controller is operating in steady state and the voltage on the inverting terminal of *Comp* has just exceeded that of the non-inverting terminal. This event brings the clock output low, and simultaneously lowers the switching threshold, given by the voltage on the non-inverting terminal of *Comp*, to

$$V_{th,on} = \frac{R_4||R_5}{R_3 + R_4||R_5}5 \tag{4.14}$$

The clock will remain low until the voltage across C decays to $V_{th,on}$. When this happens, the clock output transitions high, C begins to charge up, and the threshold

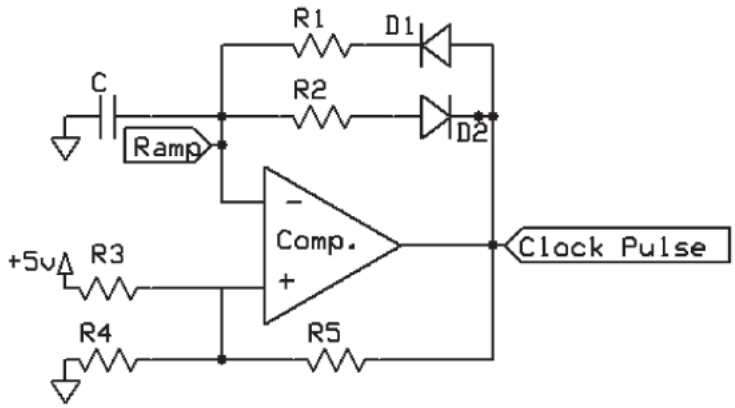

Figure 4-7: RC Exponential Type Relaxation Oscillator

on the non-inverting terminal jumps to

$$V_{th,off} = \frac{R_4}{R_4 + R_3||R_5}5 \tag{4.15}$$

In this way, the clock output continually oscillates while the voltage across C charges up and down between the two switching thresholds. The effect of these thresholds changing in the direction of comparator output voltage is known as *hysteresis*, and is the basis of operation for all relaxation oscillators [3]. The period of oscillation for this clock is directly proportional to the charge and discharge time of C through R_1 and R_2 respectively. Given that capacitor voltage is exponentially related to time in this configuration, the name *Exponential Type* is appropriate.

4.3.2 Linear Relaxation Oscillator

The clock circuit that students build is more reminiscent of an oscillator that might actually be found in a production IC [3]. A schematic of this linear type relaxation

oscillator is shown below in Fig. 4-8. The primary difference between the two oscillators presented is the method by which the timing capacitor is charged. In the exponential type, charge time is determined by the time constant of the system. In the linear type, a known, constant value of current is sourced into or sunk out of the capacitor C_1. Given the constitutive voltage to current relationship of a capacitor, the time it takes to charge from one voltage to another is given by

$$\Delta t = C_1 \frac{\Delta V_{C1}}{I_{chrg}} \tag{4.16}$$

where ΔV_{C1} is the magnitude of voltage change across the capacitor and I_{chrg} is the current flowing through the capacitor. This method of timing is preferred on an IC for multiple reasons. First, the charge and discharge times are only subject to variations in the value of C_1, rather than to variations in both R_1/R_2 and C. Additionally, the linear type circuit requires the use of fewer resistors, which is advantageous from a total die area perspective. Note that both timers in the SR controller of Chapter 3 are implemented with linear charging circuitry.

Given the multitude of functional sub-modules contained within the circuit of Fig. 4-8, the benefit of using this topology for educational purposes is clearly evident. First, students learn about high speed comparator design by examining the NPN differential input comparator at the heart of the timer. This circuit is formed by the following transistors: Q_{14}, Q_{15}, Q_{20}, Q_{21}, Q_{24}, Q_{25}, Q_{26}, and Q_{27}. Concepts such as folding legs, current steering, and bipolar saturation are all encompassed by the design of this block. Additionally, the use of output inverters to increase the switching speed and boost the current driving capability of the clock must be considered.

Second, the circuits that form the charge and discharge currents for C_1 add insight into the design of non-standard current sources. Specifically, Q_4, Q_5, Q_6, and Q_7 form two voltage controlled current sources. Here, the voltage on the base of Q_4 and Q_6 controls the collector current of Q_5 and Q_7 respectively. Noting that I_{C5} is mirrored

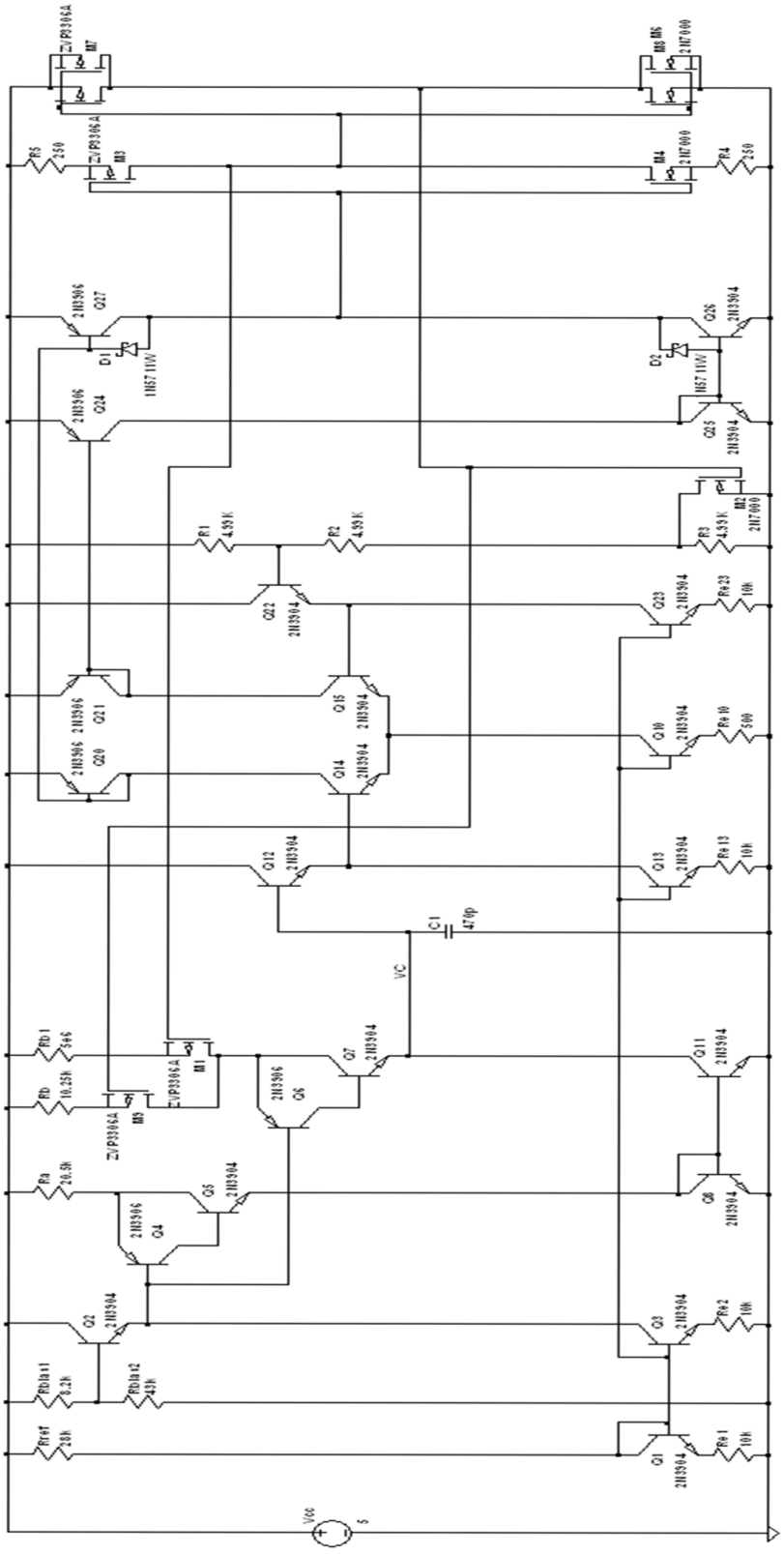

Figure 4-8: Linear Type Relaxation Oscillator Schematic

into Q_{11}, the charge current for capacitor C_1 is given by

$$I_{chrg} = I_{C7} - I_{C5} \tag{4.17}$$

Thus, by modulating the value of I_{C7} every half oscillation period, C_1 either charges up to the turn-off threshold, or down to the turn-on threshold.

To understand the exact switching behavior of this circuit, students must realize that the clock output determines the state of the system. If the output is high, I_{C7} equals zero, C_1 is discharging, and the turn-off threshold of the timing comparator can be expressed as

$$V_{th,off} = \frac{R_2}{R_1 + R_2} 5 \tag{4.18}$$

When $V_{C1} = V_{th,off}$, the clock output goes low and I_{C7} is allowed to flow. If $I_{C7} > I_{C5}$, I_{chrg} is a positive quantity, and C_1 begins to charge toward the turn-on threshold of the timing comparator, given by

$$V_{th,on} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} 5 \tag{4.19}$$

Thus, the total period length for one oscillation of this circuit can be written as

$$T = 2C_1 \frac{V_{th,on} - V_{th,off}}{I_{C5}} \tag{4.20}$$

where the assumption that $I_{C7} = 2I_{C5}$ has been made.

Simulated results for this linear oscillator circuit with *stock* component values are shown in Figs. 4-9 and 4-10 below. The designed switching frequency of the system is 50 KHz with a duty cycle of .5.

In Fig. 4-9, V_{clock} refers to the output voltage of the oscillator, V_{C1} refers to the voltage across C_1, and V_{th} refers to the voltage on the inverting terminal of the timing comparator, which is effectively the hysteretic switching threshold. As can be seen, V_{C1} looks like a triangle wave, hence the name *linear* relaxation oscillator [3]. In Fig. 4-10, the rise time of clock pulse is shown, and is roughly equal to 45 ns.

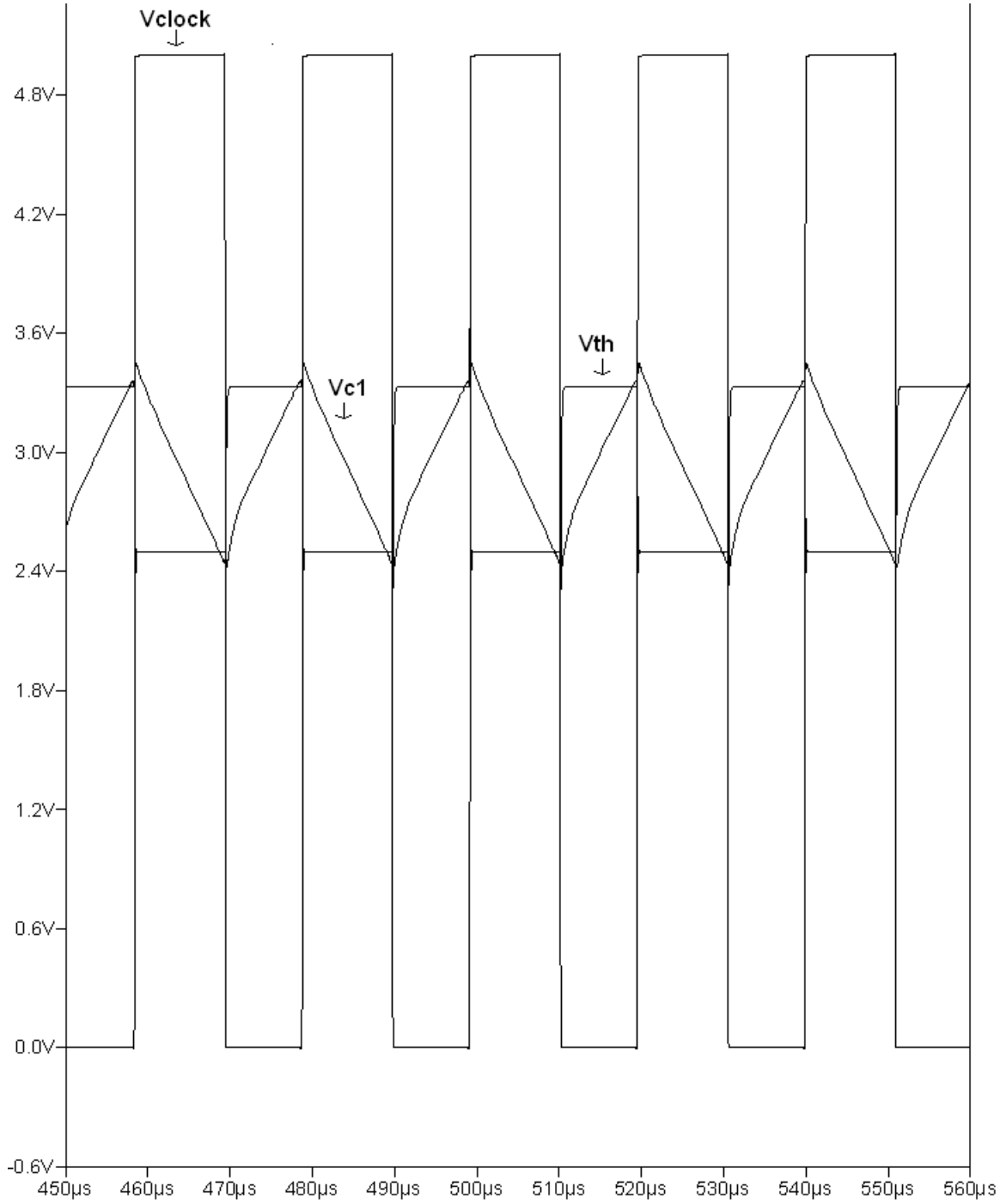

Figure 4-9: Simulated Clock Pulse Waveforms for the Linear Relaxation Oscillator $f_{clck} = 50KHz$

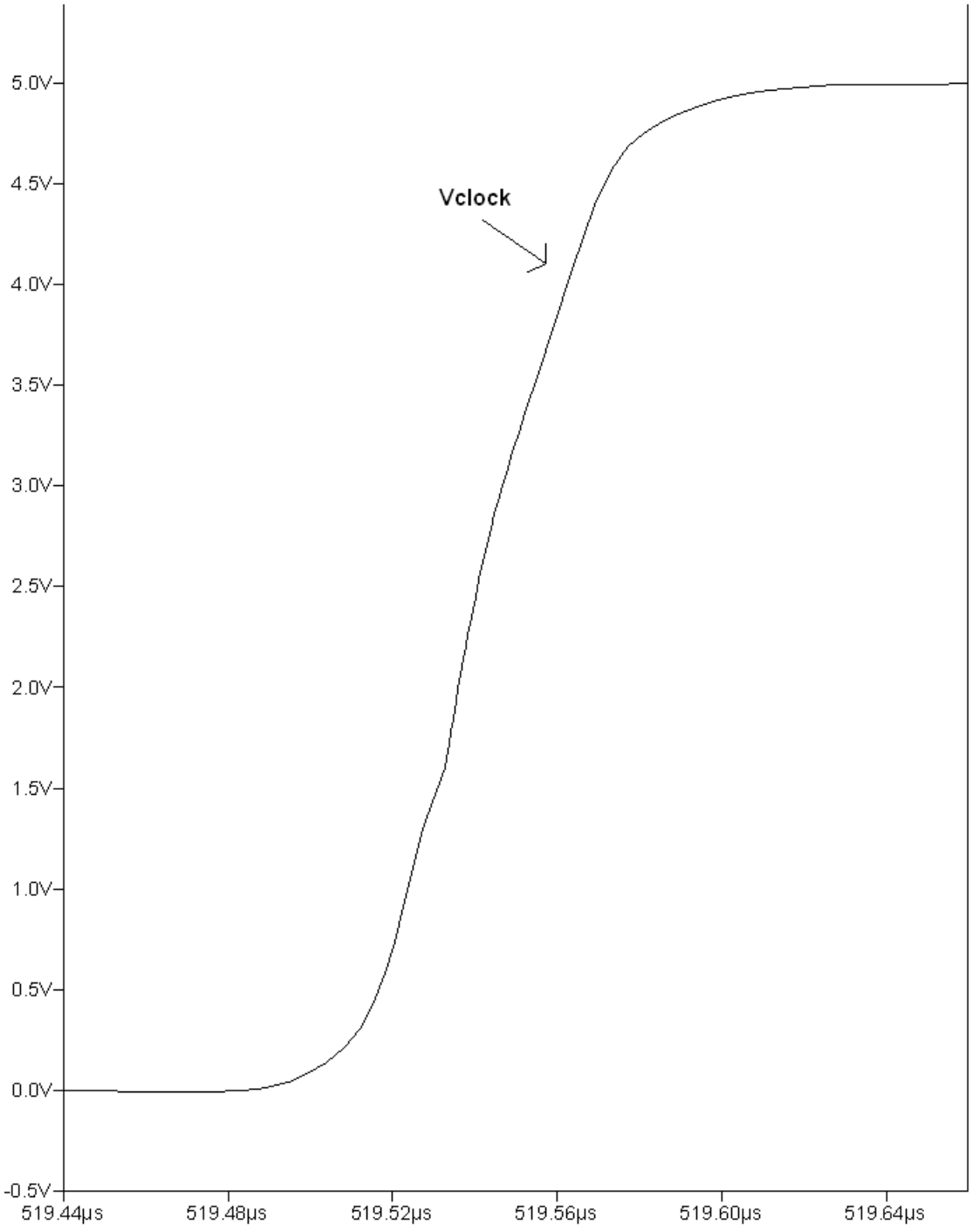

Figure 4-10: Simulated Clock Pulse Rise Time

2N3904	**2N3906**
Q_1 Q_2 Q_3 Q_4 Q_5 Q_7 Q_8 Q_{10} Q_{11} Q_{12} Q_{13} Q_{14} Q_{15} Q_{22} Q_{23} Q_{25} Q_{26}	Q_4 Q_6 Q_{20} Q_{21} Q_{24} Q_{27}
2N700	**ZVP3306A**
M_2 M_4 M_6 M_8	M_1 M_3 M_5 M_7 M_9
1N5711	**Passives**
D_1 D_2	Remaining components

Table 4.3: Bill of Materials for Clock Module

The bill of materials for the actual discrete clock module can be found in Table 4.3.

Corresponding homework problems for this laboratory module are as follows:

1. *Which transistors function as the timing comparator in this oscillator? Where is the high gain node?* By this point in the course, students will have been introduced to basic comparator design concepts, thus, recognizing a familiar structure should be relatively simple. The difficulty in this question comes from identifying the function of the folding legs and being able to trace the signal path from input to output.

2. *Why are the two output inverter stages necessary?* This question is intended to make students think about capacitive loading effects on nodes that are critical to speed. Specifically, every other circuit that the clock is connected too adds extra capacitance to the output node. Without a high current inverter driving these parasitics, the clock would not function in any reasonable frequency range.

3. *Consider Fig. 4-10. How would the rise time of the clock pulse be affected if D_1 and D_2 were removed?* Given the importance of fast circuit response, this question aims to exemplify the detrimental effect bipolar saturation has on comparator slew time and the accuracy of the clock frequency. Students can simulate the circuit without the clamp diodes and observe the effects they predict.

4. *How is hysteresis implemented in this circuit?* Understanding the method of hysteresis used in this oscillator is key to grasping the operation of the circuit as a whole.

5. *Why is I_{C7} never really allowed to go to zero?* This question reveals some of the design subtleties of using Darlington-like configurations. Specifically, the turn-on characteristics of such composite devices are terribly slow. When no current flows through either transistor, the node that connects the base of the output device to the collector/emitter of the input device has an enormous incremental impedance [3]. Thus, the charge time of the parasitic capacitance on this node is undesirably long, and any quantity that depends on current flow through the composite device is limited by this interval. The harmful effects of removing R_{b1} and M_1 in Fig. 4-8 can be seen in simulation.

4.4 Feedback Circuitry Board

At the core of every power controller is the feedback circuitry necessary to enable output voltage regulation in a given converter system. In most control implementations, two feedback loops exits: an outer voltage sense loop and a minor current sense loop [6]. This section begins with a discussion of the voltage sense circuitry.

4.4.1 Error Amplifier

A schematic of the error voltage amplifier that students design is shown in Fig. 4-11. This circuit serves dual purpose as the summing junction for the controller reference and feedback voltage, and as the compensation network for the outer feedback loop [11]. As derived in [6], proportional and integrative (PI) compensation is optimal for this type of power controller. This is achieved with a network of resistors and capacitors connected from the base of Q_5 to ground.

To understand the operation of this circuit, students are asked to consider the function of the actively loaded differential pair Q_3 and Q_4. These devices produce a

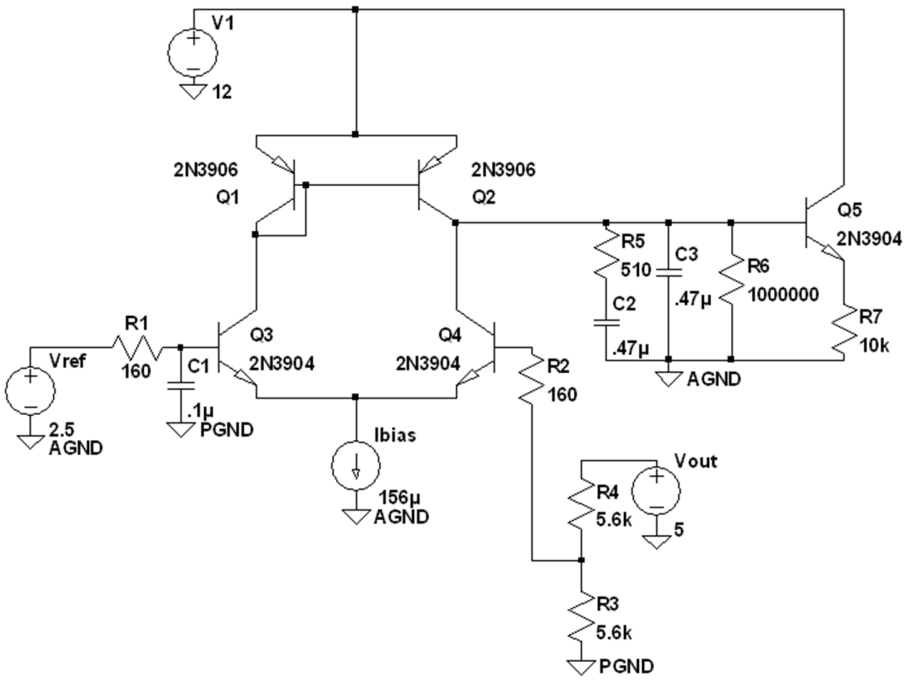

Figure 4-11: Error Amplifier Schematic

current that is proportional to the difference between the converter reference and the feedback voltage, otherwise know as the error [6]. This current is given by

$$i_{err} = g_m v_{err} \tag{4.21}$$

where g_m is the transconductance of one of the input transistors and v_{err} is the error voltage as defined above. i_{err} flows through a net impedance connected to the base of Q_5 to create a desired compensation transfer function. As derived in [11], the transfer function from v_{err} to v_{out} for the error amplifier as shown in Fig. 4-11 is

$$\frac{v_{out}}{v_{err}}(s) = \frac{R_5 C_2 s + 1}{s(R_5(C_2||C_3)s + 1)} \frac{g_m}{C_2 + C_3} \tag{4.22}$$

where v_{out} is measured from the emitter of Q_5 to ground (note that lowercase letters are used to represent incremental voltages and currents). Not only does this transfer function implement PI compensation, but it also contains an extra pole and zero

2N3904	**2N3906**
Q_3 Q_4 Q_5	Q_1 Q_2
Passives	**Notes**
Remaining components	2.5 V Ref and I_{bias} not included

Table 4.4: Bill of Materials for Error Amplifier Module

for lead compensation. This encourages students to experiment with the location of their frequency domain system dynamics and observe the effect lead compensation can have on bandwidth and stability.

A simulated bode plot for this error amplifier is shown in Fig. 4-12. As evident, the crossover frequency for this system is 270 Hz, while the phase margin is 80°. The observed bump in phase characteristic is due to placement of the lead compensation zero roughly at crossover.

The bill of materials for the actual discrete error amplifier module can be found in Table 4.4.

Corresponding homework problems for this laboratory module are as follows:

1. *Explain how this circuit block fits into the overall operation of the power controller.* While a relatively basic concept, it is important that students understand the system level functions of each circuit they design.

2. *Derive the two port model for this amplifier using small signal characteristics.* Students should be able to use what they have learned about incremental circuit models and making appropriate simplifications to derive the two port model for this amplifier.

3. *Using the model you just derived, find the transfer function from v_{err} to v_{out} and sketch a corresponding bode plot.* Note that an engineer's ability to find transfer functions and work comfortably in the frequency domain is an enormous advantage when analyzing modern, high speed systems. Thus, this course hopes to foster in students an intuition for frequency domain dynamics and design.

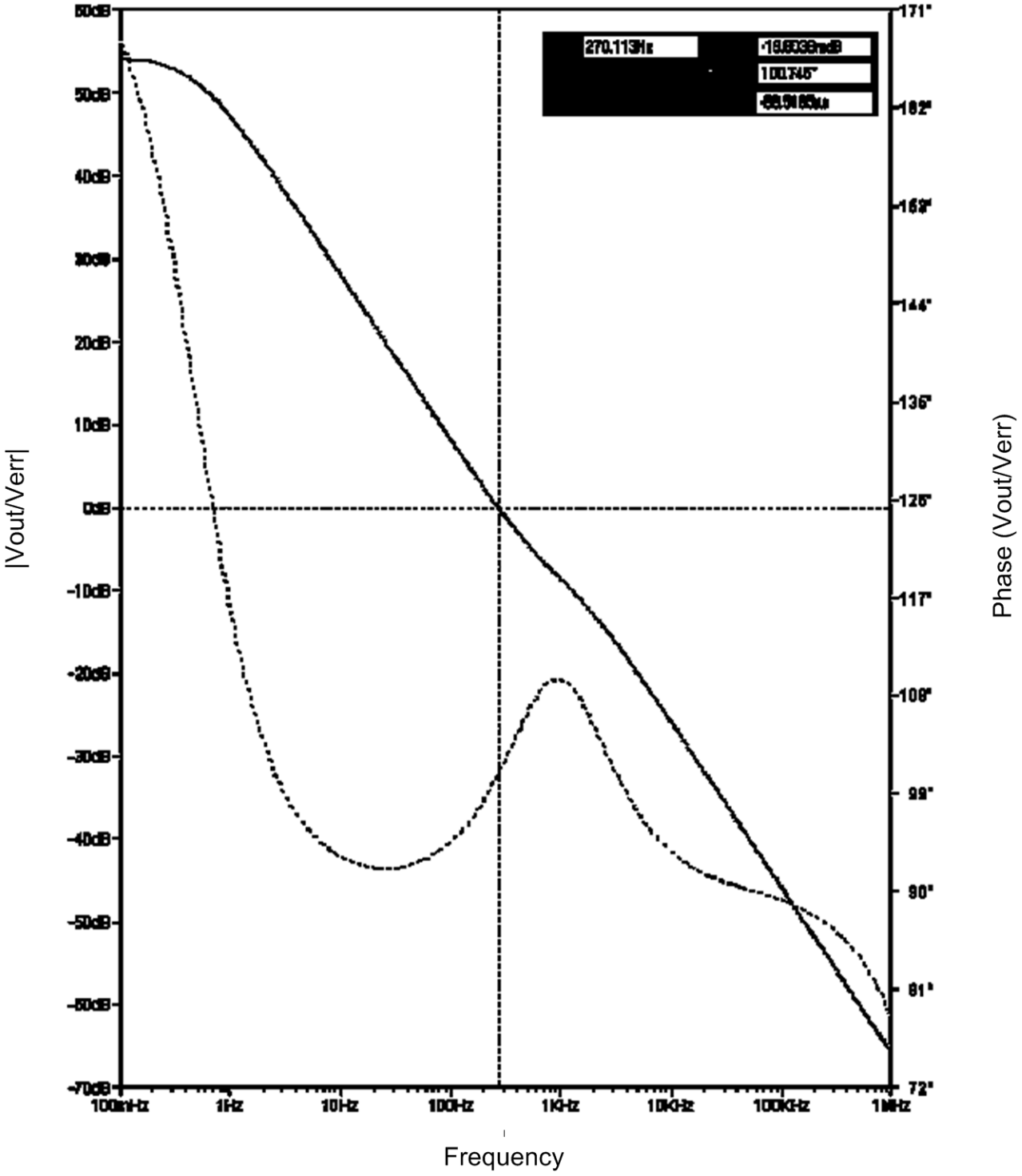

Figure 4-12: Simulated Error Amplifier Bode Plot

4. *Using SPICE, simulate the open-loop error amplifier and generate a plot of the magnitude and phase of* $\frac{v_{out}}{v_{err}}(s)$. *Does this plot agree with your sketch?* This question allows students to compare their expected and simulated results. As always, if the two disagree, design revisions are necessary.

5. *Considering the external system with which this amplifier interacts, why is the bandwidth so low?* Hopefully, students will realize that the outer voltage loop is meant to be quite slow. A fundamental design constraint of hard-switched power converters is that the output voltage remain relatively constant over a switching cycle. Thus, the response time of the converter output is orders of magnitude slower than the switching period [6].

6. *How is lead compensation used to assure closed loop stability?* This question attempts to illuminate slightly more advanced topics in stability and control. Specifically, the use of a pole zero pair to boost the phase at crossover while leaving low frequency dynamics unaffected.

4.4.2 Current Sense Amplifier

In order to implement a peak current mode minor control loop, the converter must have a signal that is proportional to the current flowing through the power stage inductor. A small resistor is placed in series with the high side MOSFET switch such that the voltage across the resistor is proportional to the inductor current when the switch is on. Given that the magnitude of the sense voltage will be small, an amplifier is necessary to gain up the signal.

A schematic of the transconductance amplifier used for this purpose is shown below in Fig. 4-13. Much like the error amplifier above, a differential input voltage generates a current at the output node of the amplifier that is given by

$$i_o = g_m v_{id} \tag{4.23}$$

where v_{id} is the magnitude of differential input voltage. Noting that i_o must flow

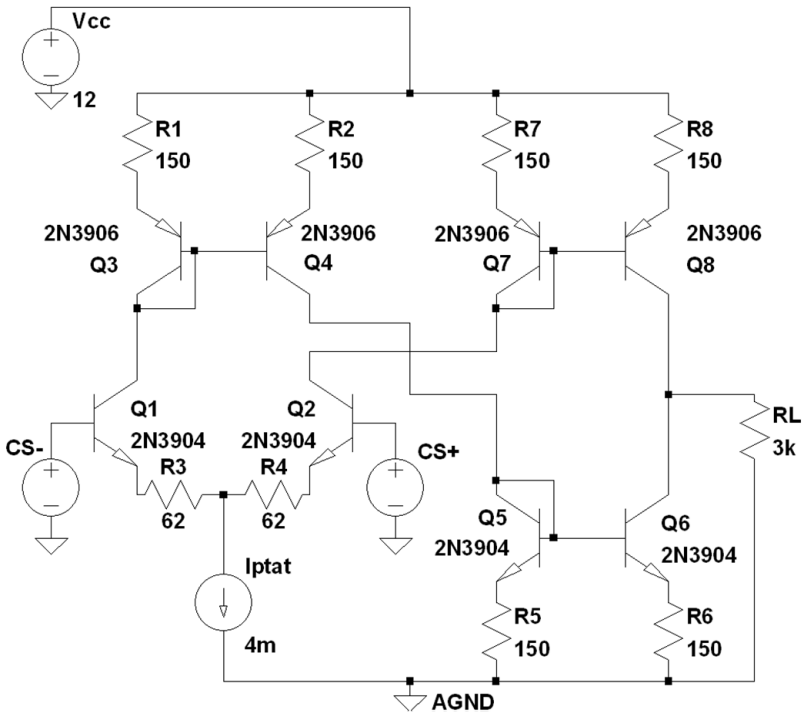

Figure 4-13: Current Sense Amplifier Schematic

through the connected load resistance, the voltage gain from input to output can be expressed as

$$A_v = g_m R_L \tag{4.24}$$

Simulation data for the circuit in Fig. 4-13 is shown in Fig. 4-14. Here, the input to the current sense amplifier is the signal V_{curr}, which represents the voltage across the high-side series resistor when the converter is operating in continuous conduction mode. Note that the switching frequency is 50 KHz, and the rise time of the current waveform is 100 ns. Even with such a fast rise time, the output of the amplifier accurately tracks the input. By investigating the function of this circuit block further, students should be able to clearly see the transient benefits of using an open-loop transconductance amplifier in such applications.

The bill of materials for the actual current sense amplifier module can be found in Table 4.5.

A few corresponding homework problems for this laboratory module are discussed

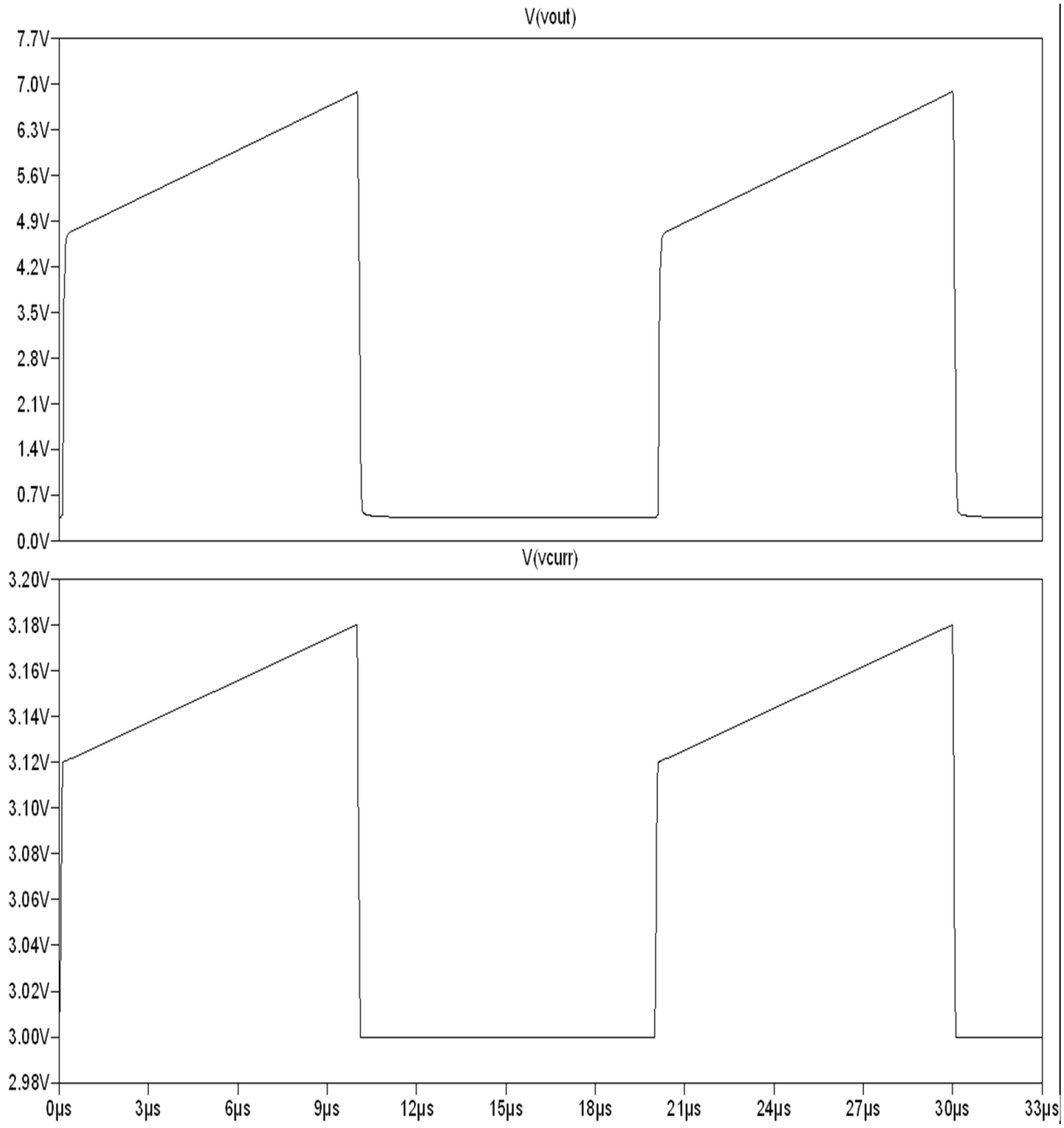

Figure 4-14: Simulated Current Sense Amplifier Response During CCM Operation, 50 KHz Swithing

2N3904	**2N3906**
Q_1 Q_2 Q_5 Q_6	Q_3 Q_4 Q_7 Q_8
Passives	**Notes**
Remaining components	I_{ptat} not included

Table 4.5: Bill of Materials for Current Sense Amplifier

below:

1. *Given that $g_m = \frac{I_C}{V_T}$, why is it necessary for the tail current source in Fig. 4-13 to be proportional to absolute temperature (PTAT)?* Continuing with the theme of industrial IC design techniques, a product must function over an extremely wide temperature range in order to be viable in the marketplace. This question intends to have students think about the temperature performance of this amplifier, with the hope they will realize that the gain is inversely proportional to temperature. As temperature rises, g_m falls. Thus, a bias current source that tends to increase I_C as temperature rises should cancel out the dependence of amplifier gain on operating temperature.

2. *What is the function of degeneration resistors R_3 and R_4? How are they sized?* As derived in [11], these resistors significantly increase the linear operating range of the current sense transconductance amplifier. Students should calculate the maximum differential input voltage expected on the inputs of the amplifier, and then use appropriate simplifications to calculate the values of R_3 and R_4 that yield enough linear amplification range.

3. *Draw a block diagram of the complete system regulation loop.* This question allows students to connect the feedback circuitry they have been studying to more theoretical control concepts, such as minor loop feedback and overall system dynamics.

4.5 Gate Drive Board

In order to translate internal converter logic into high power drive signals, capable of quickly turning on and off large external MOSFETs, specialized gate drive circuitry is necessary. In this course, students will learn about the difficulties associated with designing good gate drivers, especially for high side switches. A schematic of the discrete high side driver circuit used in this course is shown in Fig. 4-15. Here, a

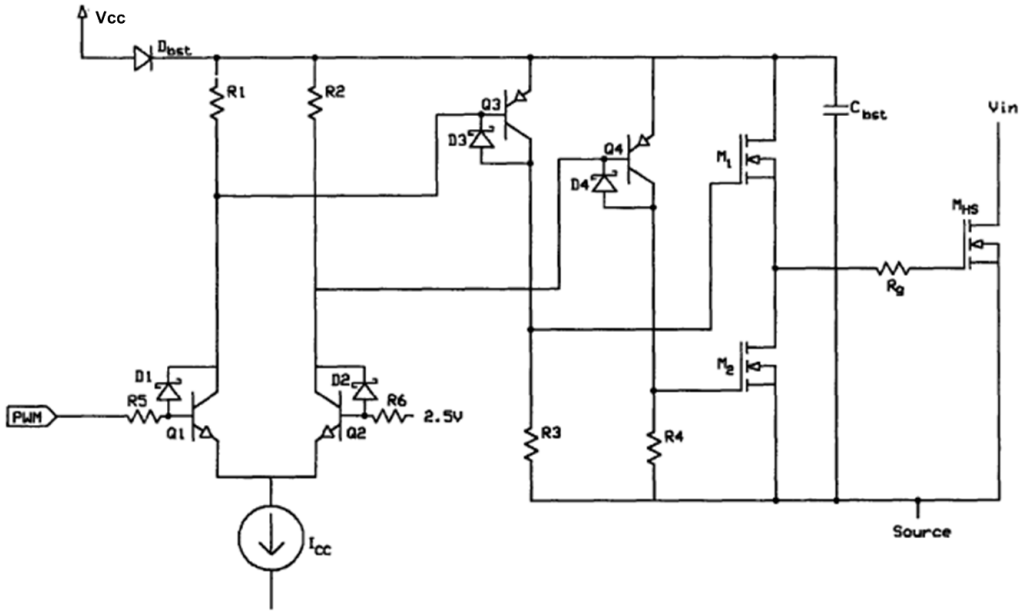

Figure 4-15: High Side Gate Drive Circuitry

high signal on the base of Q_1 strongly forward biases the emitter-base junction of Q_3. This pulls the gate of M_1 high, and the charge stored in ballast capacitor C_{bst} is transferred to the gate of high side switch M_{HS}. It is important to note that while the source of M_{HS} is technically floating while both low and high side switches are off, the voltage across C_{bst} was previously charged to V_{CC} during the low side conduction cycle. Thus, when M_1 turns on, C_{bst} is effectively strapped from gate to source of M_{HS}. Regardless of where the source voltage has floated, C_{bst} forces the gate-source voltage of M_{HS} to be equal to V_{CC}, and thereby turns on the high side switch.

A full schematic intended for student simulation of this module is shown below

in Fig. 4-16. Both low and high side gate drivers are visible, along with extra control logic for shoot through protection and under voltage lock out sensing. Note

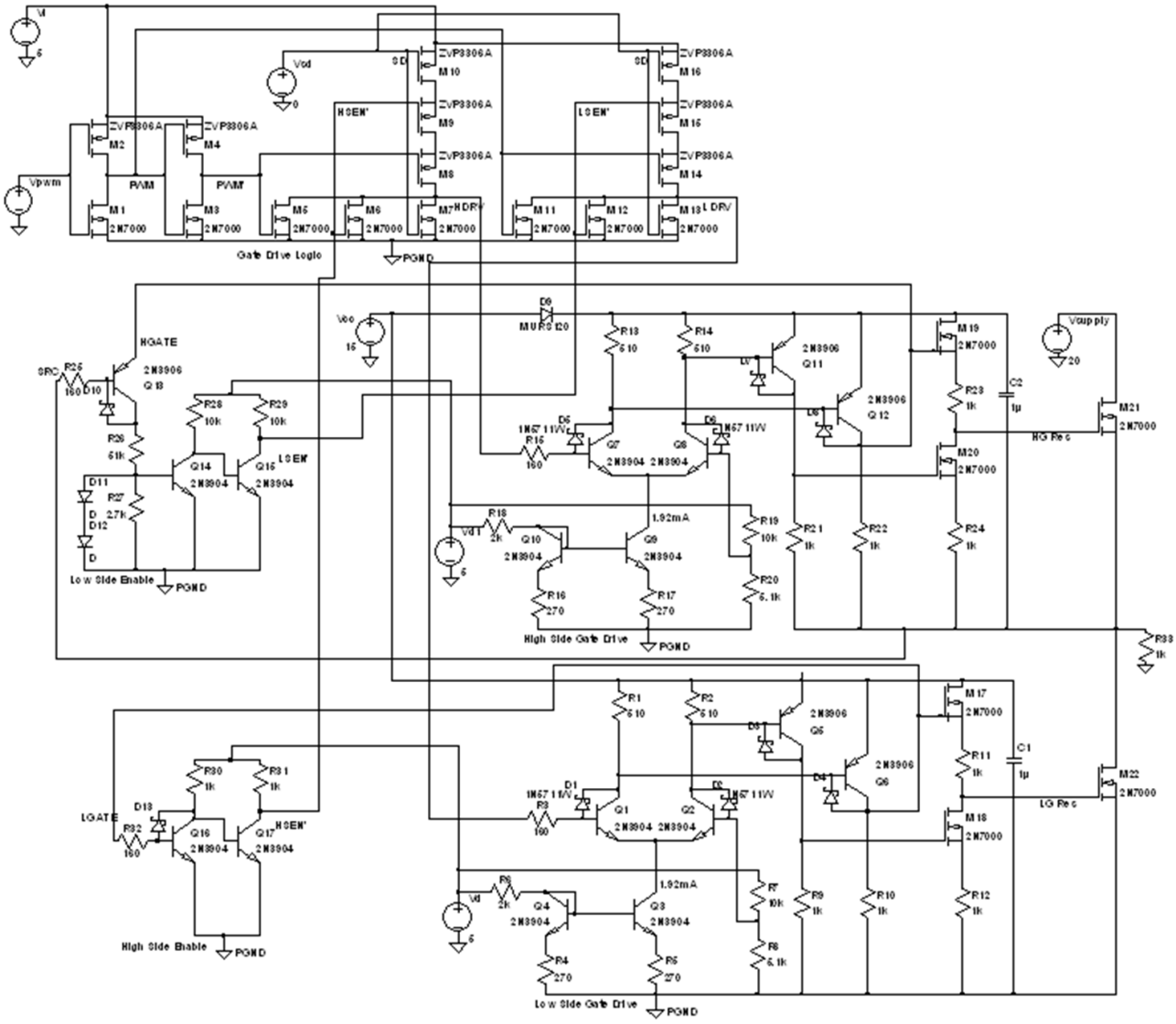

Figure 4-16: Discrete Gate Drive Board Schematic

the inclusion of schottky diodes from base to collector on almost every bipolar device. This is intended to prevent the detrimental effects of saturation on gate drive response time.

Simulated waveforms for this gate driver are presented in Fig. 4-17. As can be seen, the input to the circuit is a logic level PWM signal, while the outputs (*High*

2N3904 Q_1 Q_2 Q_3 Q_4 Q_7 Q_8 Q_9 Q_{10} Q_{14} Q_{15} Q_{16} Q_{17}	**2N3906** Q_5 Q_6 Q_{11} Q_{12} Q_{13}
2N700 M_1 M_3 M_5 M_6 M_7 M_{11} M_{12} M_{13} M_{17} M_{18} M_{19} M_{20}	**ZVP3306A** M_2 M_4 M_8 M_9 M_{10} M_{14} M_{15} M_{16}
1N4148 D_{11} D_{12}	**1N5711** D_1 D_2 D_3 D_4 D_5 D_6 D_7 D_8 D_{10} D_{13}
MUR120 D_9	**Passives** Remaining components

Table 4.6: Bill of Materials for Gate Drive Module

and *Low*) are higher voltage signals capable of turning on and off power MOSFETs. Note that shoot-through is prevented by ensuring that *High* and *Low* are never on at the same time.

Using this topological framework, students should gain a unique appreciation for the complexity of modern gate drivers and the difficulty of attaining fast transient responses in such circuits. Exposure to fundamental concepts is the primary goal of this module, as creative gate drive intuition can take years of experience to develop [3].

The bill of materials for the actual discrete gate driver module can be found in Table 4.6.

4.6 Summary

This chapter has developed the simulation and written exercise framework necessary to allow students in a potential class on power electronic control circuitry to verify their design choices and cement their understanding of course material. While fundamentally based in discrete circuit design, this course is intended to mimic the process an industrial IC designer would go through in creating and fabricating a functional product. Every circuit that students learn about and build is framed in the context of its integrated counterpart, and all supporting coursework is intended to illuminate

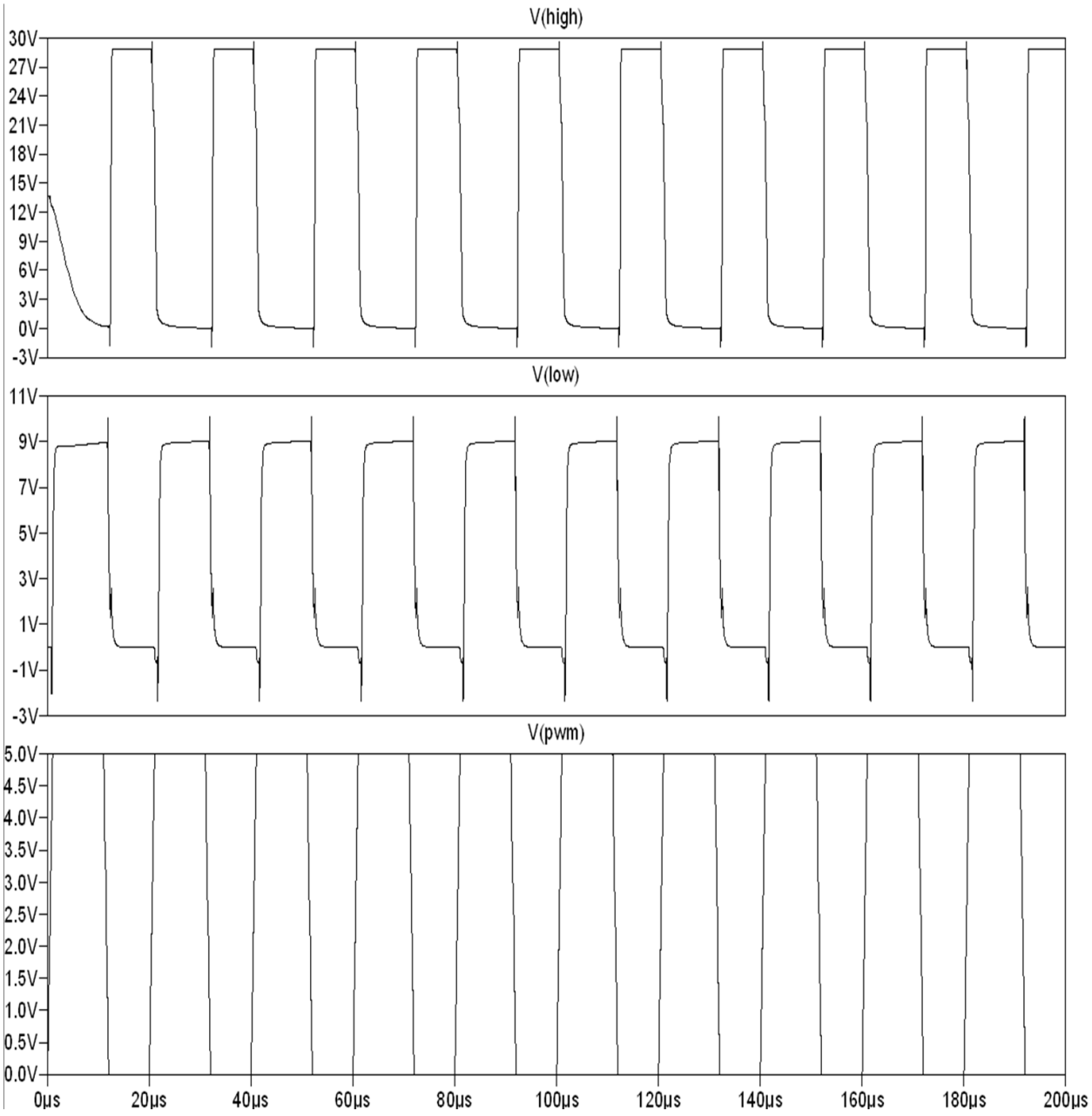

Figure 4-17: Simulated Gate Drive Operational Waveforms, 50 KHz Switching

important concepts that transcend distinctions between the two design methodologies. Thus, a student having actively participated in this course should be well suited to tackle the intricate challenges of industrial IC design.

Chapter 5

Conclusion

This thesis investigated integrated circuit design methodologies as they apply to the industrial and educational realms. First, using a proprietary Texas Instruments mixed signal silicon process, an integrated secondary side synchronous rectification controller was designed. This chip is meant for use in the LLC resonant converter topology, and conforms to the extremely high reliability and functional standards demanded of an industrial product. A vast range of possible operating conditions, as well as stringent speed and response time requirements, introduced unique and exciting challenges into the IC design process that needed to be carefully overcome. The resulting top level performance of the controller greatly exceeded all target specifications, and the chip itself will be fabricated and sold under the name UCC24600.

Many of the intricacies involved in industrial power IC design, and illustrated by the circuitry in the UCC24600, are glossed over in a normal electrical engineering curriculum due to time and resource constraints. Process variation, temperature dependence, and many other important real world issues are idealized in most academic treatment of the circuit design process. Thus, the second part of thesis developed a simulation and written exercise framework, intended to couple with a discrete hardware kit, that allows for the creation of a laboratory course in power electronic integrated circuit design. Students in such a course will design a complete power electronic control circuit, made of discrete circuit modules that mimic the function of common IC blocks. Each module will be framed in the context of its

real IC implementation, and important differences will be discussed. Relevant theory in control, analog circuitry, and power supply operation will be presented to students as well. The work demonstrated in this thesis guides students towards understanding each circuit module and being able to calculate custom component values to yield desired performance. A simulation environment has also been created where students can verify their design choices and make appropriate modifications. This process is meant to mirror that of common industrial practice.

By exploring IC design in both the academic and industrial worlds, this thesis has effectively bridged the gap between the two. Working on a real industrial product enabled the identification of important challenges not discussed in the classroom, and made it possible to develop an educational framework for teaching students how to overcome these issues. This work can, and should be expanded to ensure future graduating analog IC design students have the skills and knowledge to make an immediate difference in industry and beyond.

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