The LHC Beam Loss Monitoring System's Surface Building Installation.

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Abstract

The strategy for machine protection and quench prevention of the Large Hadron Collider (LHC) at the European Organisation for Nuclear Research (CERN) is mainly based on the Beam Loss Monitoring (BLM) system.

At each turn, there will be several thousands of data to record and process in order to decide if the beams should be permitted to continue circulating or their safe extraction is necessary.

The BLM system can be sub-divided geographically to the tunnel and the surface building installations. In this paper the surface installation is explored, focusing not only to the parts used for the processing of the BLM data and the generation of the beam abort triggers, but also to the interconnections made with various other systems in order to provide the needed functionality.

I. Introduction

The strategy for machine protection and quench prevention of the Large Hadron Collider (LHC) at the European Organisation for Nuclear Research (CERN) is presently based on the Beam Loss Monitoring (BLM) system. At each turn, there will be several thousands of data to record and process in order to decide if the beams should be permitted to continue circulating or their safe extraction is necessary.

The BLM system can be easily sub-divided geographically to the tunnel and the surface building installations. The tunnel installation consists of around 4000 detectors, placed at various locations around the ring, tunnel electronics, which are responsible for acquiring, digitising, and transmitting the data. More details can be found in [1]. In the surface installation, electronics receive the data via 2km redundant optical data links, process, analyze, store, and issue warning and abort triggers. The later provide also the connections to the Beam Interlock, the Beam Energy Tracking, the Collimation, the Logging and the Post Mortem systems (see Figure 2). In this paper, the surface building's electronics are explored providing details for the different parts combined to provide the needed functionality.

II. BLM Surface Electronics

The installation at the surface foresees VME crates spread over all of the eight LHC interaction points accommodating the processing modules, a timing card, a CPU card and a Combiner card (see Figure 1). The data acquired at the tunnel installation arrive digitized over redundant gigabit optical links.

A. VME Crate

For the BLM system, 25 VME crates will be used in total, three at each point except LHC's point 7 that will have an extra crate facilitating mainly the detectors observing the Collimation system.

All of them are making use of the extended VME64 [2] specification. This extension defines a set of features that can be added to VME and VME64 boards, backplanes and sub-racks. Some of the features included are a 160-pin connector, a P0 connector, and geographical addressing.

In order to make the best out of those features, CERN's Beam Instrumentation group has defined a custom-made backplane for the P0 connector [3]. Some of the features it provides include connections to create two daisy-chain links for the processing modules, general purpose I/Os, and additional supply voltage outputs.

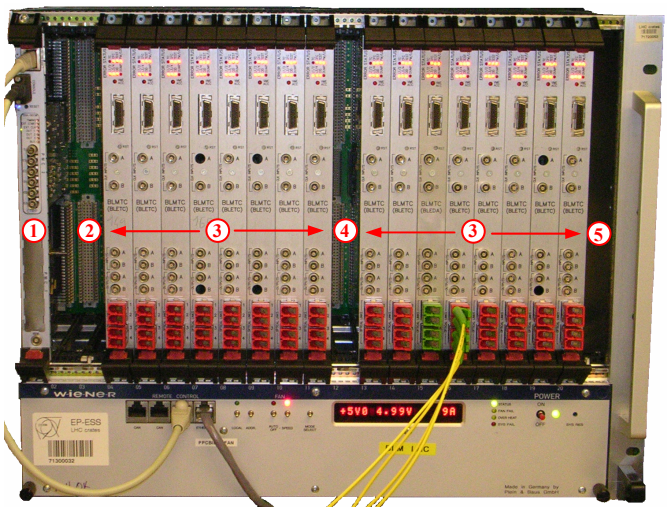

Figure 1: VME Crate's arrangement for the BLM system:
1. Crate's CPU, 2. Timing card (CTRV), 3. Processing modules (BLETC), 4. Timing card (BOBR), 5. Combiner card (BLECOM).

The VME crate, in the arrangement for the BLM system, can host, except the one CPU and two types of timing cards, 16 processing modules and one signal concentrator card (see Figure 1). Finally, its fan tray allows remote monitoring and control.

B. Processing Module (BLETC)

A VME card, named DAB64x [4] that provides the processing power, and a mezzanine card, named BLM Mezzanine [5] card that links the tunnel with this surface installation, comprise the BLETC processing module (see Figure 3). Its main task is to analyse the acquisition data, by

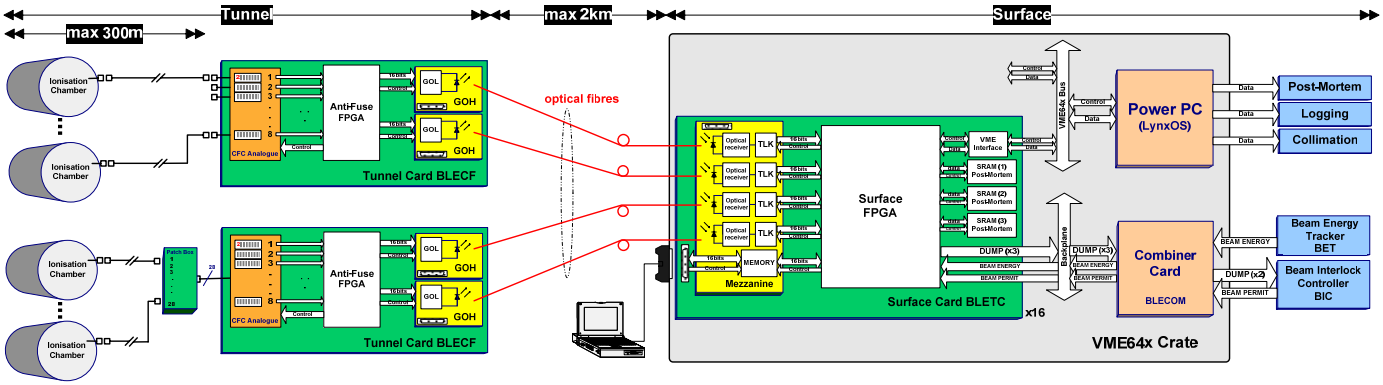

Figure 2: Overview of the LHC Beam Loss Monitoring System (including connections to other dependant systems).

keeping a history of those data and calculating various moving sum windows for each detector. It will decide whether a dump request should be initiated, by comparing those histories with predefined unique threshold values for each detector.

The BLM mezzanine card is hosting the receiver parts for four optical links. It handles the de-serialisation and decoding of the four optical gigabit data transmission lines in parallel and provides the received data to a reconfigurable field programmable gate array (FPGA) device [6], the backbone of the DAB64x card.

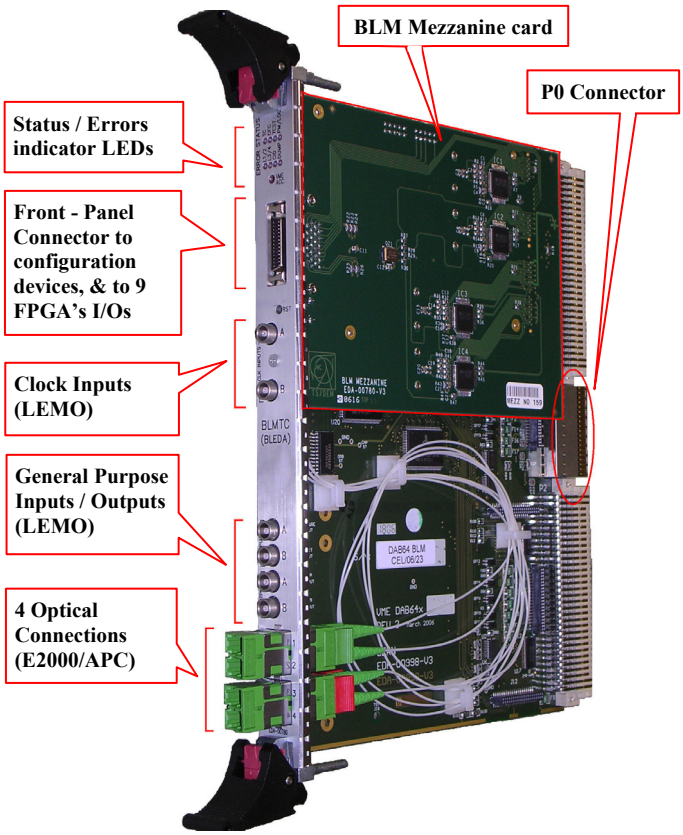

Figure 3: Processing module (BLETC)

Each module has been configured to process in real-time up to 16 detector channels. It will establish communication with the VME-bus and will be accessible through it, but at the same time, the module will be able to work autonomously for protection against main CPU failures.

The availability of all detectors, the acquisitions chain and the generation and communication of the beam abort signal needs to be verified for each channel before each injection into the LHC. The processing module checks first that the communication links are in an acceptable state and then that the statuses of the tunnel electronics (i.e. power supplies, high voltage supplies, acquisition state, etc) are also working.

C. *Timing Cards*

The timing card available on each crate is the BOBR [7] module. It is also a VME format card, designed to interface a VME crate with up to two different Timing, Trigger and Control (TTC) networks and has been developed by the Beam Instrumentation group. In this application it will provide the Time-Stamp and the Post Mortem triggers. Additionally, one of the Controls Timing Receiver (CTR) cards will be installed on each rack to provide to its VME crates the beam energy data distributed by the Safe LHC Parameters (SLP) system [8]. The initial recipient of the CTR's data is the adjustment Combiner card and from there they are re-distributed to the rest of the Combiner cards of the rack.

D. *Crate CPU*

The CPU is a PowerPC with LynxOS as operating system. Its main purpose is to access periodically the processed data from each processing module, to normalise them with their corresponding threshold values and to provide them for the Logging system before they are displayed on the fixed displays in the control room. Moreover, it will collect and time-stamp the Post Mortem and the Collimation data, stored on the circular buffers, whenever the relevant triggers arrive.

Data will be sent over the VME-bus for on-line viewing and storage by the Logging and Post-Mortem systems. The BLM system will drive an online event display and write extensive online logging (at a rate of 1 Hz) and post-mortem data (the acquired data from the last 20,000 turns plus averages of the same data of up to the last 40 minutes) to a database for offline analysis.

At the same time, the CPU will calculate and issue the Warning triggers before transmitting them to the Logging system. The Warning level will correspond to a fraction of the

Threshold value at that moment, provisionally decided to be 30%. The BLETC module will provide to the CPU the calculated Running Sums together with their corresponding threshold values through the Logging process to simplify this process.

E. Combiner card

The final receiver of the two beam permit lines, one for the Maskable and another for the Un-Maskable channels, is the Combiner card, located at the last slot of the crate. The two beam permit lines are daisy chained through each of the processing modules using a custom-made backplane in the crates. If any of the modules decides to break any of these lines a beam dump request will be given to the LHC Beam Interlock System (BIS) [9]. As an additional use, those lines will be used by the Combiner card to provide a continuous supervision of the operation of the cards in the crate. Thus, it will be able to discover immediately a disconnection from the circuit or a module failure and a dump will be requested for any of those cases.

The Combiner card is also responsible of distributing the beam energy to each of the processing modules in the crates, as well as, initiating all the test procedures and checking the results when there is not a circulating beam in the accelerator.

III. Data Processing Overview

The real-time processing of the acquired data is assigned to the FPGA accommodated in the processing module. Figure 4 illustrates an overview of the main processes involved.

The "Receive, Check and Compare" (RCC) process will receive, de-serialise and decode the transmitted packets. It will check for errors on both transmissions (primary and redundant) and compare the packets in order to select one error-free packet. Its additional tasks will be to check the status of the tunnel installation by checking the status information received at each packet. It will collect and report the errors seen. Actually, it will provide a significant part of the Status and Error Logging information by collecting the errors seen from the various checks that will be used by the expert applications to track potential problems.

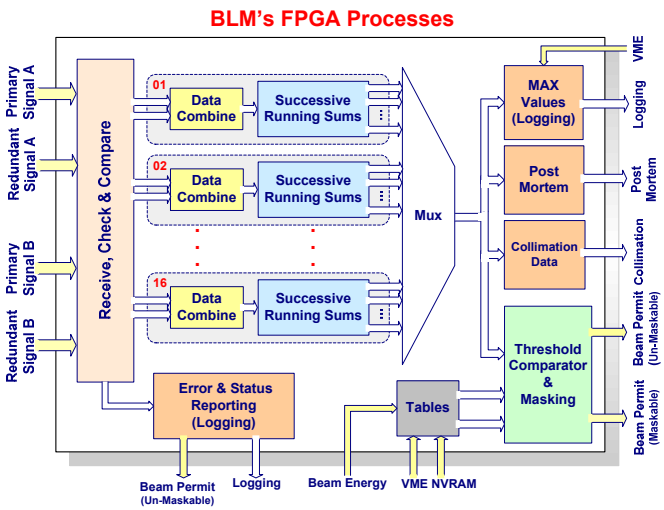

Figure 4: Overview of the Processes in the BLM's FPGA.

The "Data-Combine" process will receive from the packet the two types of data, the counter and the ADC data, coming from each detector and will make use of a merging algorithm to combine them into one value. At the same time, it will make an effort to filter noise passing through the ADC circuitry and normalise the output depending on its working range.

The combined values from each detector will be given, each time they become available, to the "Successive Running Sums" (SRS) process. This process produces and maintains a number of histories, in the form of moving sum windows, for each detector. More specifically, the procedure for the data processing, which was chosen to be followed, is based on the idea that a constantly updated moving window can be kept by adding to a register the incoming newest value and subtracting its oldest value. The number of values that are kept under the window, or differently, the difference in time between the newest and the oldest value used, defines the integration time it represents. Additionally the specific implementation (i.e. the SRS) is making use of the cascading of multiple moving windows to create longer integration periods in order to minimise the resources utilisation. The SRS will calculate and maintain continuously 12 running sums for each detector that span from 40 μs to 84 s. Table 1 shows the complete range covered by the SRS in the configuration for the LHC.

Table 1: Successive Running Sums Configuration.

The red coloured RSs (running sums) outputs, i.e. RS1, RS4, RS6, and RS7, represent their additional utilisation as inputs for the adjacent SRs (shift registers), i.e. SR2, SR3, SR4, and SR5.

Range		Refreshing		Shift Reg. Name	Signal Name
40 μs steps	ms	40 μs steps	ms		
1	0.04	1	0.04		RS0
2	0.08	1	0.04		RS1
8	0.32	1	0.04	SR1	RS2
16	0.64	1	0.04		RS3
64	2.56	2	0.08	SR2	RS4
256	10.24	2	0.08		RS5
2048	81.92	64	2.56	SR3	RS6
16384	655.36	64	2.56		RS7
32768	1310.72	2048	81.92	SR4	RS8
131072	5242.88	2048	81.92		RS9
524288	20971.52	32768	655.36	SR5	RS10
2097152	83886.08	32768	655.36		RS11

In the subsequent stage, those calculated sums are compared with their corresponding threshold limits in the "Threshold Comparator" (TC) process every time they become updated. If one or more of them are found to be higher, a dump request is signalled.

All dump requests are gathered initially by the "Masking" process, which serves the purpose of distinguishing between "Maskable", "Un-Maskable" and unused channels.

The information necessary for the operation of the TC and the Masking processes, that is, the threshold and the masking values, are stored in tables uniquely created for each card. The threshold values that will be provided to the TC process will depend on the beam energy, whose range (450 GeV to 7 TeV) was decided to be divided in 32 steps. Thus, on each processing module a unique table of 6,144 threshold values (or 32KB) and two 16 bit masking registers will be held on each card.

For supervision and logging purposes, two more processes have been added. The "Maximum Values" process, which calculates and keeps the maximum values 'seen' in a period of time by each moving sum window, and the "Error & Status Reporting" (ESR) process, which reports the errors found in the transmissions and the status of the tunnel electronics. The data accumulated by both of them are collected by the crate PowerPC and projected in the Control Room's displays.

Finally, for the correct alignment and setup of the collimators one more set of data is available. Those data, destined for the Collimation system, contain whenever requested the last 20.48 ms of acquired data in the form of 32 x 640 μs sums for each detector.

IV. Reliability and Availability Enhancement

The system has been designed with reliability and availability in mind. The BLM system must guarantee its correct operation and its fail-safety for the system to have a much higher probability of preventing superconductive magnet destruction caused by a beam loss. For those reasons, the processing modules can operate independently of CPU and Timing card failures. There is redundancy in the optical transmission with additional powerful error detection and the connection to the Beam Interlock System (BIS) is tripled.

More specifically, to ensure a reliable communication link, a double, that is, a redundant optical link has been utilised as a first measure. The error free reception of the packet will be ensured using the CRC-32 error check algorithm [10] and augmented by the 8b/10b encoding scheme [11]. By including those digital techniques, a more sophisticated receiver part was produced that is expected to achieve even higher data reliability and system availability. More specific, the CRC is able to discover any error with a length less than the length of CRC and for longer bursts (i.e. 32 bit) the probability of undetected error is small enough (non-detection probability $Pr = 1.16415*10^{-10}$). The 32-bit checksum of the CRC will be additionally used for comparison of the redundant packets. The 8b/10b encoding will provide not only the clock data recovery (CDR) and a DC-balanced serial stream, but also additional error detection capability.

The unique Threshold and Masking tables for each of the monitors can thoroughly be prepared and checked before they are uploaded. They can be quickly and easily upgraded for specific systems when the levels need to be changed and additionally be used as a calibration and offset tool. Their small size allows them to be kept internally by the FPGA device in its available embedded memory blocks, which will decrease the access time and increase the implementation simplicity, if compared to an external memory device.

Extra information embedded in the packet will allow continuous self-checking of the system from problems resulting from user errors or aging. For example, to avoid misplacement of the Threshold or Masking table, the Card ID transmitted on each packet will be used. Each tunnel card holds a unique 16-bit number that will be compared with the one loaded together with the tables.

Similarly, to avoid loss of data, the Frame ID, a 16-bit number that will increment at every transmission, will be also included on each transmitted packet. The Surface FPGA will be able in that way to compare consecutive transmissions and check for missing frames.

Finally, to ensure the correct recognition of system failures and dump requests the surface card's outputs, carrying the beam dump information, will use a frequency signal. At a dump request, reset, failure, or even card disconnection the transmitted frequency will be inevitably altered, thus, always triggering the beam abort.

V. Acknowledgements

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