XII. PROCESSING AND TRANSMISSION OF INFORMATION*

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RESEARCH OBJECTIVES

The interest of this group ranges over a wide variety of problems in the processing and transmission of information.

One current activity is the statistical investigation of information sources. The main objective is to estimate the rate at which the sources generate information and to determine how to encode their output economically, in order to decrease the channel capacity required for transmission. The group is currently continuing such an investigation on pictures as information sources by recording the pictures in digital form, for analysis and processing on a digital computer.

A second current activity is the investigation of channels for information transmission. This includes study of the fundamental theoretical relationships between transmission rate, error probability, delay, and equipment complexity, and the construction of suitable coding procedures, especially for binary channels.

In the design of coding and decoding devices, binary switching circuits play a critical role. Viewed at its terminals, a switching circuit can be considered to be a transducer that transforms an input stream of binary digits into a related output stream. In the process, information may be lost and its coded form changed drastically. In this sense a switching circuit is a rather general information channel. Research in this area deals with relationships among the number of memory elements necessary in a circuit, the number of signal feedback loops and the complexity of the signals that flow in them, and the terminal effect of nonideal behavior of the elements of the circuit.

A further intimate relationship between sequential switching circuits and information theory becomes apparent if we consider that an n-state circuit, in effect, classifies each of the infinite number of possible input sequences into one of n different sets. Thus the minimization of the complexity of a circuit corresponds essentially to the classfication of an infinite number of sequence-patterns into a minimum number of sets to be recognized.

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A. A NEW MODE OF OPERATION FOR SEQUENTIAL SWITCHING CIRCUITS

A new mode of operation for asynchronous sequential switching circuits which, under certain conditions, may be economically advantageous, compared with the usual mode considered in reference 1 and in other sources, is described.

Figure XII-1a shows the usual form of a sequential switching circuit. The signal paths leading from the output end of the function generator back to the input end will be

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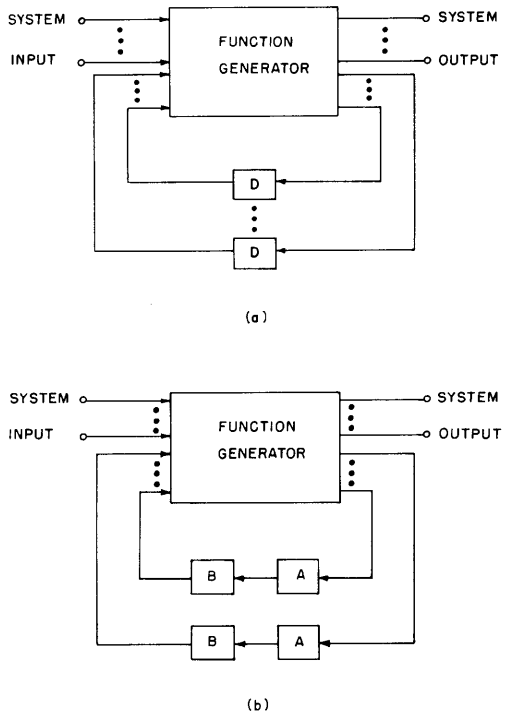

Fig. XII-1. Forms of sequential switching circuit: (a) usual form; (b) double-delay form.

called "state branches," and the signals entering and leaving these branches will be called state-branch "excitations" and "responses." A single inertial delay element in each state branch (see Fig. XII-1) is sufficient for proper operation of such a circuit, provided that the flow matrix does not include critical race conditions (1). (It might be well to explain that an "inertial" delay element of magnitude D is characterized by the fact that its output will change only after an input change has persisted for time D. All delays considered here will be inertial.)

The necessity for avoiding critical races leads, in general, to row assignments that require more state branches than would otherwise be needed (2). In this respect the proposed method, which will be called the "double-delay mode," offers an opportunity for economy. As shown in Fig. XII-1b, two cascaded inertial delays with values A and B are placed in each state branch, and if the magnitudes of these delays can be maintained within certain limits, flow-table row assignments can be made without having to avoid races. Since an amplifier is usually needed in each state branch, reducing the number of state branches leads to a saving in amplifiers, as well as to a possible reduction in the complexity of the combinational circuits that comprise the function generator. In order to achieve these advantages, a larger number of delay elements must be used, and the values of the delay elements must be held within specified tolerances.

Consider a typical flow-table transition that begins with the system in a stable state S_1. Following an input change, the system enters an unstable state S_2, and then the internal state (determined by the state-branch responses) changes, so that the system enters a new stable state S_3. In a double-delay system (see Fig. XII-1b) such a transition takes place in the following manner:

1. The system input changes, thereby altering the state of the system from S_1 to S_2, in which the excitations of the state branches correspond to S_3. This may entail having several state branches become unstable simultaneously.

2. After a time lapse that is at least equal to $A_m + B_m$ (the subscripts m and M will denote minimum and maximum values of the parameters concerned), the response of one of the state branches will change as the new excitation signal flows through the A- and B-delays of that branch, thus initiating the interval that we shall call the "error interval." If several state branches become unstable in S_2, we cannot predict the one that will be the first to change its response, unless we know the relative values of the delays involved. Hence the system may enter any of several states at the beginning of the error interval, and we can expect some of the state-branch excitations to be altered to values other than those corresponding to S_3. However, if the delay values are within the proper limits, the S_3 excitation signals will appear at the A-delay outputs before the error interval begins. This will happen if $A_m + B_m > A_M$.

3. The error interval (in which some of the state-branch excitations may be incorrect) terminates when all of the state-branch responses have assumed values corresponding to S_3. At this point, the system is in S_3, a stable state, and all of the state-branch excitations will take on the S_3 values which they had prior to the beginning of the error interval. None of the A-delay outputs will change during this period, provided that it is of sufficiently short duration; that is, if $(A_M + B_M) - (A_m + B_m) < A_m$.

The A-delays serve as buffers to absorb differences in the values of the state-branch delays. This buffering action is possible because of the inertial nature of the A-delays, which, incidentally, can be placed either before or after the B-delays in the state branches without changing the operation of the system. The B-delays need not be inertial.

By using the two inequalities stated above, constraints can be placed on the relative values of the A- and B-delays and on the permissible tolerances. Let A and B be the specified values of the two types of delay element, and define the normalized tolerances E_A and E_B so that $A_M = A(1 + E_A)$, $A_m = A(1 - E_A)$, $B_M = B(1 + E_B)$, and $B_m = B(1 - E_B)$. Thus

$$A = \frac{A_M + A_m}{2}, \qquad E_A = \frac{A_M - A_m}{2A}, \qquad \ldots$$

Manipulating the inequalities and definitions in a straightforward manner, we obtain the following relationships:

$$E_A = \frac{1 - E_B}{3 + E_B} \tag{1}$$

$$\frac{B}{A} = \frac{2}{3 + E_B} \tag{2}$$

These equations can be used to obtain equivalent constraints in other forms.

Note that, according to Eq. 1, E_B can vary from zero to one, but that E_A ranges only from zero to one-third. In other words, regardless of how precise the B-delays are made, the maximum allowed variation in A is one-third. If $E_A = E_B = E$, then E is approximately 24 per cent.

The two equations also show that the value of B should be somewhere between one-half and two-thirds the value of A, depending upon the tolerances. Either A or B can be chosen without reference to the constraints.

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References

1. D. A. Huffman, Technical Report 274, Research Laboratory of Electronics, M.I.T., Jan. 10, 1954.

2. D. A. Huffman, Technical Report 293, Research Laboratory of Electronics, M.I.T., March 14, 1955.