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PROPOSAL FOR A CAVITY PHASE OBSERVATION SYSTEM IN THE PS MACHINE

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Abstract

In multi-cavity synchrotrons it is essential to be able to measure the phase difference between RF cavities. Errors in relative phase can have a particularly deleterious effect on the beam during RF gymnastics. Currently, two methods are available to measure the relative phase in the CERN Proton Synchrotron (PS), but neither attains the desired resolution nor covers the full arsenal of cavities. This note describes a system that will measure the relative phase between cavities with high resolution. The system makes use of the digital hardware deployed in the LEIR beam control and of the corresponding DSP and FPGA signal processing. The focus is on beams controlled by the Multi Harmonic Source (MHS) clock.
The system described here is also a step towards the deployment of a new generation of digital beam control systems for the PS Complex machines, within the framework of the LHC injector consolidation and following the successful commissioning of the LEIR digital beam control system. Some expected benefits are briefly summarised at the end of this document.

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1. INTRODUCTION

The Proton Synchrotron (PS) beam is manipulated by means of numerous cavities operating at various frequencies. The main workhorse is a set of eleven ferrite-loaded cavities, tuneable over a wide range up to 10 MHz, which perform all acceleration. Additionally, fixed-frequency cavities are employed at frequencies higher than 10 MHz to carry out complex RF gymnastics. An example of this is the delicate bunch splitting operation required to produce the beams for the LHC; for this process 13 MHz, 20 MHz, 40 MHz and 80 MHz cavities are used.

It is essential to be able to observe and monitor the cavity relative phase, i.e. the phase difference between two cavities. Errors in the cavity relative phase influence the bunch splitting process and will have a negative effect for instance on the LHC filling pattern.

Currently, it is possible to measure the relative phase between 10 MHz cavities only; there is no direct means to monitor the relative phase between any two cavities with a frequency higher than 10 MHz. The phase measurement can be done for any PS beam cycle with a resolution of about 1 degree at best. Two methods are available:

a) Time-to-Digital Conversion measurements implemented in a VME crate [1]; this is a 10-years-old system providing measurements each millisecond throughout any cycle and at each RF harmonic h. The phase is measured with a resolution no better than two degrees.

b) Single-point phase discriminator measurements carried out manually at fixed $h = 20$ (as per the original PS design), without beam prior to the PS start-up. The resolution obtained is of about 1 degree and the measurement cannot be repeated during normal operation, unless a dedicated user is inserted in the PS super-cycle.

Method a) offers a convenient means to monitor the phase calibration established by method b).

This note describes a new method for measuring the relative cavity phase passively during a beam cycle. The method uses both the digital hardware (DSPs and FPGAs) and software deployed in LEIR [2] and previously tested in the PS Booster [3]. Relative phases between cavities or between a cavity and a reference point in the machine would be monitored for cavities running at 10 MHz, 13 MHz, 20 MHz, 40 MHz and 80 MHz during beam cycles where the RF is governed by a Multi Harmonic Source (MHS) clock [4]. For any value of h the system would provide a phase resolution much better than 1 degree, a significant improvement over the two methods a) and b). Furthermore, PS cycles not controlled by the MHS scheme could also be treated, by re-synchronising the MHS clock on that specific cycle. This would require minor hardware development, an exercise already carried out when the MHS system was extended from the AD cycle to the LHC cycle.

2. CAVITY PHASE OBSERVATION REQUIREMENTS

The new cavity measurement system proposed for the PS will satisfy these requirements:

a) A phase resolution better than 1 degree at all the different harmonics used to control the beam.

b) Measurement execution during normal machine operation, to allow detecting phase changes due to drifts or hardware modifications.

c) Operation with beam cycles where the RF is governed by the MHS clock and, in particular, with the LHC beams (both 75 ns and 25 ns bunch spacing).

3. SYSTEM DESCRIPTION: HARDWARE

Figure 1 shows the proposed hardware setup. All units apart from the PowerPC (PPC) and the Timing Receiver (CTRV) (i.e. the standard AB/CO modules) are RF-custom modules. Each cavity return signal is analogically filtered, digitised, digitally low-pass filtered and decimated by a Digital Down Converter (DDC) channel. Four channels are available on one DDC daughter card; two daughter cards can be carried by each DSP carrier board, hence the proposed system can treat up to 20 cavities at the same time. Cavity return signals from the 10 MHz and 13/20 MHz cavities can be processed directly by the system. Signals from higher-frequency cavities, such as the 40 MHz and the 80 MHz, need a frequency divider stage owing to the low-pass antialising filter located on the daughter cards.

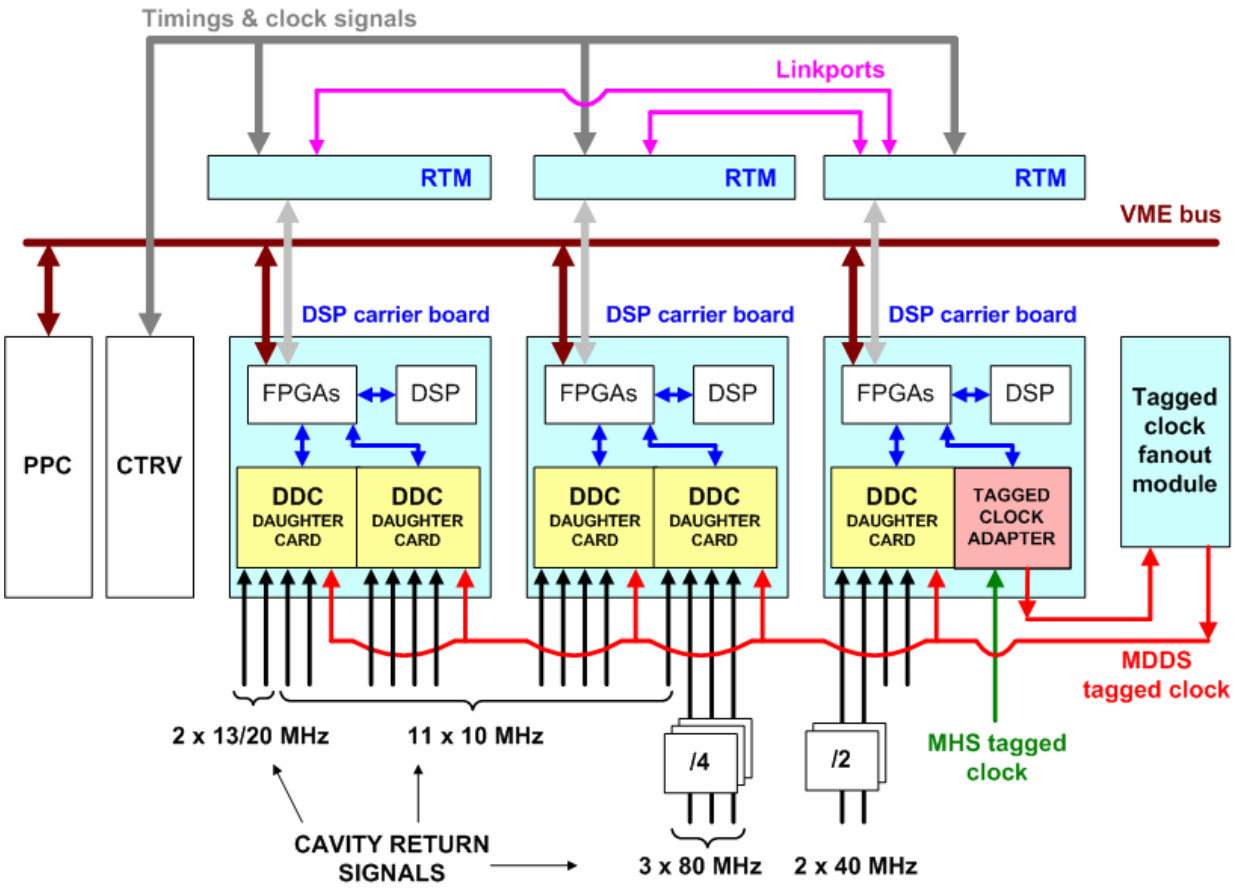

Figure 1: *Schematic overview of the proposed cavity phase measurement system. Keys: DDC – Digital Down Converter, RTM – Rear Transition Module, CTRV – timing receiver module, PPC – Power PC. The daughter card inputs are the cavity return signals.*

Each DDC daughter card is clocked by the same tagged clock, i.e. a clock containing a width-modulated pulse called a tag. The daughter cards require a tagged clock in the MDDS (Master Direct Digital Synthesizers) format, while the clock available in PS follows the MHS format. A tagged clock adapter module, to be built, converts the MHS tagged clock to the MDDS format

and a tagged clock fanout module distributes the MDDS clock. Details on the differences between MDDS and MHS clock and on the tagged clock adapter card are given later in this section.

In Figure 1, the DSP carrier board is a VME module processing DDC digital outputs through a DSP. The DSP is Analog Devices' ADSP-21160M "SHARC" DSP, a 32-bit IEEE processor optimised for high performance DSP applications. It includes an 80 MHz core and a 4 Mbits on-chip, dual-ported SRAM. Six linkports are available for high-bandwidth (80 MB/sec) glueless inter-processor communication and I/O. The DSP carrier board includes several memory banks, visible and accessible for reading/writing from the VMEbus. Through these the on-board DSP interfaces with the higher software layer, namely the Real-Time Task (RTT) running on the PPC. One Rear Transition Module (RTM) associated to each DSP carrier board allows the reception of machine-related timings and clocks generated by a CTRV. The RTM also allows different DSP carrier boards to communicate through linkports.

Figure 2 shows the main elements included in one DDC channel. The Low-Pass Filter (LPF) has a cutoff frequency f_{CO} = 20 MHz and the ADC is Analog Devices' AD9245, a 14-bit resolution device capable of sampling at a rate of up to 80 MHz. The FPGA implements a programmable Cascaded-Integrator-Comb (CIC) filter and more details are given in paragraph 4.1. It should be noted that there is one FPGA on each DDC daughter card, which takes care of the digital signal processing for all four channels. The main setup parameters for each channel are the frequency of the local oscillator and the characteristics of the digital CIC filter. The DDC channel output is the cavity return signal modulation around the local oscillator reference. Each data pair {*I, Q*} is the in-phase (*I*) and quadrature (*Q*) component of the signal. It should be noted that the LPF filters should be of the same type for all channels, so as to have the same group delay. Additionally, it is essential to equalise the electrical paths for all cavity return signals.

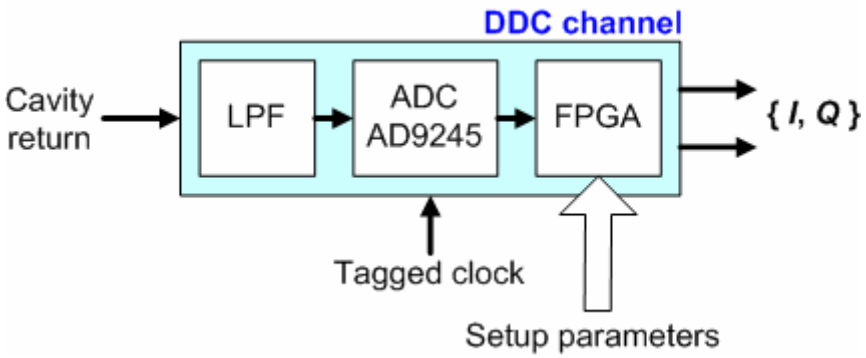

Figure 2: *One DDC channel – schematic view. Keys: LPF – Low Pass Filter, ADC – Analogue-to-Digital Converter, FPGA – Field Programmable Gate Array.*

A tagged clock adapter module is needed to convert both electrical and tag formats from the MHS clock to the MDDS one. In fact, the MHS clock is always equal to 128 times the revolution frequency f_{REV}. It is distributed with a NECL electrical format and its duty cycle is 50%. A clock cycle with a duty cycle of 25 % is issued once per revolution and acts as a revolution frequency marker or tag. The MDDS clock is instead distributed on cable with an LVDS format and its frequency is double that effectively used for clocking the ADC on the DDC daughter cards. The duty cycle is slightly larger than 50% and the tag clock has a fixed duration of 1.8 ns. The MDDS tagged clock can include both a single and a double tag. The single tag acts as a frequency marker, as for the MHS clock; the double tag, composed of two single tag cycles separated by a normal cycle, triggers specific actions in the daughter cards.

Figure 3 shows a conceptual design of the tagged clock adapter board, to be implemented as a daughter card hosted on the DSP carrier board and interfaced with the DSP. The case considered in Figure 3 is that of a proton cycle, characterized by a MHS tagged clock varying between 55.8 MHz at injection and 61 MHz at extraction. The clock is first detagged; this detagged version will then have its frequency doubled and a MDDS-compliant tag will be inserted following a resynchronization step. Finally, the clock physical format will be converted to LVDS and distributed via the tagged clock fanout module. An FPGA will be used to implement the tagged clock conversion.

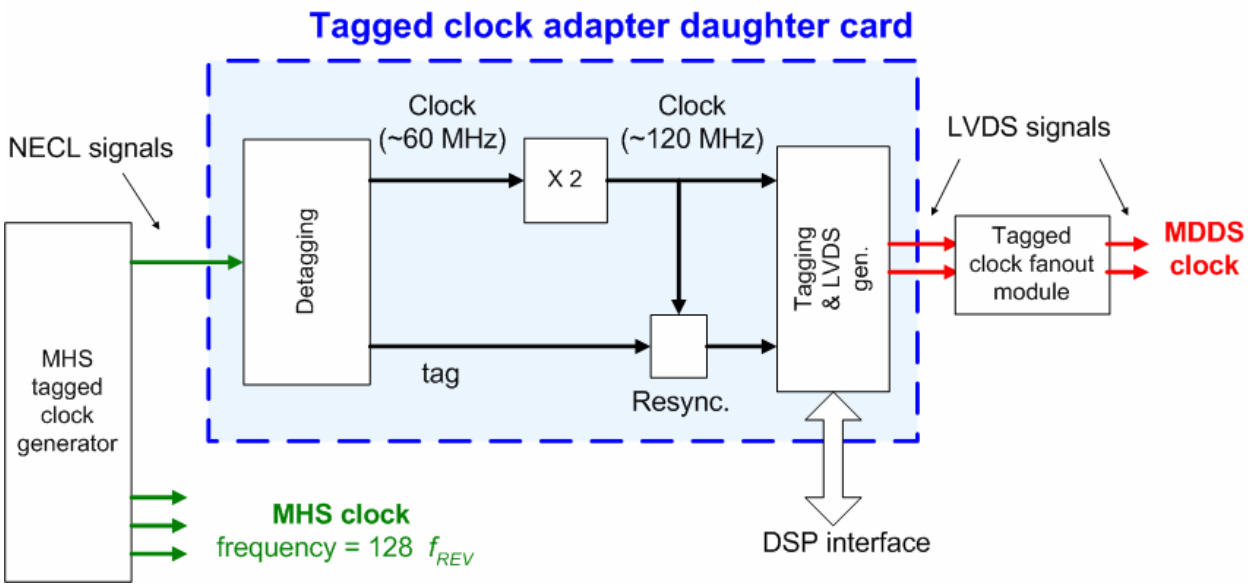

Figure 3: *Schematic design of the daughter card providing tagged clock conversion from MHS to MDDS clock. The case considered is that of a proton beam.*

The tagged clock adapter daughter card will also measure the current value of f_{REV} included in the MHS clock. The DSP on the board carrying the tagged clock adapter daughter card will read f_{REV} and broadcast it to the other DSPs, for use in the frequency-dependent phase rotation implementation (see paragraph 4). Additionally, the tagged clock adapter daughter card will generate a double tag under DSP control. During the beam cycle this will be used to freeze the DDC outputs at exactly the same time, i.e. upon reception of the double tag, prior to a phase measurement, hence avoiding any DSP data acquisition time skew. The value of f_{REV} corresponding to the measurement will also be frozen, i.e. not updated until the DSP reads it, so as to use the correct f_{REV} value when implementing the phase rotation.

Some small adaptation is needed on the FPGA code of the DDC daughter cards. In fact, the phase accumulator must be reset every time the programmed frequency word is an integer harmonic, i.e. when the fractional bits in it are all zeroes. This allows all daughter cards to be locked together in phase unambiguously even after a harmonic number change. A second adaptation will allow the daughter cards to load a new harmonic number directly after the DSP writes it to the daughter card and not following a double tag.

The described scheme can be applied to ion cycles, where the MHS clock frequency varies between 22.7 MHz and 60.5 MHz, owing to the lack of aliased spectral components. A slightly increased SNR should however be expected.

Table 1 summarises the RF-custom modules needed, their number and their current status.

Module description	Quantity	Current status (Q1 2006)
DSP carrier board (VME module)	3	Available & deployed in LEIR.
Rear Transition Module (RTM)	3	Available & deployed in LEIR.
Digital Down Converter (DDC) daughter card	5	Available & deployed in LEIR. Small modification needed to FPGA code.
Tagged clock fanout (VME module)	1	Available & deployed in LEIR.
Tagged clock adapter (daughter card)	1	To be designed & manufactured as modified LEIR MDDS daughter card

Table 1: *RF-custom modules needed for the proposed PS cavity phase observation system, listed with their current state.*

4. SYSTEM DESCRIPTION: SOFTWARE PROCESSING

4.1 OVERVIEW

A schematic of data processing flow for one channel is presented in Figure 4, where the blue boxes represent signal treatment (both analogue conditioning and digital data processing) carried out in the daughter cards, while yellow boxes show signal processing carried out by the DSP. The data pair $\{\rho, \varphi\}$ is the representation in polar coordinates of the data couple $\{I_{ROT}, Q_{ROT}\}$, where ρ is the vector magnitude and φ is its phase.

The cavity return signal can reach a maximum of 2 V_{pp} on a 50 Ω input impedance. Its typical value is 0.5 V_{pp} on the 10 MHz cavities and slightly larger for the other cavities. The typical noise level, observed on an oscilloscope without beam and prior to the PS start-up, for this signal is 10 mV_{pp}.

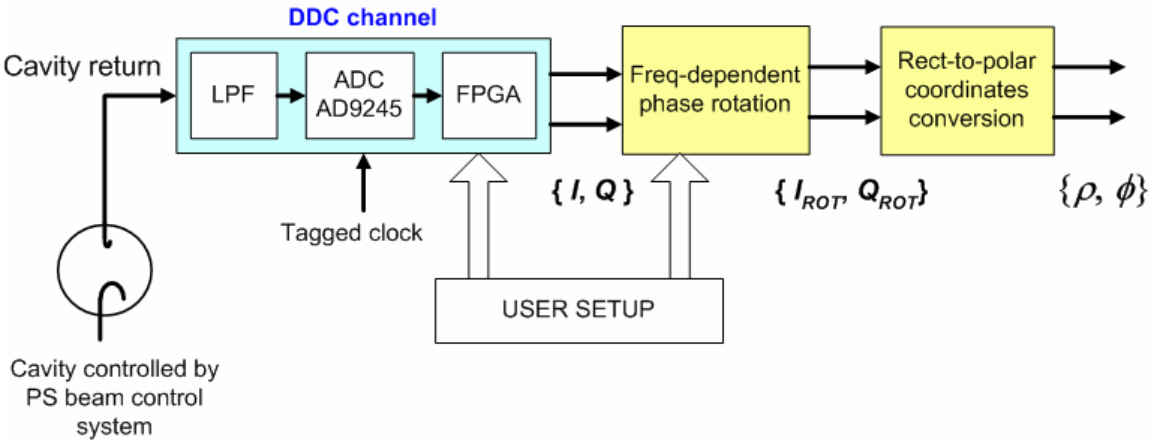

Figure 4: *Schematics of the digital signal processing for one cavity. Blocks in blue represent data treatment carried out in the daughter card, while yellow blocks represent processing carried out by the DSP.*

After the LPF and ADC (filter and sample) stages, cavity return signals are processed in the FPGA, providing the DSP with the $\{I, Q\}$ data. Figure 5 shows the structure of one of the four channels, the others reproducing the same structure. Three blocks compose the DDC, namely the

NCO (Numerically Controlled Oscillator), the Complex Mixer and the digital Low-Pass Filter. The NCO generates a quadrature sine wave from the MDDS clock. The Complex Mixer block consists of two digital multipliers and the Low-Pass Filter block is made of two configurable CIC filters, with main role to remove the unwanted high frequency components from the mixing stage. The output of a DDC channel consists of two 32-bit values.

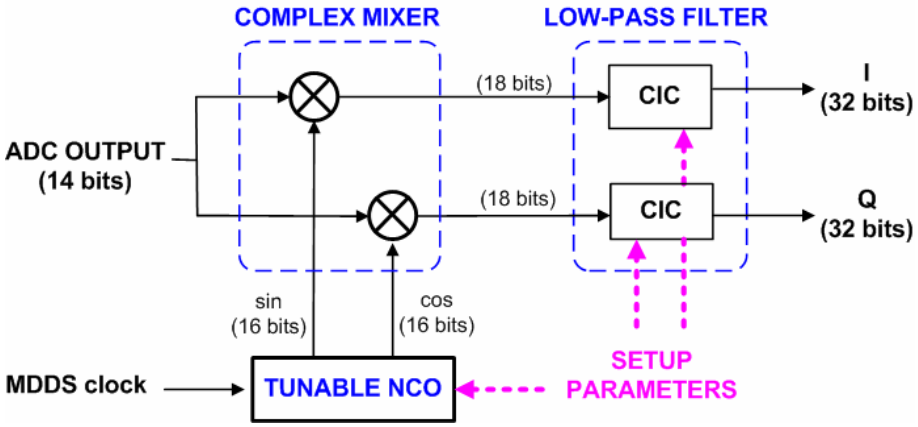

Figure 5: *Schematics of the FPGA code for one DDC channel, emphasising the three main blocks: NCO, Complex Mixer and Low-Pass Filter. The structure is the same for each channel.*

The CIC filter is a low-pass filter with frequency response fully determined by three parameters, namely a) N = number of cascaded integrator and decimator stages, b) R = decimation ratio and c) M = number of delays in the cascaded differentiator stages. These parameters are under DSP control and depend on the user setup. The decimating CIC structure, shown in Figure 6, consists of three main sections: a cascade of N digital integrators, a decimating section and a cascade of N digital differentiators (also called combs). The time elapsed between two consecutive samples at the CIC output $T_{DDC\text{-}OUT}$ corresponds to the sampling period T_S multiplied by the decimation factor R. The averaging time t_{AVGN} for one CIC filter stage ($N = 1$) is given by:

$$t_{AVGN} = T_S \cdot R \cdot M \qquad (1)$$

As an example, CIC setup values N = 1, M = 150 and R = 2 correspond to an integration duration of 5 μs for a 60 MHz sampling frequency.

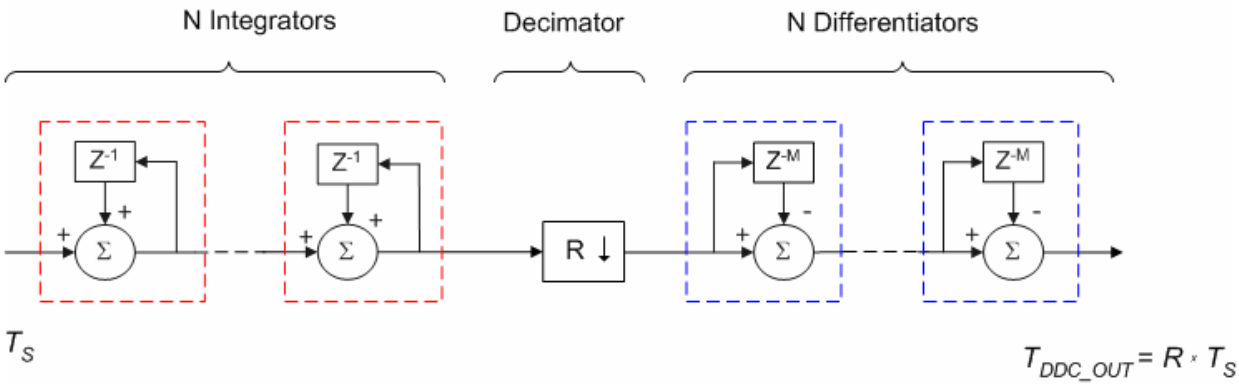

Figure 6: *CIC filter - schematic view.*

The frequency-dependent phase rotation is a DSP-processing block that allows the phase of the cavity to be measured with respect either to another cavity or to a reference point in the machine.

The rectangular-to-polar conversion relies on a fast *atan* calculation module, which is also deployed in the LEIR beam control system. Both phase rotation and rectangular-to-polar conversion are optimised for speed, whilst maintaining high resolution. Details on the algorithms' resolution and execution times are given in section 5.2. The DSP can carry out a new phase measurement for eight DDC channels as often as every 10 μs. The user could for instance select a subset of data of interest and have them transferred to the application program to analyse them. Lower sampling frequencies would also be possible, together with a longer CIC integration time.

Finally, the system works in Pulse-to-Pulse modulation (PPM). A dedicated RTT running on the PPC board will collect data in polar coordinates from each processing chain and will pass them to the user by means of a dedicated application program.

4.2 DSP REQUIRED INPUT

For each cavity and in PPM mode the following information needs to be known by the cavity phase measurement system:

a) The user-selectable reference function that defines the RF harmonic numbers used during acceleration. The actual RF harmonic number used on each cavity can also be confirmed by the phase measurement system.

b) The user-selectable reference function that defines the cavity voltage during acceleration. This information is used to determine whether a cavity is active or not, hence whether the measurement associated to it is valid or not.

c) The timings associated to the reference functions mentioned in point a) and b).

d) The MHS phase control output, which can take values of 0 or π.

e) The value of f_{REV}, so as to implement the frequency-dependent phase rotation. This value is obtained by a direct measurement of the MHS clock carried out in the tagged clock adapter daughter card. The value is broadcasted by the DSP carrying the tagged clock adapter to the other DSPs in the system through the linkports.

f) The tuning group the spare 10 MHz cavity belongs to.

5. SYSTEM DESCRIPTION: PHASE MEASUREMENT RESOLUTION

This paragraph shows how to calculate the resolution of the system as a function of the hardware and of the digital signal processing involved, for a given input signal SNR. In particular, it shows that the digital signal processing can improve by 20 dB or more the measurement resolution. The input signal SNR used for the calculations is that observed on a scope without beam and corresponds to 10 mV_{pp}, uniformly distributed in its bandwidth.

It should be emphasised that the actual input SNR determining the error at the DDC output depends on many factors, such as the input signal noise spectral distribution. In addition the received noise on the cavity returns may be dominated by parasitic noise pick-up. The main source of this parasitic RF signal leakage is the cable transfer impedance, which is a strong function of frequency owing mainly to the skin effect. Particularly detrimental is RF leakage

from the beam (through imperfect RF decoupling of the insulated flanges - RF by-pass circuits and the finite transfer impedance of the cavity return cables), which usually presents strong harmonic contents at the harmonics the cavities are operated on. As a consequence, RF leakage from the beam will induce an additional RF vector on the cavity return, hence generating a bias and systematic phase or voltage error that cannot be reduced by the filter in the DDC. In this case, the SNR can be drastically improved by reducing the cable transfer impedance. A Low Transfer Impedance (LTI) cable with no PVC or halogen content has been developed for CERN to be used in the Antiproton Decelerator (AD), where it was installed in the year 2001. This cable, denominated C-50-6-2 (CERN store SCEM 04.61.11.FC), has improved the SNR by more than 20 dB. Figure 7 shows the parasitic noise pick-up quantified by the transfer impedance *Z_t* as a function of frequency for five cable types. The parasitic noise pick-up with the C-50-6-2 cable (referred to as LTI in Figure 7) is between 20 and 40 dB lower than with the standard C-50-6-1 cable in the frequency range 0.1 to 10 MHz. This cable is much more effective than two individual coaxial cables running in parallel and it is simpler to use than balanced transmission; screw-on N-type connectors are also available.

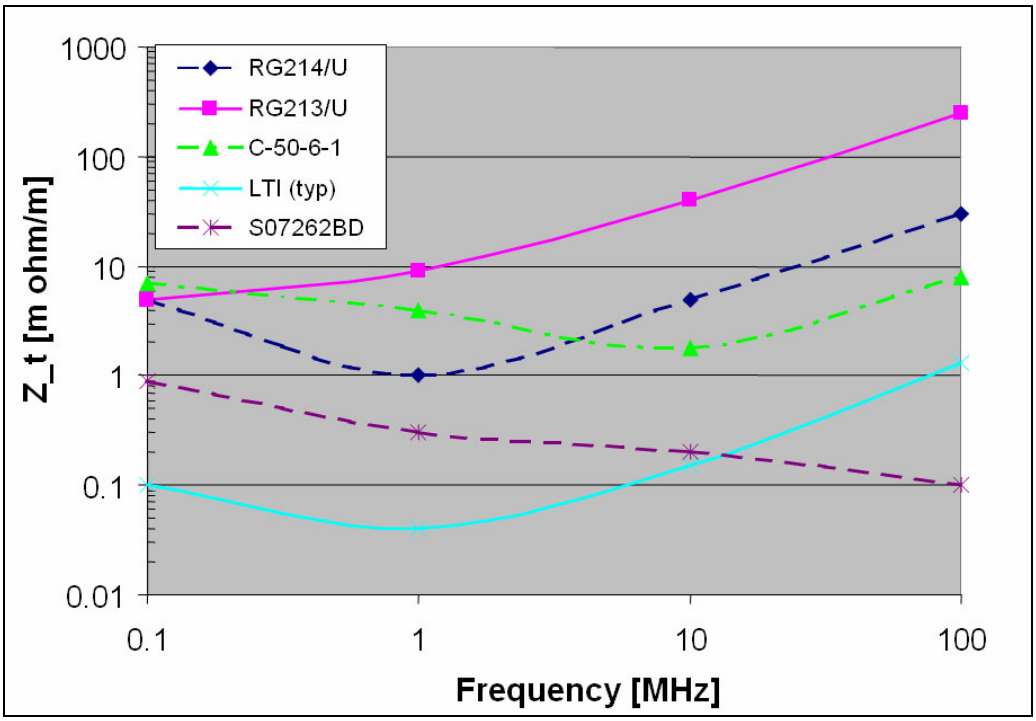

Figure 7: *Parasitic noise pick-up comparison of five cable types. The newly-developed cable is referred to as LTI and offers a parasitic noise pick-up lower by 20 to 40 dB than that given by the C-50-6-1.*

5.1 PRE-DSP PROCESSING RESOLUTION

The signal-to-noise ratio (SNR) of data given to the DSP depends on the overall system noise, which is given by three contributions:

a) ADC SNR;
b) input signals (i.e. the cavity returns) SNR and full scale values;
c) digital filter processing gain.

The combined a) plus b) noise can be determined by converting the noise contribution from a) and from b) to power, adding them and calculating the equivalent SNR in dB. Then the digital

filter processing gain c) is added.

The AD9245 ADC has a typical SNR of 72 dB and a 2 V_{pp} input. The noise voltage $V_{NOISE,ADC}$ representing thermal and quantisation noises within the ADC is:

$$V_{NOISE,ADC} = 0.707 \cdot 10^{-\frac{SNR}{20}} = 0.707 \cdot 10^{-\frac{72}{20}} = 1.776 \cdot 10^{-4} \text{ V} \quad (2)$$

with a corresponding noise power $P_{NOISE,ADC}$ of

$$P_{NOISE,ADC} = \frac{V^2_{NOISE,ADC}}{Z_I} = 6.308 \cdot 10^{-10} \text{ W} \quad (3)$$

where $Z_I = 50\,\Omega$ is the input impedance.

The input signal noise is 10 mV_{pp}. The equivalent input noise $V_{NOISE,FRONTEND}$ is

$$V_{NOISE,FRONTEND} = 5 \cdot 10^{-3} \cdot 0.707 = 3.535 \cdot 10^{-3} \text{ V} \quad (4)$$

Where the corresponding noise power $P_{NOISE,FRONTEND}$ is

$$P_{NOISE,FRONTEND} = 2.499 \cdot 10^{-7} \text{ W} \quad (5)$$

The total noise power of the front-end and the ADC is obtained by adding (3) to (5), i.e.

$$P_{NOISE,ADC+FRONTEND} = 2.5 \cdot 10^{-7} \text{ W} \quad (6)$$

In the considered case the noise in the input signal dominates the ADC noise.

The resulting maximum SNR_{MAX} corresponds to the maximum full scale input power, i.e. 10 mW and is give by:

$$SNR_{MAX} = 10 \cdot \log_{10}\left(\frac{10\ mW}{2.5 \cdot 10^{-7} W}\right) = 46\ dB \quad (7)$$

As the typical amplitude of the input signal is 0.5 V_{pp} for the 10 MHz cavities (that have the lowest input signal level), the corresponding SNR is:

$$SNR_{TYPICAL} = 10 \cdot \log_{10}\left(\frac{0.625\ mW}{2.5 \cdot 10^{-7} W}\right) = 34\ dB \quad (8)$$

The digital filter processing gain c) is caused by sampling the input signal at high frequency and then digitally filtering it by the CIC filter. As a consequence, the noise outside the band of interest is digitally removed and the SNR is improved. The minimum desired values the CIC parameters take are $N = 1$, $M = 150$ and $R = 2$. The corresponding processing gain, expressed in dB, is:

$$PG_{CIC} = 10 \cdot \log_{10}(R \cdot M) = 24.77 dB \quad (9)$$

Hence, the total SNR of the system is:

$$SNR = 34\ dB + 24.77\ dB = 58.77\ dB \tag{10}$$

Finally, the ratio between the RMS value of the input signal and the RMS value of the noise is given by:

$$\frac{|RMS(input)|}{|RMS(noise)|} = 10^{-\frac{58.77}{20}} = \frac{1}{868} = 1.152 \cdot 10^{-3} \tag{11}$$

In other words, the noise contained in each $\{I, Q\}$ pair given to the DSP is slightly worse than 1‰ for the typical 10 mV input signal noise.

5.2 DSP PROCESSING RESOLUTION

Equation (11) provides a good estimate of the phase measurement resolution. In fact, due to the high dynamic range inherent in the use of 32-bits floating point arithmetic, the DSP processing does not actually affect the error.

The most critical operations in terms of digital signal processing precision are:

a) the calculation of the *sine* and *cosine* components for the phase rotation;
b) the *atan* calculation to perform the rectangular-to-polar conversion.

Both calculations have been implemented at CERN with 32-bit floating point, single resolution and are optimised for speed, without reducing significantly the available resolution.

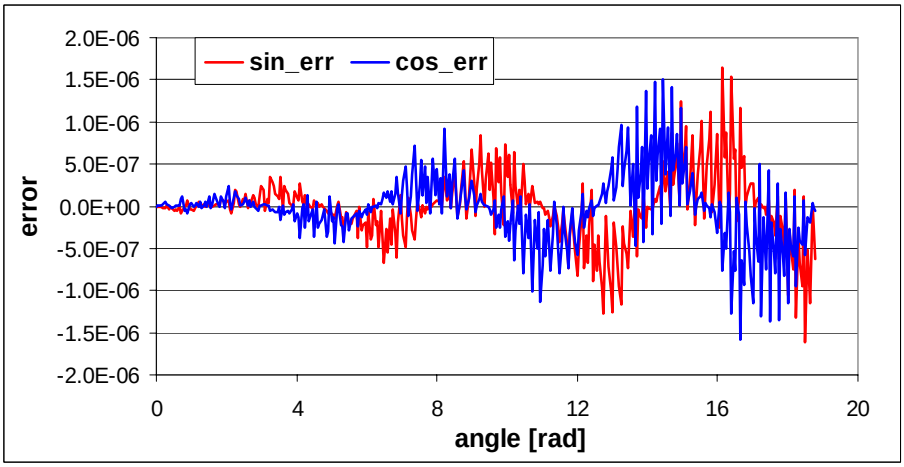

Figure 8: *The error magnitude of CERN sine and cosine functions single precision implementation compared to the double precision implementation provided by the VisualDSP++ library.*

The *sine* and *cosine* calculation algorithm has been implemented by a polynomial expansion of the 7th order instead of the usual Taylor series expansion of sine and cosine. The polynomial coefficients are obtained from a number of linear equations where the error has been set to zero at strategic points in the argument φ range, i.e. equidistant on a φ^2 scale. This results in an error which oscillates within fixed error limits that, according to Matlab simulations, are more than

100 times smaller than what is provided by the Taylor series method. Sine and cosine are calculated simultaneously thanks to the Single Input Multiple Output (SIMD) hardware feature of the SHARC DSP. The argument φ range is reduced from [0, 2π] to [$-\pi/4$, $+\pi/4$], hence allowing the use of a polynomial order as low as 7, instead of 15 or more. Once sine and cosine are evaluated for the argument range [$-\pi/4$, $+\pi/4$], they are swapped and/or their sign is changed to get the results corresponding to the original argument quadrant. Figure 8 shows the error of the CERN implementation with respect to the highly precise 64-bits, double precision function provided by the DSP development environment VisualDSP++, for an argument ranging in [0, 6π]. It is shown that the error is always less than $2 \cdot 10^{-6}$; as soon as the error is outside the first quadrant, the rounding error is dominated by the rounding of the input argument and the rounding of the $2/\pi$ constant used for radiant-to-quadrant conversion.

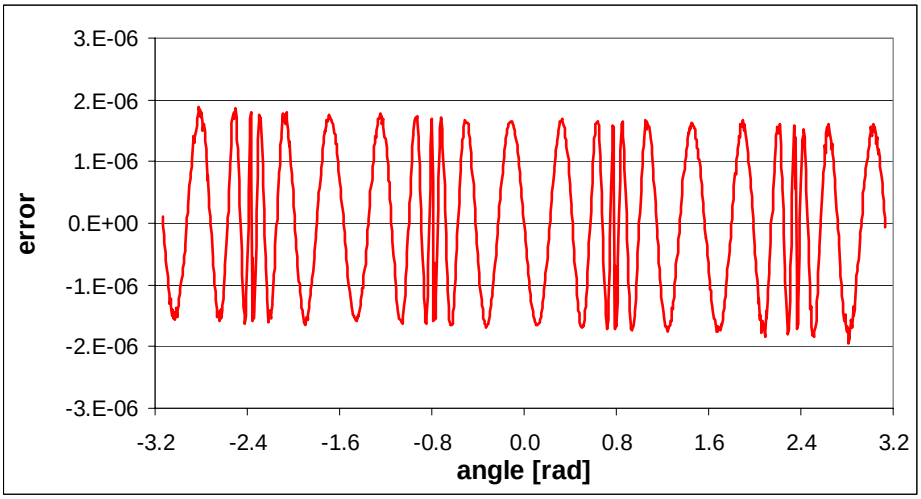

Figure 9: *The error magnitude of CERN atan function single-precision implementation compared to the double-precision implementation provided by a VisualDSP++ library.*

The *atan* function is implemented similarly to the *sine* and *cosine* functions, i.e. by a polynomial approximation. Figure 9 shows the error thus obtained with respect to the highly precise 64-bits, double precision function provided by the DSP development environment VisualDSP++, for an argument in the [$-\pi$, $+\pi$] interval. Again, the error is always less than $2 \cdot 10^{-6}$.

The execution times of the CERN single precision implementations, the VisualDSP++ single precision and the VisualDSP++ double precision implementations are compared in Table 2. In particular, the *sine* and *cosine* functions are calculated 43 times faster than the double-precision calculation provided by the VisualDSP++ library; the *atan* is calculated about 13.6 times faster.

	Execution time [µs]		
Function	**CERN single precision implementation**	**VisualDSP++ single precision implementation**	**VisualDSP ++ double precision implementation**
cosine	0.25 (for a sine/cosine couple)	0.59	5.5
sine		0.59	5.3
atan	0.4125	1.4	5.6

Table 2: *Summary of DSP functions execution times.*

5.3 SUMMARY OF RESOLUTION

The proposed cavity phase measurement system will achieve a phase resolution of about 0.001 degrees for a 10 mV_{pp} cavity return signal noise, owing to the processing gain obtained from digital down conversion and to the high dynamic range and resolution provided by the floating-point processing available in the DSP. This resolution is higher than what either of the phase measurement methods mentioned in section 1 can provide. The cavity return signal quality is crucial for the measurement resolution and can be improved by using a LTI cable, as experienced in the AD machine.

6. CONCLUSIONS AND MEDIUM TERM PLAN

A new digital system for measuring the relative phase of the cavities in the PS machine is proposed. The system is based on hardware and software blocks deployed in the LEIR digital beam control system. Measurements are obtained in a passive way throughout the beam cycle and at rates of up to 100 kHz. This note addressed in particular beam cycles governed by the MHS scheme; the MHS scheme could however be extended to all the other cycles, allowing the proposed system to treat them. This high-resolution observation of relative cavity phase differences will be particularly beneficial for the LHC beam, by improving the splitting process.

The successful commissioning of the new LEIR digital beam control system has paved the way for migrating the same technology to other accelerators in the CPS. The master-slave, PS-inherited architecture deployed in LEIR and the digital signal processing carried out by the system is in fact particularly suited for fast-cycling machines with high frequency swing. An important benefit of migrating this technology to the PS is the implementation of a phase feedback on individual cavity phases based on cavity return signals. This will reduce the phase variations due to beam loading and varying phase shifts in the high level RF equipments. Other benefits of a migration for all CPS accelerators include a) the possibility to implement systems where all control and acquisition parameters are fully PPM; b) full remote control and data access; c) improved uniformity of the CPS beam control systems hence an easier maintenance.

8. ACKNOWLEDGMENTS

The authors wish to express their gratitude to R. Garoby for helpful comments and suggestions.

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