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# The Beetle Reference Manual

— chip version 1.2 —

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document version: 1.3

## Abstract

This paper details the electrical specifications, operating conditions and port definitions of the readout chip *Beetle 1.2*. The chip is developed for the LHCb experiment and fulfils the requirements of the silicon vertex detector (VELO, VETO), the silicon tracker and the RICH detector in case of multi-anode photomultiplier readout.

It integrates 128 channels with low-noise charge-sensitive preamplifiers and shapers. The pulse shape can be chosen such that it complies with LHCb specifications: a peaking time of 25 ns with a remainder of the peak voltage after 25 ns of less than 30%. A comparator per channel with configurable polarity provides a binary signal. Four adjacent comparator channels are being ORed and brought off chip via LVDS ports. Either the shaper or comparator output is sampled with the LHC-bunch-crossing frequency of 40 MHz into an analog pipeline. This ring buffer has a programmable latency of max. 160 sampling intervals and an integrated derandomising buffer of 16 stages. For analog readout data is multiplexed with up to 40 MHz onto 1 or 4 ports. A binary readout mode operates at up to 80 MHz output rate on two ports. Current drivers bring the serialised data off chip. The chip can accept trigger rates of up to 1.1 MHz to perform a dead-timeless readout within 900 ns per trigger. For testability and calibration purposes, a charge injector with adjustable pulse height is implemented. The bias settings and various other parameters can be controlled via a standard I<sup>2</sup>C-interface.

Appropriate design measures have been taken to ensure the radiation hardness against total ionising dose effects in excess of 10 Mrad. A robustness against Single Event Upset is achieved by redundant logic.

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## Document Edition History

This manual describes the chip version 1.2. For versions 1.0 and 1.1 please refer to the corresponding version of this manual (LHCb-note LHCb-2001-046).

| Version | Date       | Author | Description                                |
|---------|------------|--------|--|
| 1.0     | 20.04.2002 | DB, SL | document created                           |
| 1.1     | 20.02.2003 | DB, SL | draft version published                    |
| 1.2     | 31.01.2004 | SL     | updated draft version published            |
| 1.3     | 17.02.2004 | SL     | final version, document maintenance closed |

## Chip Version History

| Version   | Submission Date | Changes relating to previous version  |
|-----------|-----------------|---|
| Beetle1.0 | April 2000      |   |
| Beetle1.1 | March 2001      | test channel extended till pipeline readout amplifier (pipeamp) output<br>modified pipeline layout<br>analog delay element for I <sup>2</sup> C-SDA line added<br>modified pipeamp<br>modified bias network of pipeamp<br>modified multiplexer<br>modified tristate buffer in control circuit   |
| Beetle1.2 | April 2002      | implementation of a new front-end (set 2c of <i>BeetleFE1.1</i> )<br>modified analog input pad geometry (elongated pad opening)<br>introduction of SEU robustness scheme<br>restriction of readout time to 900 ns<br>introduction of 8 additional status bits in data header<br>introduction of a power-up reset<br>introduction of comparator mask bit per channel<br>introduction of test pulse selection bit per channel<br>additional LVDS mode of current output buffer<br>on-chip trigger synchronisation<br>increase of pipeline depth by 1<br>hard-wired I <sup>2</sup> C-chip address (defined via bond pads)<br>introduction of SCHMITT-triggers in the I <sup>2</sup> C-pads<br>reduction of DAC resolution from 10 to 8 bits<br>increase of max. deliverable bias current to 2 mA<br>additional power pads at the back side |

# 1 Chip Architecture

The *Beetle* can be operated as analog or alternatively as binary pipelined readout chip. It implements the basic RD20 front-end electronics architecture [1, 2, 3]. Fig. 1 shows a schematic block diagram of the chip.

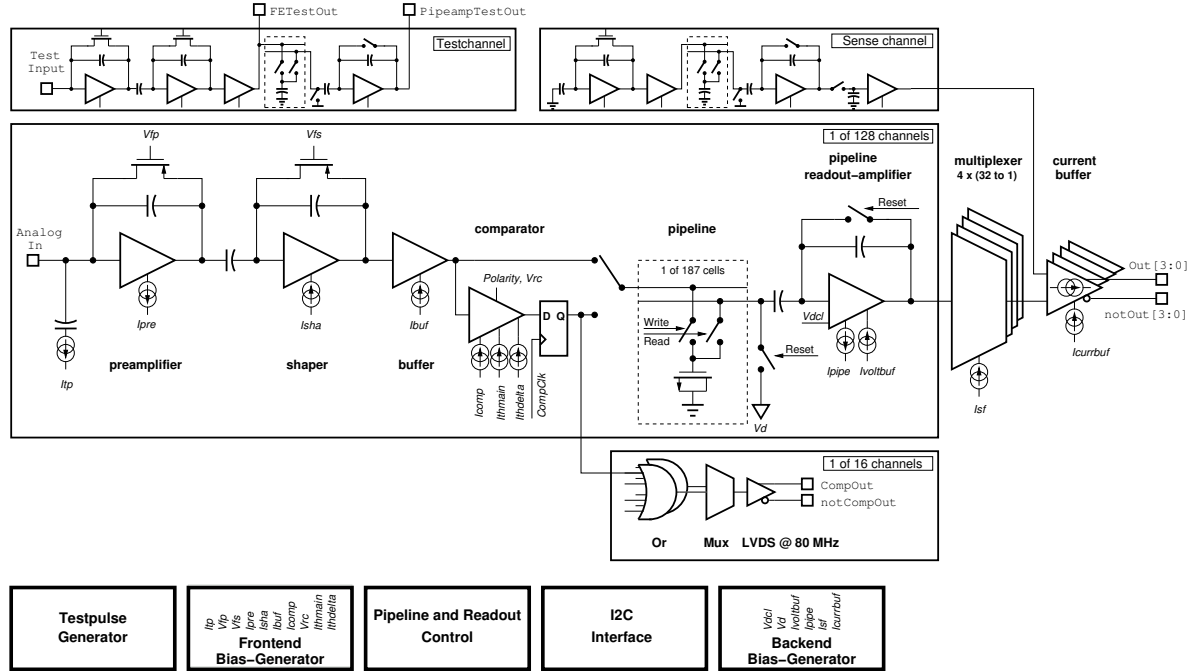


Figure 1: Schematic block diagram of the *Beetle* readout chip<sup>3</sup>.

The chip integrates 128 channels, each consisting of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. They form the analog front-end. The equivalent noise charge (ENC) of the front-end has been measured as  $ENC = 497 e^- + 48.3 e^- / pF \cdot C_{in}$ . The shape of the front-end pulse can be chosen according to the specific requirements of the application. The minimum risetime (10 – 90%) is well below 25 ns, the remainder of the peak voltage after 25 ns can be adjusted to less than 30% for load capacitances  $\leq 35$  pF. A comparator discriminates the front-end's output pulse. The threshold is adjustable per channel and input signals of both polarities can be processed. Four adjacent comparator channels are grouped by a logic OR, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signalling (LVDS) ports at 80 MHz. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency at 40 MHz into an analog pipeline which has a programmable latency of max. 160 sampling intervals and an integrated multi-event buffer of 16 stages. The signal stored in the pipeline is transferred to the multiplexer via a resettable charge-sensitive amplifier (pipeamp). Within a readout time of 900 ns current drivers bring the serialised data off chip. The output of a dummy channel is subtracted from the analog data to compensate common mode effects. All amplifier stages are biased by forced currents. On-chip digital-to-analog converters (DACs) with 8 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard I<sup>2</sup>C-interface [8]. All digital control and data signals, except those for the I<sup>2</sup>C-ports, are routed via LVDS ports.

The choice of a deep-submicron process technology (0.25  $\mu$ m standard CMOS) with a thin gate oxide ( $t_{ox} \approx 62$  Å) and the consistent use of enclosed NMOS transistors reduces a shift in the transistor

<sup>3</sup>For a derivation of the pipeline depth refer to [4].

threshold voltage and eliminates "end-around" leakage current paths. This establishes a total ionising dose (TID) radiation hardness in excess of 45 Mrad. Single Event Latch-up (SEL) is suppressed due to the implementation of guard-rings. The continuous use of triple-redundant logic ensures a robustness against Single Event Upset (SEU).

## 2 Electrical Specifications

### 2.1 DC Characteristics

Table 1: DC characteristics of *Beetle1.2*

| Supply  | Min.<br>[V] | Nom.<br>[V] | Max.<br>[V] | Description                                    |
|---------|-------------|-------------|-------------|--|
| Vdda    | 2.2         | 2.5         | 2.7         | Positive analog supply                         |
| Gnda    | 0           | 0           | 0           | Negative analog supply                         |
| Vddd    | 2.2         | 2.5         | 2.7         | Positive digital supply                        |
| Gnnd    | 0           | 0           | 0           | Negative digital supply                        |
| VddPre  | 2.2         | 2.5         | 2.7         | Positive preamplifier supply                   |
| GndPre  | 0           | 0           | 0           | Negative preamplifier supply (detector ground) |
| VddComp | 2.2         | 2.5         | 2.7         | Positive comparator output supply              |
| GndComp | 0           | 0           | 0           | Negative comparator output supply              |

### 2.2 Signal Levels

The *Beetle* chip has 3 different kind of I/O pads. The signal levels for these pads are given in table 2.

Table 2: Specification of signal levels.

| I <sup>2</sup> C         |                |      |      |                      |      |      |      |
|--------------------------|----------------|------|------|----------------------|------|------|------|
|                          | logic 0        |      |      | logic 1              |      |      | Unit |
|                          | Min.           | Max. | Typ. | Min.                 | Max. | Typ. |      |
| input                    | -0.7           | 1.1  | 0.0  | 1.5                  | 3.3  | 2.5  | V    |
| output                   | —              | —    | 0.0  | —                    | —    | 2.5  | V    |
| CMOS                     |                |      |      |                      |      |      |      |
|                          | logic 0        |      |      | logic 1              |      |      | Unit |
|                          | Min.           | Max. | Typ. | Min.                 | Max. | Typ. |      |
| input                    | -0.7           | 1.1  | 0.0  | 1.4                  | 3.3  | 2.5  | V    |
| output                   | —              | —    | 0.0  | —                    | —    | 2.5  | V    |
| LVDS (100 Ω termination) |                |      |      |                      |      |      |      |
|                          | offset voltage |      |      | differential voltage |      |      | Unit |
|                          | Min.           | Max. | Typ. | Min.                 | Max. | Typ. |      |
| input                    | 0.0            | 2.5  | 1.2  | 0.1                  | 2.5  | 0.2  | V    |
| output                   | —              | —    | 1.02 | —                    | —    | 1.38 | V    |

### 2.3 Output Characteristics

The *Beetle* chip provides an *analog* as well as a *binary* output mode. A differential current is transmitted in each case, where in binary mode, the output signal is compatible with the LVDS standard [6].

Fig. 2 gives an example of a receiver circuit for analog signals using the CLC400 transimpedance amplifier [5] and binary signals using the DS90C032 [7] LVDS receiver.

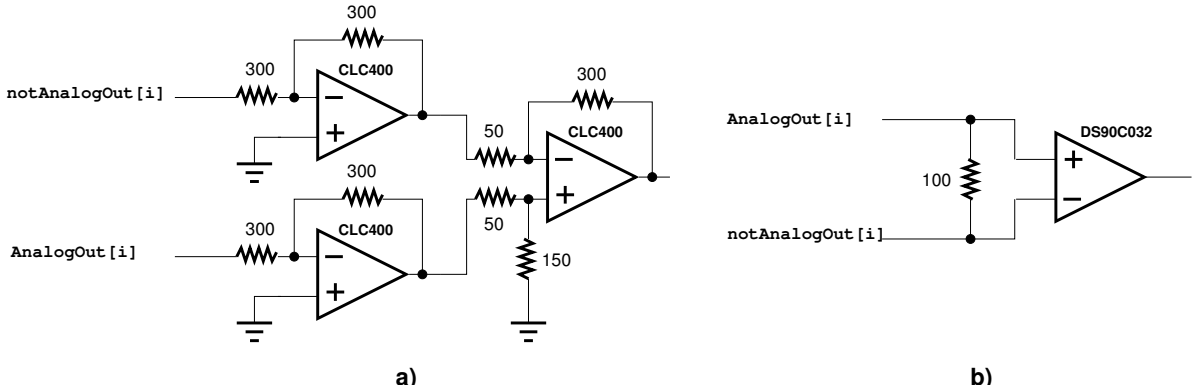


Figure 2: Example of a receiver circuit for the analog (a) and binary (b) output signals. In case of analog signals the CLC400 transimpedance amplifier is used, in case of binary signals the DS90C032 LVDS receiver.



## 3 Operating the *Beetle* Chip

### 3.1 Front-end Pulse Shape

The front-end output signal is a semi-Gaussian pulse which can be characterised by three parameters:

- peaking time  $t_p$  (0 – 100%),
- peaking voltage  $V_p$  and
- remainder  $R$ , which is the ratio between the signal voltage 25 ns after the peak ( $V_{25+}$ ) and  $V_p$ .

The peaking time is sometimes hard to measure since the starting point of the pulse is not well defined, so the rise time  $t_r$  (10 – 90%) is usually quoted. Fig. 3 explains the various parameters.

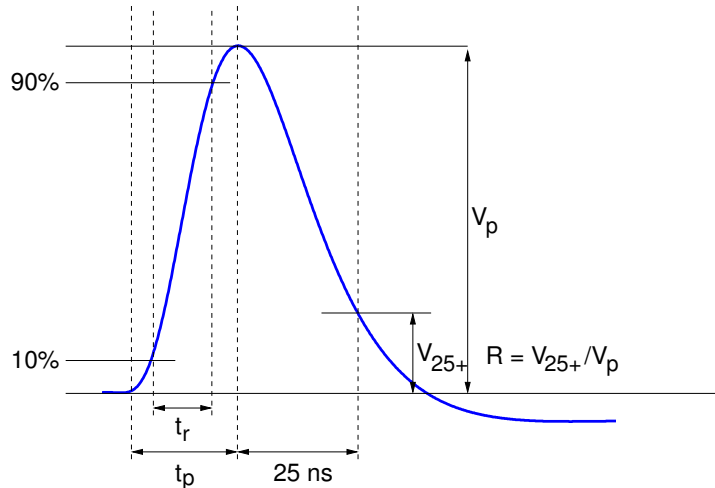


Figure 3: Semi-Gaussian pulse with the corresponding parameters characterising the shape.

Information about the front-end's pulse shape can be obtained on a *Beetle* readout chip from either the test channel output (`TestOutput`, pad no. 245) or from a *pulse shape scan*. Here, the front-end's output is read out via the pipelined path while the preamplifier input signal is shifted w. r. t. the sampling clock.

The pulse shape can be varied by 5 bias parameters:

**Ipre** sets the preamplifier bias current. Higher currents decrease the rise time and the remainder and increase the pulse undershoot.

**Isha** defines the shaper bias current. Increasing currents shift the DC-offset to lower values and result in a slightly decreasing rise time, remainder and undershoot.

**Ibuf** sets the buffer bias current. It does not affect the shape of the pulse, but the DC-offset.

**Vfp** determines the preamplifier feedback resistance. It defines the time constant for discharging the preamplifier's integration capacitor and therefore the tolerable input charge rate.

**Vfs** controls the shaper feedback resistance. Increasing  $Vfs$  values enlarge the peaking time, the peaking voltage as well as the remainder.

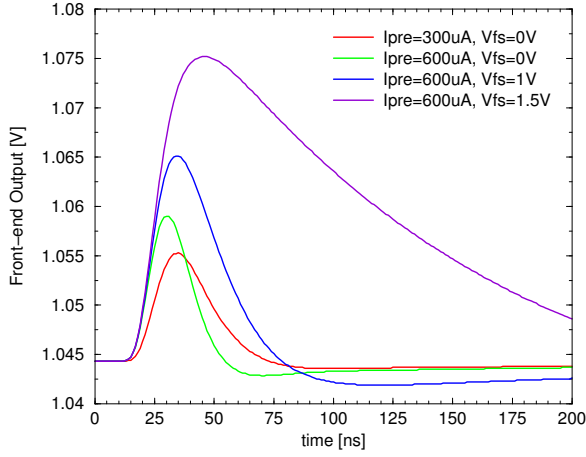


Figure 4: Variation of the front-end pulse shape for different bias settings ( $I_{sha} = I_{buf} = 80 \mu\text{A}$ ,  $V_{fp} = 0\text{V}$ ).

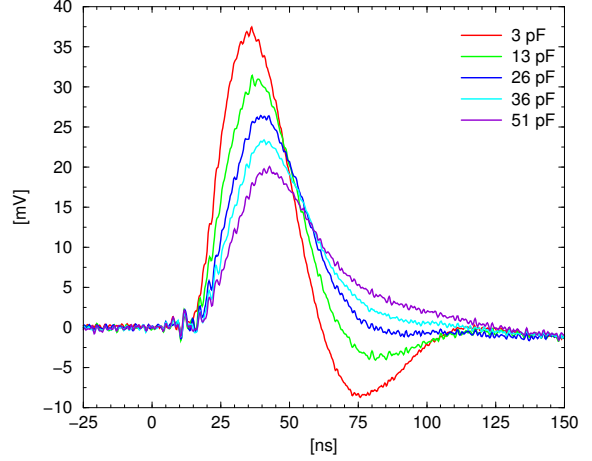


Figure 5: *Beetle1.2* front-end output signal for load capacitances varying between 3 and 51 pF.

Fig. 4 depicts the variation of the pulse shape for four example bias parameter settings. For the nominal settings listed in table 8, i.e.  $I_{pre} = 600 \mu\text{A}$ ,  $I_{sha} = I_{buf} = 80 \mu\text{A}$ ,  $V_{fp} = V_{fs} = 0\text{V}$ , the front-end sensitivity  $A_Q = V_{FEout}/Q_{in} = 38\text{mV}/22,000\text{e}^- = 38\text{mV}/\text{MIP}$ .

For fixed bias parameters the shape of the front-end output pulse varies with the external load capacitance (cf. fig. 5).

### 3.2 Test Channel

The *Beetle* chip integrates beside the 128 channels a *test channel* with direct access to the front-end output (**TestOutput**, pad no. 245) as well as the pipeamp output (**PipeampTestOut**, pad no. 221). An input charge can be injected either via the **TestInput** port (pad no. 2) or via the internal test pulse generator (+1 step, cf. 3.5). Additionally, 5 internal voltage nodes of the test channel's front-end are accessible on pads: **Prebias** (pad no. 250), **Prebias1** (pad no. 249), **Shabias** (pad no. 248), **Shabias1** (pad no. 247) and **Bufbias** (pad no. 246). Fig. 6 illustrates the various bias nodes.

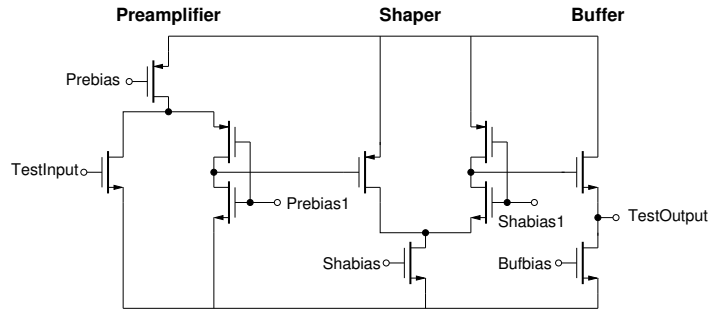


Figure 6: Test channel bias nodes.

### 3.3 Reset Modes

Two different types of reset exist on *Beetle1.2*.

- *Power-up reset* is activated immediately when the power of the chip is switched on. The reset's time-constant, i.e. the time between "power-on" and the reset becoming inactive, can be adjusted via an external capacitance connected to the `PowerupReset` pad. For typical capacitance values like  $C_{ext} = 10 \text{ nF}$  (100 nF), the time constant  $\tau = 28 \text{ ms}$  (280 ms). All *Beetle* registers are reset to 0 and the I<sup>2</sup>C-interface is initialised.
- *External reset* follows the `Reset` port (see section A.3). It resets the pipeline write and trigger pointer to column number 0 and initialises the control logic's state machines. The rising edge of `Reset` re-initialises the I<sup>2</sup>C-interface. The minimum reset width is 25 ns, i.e. one sampling clock cycle.

### 3.4 Readout Modes

The readout of the *Beetle* chip is synchronous to the readout clock *Rclk*, which is generated on-chip from the sampling clock *Sclk* (`Clk` port). For operation at LHC, sampling and readout clock have the same frequency. For other applications, the readout clock frequency can be reduced to a fraction of *Sclk* (cf. 4.2).

*Beetle1.2* provides three different readout modes<sup>4</sup>:

**Analog readout on 4 ports** Each port carries 4 header bits plus 32 channels. Data is transmitted synchronous to the rising edge of the readout clock and takes 900 ns.

**Binary readout on 2 ports** Each port carries 8 header bits plus 64 channels. Data is transmitted synchronous to both edges of *Rclk*. The readout takes 900 ns.

**Analog readout on 1 port** This is for applications with less demanding readout speed requirements. The readout lasts 3.6  $\mu\text{s}$ .

Fig. 7 shows the assignment of the header bits and analog input channels to the output channels in the different modes. The meaning of the various header bits is given in table 3.

Table 3: Header bits in *Beetle1.2*'s data burst.

| Bit | Description  |  |
|-----|--|--|
| I0  | LeadingBit   | always active (= 1)  |
| I1  | ParPCN   | (even) parity of pipeline column number (PCN)                        |
| I2  | ActiveEDC  | 1 indicates active error detection and correction (EDC) logic        |
| I3  | ParCompChTh  | (even) parity of register <i>CompChTh</i> (reg. no. 20, cf. table 8) |
| I4  | ParCompMask  | (even) parity of register <i>CompMask</i> (reg. no. 21, cf. table 8) |
| I5  | ParTpSelect  | (even) parity of register <i>TpSelect</i> (reg. no. 22, cf. table 8) |
| S0  | LSB of register <i>SEUcounter</i> (reg. no. 23, cf. table 8)   |  |
| S1  | bit 1 of register <i>SEUcounter</i> (reg. no. 23, cf. table 8) |  |
| P0  | LSB of pipeline column number                                  |  |
| P1  | bit 1 of pipeline column number                                |  |
| P2  | bit 2 of pipeline column number                                |  |
| P3  | bit 3 of pipeline column number                                |  |
| P4  | bit 4 of pipeline column number                                |  |
| P5  | bit 5 of pipeline column number                                |  |
| P6  | bit 6 of pipeline column number                                |  |
| P7  | MSB of pipeline column number                                  |  |

<sup>4</sup>The specification of the readout time assumes  $Rclk = Sclk = 40 \text{ MHz}$ .

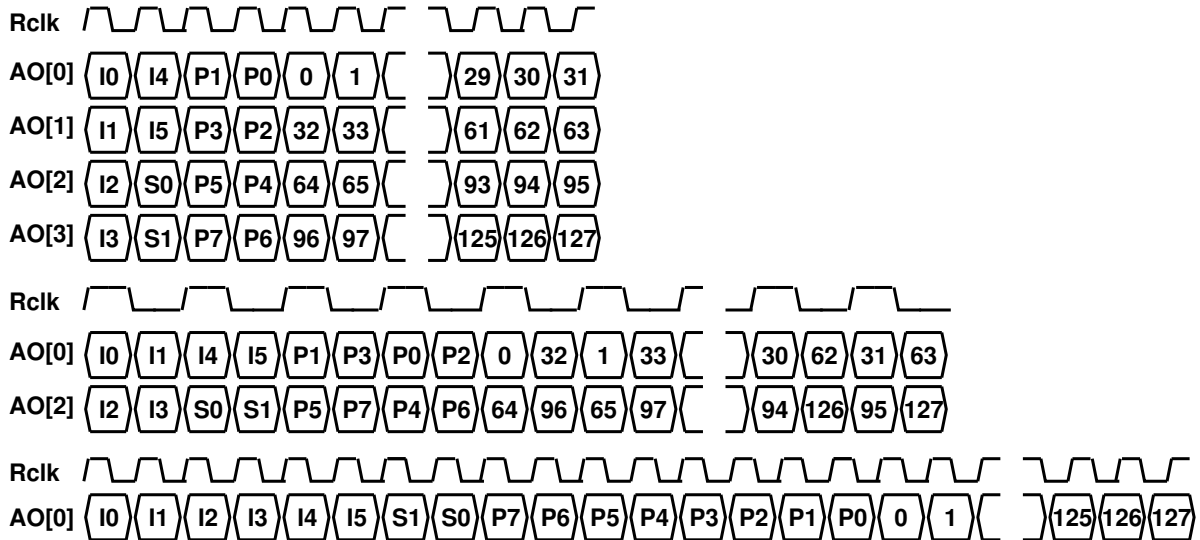


Figure 7: *Beetle1.2* readout data formats. From top to bottom: Analog readout mode: 32 analog channels are multiplexed onto 4 ports with up to 40 MHz. Binary readout mode: 64 binary channels are multiplexed onto 2 ports with up to 80 MHz. Readout mode for less demanding readout speed requirements: 128 analog channels are multiplexed onto 1 port with up to 40 MHz.

### 3.5 Internal Test Pulses

Test pulses can be injected into the preamplifier with an on-chip generator. A step like pattern corresponding to +2, +1, -1 and -2 times a reference signal amplitude is coupled modulo 4 to the 128 channels (table 4). The amplitude of the reference pulse can be adjusted with the *Itp* bias register (cf. table 8). A test pulse is triggered via the *Testpulse* port (pad no. 176, 177) and can be enabled per channel by the *TpSelect* register (cf. 4.2). Fig. 8 shows the correlation between the *Testpulse* port and the internal test pulse trigger.

Table 4: Mapping of test pulse amplitudes to analog channels.

| Channel no.            | 0  | 1  | 2  | 3  | ... | 124 | 125 | 126 | 127 |
|------------------------|----|----|----|----|-----|-----|-----|-----|-----|
| Test pulse step height | +2 | +1 | -1 | -2 | ... | +2  | +1  | -1  | -2  |

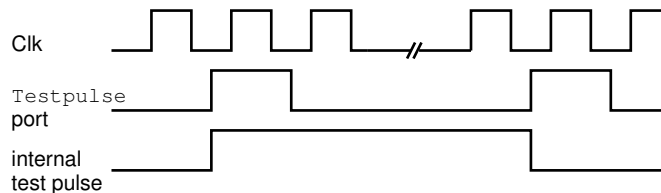


Figure 8: Test pulse triggering.

## 3.6 Comparator Operation

The comparator circuit consists of an integrator, a threshold generator and a discriminator. The integrator extracts the DC-offset of the shaped pulse with a variable time constant between 1 and  $20\ \mu\text{s}$ , which can be adjusted via the *Vrc* register (cf. table 8). The DC-offset varies from channel to channel and is added to the threshold voltage. The threshold level is adjustable per channel with a resolution of 3 bits. The comparator output is latched with the comparator clock (*CompClk*, pad no. 143, 144) before feeding it to the pipeline resp. the comparator LVDS output drivers (cf. fig. 1). For operating the comparator it is mandatory to assert the *CompClk*. It is different from the sampling clock *Sclk* to enable the freedom of a phase between *Sclk* and *CompClk*.

### 3.6.1 Comparator Configuration

The comparator is configured via the register *CompControl* (cf. table 8 and table 10). *PipelineMode* defines the mode of operation of the comparator. *PipelineMode* = 0 selects the analog mode, in which the output of the front-end amplifier is transferred to the pipeline. In binary mode (*PipelineMode* = 1) the comparator output is fed into the pipeline. *CompDisable* = 1 turns off the comparator's bias current. *CompPolarity* selects between an inverting (0) or non-inverting (1) comparator operation. *CompMode* switches between two different kinds of output signal. With *CompMode* = 0 the output is active as long as the comparator input signal is above the threshold level. With *CompMode* = 1 the output is only one *CompClk* cycle active, independent of the time, that the input signal is above the threshold.

### 3.6.2 Threshold Adjustment

The threshold level is generated from two programmable currents. *Ithmain* (register address 8) determines the global threshold, which is common to all channels. *Ithdelta* (register address 7) defines an additional delta threshold.

The comparator threshold register (*CompChTh*, address 20) selects the number of delta thresholds which are being added to the global threshold. This register is operated as a shift register. The bits *CompChTh*[2:0] are being assigned to channel *k*, the bits *CompChTh*[6:4] to channel *k+1*. To define the delta threshold of all channels, the *CompChTh* register has to be programmed 64 times consecutively. A shift mechanism provides the bits to the channels in the order (Ch[0], Ch[1]), (Ch[2], Ch[3]), ..., (Ch[126], Ch[127]).

### 3.6.3 Comparator Channel Mapping

The comparator outputs are LVDS drivers. Each driver sends data of two combined comparator groups, the first group of ORed channels during the high phase of *CompClock*, the second during the low phase. The mapping of the channels to the comparator outputs is shown in table 5.

## 3.7 Timing Specifications

**Reset, Trigger, Test pulse** The timing relation between *Reset* and *Trigger* in order to trigger on pipeline column number *n* can be depicted from fig. 9, whereas  $n = k$  modulo 187. *k* must be equal or greater than 1, *Latency* refers to the content of the Latency register (no. 16).

Figure 10 depicts the timing relation between *Testpulse* and *Trigger*. *Latency* refers again to the content of the Latency register.

**Readout Timing** The *Beetle* chip has two different possible readout timings called *non-consecutive* and *consecutive* readout. A non-consecutive readout starts after a trigger occurs during a non-readout. If the *Beetle* receives a second trigger before a last readout is completed, the next readout is send as a consecutive readout.

Table 5: Mapping of analog input channels to comparator output channels on *Beetle1.2*.

| Output port | High phase of CompClock         | Low phase of CompClock          |
|-------------|---------------------------------|---------------------------------|
| CompOut[15] | Ch[127]∨Ch[126]∨Ch[125]∨Ch[124] | Ch[123]∨Ch[122]∨Ch[121]∨Ch[120] |
| CompOut[14] | Ch[119]∨Ch[118]∨Ch[117]∨Ch[116] | Ch[115]∨Ch[114]∨Ch[113]∨Ch[112] |
| CompOut[13] | Ch[111]∨Ch[110]∨Ch[109]∨Ch[108] | Ch[107]∨Ch[106]∨Ch[105]∨Ch[104] |
| CompOut[12] | Ch[103]∨Ch[102]∨Ch[101]∨Ch[100] | Ch[99]∨Ch[98]∨Ch[97]∨Ch[96]     |
| CompOut[11] | Ch[95]∨Ch[94]∨Ch[93]∨Ch[92]     | Ch[91]∨Ch[90]∨Ch[89]∨Ch[88]     |
| CompOut[10] | Ch[87]∨Ch[86]∨Ch[85]∨Ch[84]     | Ch[83]∨Ch[82]∨Ch[81]∨Ch[80]     |
| CompOut[9]  | Ch[79]∨Ch[78]∨Ch[77]∨Ch[76]     | Ch[75]∨Ch[74]∨Ch[73]∨Ch[72]     |
| CompOut[8]  | Ch[71]∨Ch[70]∨Ch[69]∨Ch[68]     | Ch[67]∨Ch[66]∨Ch[65]∨Ch[64]     |
| CompOut[7]  | Ch[63]∨Ch[62]∨Ch[61]∨Ch[60]     | Ch[59]∨Ch[58]∨Ch[57]∨Ch[56]     |
| CompOut[6]  | Ch[55]∨Ch[54]∨Ch[53]∨Ch[52]     | Ch[51]∨Ch[50]∨Ch[49]∨Ch[48]     |
| CompOut[5]  | Ch[47]∨Ch[46]∨Ch[45]∨Ch[44]     | Ch[43]∨Ch[42]∨Ch[41]∨Ch[40]     |
| CompOut[4]  | Ch[39]∨Ch[38]∨Ch[37]∨Ch[36]     | Ch[35]∨Ch[34]∨Ch[33]∨Ch[32]     |
| CompOut[3]  | Ch[31]∨Ch[30]∨Ch[29]∨Ch[28]     | Ch[27]∨Ch[26]∨Ch[25]∨Ch[24]     |
| CompOut[2]  | Ch[23]∨Ch[22]∨Ch[21]∨Ch[20]     | Ch[19]∨Ch[18]∨Ch[17]∨Ch[16]     |
| CompOut[1]  | Ch[15]∨Ch[14]∨Ch[13]∨Ch[12]     | Ch[11]∨Ch[10]∨Ch[9]∨Ch[8]       |
| CompOut[0]  | Ch[7]∨Ch[6]∨Ch[5]∨Ch[4]         | Ch[3]∨Ch[2]∨Ch[1]∨Ch[0]         |

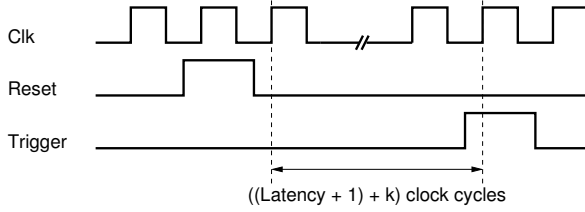


Figure 9: Timing relation between *Reset* and *Trigger* in order to trigger on column no.  $k$ . *Latency* refers to the content of the latency register.

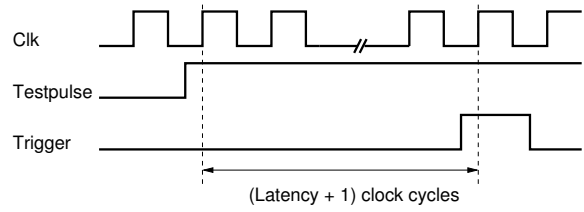


Figure 10: Timing relation between *Testpulse* and *Trigger*. *Latency* refers to the content of the latency register.

Figure 11 describe the readout timing of *Trigger*, *DataValid* and *AnalogOut* of the analog readout mode on 4 ports. The upper plot shows a single readout burst (non-consecutive readout), the lower the case of a consecutive readout.

### 3.8 Diagnostic Signals

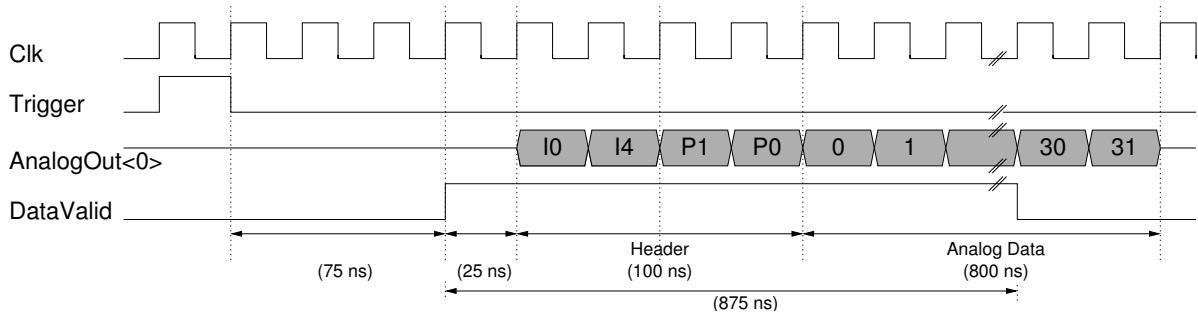
The *Beetle* chip provides several digital signals for monitoring or diagnostics purposes which are explained briefly in table 6.

*WriteMon* and *TrigMon* allow to check the physical latency of the chip. They are pulses with a width of one sampling clock cycle and a period of 187 cycles. Their relative distance is  $(Latency + 1)$  clock cycles.

### 3.9 Daisy Chain

The daisy chain allows several chips to share one, two or four output lines. It consists of two signal paths, a *token* and a *return token* path. They are built up by connecting the *RoTokenOut* (*RoReTokenIn*) pad of one chip with the *RoTokenIn* (*RoReTokenOut*) of the neighbouring chip (see fig. 12). The chip position in the chain has to be configured in the *ROCtrl* register (bits 3 and 4). A chip can be the first (*DaisyFirst* = 1), an intermediate or the last (*DaisyLast* = 1) in the daisy chain.

### Single Readout



### Consecutive Readout

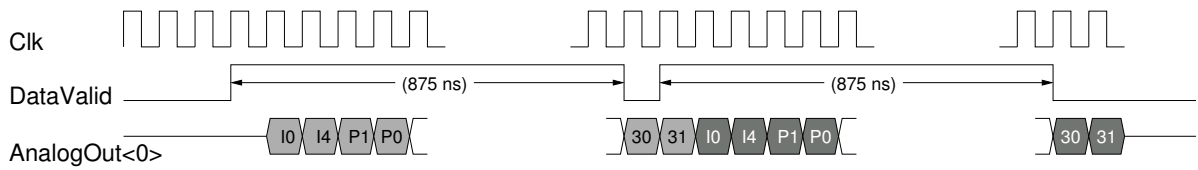


Figure 11: Readout timing schemes of the analog readout mode on 4 ports. Only channel 0 is depicted. The upper plot shows a single readout burst, the lower the case of consecutive readout.

Table 6: Digital signals for monitoring or diagnostics purposes. All signals are active-high.

| signal name | pad no.  | description  |
|-------------|----------|--|
| DataValid   | 180, 181 | indicates presence of valid data on the <code>AnalogOut</code> ports; see fig. 11 for timing specifications                  |
| FifoFull    | 163      | indicates full derandomising trigger buffer; with 15 occupied FIFO entries, the next trigger activates <code>FifoFull</code> |
| TrigMon     | 170      | indicates if pipeline trigger pointer passes column number 0   |
| WriteMon    | 171      | indicates if pipeline write pointer passes column number 0   |

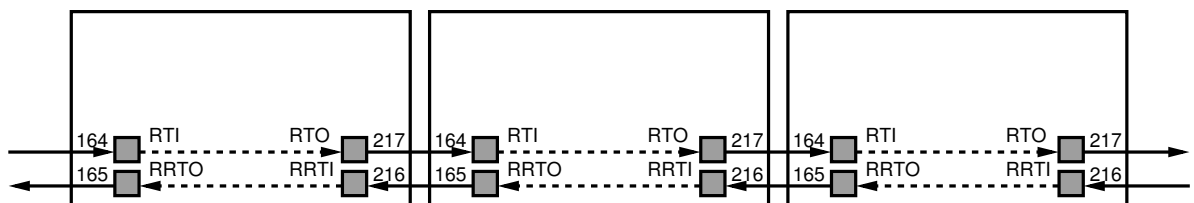


Figure 12: Daisy chain composition. The figures indicate the pad reference numbers (RTI = RoTokenIn, RRTO = RoReTokenOut, RTO = RoTokenOut, RRTI = RoReTokenIn).

## 4 Slow Control

### 4.1 I<sup>2</sup>C-Interface

The chip's slow control interface is a standard mode I<sup>2</sup>C-slave device featuring a transfer rate of 100 kbit/s. The chip address, necessary to access a single device via the I<sup>2</sup>C-bus, is 7 bits wide and assigned via the address pads `I2CAAddr[6:0]` (cf. section A.3). The *Beetle* chip responds to addresses in the range 8 – 119. The addresses 0000XXX and 1111XXX are reserved in the I<sup>2</sup>C-standard for other purposes [8].

The internal registers are being accessed via a *pointer register*. This contains the address of the register to be written or read first. The pointer is internally incremented by 1 after each transferred data frame. In this way registers with adjacent addresses can be accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position. Fig. 13 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode the chip address is transmitted after initialising the transfer, followed by the pointer byte and the data. After the transmission of one data frame, the pointer addresses the successive register because of its auto-incrementing function. The registers with addresses 20 – 23 have an exceptional status. The registers 20 – 22 are implemented as 128-bit shift-registers (cf. 4.2), register 23 is the output of the SEU counter. A write access to this register resets it to 0. Hence, the auto-incrementing of the address pointer is only performed for addresses  $\leq 19$ . To access the addresses 20 – 23 the corresponding register has to be addressed directly.

The transfer of the pointer byte is obligatory in write mode. In read mode there are two versions:

- **Preset pointer**  
After initialising the transfer and sending the chip address data is immediately read out. The pointer has been set in a previous transfer.
- **Pointer set followed by immediate read-out**  
After initialising the transfer and sending the chip address the pointer byte is transferred. The I<sup>2</sup>C-bus is re-initialised, the chip address is sent and data is read out.

Commercially available I<sup>2</sup>C-devices usually operate at 3.3 V or 5 V. To interconnect these devices with a *Beetle* I<sup>2</sup>C-interface a bidirectional level shifter is necessary. A simple solution to this problem is the use of a discrete MOSFET for each bus line [9]. Fig. 14 illustrates the level shifter circuit. An example for a single MOSFET device is type BSN20 from Philips Semiconductors.

### 4.2 Bias and Configuration Registers

*Beetle1.2* contains 24 8-bit registers with the addresses 0 – 23. Table 8 lists all registers with physical range, resolution and nominal setting. Registers 0 – 15 are bias registers for the analog stages.

**Pipeamp reset potential:  $V_d$**  Register 11 determines the potential to which the pipeamp is reset. This voltage should correspond to the DC output level of the front-end and is therefore depending on *Isha* and *Ibuf* (cf. 3.1).

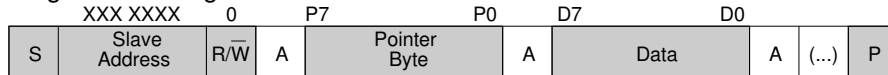
**Pipeamp reference potential:  $V_{dcl}$**  Register 12 adjusts the potential of the non-inverting input of the pipeamp.

**Latency** Register 16 defines the latency which has to be  $\geq 10$  and  $\leq 160$  for reliable chip operation.  
 $\leadsto$  A change of the latency register will only have an effect after applying a reset.



## Write mode

### Single addressing

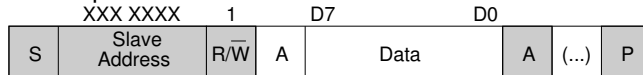


### General call addressing



## Read mode

### Preset pointer



### Pointer set followed by immediate readout

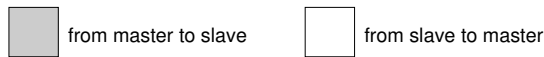
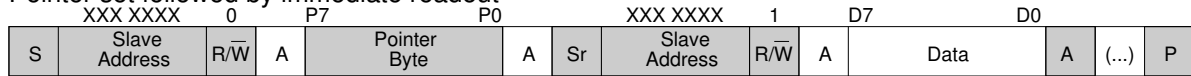


Figure 13: I<sup>2</sup>C-bus write and read sequences for accessing registers on the *Beetle*.

**Rclk divider: *RclkDiv*** Register 18 defines the ratio between the readout clock *Rclk* and the sampling clock *Sclk*. The ratio  $\nu_{Rclk}/\nu_{Sclk}$  is  $1/(RclkDiv+1)$  and allows *Rclk* frequencies from 40 MHz down to  $\approx 156$  kHz.  $RclkDiv = 0$  means, that *Sclk* and *Rclk* have the same frequency.

↪ A change of the *RclkDiv* register requires a succeeding reset for proper chip operation.

**Mode of operation: *ROCtrl*, *CompCtrl*** The registers 17 and 19 select the chip's mode of operation (readout mode, daisy chain configuration) and define the comparator configuration. Tables 9 and 10 show the detailed bit assignment of the registers *ROControl* and *CompControl*. Note, that the three *ModeSelect* bits are exclusive, i.e. only one bit is allowed to be set.

↪ A change of the *ROCtrl* register requires a succeeding reset for proper chip operation.

**Shift registers** Registers 20 – 22 (*CompChTh*, *CompMask*, *TpSelect*) are operated as shift-registers: *CompMask* and *TpSelect* form a 128-bit register each, segmented in 16 8-bit registers, *CompChTh* establishes a 512 (=  $128 \times 4$ ) bit register divided into 64 8-bit registers, whereas only 6 of the 8 bits per frame are assigned (cf. section 3.6.2). A consecutive write-access to the corresponding register address shifts the data in 8-bit frames starting from the largest channel number (see table 7). A read access to such a register returns the bits corresponding to channels 7 – 0 in case of *CompMask* and *TpSelect* and 1 – 0 in case of *CompChTh*. This allows a verification of the shifted data.

↪ Note, that write access to the shift registers is prohibited during readout operation.

**SEU counter** Register 23 is the output of the SEU counter (cf. 4.3). A write access to this register resets the content to 0. Note, that the two LSB of the register *SEUcounts* are transmitted in the header (*S*[1:0]) of the analog output stream (cf. 3.4).

<sup>5</sup>see section 6

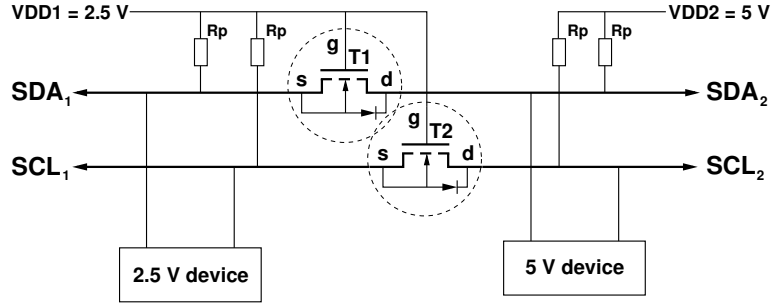


Figure 14: Bidirectional level shifter circuit to connect two different voltage level sections of an I<sup>2</sup>C-bus system. An example for a single MOSFET device is type BSN20 from Philips Semiconductors.

Table 7: Channel sequence for write and read access to the shift registers *CompMask*, *TpSelect* and *CompChTh*.

|                 | Write access                  | Read access |
|-----------------|-------------------------------|-------------|
| <i>CompMask</i> | Ch[127:120], Ch[119:112], ... | Ch[7:0]     |
| <i>TpSelect</i> | Ch[127:120], Ch[119:112], ... | Ch[7:0]     |
| <i>CompChTh</i> | Ch[127:126], Ch[125:124], ... | Ch[1:0]     |

### 4.3 Single Event Upset Robustness

*Beetle1.2* continuously uses triple-redundant logic in order to assure the robustness against Single Event Upset (SEU), i.e. the change of the state of a memory device induced by a single particle. A logic bit is represented by the majority of the outputs of three flip-flops. The flip-flops on *Beetle1.2* can be categorised into two groups:

**Clocked flip-flops** They are used in the control logic which operates with the sampling clock frequency of 40 MHz in case of the *Fast Control* and the I<sup>2</sup>C-clock of 100 kHz in case of the *Slow Control*.

**Static flip-flops** They form the bias and configuration registers. These flip-flops use triple-redundant majority voting in combination with a self-triggered correction mechanism. A single SEU per bit will be corrected.

An 8-bit counter is integrated in *Beetle1.2* to indicate the number of single event upsets in the bias and configuration registers. All registers, including the shift-registers *CompChTh*, *CompMask* and *TpSelect*, can increment the SEU counter. The bits used in the logic control circuits (clocked flip-flops) are *not* taken into account. The counter output is readable via the I<sup>2</sup>C-bus (cf. 4.2). The two least significant bits are additionally transferred in the header of the analog output stream (fig. 7, table 3). This allows a fast monitoring of SEUs during readout. An I<sup>2</sup>C-write access to the counter register resets it.

Table 8: Bias and configuration registers of *Beetle1.2*.

| Reg. no. | Reg. Name        | Class | Range                | Res.      | Nominal Setting |              | Description  |
|----------|------------------|-------|----------------------|-----------|-----------------|--------------|--|
|          |                  |       |                      |           | Value           | Reg. content |  |
| 0        | <i>Itp</i>       | I     | 0 – 2 mA             | 8 $\mu$ A | 0 $\mu$ A       | 0x00         | test pulse bias current                                    |
| 1        | <i>Ipre</i>      | I     | 0 – 2 mA             | 8 $\mu$ A | 600 $\mu$ A     | 0x4C         | preamplifier bias current                                  |
| 2        | <i>Isha</i>      | I     | 0 – 2 mA             | 8 $\mu$ A | 80 $\mu$ A      | 0x0A         | shaper bias current  |
| 3        | <i>Ibuf</i>      | I     | 0 – 2 mA             | 8 $\mu$ A | 80 $\mu$ A      | 0x0A         | front-end buffer bias current                              |
| 4        | <i>Vfp</i>       | V     | 0 – 2.5 V            | 9.8 mV    | 0 V             | 0x00         | preamplifier feedback voltage                              |
| 5        | <i>Vfs</i>       | V     | 0 – 2.5 V            | 9.8 mV    | 0 V             | 0x00         | shaper feedback voltage                                    |
| 6        | <i>Icomp</i>     | I     | 0 – 2 mA             | 8 $\mu$ A | 40 $\mu$ A      | 0x05         | comparator bias current                                    |
| 7        | <i>Ithdelta</i>  | I     | 0 – 2 mA             | 8 $\mu$ A | —               | —            | current defining incremental comparator threshold          |
| 8        | <i>Ithmain</i>   | I     | 0 – 2 mA             | 8 $\mu$ A | —               | —            | current defining common comparator threshold               |
| 9        | <i>Vrc</i>       | V     | 0 – 1.25 V           | 4.9 mV    | 0 V             | 0x00         | comparator RC time constant                                |
| 10       | <i>Ipipe</i>     | I     | 0 – 2 mA             | 8 $\mu$ A | 100 $\mu$ A     | 0x0D         | pipeamp bias current                                       |
| 11       | <i>Vd</i>        | V     | 0 – 2.5 V            | 9.8 mV    | 1 V             | 0x66         | pipeamp reset potential                                    |
| 12       | <i>Vdcl</i>      | V     | 0 – 2.5 V            | 9.8 mV    | 1.1 V           | 0x70         | pipeamp reference voltage                                  |
| 13       | <i>Ivltbuf</i>   | I     | 0 – 2 mA             | 8 $\mu$ A | 200 $\mu$ A     | 0x1A         | pipeamp buffer bias current                                |
| 14       | <i>Isf</i>       | I     | 0 – 2 mA             | 8 $\mu$ A | 200 $\mu$ A     | 0x1A         | multiplexer buffer bias current                            |
| 15       | <i>Icurrbuf</i>  | I     | 0 – 2 mA             | 8 $\mu$ A | 200 $\mu$ A     | 0x1A         | output buffer bias current                                 |
| 16       | <i>Latency</i>   | Dig.  | 10 – 160             | —         | 160             | 0xA0         | trigger latency  |
| 17       | <i>ROCtrl</i>    | Dig.  | —                    | —         | cf. table 9     |              | readout control  |
| 18       | <i>RclkDiv</i>   | Dig.  | 0 – 255 <sup>5</sup> | —         | 0               | 0x00         | ratio between Rclk and Sclk                                |
| 19       | <i>CompCtrl</i>  | Dig.  | —                    | —         | cf. table 10    |              | comparator control   |
| 20       | <i>CompChTh</i>  | Dig.  | 0 – 7                | —         | —               | —            | comparator channel threshold shift register implementation |
| 21       | <i>CompMask</i>  | Dig.  | —                    | —         | 0               | 0x00         | comparator mask shift register implementation              |
| 22       | <i>TpSelect</i>  | Dig.  | —                    | —         | 0               | 0x00         | testpulse selection shift register implementation          |
| 23       | <i>SEUcounts</i> | Dig.  | 0 – 255              | —         | —               | —            | sum of single event upsets                                 |

Table 9: Bit assignment of the configuration register *ROCtrl*. All switches are active-high. 1 enables the switch, 0 disables it.

| Bit | Function        | Description   |
|-----|-----------------|---|
| 0   | BinRO2          | binary readout on 2 ports   |
| 1   | AnaRO1          | analog readout on 1 port  |
| 2   | AnaRO4          | analog readout on 4 ports   |
| 3   | DaisyFirst      | first chip in daisy chain   |
| 4   | DaisyLast       | last chip in daisy chain  |
| 5   | LVDSmode        | LVDS mode of current driver   |
| 6   | <i>not used</i> | —   |
| 7   | ProbeEnable     | enables probe pads <b>ProbeVrefFE</b> (pad no. 138), <b>ProbeVrefBE</b> (pad no. 219) |

Table 10: Bit assignment of the configuration register *CompCtrl*.

| Bit | Function        | Description   |
|-----|-----------------|---|
| 0   | EnableCompLVDS  | 0: disable comparator LVDS output ports<br>1: enable comparator LVDS output ports |
| 1   | CompPolarity    | 0: inverting<br>1: non-inverting  |
| 2   | PipelineMode    | 1: binary readout<br>0: analog readout  |
| 3   | CompDisable     | 0: enable comparator<br>1: disable comparator                                     |
| 4   | CompMode        | 0: track mode<br>1: pulse mode  |
| 5   | <i>not used</i> | —   |
| 6   | <i>not used</i> | —   |
| 7   | <i>not used</i> | —   |

## 5 How to get the *Beetle* chip working

This section describes important steps to get the *Beetle* chip working. Some may be trivial, but ignoring them can cause lengthy trouble in running the chip.

### Power and Blocking

- Power the chip:
  - for analog operation:
    - connect to Vdd: pad no.: 1, 3 – 5, 140, 166 – 167, 206 – 210, 243
    - connect to Gnd: pad no.: 134 – 137, 139, 168 – 169, 201 – 205, 244
  - for binary operation connect *additionally* to the above listed pads:
    - to Vdd: pad no.: 141, 161, 224, 242
    - to Gnd: pad no.: 142, 162, 223, 241
- Block the following pads with  $\mathcal{O}(100\text{ nF})$  to ground: `Icurrbuf` (pad no. 211), `Isf` (pad no. 212), `Ipipe` (pad no. 213), `Vdc1buf` (pad no. 214), `Vdbuf` (pad no. 215).

### Minimum number of pads to be bonded

The following list specifies the minimum number of *input ports* to be bonded for proper chip operation in addition to power and blocking pads:

- `Trigger` (pad no. 172, 173),
- `Clock` (pad no. 174, 175),
- `Reset` (pad no. 178, 179),
- `SDA`, `SCL` (pad no. 189, 190).

Beside the analog output ports `AnalogOut<i>` (pad no. 193 – 200) or the comparator output ports `CompOut<i>` (pad no. 145 – 160, 225 – 240), it is recommended to bond the *digital output pads* listed in table 6.

### LVDS ports

Define the levels of all LVDS input ports, e.g. `Clock`, `Trigger`, `Reset`, `Testpulse`, i.e. do not leave any input pads floating.

### Power-up reset

Connect the `PowerupReset` port (pad no. 191) with  $\mathcal{O}(100\text{ nF})$  to ground.

### I<sup>2</sup>C-bus

- Define the chip ID via the pads `I2CAddr[6:0]` for individual chip access, or use general call mode. The chip responds to addresses in the range 8 – 119.
- Assure, that different chips sharing one I<sup>2</sup>C-bus line have unique addresses.
- Assure, that the `Reset` port has a defined logic level and does not change while programming the chip via I<sup>2</sup>C-bus.
- For the bidirectional transfer on the SDA-line it is important, that the chip operates not below 2.5 V. Assure, that the positive supply voltage *at the place of the chip* is 2.5 V or more.

## Fast Control

- Define the chip as *DaisyFirst* as well as *DaisyLast* (*ROCtrl* register is XXX11XXX).
- A change of the content of the *Latency* register (register ID 16) is taken over by the logic circuitry only after applying an external reset via the **Reset** port. To check the *physical* latency, determine the time distance of the **WriteMon** (pad no. 171) and **TrigMon** (pad no. 170) signals, which is  $Latency + 1$ .  
 $\leadsto$  *Latency* has to be in the range 10 – 160 for proper chip operation.
- Connect the port **RoReTokenIn** of the last chip in a daisy chain (*DaisyLast*) to ground for proper chip operation (cf. section 6).

## Comparators

For comparator operation it is mandatory to assert the comparator clock *CompClk* (pad no. 143: **notCompClock**, pad no. 144: **CompClock**). It is different from the sampling clock *Sclk* to enable the freedom of a phase between *Sclk* and *CompClk*.

## 6 Known Problems and Limitations

### Problem Behaviour at consecutive readout

For consecutive readout, i.e. asserting a trigger during the readout of the previous event, the *Beetle1.2* chip shows two effects: a carry-over of roughly 30% of the signal amplitude of the previous readout frame accompanied by a change in the signal polarity, and a strong variation of the baseline for higher channel numbers. Fig. 15 depicts the readout behaviour for consecutive (left) and non-consecutive (right) readout. Two data frames are acquired each, whereas only the first one comprises real input signals while no input data has been provided to the second trigger.

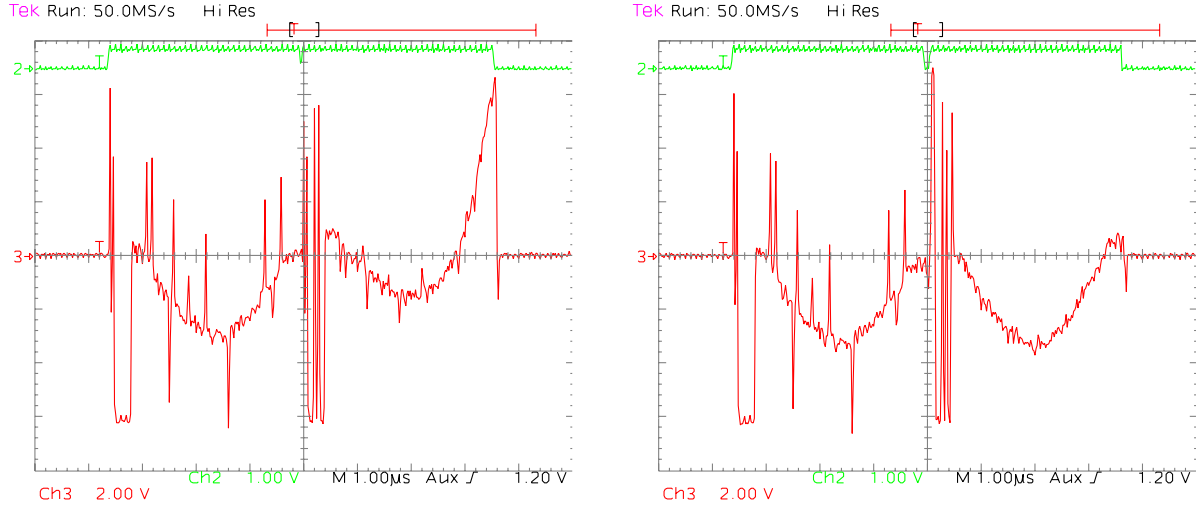


Figure 15: Readout behaviour for consecutive (left) and non-consecutive (right) triggers with internal test pulses applied.

### Problem Channel dependence of front-end pulse remainder $R$ and peaking time $t_p$

**Limitation** The last chip in a daisy chain (*DaisyLast*) is sensitive to external signals on the return token port: pad `RoReTokenIn` needs to be grounded for proper chip operation for the last chip in the chain.

### Limitation Restricted $Rclk$ frequency

The division factor between  $Rclk$  and  $Sclk$  ( $CR = \nu_{Sclk}/\nu_{Rclk}$ ) is restricted to  $\leq 2$ .

### Limitation Variation of the readout baseline

The U-shaped baseline variation (cf. fig. 15, right) shows a strong bias setting dependence (mainly of  $I_{sha}$ ,  $I_{pipe}$ ,  $V_d$ ,  $V_{dcl}$ ). For  $I_{sha} = 80 \mu A$ ,  $I_{pipe} = 100 \mu A$ ,  $V_d = 1 V$  and  $V_{dcl} = 1.1 V$ , the amplitude of the variation is approximately  $22,000 e^-$ .

Beside a fix of the above mentioned items, a further chip version will integrate 5 V compatible  $I^2C$ -pads, which will render superfluous any external (radiation hard) level shifting devices.

## A Pad Description

A reference number has been assigned to each pad. The numbering starts in the upper left corner of the die (with the analog input pads left) and runs counter-clockwise (cf. fig. 16). The following tables summarise the signals and explain them. The pad coordinates refer to the lower left corner of the pad opening, which is  $120\ \mu\text{m} \times 95\ \mu\text{m}$  in case of the front pads and  $95\ \mu\text{m} \times 95\ \mu\text{m}$  for all others. The origin of the coordinate system is defined by the lower left chip corner (0,0). The dimensions of the chip die are  $5,100\ \mu\text{m} \times 6,100\ \mu\text{m}$ <sup>6</sup>. The analog input pads have a pitch of  $40.24\ \mu\text{m}$ , all others  $115\ \mu\text{m}$ .

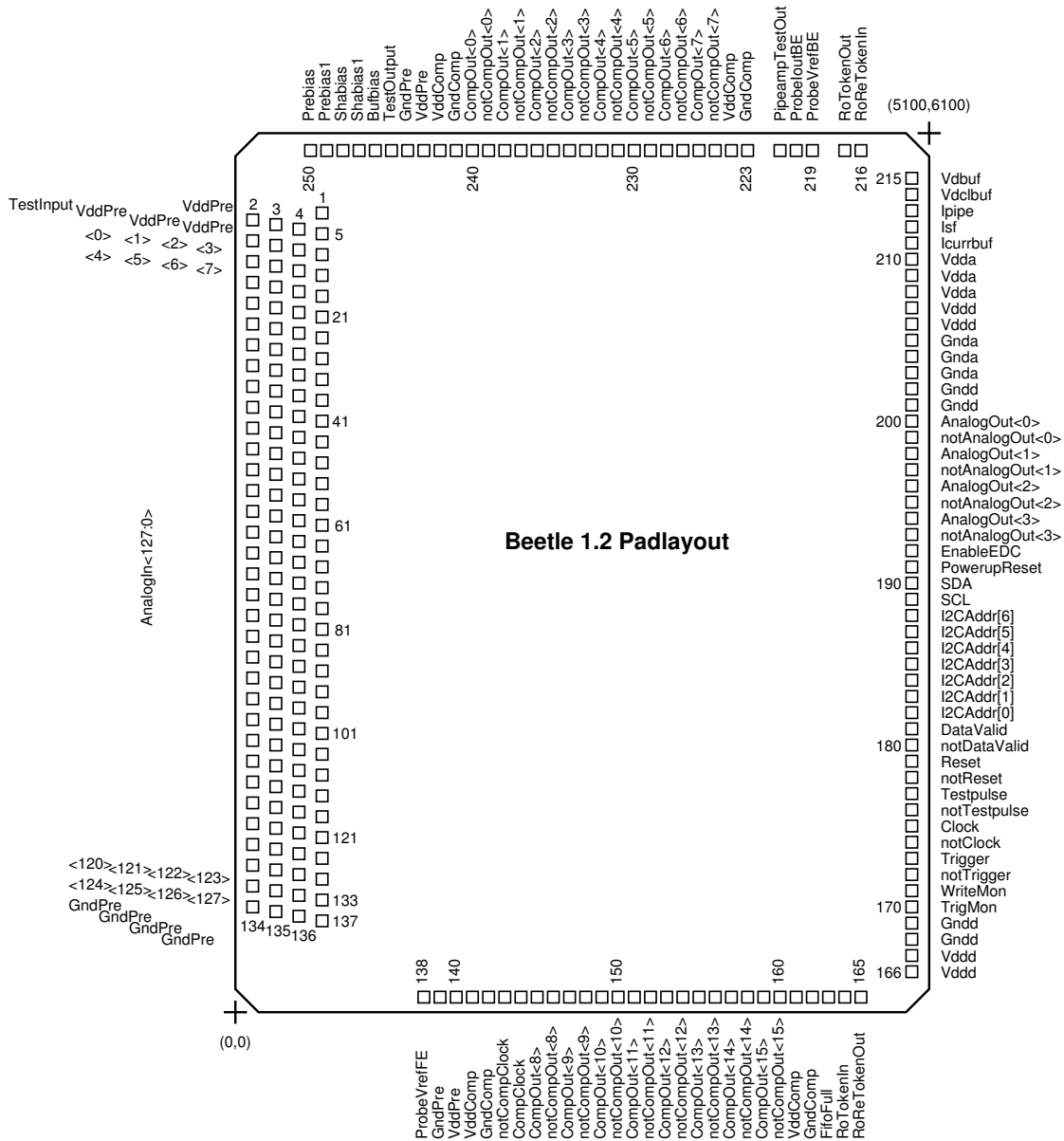


Figure 16: Pad layout of *Beetle1.2*. The die size is  $(5.1 \times 6.1)\ \text{mm}^2$ .

<sup>6</sup>Note, that this are the dimensions of the chip's scribe line, i.e. not including cutting margins. They could add some  $100\ \mu\text{m}$  to the chip dimensions.



## A.1 Front Pads

| Ref. no. | Pin name     | Coordinates         |                     | Type        | Description                  |
|----------|--------------|---------------------|---------------------|-------------|------------------------------|
|          |              | x [ $\mu\text{m}$ ] | y [ $\mu\text{m}$ ] |             |                              |
| 1        | VddPre       | 490.00              | 5836.30             | power input | positive preamplifier supply |
| 2        | TestInput    | 25.00               | 5796.06             | input       | input of test channel        |
| 3        | VddPre       | 180.00              | 5755.82             | power input | positive preamplifier supply |
| 4        | VddPre       | 335.00              | 5715.58             | power input | positive preamplifier supply |
| 5        | VddPre       | 490.00              | 5675.34             | power input | positive preamplifier supply |
| 6        | AnalogIn[0]  | 25.00               | 5635.10             | input       | input of channel 0           |
| 7        | AnalogIn[1]  | 180.00              | 5594.86             | input       | input of channel 1           |
| 8        | AnalogIn[2]  | 335.00              | 5554.62             | input       | input of channel 2           |
| 9        | AnalogIn[3]  | 490.00              | 5514.38             | input       | input of channel 3           |
| 10       | AnalogIn[4]  | 25.00               | 5474.14             | input       | input of channel 4           |
| 11       | AnalogIn[5]  | 180.00              | 5433.90             | input       | input of channel 5           |
| 12       | AnalogIn[6]  | 335.00              | 5393.66             | input       | input of channel 6           |
| 13       | AnalogIn[7]  | 490.00              | 5353.42             | input       | input of channel 7           |
| 14       | AnalogIn[8]  | 25.00               | 5313.18             | input       | input of channel 8           |
| 15       | AnalogIn[9]  | 180.00              | 5272.94             | input       | input of channel 9           |
| 16       | AnalogIn[10] | 335.00              | 5232.70             | input       | input of channel 10          |
| 17       | AnalogIn[11] | 490.00              | 5192.46             | input       | input of channel 11          |
| 18       | AnalogIn[12] | 25.00               | 5152.22             | input       | input of channel 12          |
| 19       | AnalogIn[13] | 180.00              | 5111.98             | input       | input of channel 13          |
| 20       | AnalogIn[14] | 335.00              | 5071.74             | input       | input of channel 14          |
| 21       | AnalogIn[15] | 490.00              | 5031.50             | input       | input of channel 15          |
| 22       | AnalogIn[16] | 25.00               | 4991.26             | input       | input of channel 16          |
| 23       | AnalogIn[17] | 180.00              | 4951.02             | input       | input of channel 17          |
| 24       | AnalogIn[18] | 335.00              | 4910.78             | input       | input of channel 18          |
| 25       | AnalogIn[19] | 490.00              | 4870.54             | input       | input of channel 19          |
| 26       | AnalogIn[20] | 25.00               | 4830.30             | input       | input of channel 20          |
| 27       | AnalogIn[21] | 180.00              | 4790.06             | input       | input of channel 21          |
| 28       | AnalogIn[22] | 335.00              | 4749.82             | input       | input of channel 22          |
| 29       | AnalogIn[23] | 490.00              | 4709.58             | input       | input of channel 23          |
| 30       | AnalogIn[24] | 25.00               | 4669.34             | input       | input of channel 24          |
| 31       | AnalogIn[25] | 180.00              | 4629.10             | input       | input of channel 25          |
| 32       | AnalogIn[26] | 335.00              | 4588.86             | input       | input of channel 26          |
| 33       | AnalogIn[27] | 490.00              | 4548.62             | input       | input of channel 27          |
| 34       | AnalogIn[28] | 25.00               | 4508.38             | input       | input of channel 28          |
| 35       | AnalogIn[29] | 180.00              | 4468.14             | input       | input of channel 29          |
| 36       | AnalogIn[30] | 335.00              | 4427.90             | input       | input of channel 30          |
| 37       | AnalogIn[31] | 490.00              | 4387.66             | input       | input of channel 31          |
| 38       | AnalogIn[32] | 25.00               | 4347.42             | input       | input of channel 32          |
| 39       | AnalogIn[33] | 180.00              | 4307.18             | input       | input of channel 33          |
| 40       | AnalogIn[34] | 335.00              | 4266.94             | input       | input of channel 34          |
| 41       | AnalogIn[35] | 490.00              | 4226.70             | input       | input of channel 35          |
| 42       | AnalogIn[36] | 25.00               | 4186.46             | input       | input of channel 36          |
| 43       | AnalogIn[37] | 180.00              | 4146.22             | input       | input of channel 37          |
| 44       | AnalogIn[38] | 335.00              | 4105.98             | input       | input of channel 38          |
| 45       | AnalogIn[39] | 490.00              | 4065.74             | input       | input of channel 39          |
| 46       | AnalogIn[40] | 25.00               | 4025.50             | input       | input of channel 40          |
| 47       | AnalogIn[41] | 180.00              | 3985.26             | input       | input of channel 41          |
| 48       | AnalogIn[42] | 335.00              | 3945.02             | input       | input of channel 42          |
| 49       | AnalogIn[43] | 490.00              | 3904.78             | input       | input of channel 43          |
| 50       | AnalogIn[44] | 25.00               | 3864.54             | input       | input of channel 44          |
| 51       | AnalogIn[45] | 180.00              | 3824.30             | input       | input of channel 45          |

| Ref. no. | Pin name     | Coordinates         |                     | Type  | Description         |
|----------|--------------|---------------------|---------------------|-------|---------------------|
|          |              | x [ $\mu\text{m}$ ] | y [ $\mu\text{m}$ ] |       |                     |
| 52       | AnalogIn[46] | 335.00              | 3784.06             | input | input of channel 46 |
| 53       | AnalogIn[47] | 490.00              | 3743.82             | input | input of channel 47 |
| 54       | AnalogIn[48] | 25.00               | 3703.58             | input | input of channel 48 |
| 55       | AnalogIn[49] | 180.00              | 3663.34             | input | input of channel 49 |
| 56       | AnalogIn[50] | 335.00              | 3623.10             | input | input of channel 50 |
| 57       | AnalogIn[51] | 490.00              | 3582.86             | input | input of channel 51 |
| 58       | AnalogIn[52] | 25.00               | 3542.62             | input | input of channel 52 |
| 59       | AnalogIn[53] | 180.00              | 3502.38             | input | input of channel 53 |
| 60       | AnalogIn[54] | 335.00              | 3462.14             | input | input of channel 54 |
| 61       | AnalogIn[55] | 490.00              | 3421.90             | input | input of channel 55 |
| 62       | AnalogIn[56] | 25.00               | 3381.66             | input | input of channel 56 |
| 63       | AnalogIn[57] | 180.00              | 3341.42             | input | input of channel 57 |
| 64       | AnalogIn[58] | 335.00              | 3301.18             | input | input of channel 58 |
| 65       | AnalogIn[59] | 490.00              | 3260.94             | input | input of channel 59 |
| 66       | AnalogIn[60] | 25.00               | 3220.70             | input | input of channel 60 |
| 67       | AnalogIn[61] | 180.00              | 3180.46             | input | input of channel 61 |
| 68       | AnalogIn[62] | 335.00              | 3140.22             | input | input of channel 62 |
| 69       | AnalogIn[63] | 490.00              | 3099.98             | input | input of channel 63 |
| 70       | AnalogIn[64] | 25.00               | 3059.74             | input | input of channel 64 |
| 71       | AnalogIn[65] | 180.00              | 3019.50             | input | input of channel 65 |
| 72       | AnalogIn[66] | 335.00              | 2979.26             | input | input of channel 66 |
| 73       | AnalogIn[67] | 490.00              | 2939.02             | input | input of channel 67 |
| 74       | AnalogIn[68] | 25.00               | 2898.78             | input | input of channel 68 |
| 75       | AnalogIn[69] | 180.00              | 2858.54             | input | input of channel 69 |
| 76       | AnalogIn[70] | 335.00              | 2818.30             | input | input of channel 70 |
| 77       | AnalogIn[71] | 490.00              | 2778.06             | input | input of channel 71 |
| 78       | AnalogIn[72] | 25.00               | 2737.82             | input | input of channel 72 |
| 79       | AnalogIn[73] | 180.00              | 2697.58             | input | input of channel 73 |
| 80       | AnalogIn[74] | 335.00              | 2657.34             | input | input of channel 74 |
| 81       | AnalogIn[75] | 490.00              | 2617.10             | input | input of channel 75 |
| 82       | AnalogIn[76] | 25.00               | 2576.86             | input | input of channel 76 |
| 83       | AnalogIn[77] | 180.00              | 2536.62             | input | input of channel 77 |
| 84       | AnalogIn[78] | 335.00              | 2496.38             | input | input of channel 78 |
| 85       | AnalogIn[79] | 490.00              | 2456.14             | input | input of channel 79 |
| 86       | AnalogIn[80] | 25.00               | 2415.90             | input | input of channel 80 |
| 87       | AnalogIn[81] | 180.00              | 2375.66             | input | input of channel 81 |
| 88       | AnalogIn[82] | 335.00              | 2335.42             | input | input of channel 82 |
| 89       | AnalogIn[83] | 490.00              | 2295.18             | input | input of channel 83 |
| 90       | AnalogIn[84] | 25.00               | 2254.94             | input | input of channel 84 |
| 91       | AnalogIn[85] | 180.00              | 2214.70             | input | input of channel 85 |
| 92       | AnalogIn[86] | 335.00              | 2174.46             | input | input of channel 86 |
| 93       | AnalogIn[87] | 490.00              | 2134.22             | input | input of channel 87 |
| 94       | AnalogIn[88] | 25.00               | 2093.98             | input | input of channel 88 |
| 95       | AnalogIn[89] | 180.00              | 2053.74             | input | input of channel 89 |
| 96       | AnalogIn[90] | 335.00              | 2013.50             | input | input of channel 90 |
| 97       | AnalogIn[91] | 490.00              | 1973.26             | input | input of channel 91 |
| 98       | AnalogIn[92] | 25.00               | 1933.02             | input | input of channel 92 |
| 99       | AnalogIn[93] | 180.00              | 1892.78             | input | input of channel 93 |
| 100      | AnalogIn[94] | 335.00              | 1852.54             | input | input of channel 94 |
| 101      | AnalogIn[95] | 490.00              | 1812.30             | input | input of channel 95 |
| 102      | AnalogIn[96] | 25.00               | 1772.06             | input | input of channel 96 |
| 103      | AnalogIn[97] | 180.00              | 1731.82             | input | input of channel 97 |
| 104      | AnalogIn[98] | 335.00              | 1691.58             | input | input of channel 98 |

| Ref. no. | Pin name      | Coordinates         |                     | Type        | Description                                    |
|----------|---------------|---------------------|---------------------|-------------|--|
|          |               | x [ $\mu\text{m}$ ] | y [ $\mu\text{m}$ ] |             |  |
| 105      | AnalogIn[99]  | 490.00              | 1651.34             | input       | input of channel 99                            |
| 106      | AnalogIn[100] | 25.00               | 1611.10             | input       | input of channel 100                           |
| 107      | AnalogIn[101] | 180.00              | 1570.86             | input       | input of channel 101                           |
| 108      | AnalogIn[102] | 335.00              | 1530.62             | input       | input of channel 102                           |
| 109      | AnalogIn[103] | 490.00              | 1490.38             | input       | input of channel 103                           |
| 110      | AnalogIn[104] | 25.00               | 1450.14             | input       | input of channel 104                           |
| 111      | AnalogIn[105] | 180.00              | 1409.90             | input       | input of channel 105                           |
| 112      | AnalogIn[106] | 335.00              | 1369.66             | input       | input of channel 106                           |
| 113      | AnalogIn[107] | 490.00              | 1329.42             | input       | input of channel 107                           |
| 114      | AnalogIn[108] | 25.00               | 1289.18             | input       | input of channel 108                           |
| 115      | AnalogIn[109] | 180.00              | 1248.94             | input       | input of channel 109                           |
| 116      | AnalogIn[110] | 335.00              | 1208.70             | input       | input of channel 110                           |
| 117      | AnalogIn[111] | 490.00              | 1168.46             | input       | input of channel 111                           |
| 118      | AnalogIn[112] | 25.00               | 1128.22             | input       | input of channel 112                           |
| 119      | AnalogIn[113] | 180.00              | 1087.98             | input       | input of channel 113                           |
| 120      | AnalogIn[114] | 335.00              | 1047.74             | input       | input of channel 114                           |
| 121      | AnalogIn[115] | 490.00              | 1007.50             | input       | input of channel 115                           |
| 122      | AnalogIn[116] | 25.00               | 967.26              | input       | input of channel 116                           |
| 123      | AnalogIn[117] | 180.00              | 927.02              | input       | input of channel 117                           |
| 124      | AnalogIn[118] | 335.00              | 886.78              | input       | input of channel 118                           |
| 125      | AnalogIn[119] | 490.00              | 846.54              | input       | input of channel 119                           |
| 126      | AnalogIn[120] | 25.00               | 806.30              | input       | input of channel 120                           |
| 127      | AnalogIn[121] | 180.00              | 766.06              | input       | input of channel 121                           |
| 128      | AnalogIn[122] | 335.00              | 725.82              | input       | input of channel 122                           |
| 129      | AnalogIn[123] | 490.00              | 685.58              | input       | input of channel 123                           |
| 130      | AnalogIn[124] | 25.00               | 645.34              | input       | input of channel 124                           |
| 131      | AnalogIn[125] | 180.00              | 605.10              | input       | input of channel 125                           |
| 132      | AnalogIn[126] | 335.00              | 564.86              | input       | input of channel 126                           |
| 133      | AnalogIn[127] | 490.00              | 524.62              | input       | input of channel 127                           |
| 134      | GndPre        | 25.00               | 484.38              | power input | negative preamplifier supply (detector ground) |
| 135      | GndPre        | 180.00              | 444.14              | power input | negative preamplifier supply (detector ground) |
| 136      | GndPre        | 335.00              | 403.90              | power input | negative preamplifier supply (detector ground) |
| 137      | GndPre        | 490.00              | 363.66              | power input | negative preamplifier supply (detector ground) |

## A.2 Bottom Pads

| Ref. no. | Pin name        | Coordinates         |                     | Type        | Description  |
|----------|-----------------|---------------------|---------------------|-------------|--|
|          |                 | x [ $\mu\text{m}$ ] | y [ $\mu\text{m}$ ] |             |  |
| 138      | ProbeVrefFE     | 1754.12             | 37.50               | output      | analog probe pad for front-end current source                |
| 139      | GndPre          | 1869.12             | 37.50               | power input | negative preamplifier supply (detector ground)               |
| 140      | VddPre          | 1984.12             | 37.50               | power input | positive preamplifier supply                                 |
| 141      | VddComp         | 2099.12             | 37.50               | power input | positive comparator supply                                   |
| 142      | GndComp         | 2214.12             | 37.50               | power input | negative comparator supply                                   |
| 143      | notCompClock    | 2329.12             | 37.50               | LVDS input  | comparator clock   |
| 144      | CompClock       | 2444.12             | 37.50               | LVDS input  | comparator clock   |
| 145      | CompOut [8]     | 2559.12             | 37.50               | LVDS output | comparator output ch. 8                                      |
| 146      | notCompOut [8]  | 2674.12             | 37.50               | LVDS output | comparator output ch. 8                                      |
| 147      | CompOut [9]     | 2789.12             | 37.50               | LVDS output | comparator output ch. 9                                      |
| 148      | notCompOut [9]  | 2904.12             | 37.50               | LVDS output | comparator output ch. 9                                      |
| 149      | CompOut [10]    | 3019.12             | 37.50               | LVDS output | comparator output ch. 10                                     |
| 150      | notCompOut [10] | 3134.12             | 37.50               | LVDS output | comparator output ch. 10                                     |
| 151      | CompOut [11]    | 3249.12             | 37.50               | LVDS output | comparator output ch. 11                                     |
| 152      | notCompOut [11] | 3364.12             | 37.50               | LVDS output | comparator output ch. 11                                     |
| 153      | CompOut [12]    | 3479.12             | 37.50               | LVDS output | comparator output ch. 12                                     |
| 154      | notCompOut [12] | 3594.12             | 37.50               | LVDS output | comparator output ch. 12                                     |
| 155      | CompOut [13]    | 3709.12             | 37.50               | LVDS output | comparator output ch. 13                                     |
| 156      | notCompOut [13] | 3824.12             | 37.50               | LVDS output | comparator output ch. 13                                     |
| 157      | CompOut [14]    | 3939.12             | 37.50               | LVDS output | comparator output ch. 14                                     |
| 158      | notCompOut [14] | 4054.12             | 37.50               | LVDS output | comparator output ch. 14                                     |
| 159      | CompOut [15]    | 4169.12             | 37.50               | LVDS output | comparator output ch. 15                                     |
| 160      | notCompOut [15] | 4284.12             | 37.50               | LVDS output | comparator output ch. 15                                     |
| 161      | VddComp         | 4399.12             | 37.50               | power input | positive comparator supply                                   |
| 162      | GndComp         | 4514.12             | 37.50               | power input | negative comparator supply                                   |
| 163      | FifoFull        | 4629.12             | 37.50               | CMOS output | indicates a full derandomising buffer                        |
| 164      | RoTokenIn       | 4744.12             | 37.50               | CMOS input  | input of the readout token in the daisy-chain operation mode |
| 165      | RoReTokenOut    | 4859.12             | 37.50               | CMOS output | readout return token output in daisy-chain mode              |

## A.3 Backside Pads

| Ref. no. | Pin name     | Coordinates         |                     | Type        | Description                                  |
|----------|--------------|---------------------|---------------------|-------------|--|
|          |              | x [ $\mu\text{m}$ ] | y [ $\mu\text{m}$ ] |             |  |
| 166      | Vddd         | 4974.62             | 184.72              | power input | positive digital supply                      |
| 167      | Vddd         | 4974.62             | 299.72              | power input | positive digital supply                      |
| 168      | Gddd         | 4974.62             | 414.72              | power input | negative digital supply                      |
| 169      | Gddd         | 4974.62             | 529.72              | power input | negative digital supply                      |
| 170      | TrigMon      | 4974.62             | 644.72              | CMOS output | indicates if trigger pointer passes column 0 |
| 171      | WriteMon     | 4974.62             | 759.72              | CMOS output | indicates if write pointer passes column 0   |
| 172      | notTrigger   | 4974.62             | 874.72              | LVDS input  | trigger                                      |
| 173      | Trigger      | 4974.62             | 989.72              | LVDS input  | trigger                                      |
| 174      | notClock     | 4974.62             | 1104.72             | LVDS input  | sampling clock                               |
| 175      | Clock        | 4974.62             | 1219.72             | LVDS input  | sampling clock                               |
| 176      | notTestpulse | 4974.62             | 1334.72             | LVDS input  | test pulse                                   |
| 177      | Testpulse    | 4974.62             | 1449.72             | LVDS input  | test pulse                                   |

| Ref. no. | Pin name        | Coordinates         |                     | Type                   | Description                                   |
|----------|-----------------|---------------------|---------------------|------------------------|---|
|          |                 | x [ $\mu\text{m}$ ] | y [ $\mu\text{m}$ ] |                        |   |
| 178      | notReset        | 4974.62             | 1564.72             | LVDS input             | system reset                                  |
| 179      | Reset           | 4974.62             | 1679.72             | LVDS input             | system reset                                  |
| 180      | notDataValid    | 4974.62             | 1794.72             | LVDS output            | indicates presence of valid data on AnalogOut |
| 181      | DataValid       | 4974.62             | 1909.72             | LVDS output            | indicates presence of valid data on AnalogOut |
| 182      | I2CAddr[0]      | 4974.62             | 2024.72             | CMOS input (pull-down) | chip address bit 0                            |
| 183      | I2CAddr[1]      | 4974.62             | 2139.72             | CMOS input (pull-down) | chip address bit 1                            |
| 184      | I2CAddr[2]      | 4974.62             | 2254.72             | CMOS input (pull-down) | chip address bit 2                            |
| 185      | I2CAddr[3]      | 4974.62             | 2369.72             | CMOS input (pull-down) | chip address bit 3                            |
| 186      | I2CAddr[4]      | 4974.62             | 2484.72             | CMOS input (pull-down) | chip address bit 4                            |
| 187      | I2CAddr[5]      | 4974.62             | 2599.72             | CMOS input (pull-down) | chip address bit 5                            |
| 188      | I2CAddr[6]      | 4974.62             | 2714.72             | CMOS input (pull-down) | chip address bit 6                            |
| 189      | SCL             | 4974.62             | 2829.72             | CMOS input             | I2C-bus clock port                            |
| 190      | SDA             | 4974.62             | 2944.72             | CMOS input/output      | I2C-bus data port                             |
| 191      | PowerupReset    | 4974.62             | 3059.72             | block input/output     | block pad for power-up reset                  |
| 192      | EnableEDC       | 4974.62             | 3174.72             | CMOS input (pull-up)   | enables Error Detection and Correction        |
| 193      | notAnalogOut[3] | 4974.62             | 3289.72             | output                 | analog output ch. 3                           |
| 194      | AnalogOut[3]    | 4974.62             | 3404.72             | output                 | analog output ch. 3                           |
| 195      | notAnalogOut[2] | 4974.62             | 3519.72             | output                 | analog output ch. 2                           |
| 196      | AnalogOut[2]    | 4974.62             | 3634.72             | output                 | analog output ch. 2                           |
| 197      | notAnalogOut[1] | 4974.62             | 3749.72             | output                 | analog output ch. 1                           |
| 198      | AnalogOut[1]    | 4974.62             | 3864.72             | output                 | analog output ch. 1                           |
| 199      | notAnalogOut[0] | 4974.62             | 3979.72             | output                 | analog output ch. 0                           |
| 200      | AnalogOut[0]    | 4974.62             | 4094.72             | output                 | analog output ch. 0                           |
| 201      | Gndd            | 4974.62             | 4209.72             | power input            | negative digital supply                       |
| 202      | Gndd            | 4974.62             | 4324.72             | power input            | negative digital supply                       |
| 203      | Gnda            | 4974.62             | 4439.72             | power input            | negative analog supply                        |
| 204      | Gnda            | 4974.62             | 4554.72             | power input            | negative analog supply                        |
| 205      | Gnda            | 4974.62             | 4669.72             | power input            | negative analog supply                        |
| 206      | Vddd            | 4974.62             | 4784.72             | power input            | positive digital supply                       |
| 207      | Vddd            | 4974.62             | 4899.72             | power input            | positive digital supply                       |
| 208      | Vdda            | 4974.62             | 5014.72             | power input            | positive analog supply                        |
| 209      | Vdda            | 4974.62             | 5129.72             | power input            | positive analog supply                        |
| 210      | Vdda            | 4974.62             | 5244.72             | power input            | positive analog supply                        |
| 211      | Icurrbuf        | 4974.62             | 5359.72             | block output           | analog probe pad (to be blocked)              |
| 212      | Isf             | 4974.62             | 5474.72             | block output           | analog probe pad (to be blocked)              |
| 213      | Ipipe           | 4974.62             | 5589.72             | block output           | analog probe pad (to be blocked)              |
| 214      | Vdc1buf         | 4974.62             | 5704.72             | block output           | analog probe pad (to be blocked)              |
| 215      | Vdbuf           | 4974.62             | 5819.72             | block output           | analog probe pad (to be blocked)              |

## A.4 Top Pads

| Ref. no. | Pin name       | Coordinates         |                     | Type        | Description                                    |
|----------|----------------|---------------------|---------------------|-------------|--|
|          |                | x [ $\mu\text{m}$ ] | y [ $\mu\text{m}$ ] |             |  |
| 216      | RoReTokenIn    | 4859.12             | 5967.52             | CMOS input  | readout return token input in daisy-chain mode |
| 217      | RoTokenOut     | 4744.12             | 5967.52             | CMOS output | readout token output in daisy-chain mode       |
| 219      | ProbeVrefBE    | 4514.12             | 5967.52             | output      | analog probe pad for back-end current source   |
| 220      | ProbeIoutBE    | 4399.12             | 5967.52             | output      | analog probe pad for back-end current source   |
| 221      | PipeampTestOut | 4284.12             | 5967.52             | output      | pipeamp output of test channel                 |
| 223      | GndComp        | 4054.12             | 5967.52             | power input | negative comparator supply                     |
| 224      | VddComp        | 3939.12             | 5967.52             | power input | positive comparator supply                     |
| 225      | notCompOut [7] | 3824.12             | 5967.52             | LVDS output | comparator output ch. 7                        |
| 226      | CompOut [7]    | 3709.12             | 5967.52             | LVDS output | comparator output ch. 7                        |
| 227      | notCompOut [6] | 3594.12             | 5967.52             | LVDS output | comparator output ch. 6                        |
| 228      | CompOut [6]    | 3479.12             | 5967.52             | LVDS output | comparator output ch. 6                        |
| 229      | notCompOut [5] | 3364.12             | 5967.52             | LVDS output | comparator output ch. 5                        |
| 230      | CompOut [5]    | 3249.12             | 5967.52             | LVDS output | comparator output ch. 5                        |
| 231      | notCompOut [4] | 3134.12             | 5967.52             | LVDS output | comparator output ch. 4                        |
| 232      | CompOut [4]    | 3019.12             | 5967.52             | LVDS output | comparator output ch. 4                        |
| 233      | notCompOut [3] | 2904.12             | 5967.52             | LVDS output | comparator output ch. 3                        |
| 234      | CompOut [3]    | 2789.12             | 5967.52             | LVDS output | comparator output ch. 3                        |
| 235      | notCompOut [2] | 2674.12             | 5967.52             | LVDS output | comparator output ch. 2                        |
| 236      | CompOut [2]    | 2559.12             | 5967.52             | LVDS output | comparator output ch. 2                        |
| 237      | notCompOut [1] | 2444.12             | 5967.52             | LVDS output | comparator output ch. 1                        |
| 238      | CompOut [1]    | 2329.12             | 5967.52             | LVDS output | comparator output ch. 1                        |
| 239      | notCompOut [0] | 2214.12             | 5967.52             | LVDS output | comparator output ch. 0                        |
| 240      | CompOut [0]    | 2099.12             | 5967.52             | LVDS output | comparator output ch. 0                        |
| 241      | GndComp        | 1984.12             | 5967.52             | power input | negative comparator supply                     |
| 242      | VddComp        | 1869.12             | 5967.52             | power input | positive comparator supply                     |
| 243      | VddPre         | 1754.12             | 5967.52             | power input | positive preamplifier supply                   |
| 244      | GndPre         | 1639.12             | 5967.52             | power input | negative preamplifier supply (detector ground) |
| 245      | TestOutput     | 1524.12             | 5967.52             | output      | front-end output of test channel               |
| 246      | Bufbias        | 1409.12             | 5967.52             | output      | analog probe pad                               |
| 247      | Shabias1       | 1294.12             | 5967.52             | output      | analog probe pad                               |
| 248      | Shabias        | 1179.12             | 5967.52             | output      | analog probe pad                               |
| 249      | Prebias1       | 1064.12             | 5967.52             | output      | analog probe pad                               |
| 250      | Prebias        | 949.12              | 5967.52             | output      | analog probe pad                               |

## B Heidelberg Test Boards

For a standalone characterisation of the *Beetle* chip, i.e. without a silicon sensor applied to its input, a test setup consisting of two printed circuit boards has been developed in Heidelberg. This section summarises the pin configurations and bonding schemes of the two boards. The *daughter board* can carry two *Beetle* chips and is mounted on a second board, called *mother board*, which integrates the I<sup>2</sup>C-level-shifting circuit (fig. 14) as well as the receiver circuitry for the output stages (fig. 2). The setup allows the charge injection to 12 input channels per chip via a resistive voltage divider (located on the mother board) and a serial capacitance. Parallel capacitances can be applied as load. Serial and parallel capacitances are located on the daughter board.

Fig. 17 shows the pin configuration of the daughter board, Figs. 18 and 19 the corresponding bonding schemes. The pin configuration of the mother board is depicted in fig. 20.

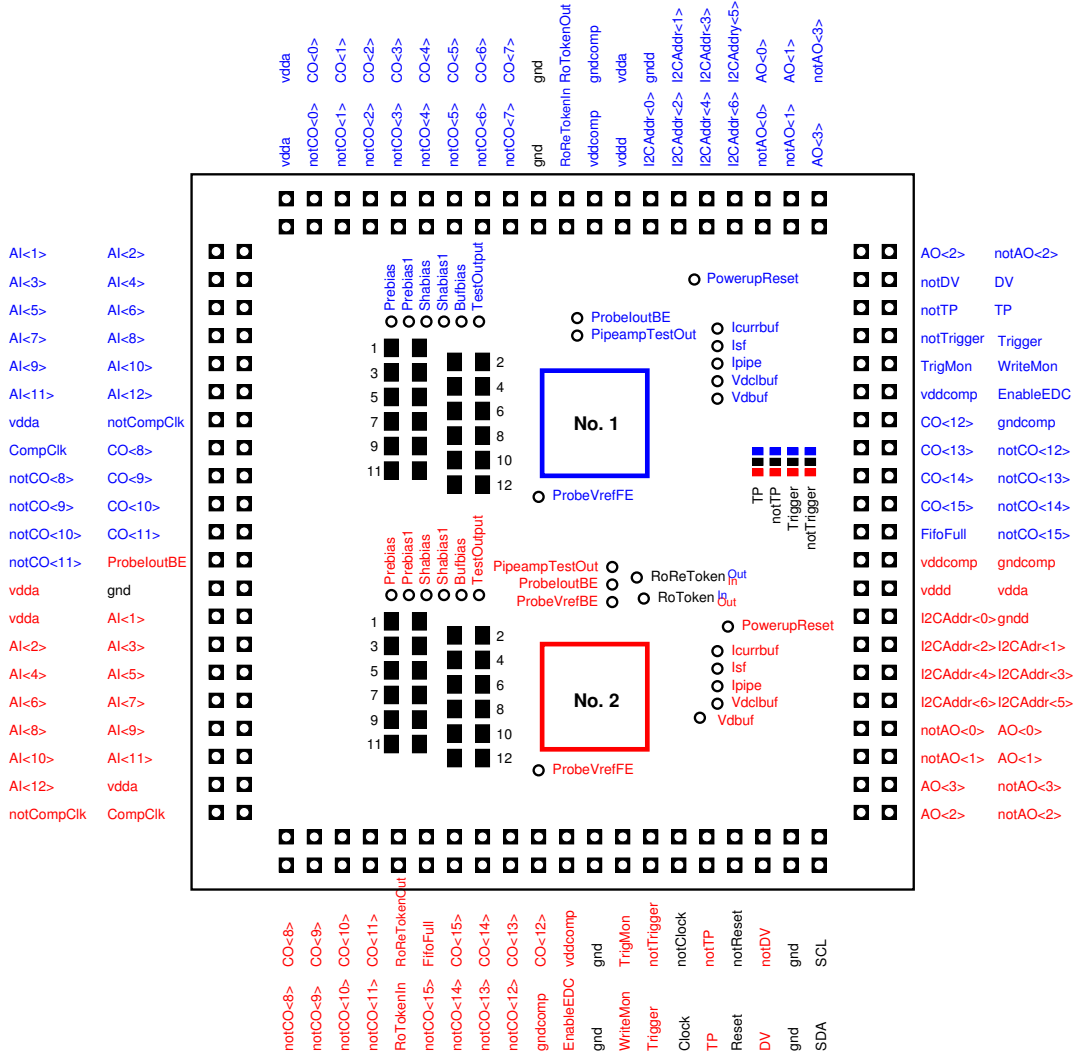


Figure 17: Pin configuration of the daughter board. The four jumper rows labelled *TP*, *notTP*, *Trigger*, *notTrigger* refer to chip no. 1 and select between the signal pins on the right side (upper position) and on the bottom side (lower position). Using the lower jumper positions, both chips receive *Trigger* and *TP* signals via the bottom side pins.

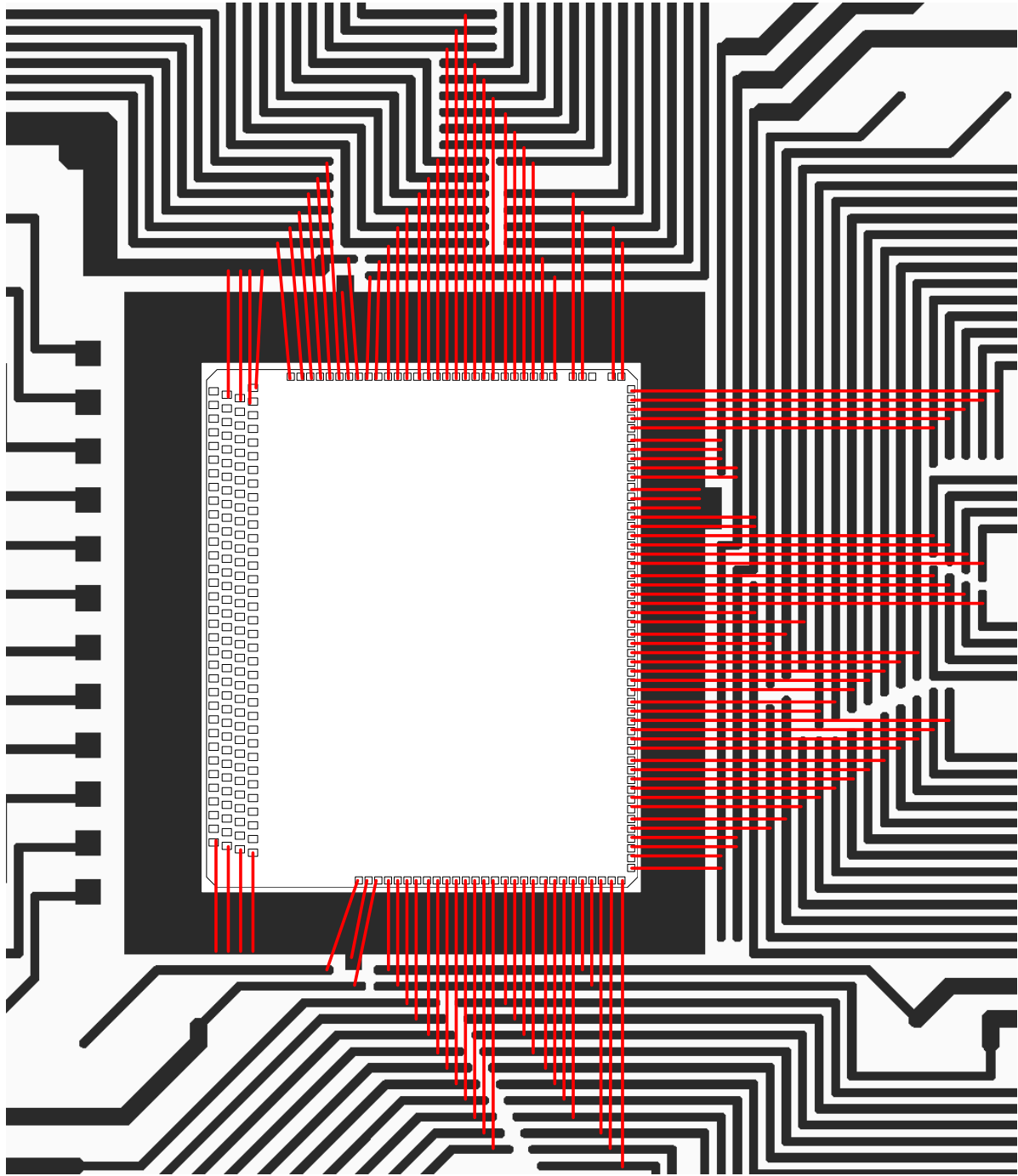


Figure 18: Bonding scheme of chip 1 on the daughter board.



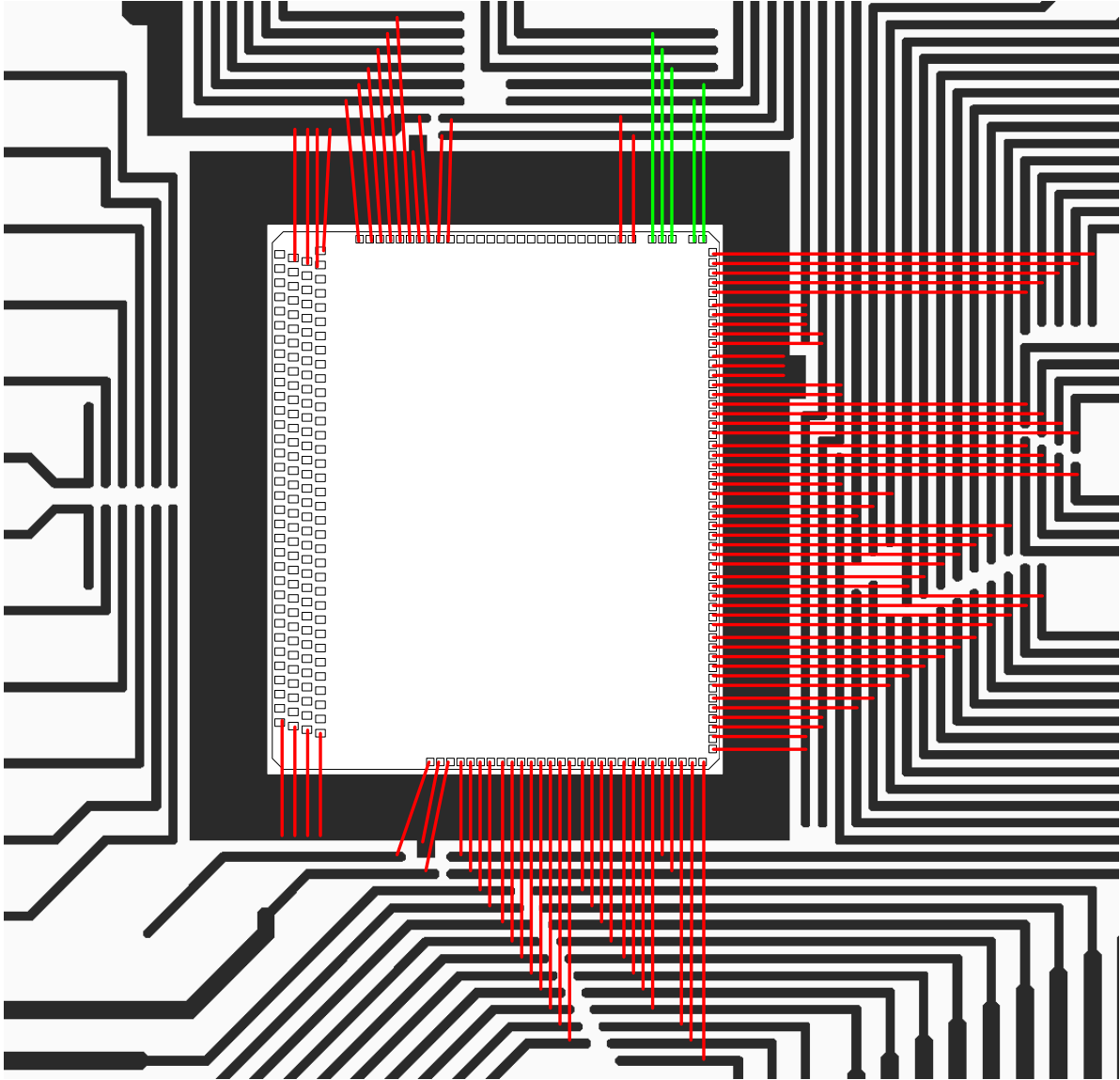


Figure 19: Bonding scheme of chip 2 on the daughter board.

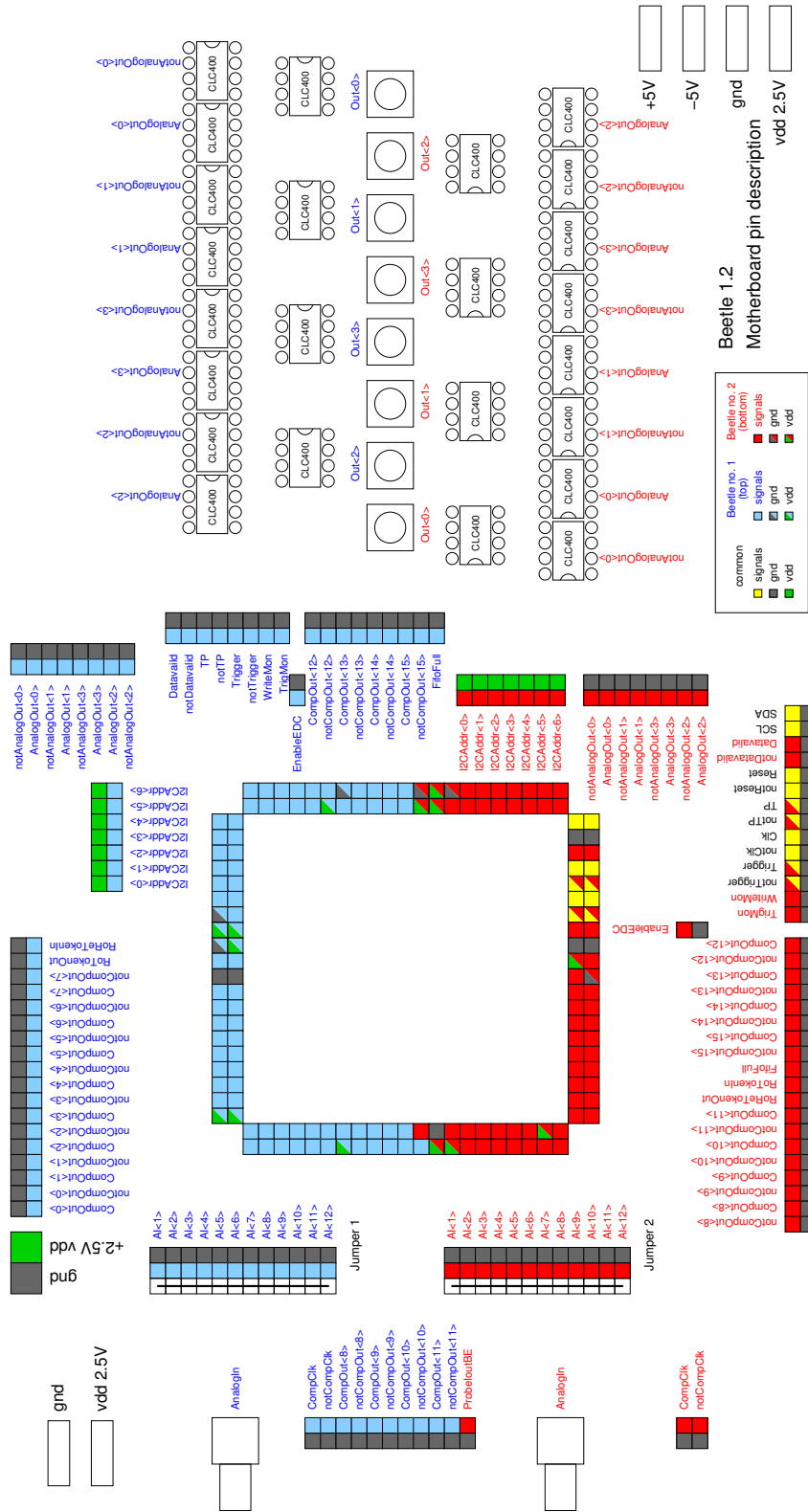


Figure 20: Pin configuration of the motherboard.

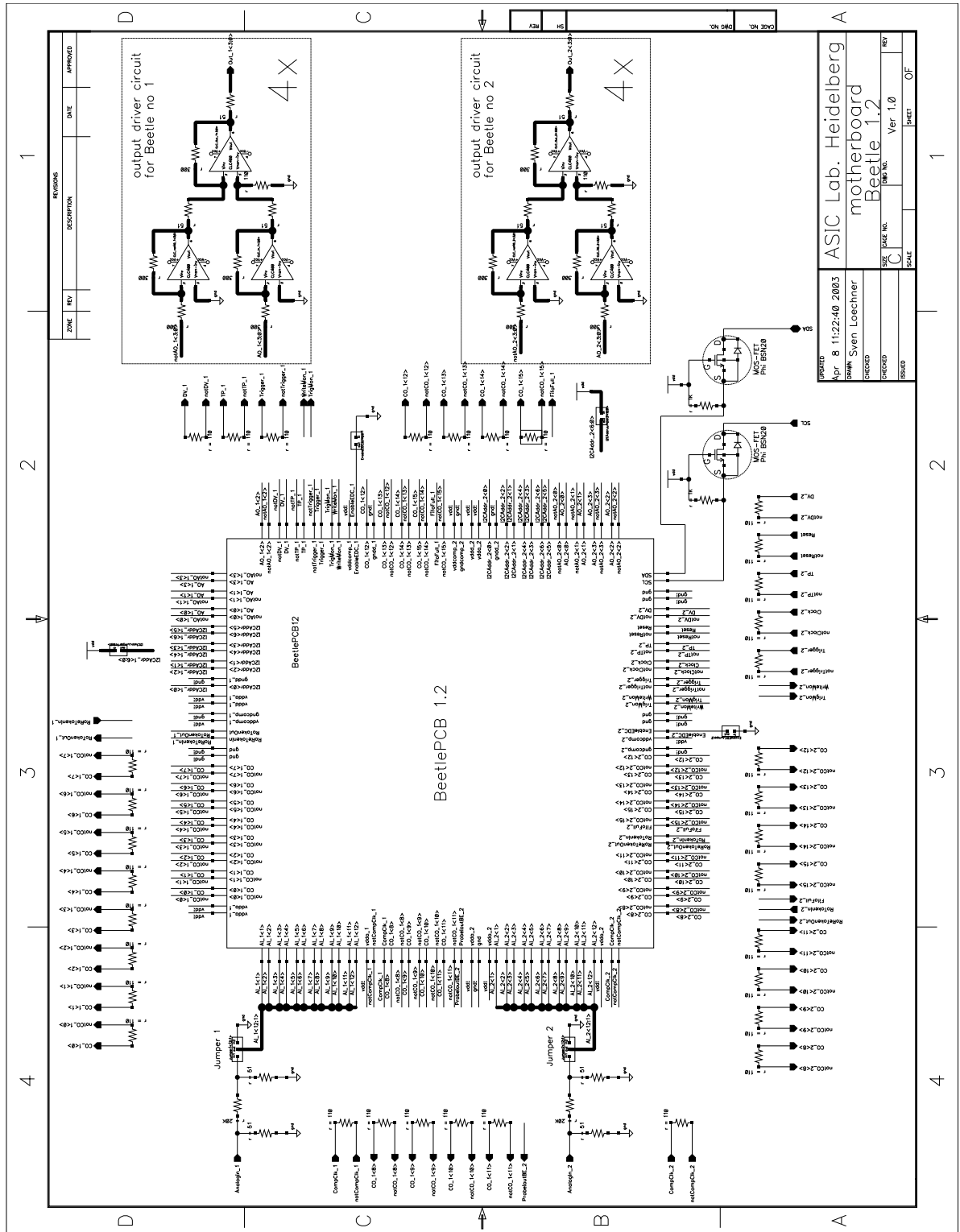


Figure 21: Schematic diagram of the mother board.

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